TOLT Design Guideline

A design reference for users

About this document

Scope and purpose

This document is intended to give guidance on how to implement the Infineon TOLT package into the system based on known special challenges during assembly as well as the design phase of the PCB and the mechanics.

Intended audience

This document is intended for system engineers taking care of mechanical and electrical design in automotive high power applications.

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1 Introduction

It is recommended to first read through the application notes mentioned in table 1 to get a better understanding about the TOLT package in general. The focus of this document are special challenges with respect to negative standoff of the package, PCB design and the thermal interface material (TIM).

Table 1

App. Note	Content overview
TO-Leaded Topside-Cooled (TOLT) Package Automotive Power MOSFET – A new package for high power densities	Introduction of TOLT package (basic knowledge) Differences between top side and back side cooling Special features of the TOLT package TIM materials and influence of thinckness Simulations of various Rth (1s0p, 2s2p, etc.) First hints of design integration
Recommendations for Board Assembly of Infineon Packages with Dual Row Gullwing Leads	Solderability and placement on the board
General Recommendations for Assembly of Infineon Packages	How to solder packages, basic knowledge
TOLT Design Guideline	Detailed design recommendations for the TOLT package
TOLT vs TOLL thermal comparison	Thermal comparison between the TOLT package and the TOLL standard package

2 Package bottom and PCB assembly

This section provides recommendations on how to solve special challenges during assembly, PCB design and device positioning.

2.1 Package Outline

The device package has negative standoff. Therefore a rather high stencil thickness is required to create an appropriate solder connection to the device pins. Good results can be achieved with a 200 µm stencil thickness and recommended footprints. For more information about TOLT package dimensions and footprint, please refer to following link:

https://www.infineon.com/cms/en/product/packages/PG-HDSOP/PG-HDSOP-16-1/

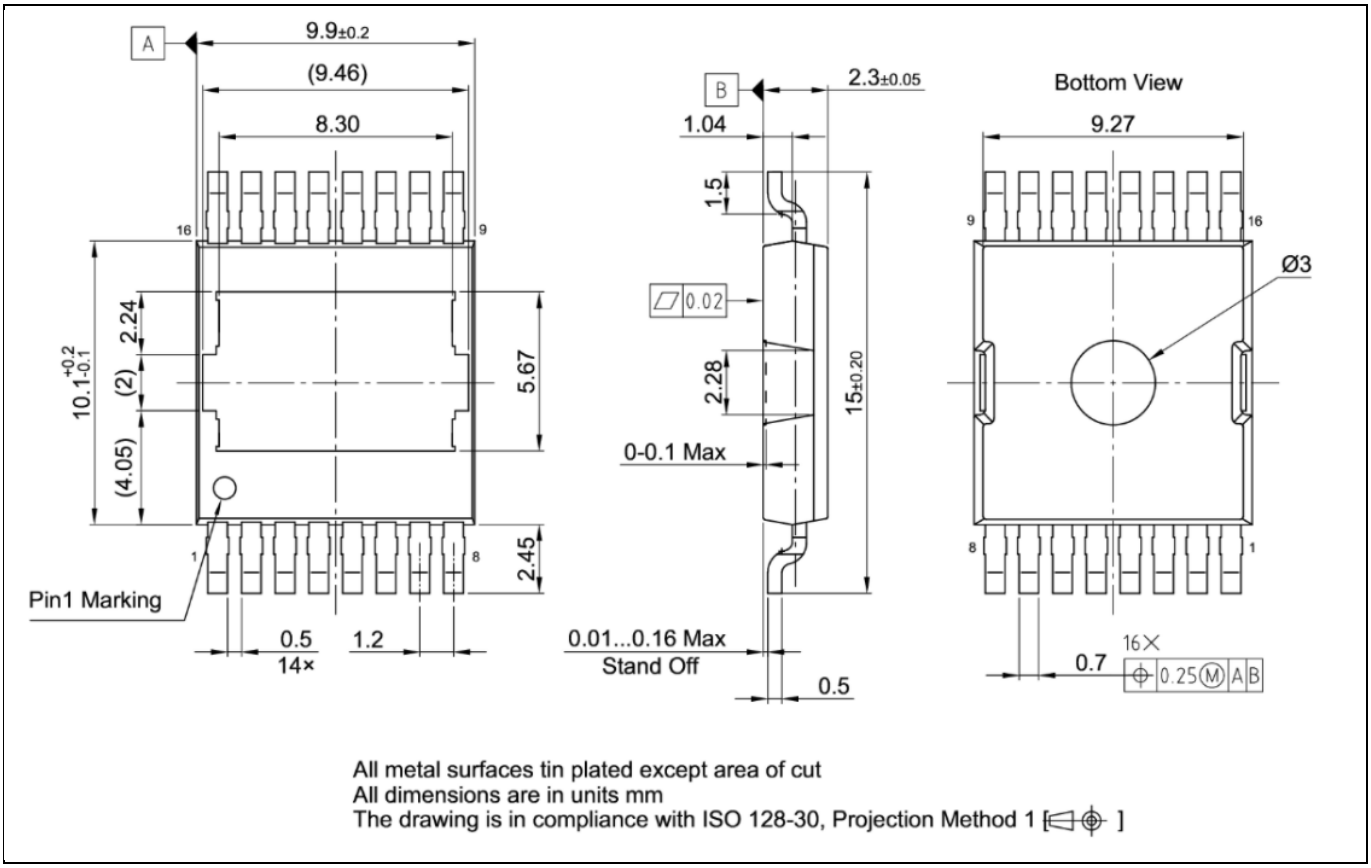


Figure 1 Package outline drawing

The stencil mask mentioned above and given in Figure 3 is probably too thick for fine pitch components such as controllers and gate drivers. As they can't use the same stencil, it could be seen as a design challenge. There are simple countermeasures, which can be used:

- Two different stencil heights and masks on same board side
- Components with fine pitch mounted on the other board side
- Different board for finepitch components (allows also a dedicated layout for power and logic)

For a proper board design it is recommended to have the power components on the same board side or using a different board for the TOLT package. This way it's easier to have synergies in stencil mask and power/current level the component dissipates versus the other approaches.

2.2 PCB Layout

In the previous section it was explained that components which require a lower stencil height than the TOLT package should be mounted on the other board side. This applies also for the separation of low and high power components to both sides of the board (bottom and top layer). Therefore, it is recommended to use one board side for the TOLT packages together with the power parts such as capacitors and measuring parts and on the opposite the controlling hardware.

DC link capacitors and snubber circuits should be placed as close as possible to the TOLT package on the power side of the board. In this way parasitic inductances of PCB traces and vias are minimized. Keep in mind, that the stray inductance of TOLT is typically 4 nH and therefore a bit increased compared to the TOLL package.

Thermal reliefs and symmetrical layout help to reduce issues with inhomogeneous temperature distribution during soldering, which could lead to the so called tomb stone effect (lifting of the package on one side during assembly). Other possibilities are increasing the heating time or soaking time during reflow. But this has to be individually analyzed dependent on the individual design.

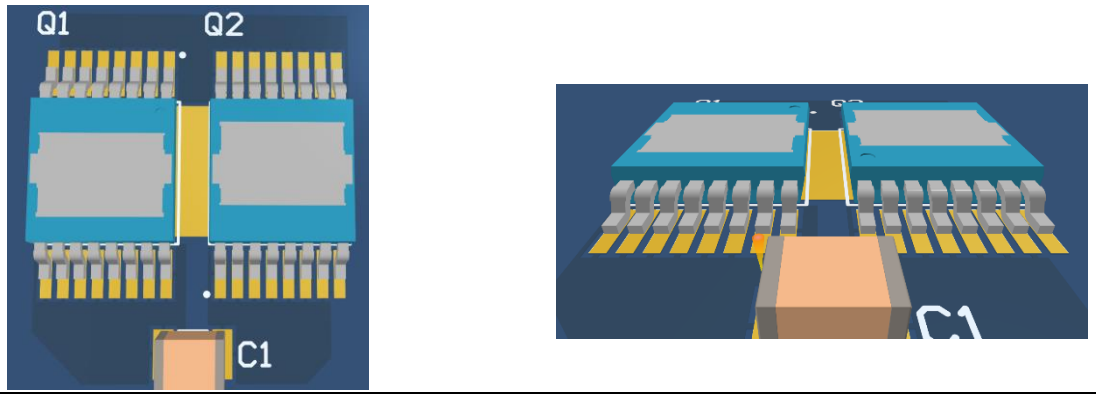


Figure 2 Example of MosFET Half-Bridge (Phase out upper side/DC-Link lower side) & shared metal plate between high side and low side switch

Special attention should be given to the mold body, which is in direct contact with the PCB. The area below the package should be kept clean to avoid that impurities or particles lead to a skewed package, because it is not attached flat to the PCB. A cleaning before the soldering reflow can help improve the cleanliness of the surface. A large copper area is recommended which can also be used as the drain or source contact.

Please refer also to the app note: Recommendations for Board Assembly of Infineon Packages with Dual Row Gullwing Leads section 2.2 Pad design, remember this solder mask clearance between pins and the copper pad.

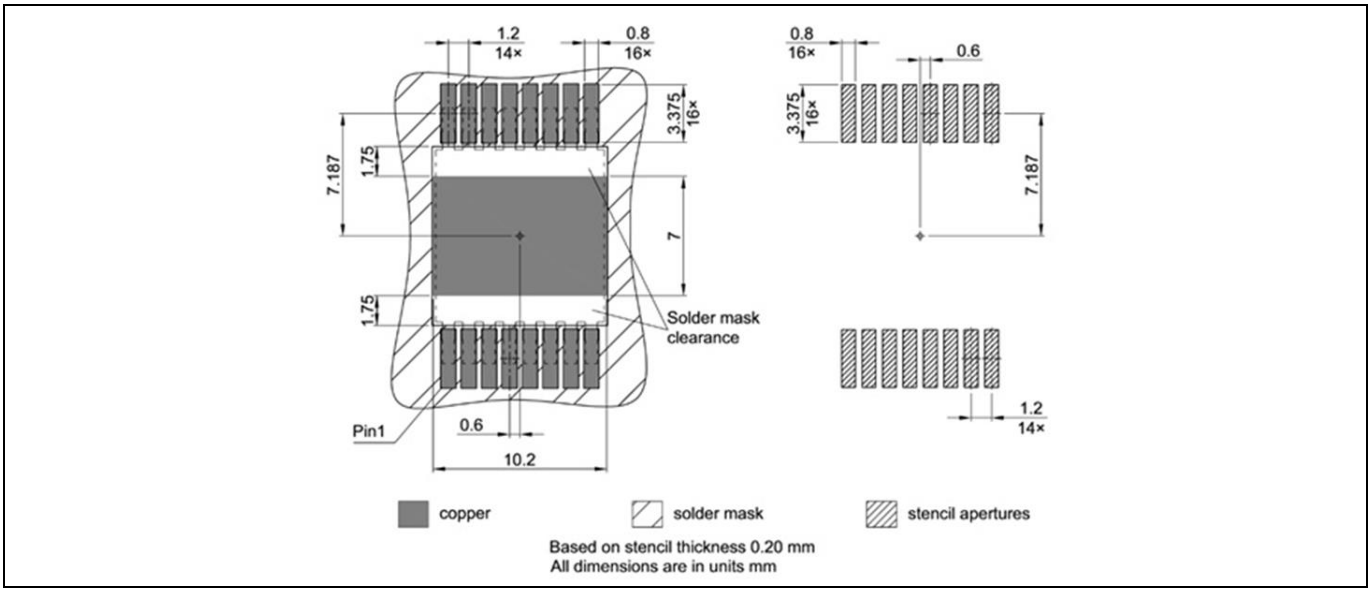


Figure 3 Recommended footprint with copper area below the package body

It is recommended to not cover the large copper area with a solder mask or silkscreen as it is adding additional tolerances and accordingly increases the risk of package skewing.

Skewing of the package may lead to reduced thermal performance due to a modified thickness of the thermal interface material applied to the top side of the package. Even further it could lead to problems during soldering and assembly on the board.

3 Package top and heat sink interface

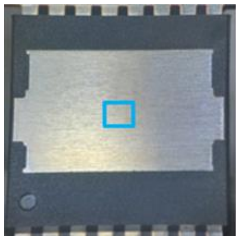
The package top side is the key for the cooling performance and will be handled in this section.

3.1 Top side pad

The top side pad is plated with nickel (NiNiP), instead of tin (Sn). Nickel has improved tolerance properties during the reflow process. This enables the top side to have the same flatness as the bottom of the package, which is given in the package outline drawing as 0.02 mm (only the exposed pad is 0.01 mm).

Furthermore, the top side pad has a very low roughness grade see table 2 for typical values of the different area roughness parameters.

Table 2

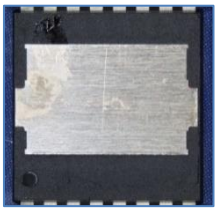
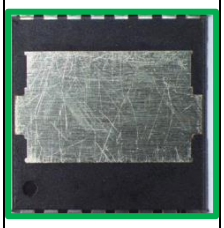
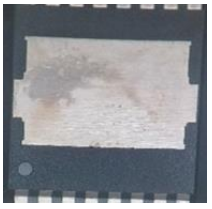
Location of the measurement	Roughness peak S_p (typ.)	Roughness valley S_v (typ.)	Roughness average S_a (typ.)	Unit
	1.9	1.5	0.15	µm

The roughness peak is the height of the highest peak within the defined area (blue rectangle). The roughness valley is the absolute value of the height of the largest pit (valley) within the defined area. The roughness average expresses the difference in height of each point in the defined area to the arithmetical mean of the surface. This parameter is often used to evaluate surface roughness.

The low roughness values given in the table enabling also the usage of non-highly fluid TIM materials. If the heat sink side has the same flatness more and more simple gap fillers could be used. In combination with the negative stand-off is now visible that a thin TIM thickness can be used depending on the mechanical tolerances between heat sink, package and board.

Find the quality aspects of the pad in table 1.

Table 3 Quality of the top side pad

	Glue residues	Scratches	Stain
Example			
Occurrence rate within shipped parts (based on ~90kpcs)	<50ppm	<1%	<1%

Reject criteria	More than 5% of exposed pad covered with glue residue	Exposed Cu	Blue or purple discoloration
Dimension/details of shipped parts	▪ Height of up to 30µm (based on manual feasibility) ▪ Mainly based on Carbon & Oxygen	Depth of scratch typically around 1µm	▪ No height difference ▪ No foreign material

3.2 Thermal interface material (TIM)

As discussed in section 2.4 of the TOLT package application note, the manufacturing process of the heat sink has an impact on the thickness and consistency of the interface material. To enable the lowest possible TIM thickness (which is around 300µm) the mechanical tolerance of the heatsink should be in a range of +/-50µm. The TIM will expand and shrink as the temperature rises and falls. This could cause voids in the TIM when the board is bending due to thermo-mechanical stress. To minimize this effect it is recommended to use mechanical supports as shown in figure 4. Optimized supports without screwing could also be directly below the package on the opposite side of the board. Thus the bending effect away from the heat sink during thermal cycles is minimized. To gain the best in performance and reliability versus effort it is recommended to simulate to better understand the generated design and its challenges. Mechanical and thermal models can be provided. Please contact your closest Infineon sales office (if you are a registered user you can find mechanical models here).

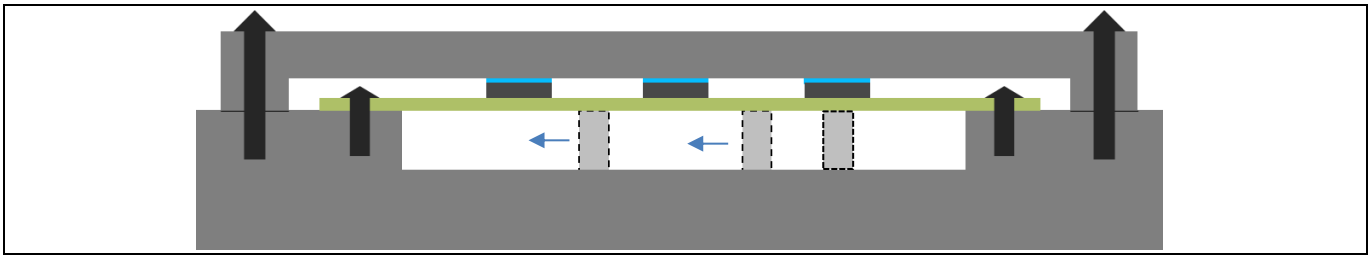


Figure 4 Additional supports below board

The thermal cycles affect also the TIM and wetting out. As the flatness and roughness of the TOLT top side pad would allow to use also less wet gap fillers like silicone pads and similar. To find the best material for your heat sink it is recommended to contact the manufactuer of that materials (examples are mentioned in the TOLT package app. note). In this way it is easier to choose between phase change materials, two component gap fillers, gap filler pads and greases.

3.3 Heat sink

For the heat sink needs to be considered the aspects from 3.1 & 3.2. An additional point to consider is the heat spread into the aluminum or copper. Therefore thermal simulations like shown in the TOLT package application note (see section 5) should be done on system level to understand better the influence of the different heat spreads vs. each other.

4 References

[1] TO-Leaded Topside-Cooled (TOLT) Package Automotive Power MOSFET – A new package for high power densities v1.0. See the document at https://www.infineon.com/dgdl/Infineon-TO-Leaded-Topside-Cooled-(TOLT)-Package-ApplicationNotes-v01_00-EN.pdf?fileId=5546d46278d64ffd01790dccfd10480f

[2] Recommendations for Board Assembly of Infineon Packages with Dual Row Gullwing Leads v5.0. See the document at https://www.infineon.com/dgdl/Infineon-Board_Assembly_Recommendations-Gullwing-Package-v05_00-EN.pdf?fileId=5546d46275b79adb0175b7da356300e6

[3] General Recommendations for Assembly of Infineon Packages v4.0. See the document at https://www.infineon.com/dgdl/Infineon-General_Recommendations_for_Assembly_of_Infineon_Packages-P-v04_00-EN.pdf?fileId=5546d4625cc9456a015ccaf4a1fe3a32

[4] TOLL-vs-TOLT thermal comparison v1.0. See the document at https://www.infineon.com/dgdl/Infineon-TOLL-vs-TOLT-ApplicationNotes-v01_00-EN.pdf?fileId=8ac78c8c7bb971ed017bcf03a25a0679

Revision history

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V 0.1	01.04.2021	Initial document creation.
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