TOLL vs. TOLT

Thermal Performance Comparison

About this document

Scope and purpose

This document provides a thermal performance comparion between the Automotive MOSFET TOLL package and its topside-cooled sibling, the TOLT.

Intended audience

This document is intended for engineers designing high-power automotive applications.

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1 Introduction

Released in the end of 2020, Infineon's TOLT (JEDEC: HDSOP-16) is a modern topside-cooled package, that has been specially designed to enable high power densities in demanding automotive applications. Since the TOLT package complements Infineon's TOLx package family, which also includes the TO-Leadless (TOLL) and the TOLG packages, many questions typically arise about how the TOLL and the TOLT compare thermally. This document provides a thermal performance comparison between the Automotive MOSFET TOLL and TOLT packages, under similar conditions and considering two different cooling setups.

Figure 1 Infineon's TOLx family. Left to right: TOLT (PG-HDSOP-16), TOLL (PG-HSOF-8-1) and TOLG (PG-HSOG-8)

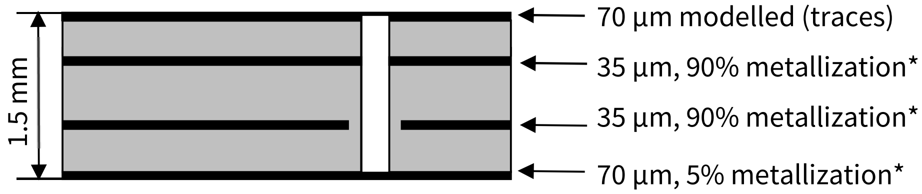
In another application note titled *TO-Leaded Topside-Cooled (TOLT) Package* (Z8F80044621), available on infineon.com, the TOLT package is introduced and all its benefits and design advantages are thoroughly explained. Please refer to that application note for a detailed introduction to the TOLT MOSFET.

Some of the key advantages and unique selling points the TOLT has to offer include:

- Reduced heat path
- Minimal heat dissipation through the PCB
- Negative standoff
- Tin-free cooling pad
- Elongated creepage distance

2 Boundary conditions & setup description

In this application note, the maximum junction-ambient thermal resistances ($R_{th(ja)}$) of the TOLL and the TOLT are investigated under similar conditions. The results presented are for a simple, 1.5-mm thick, four-layer test board that has been defined according to JEDEC standards (JESD51-5, -7) as shown below in figure 2. The PCB material is standard FR4 and the board dimensions are 114 x 76 mm^2.



*: percentage of copper metallization in each layer

Figure 2 Board cross section (JEDEC 2s2p)

In all the simulations conducted, the MOSFET is cooled from one side only. The MOSFET is soldered on the PCB, which is placed inside a 2-mm thick aluminum housing as shown in figures 3 and 4 below. The TOLL is cooled from the bottom side using an aluminum heat sink as shown in figure 3, while the TOLT is cooled from the top side with the exact same heat sink used for the TOLL, as shown in figure 4. The ambient temperature is set at 85 °C for all simulations and the power dissipated through each device is 1 W. The PCB size, the heat sink size and the MOSFET chip size are identical in both setups. The assembly and soldering guidelines can be found on the Infineon package website.

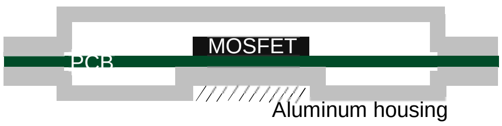


Figure 3 Cooling setup for the TOLL soldered on a PCB and placed within an aluminum housing

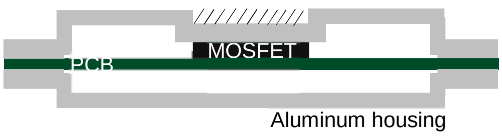


Figure 4 Cooling setup for the TOLT soldered on a PCB and placed within an aluminum housing

A 400 µm thick layer of 4 W/mK thermal insulation material (TIM) is spread between the TOLT and the heat sink above it, as illustrated in figure 5. On the other hand, a 100 µm thick layer of 0.7 W/mK is spread between the PCB of the TOLL and the heat sink below it.

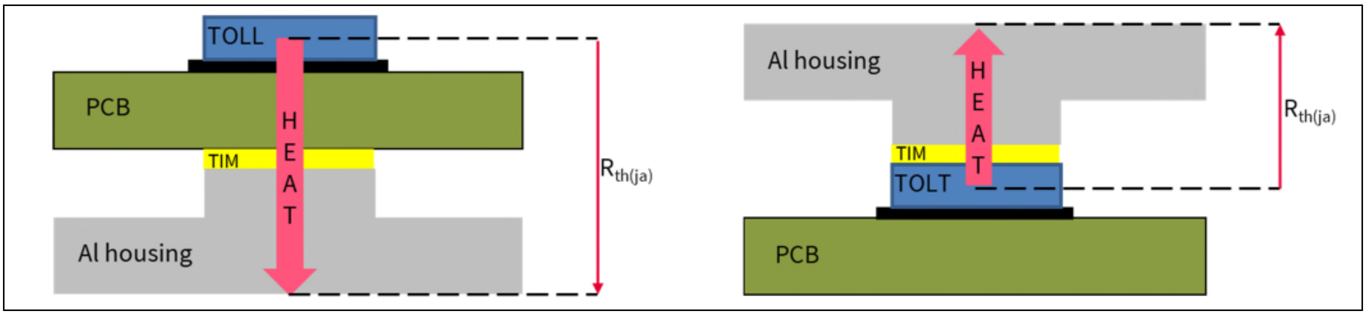


Figure 5 Illustration of the cooling setup and the heat flow. Left: TOLL, right: TOLT.

Figure 5 also shows that the heat path from the TOLL's chip to the bottom heat sink includes the PCB, the TIM and the heat sink itself. On the other hand, the heat generated by the TOLT's chip traverses the TIM layer and goes directly through the heat sink. This is the unique selling point of the TOLT; the TOLT allows decoupling the heat from the PCB. By placing the chip right under the heat sink, with a TIM layer inbetween, the TOLT effectively reduces the heat path by excluding the PCB. Thus, under similar conditions, the TOLT offers a better thermal performance than the TOLL.

3 TOLL vs. TOLT, free convection

The transient thermal impedance curves for the TOLL and TOLT, with the housing left at free convection, are presented in figure 6 below. These results pertain to the two best-in-class TOLL and TOLT devices with the largest chip size.

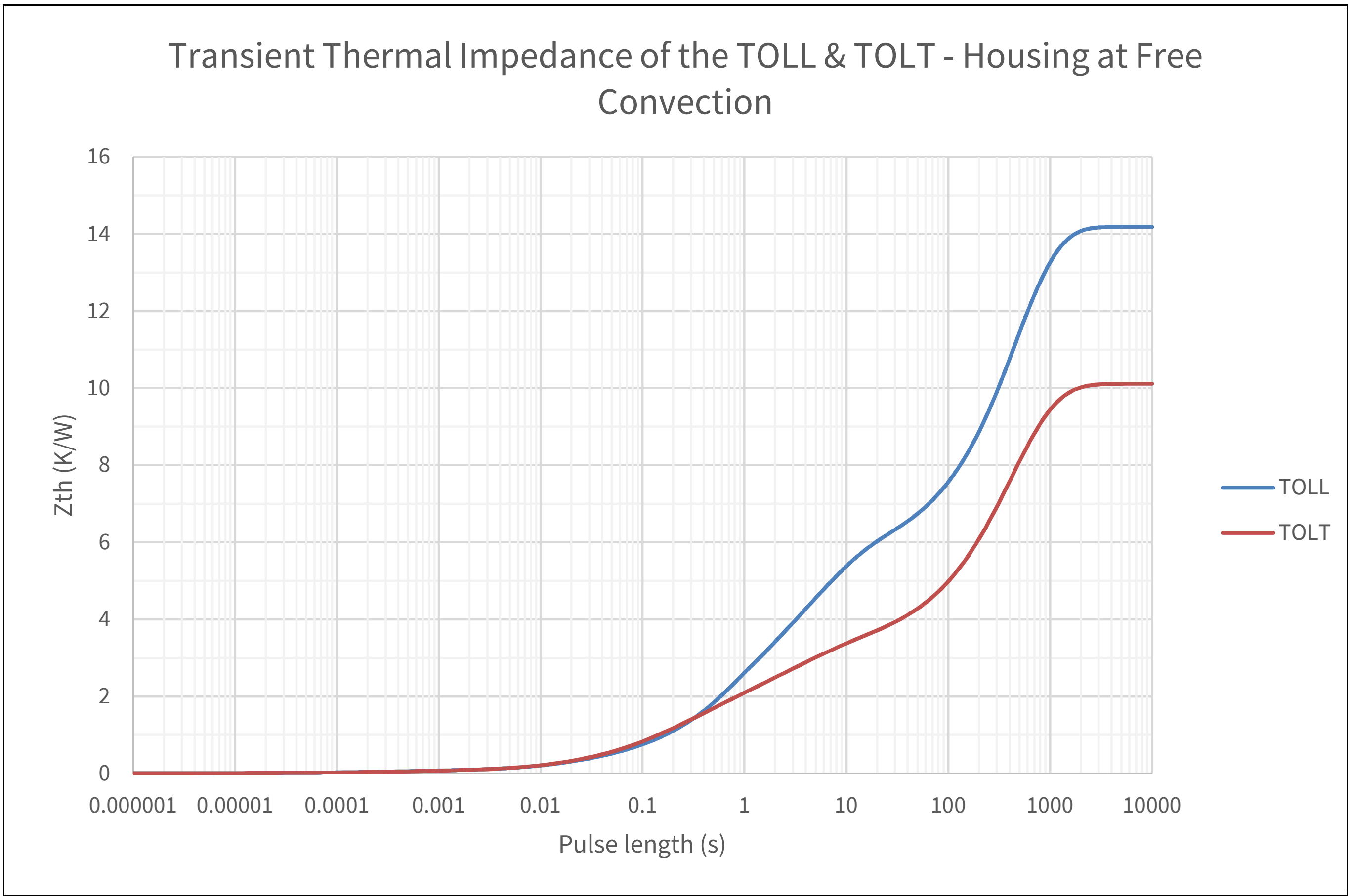


Figure 6 Transient thermal impedance (junction-ambient) of TOLL and TOLT with the housing left at free convection

The curves show that the Zth for both devices remains under 0.2 K/W for pulses shorter than 0.01 s. The two curves rise together to about 1.5 K/W for a 0.3 s pulse beyond which the two curves diverge. As explained in section 2 and illustrated in figure 5, the primary difference in thermal operation between the TOLL and the TOLT is that the TOLT allows removing the PCB from the heat path. The heat generated by the TOLT chip goes through the TIM straight to the heat sink, while in the case of the TOLL, the heat has to additionally go through the PCB. This is evident in figure 6, where for pulses longer than the 0.3 s, the TOLT has lower Zth values than the TOLL. The two curves continue to rise till they both reach their steady-state values past 2,000 seconds. The Rth value of the TOLL is 14.2 K/W, while the TOLT has an Rth of 10.1 K/W, almost 30% lower than that of the TOLL, thanks to the TOLT's innovative package design.

The effectivity of the topside-cooled TOLT compared to the bottom-cooled TOLL is further illustrated in the heat distribution plots in figure 7 below. The diagram shows that the TOLL's junction temperature rises to over 155 °C. But with the TOLT's chip being closer to the heat sink, the majority of the chip's heat is diffused to the upper side and, as a result, the temperature of the PCB beneath the TOLT rises to only 92 °C as shown below in figure 7 and table 1 below. This indicates that under similar conditions the TOLT helps keep the PCB temperature about 40% lower compared to the TOLL, by dissipating the heat to the top instead of through the PCB.

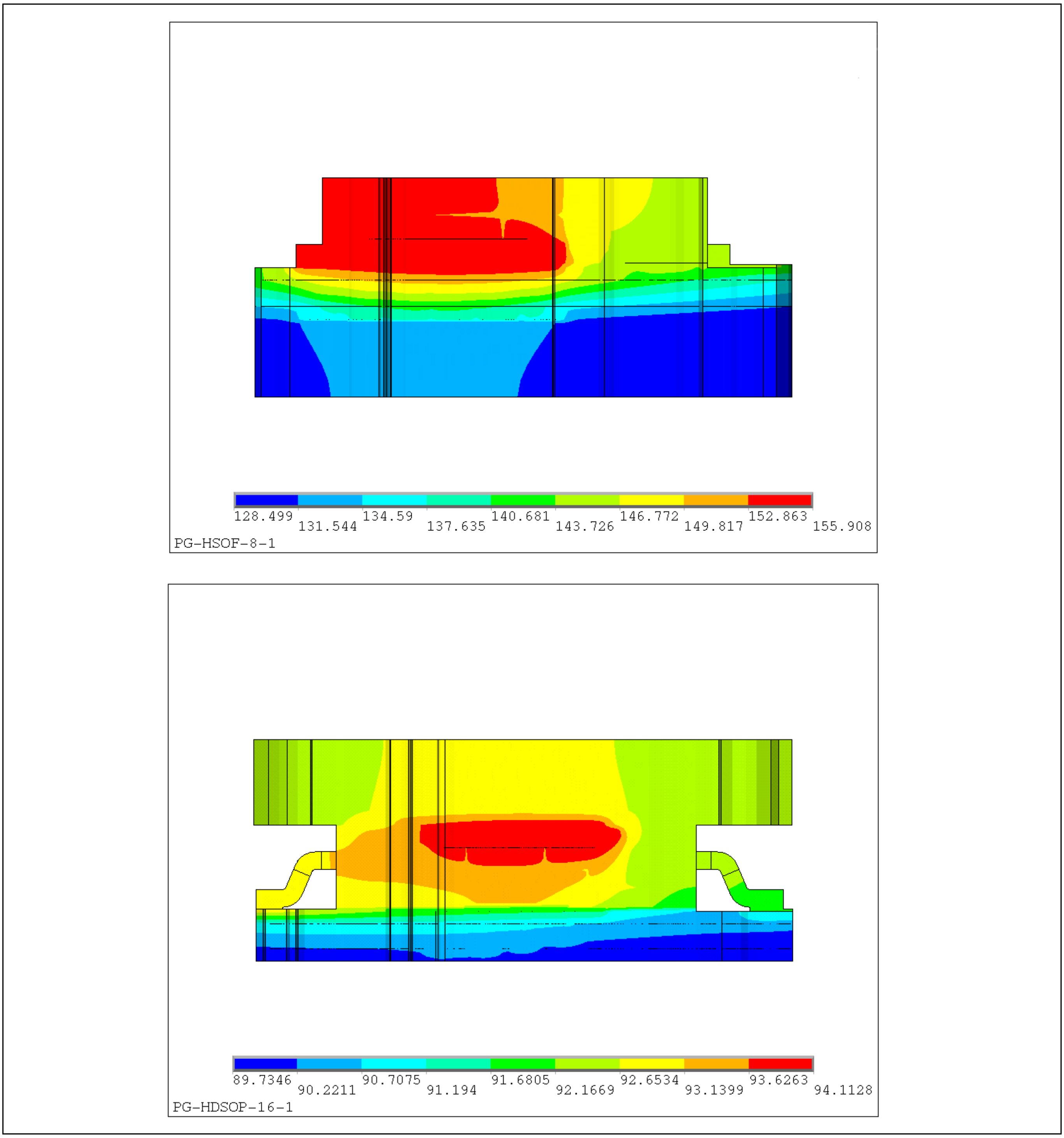


Figure 7 **Heat distribution plots for the TOLL (top) and the TOLT (bottom) with the housing left at free convection**

Table 1 **Junction and PCB temperatures for each of the TOLL and TOLT with the housing left at free convection**

	TOLL	TOLT	Percentage decrease
Junction temperature (°C)	155.9	95.1	39%
PCB temperature (°C)	155.4	93.5	40%

4 TOLL vs. TOLT, fixed at ambient temperature

Figure 8 presents the transient thermal impedance curves for the TOLL and TOLT, with the housing fixed at ambient temperature. As with the results from section 3, these values pertain to the two best-in-class TOLL and TOLT devices with the largest chip size.

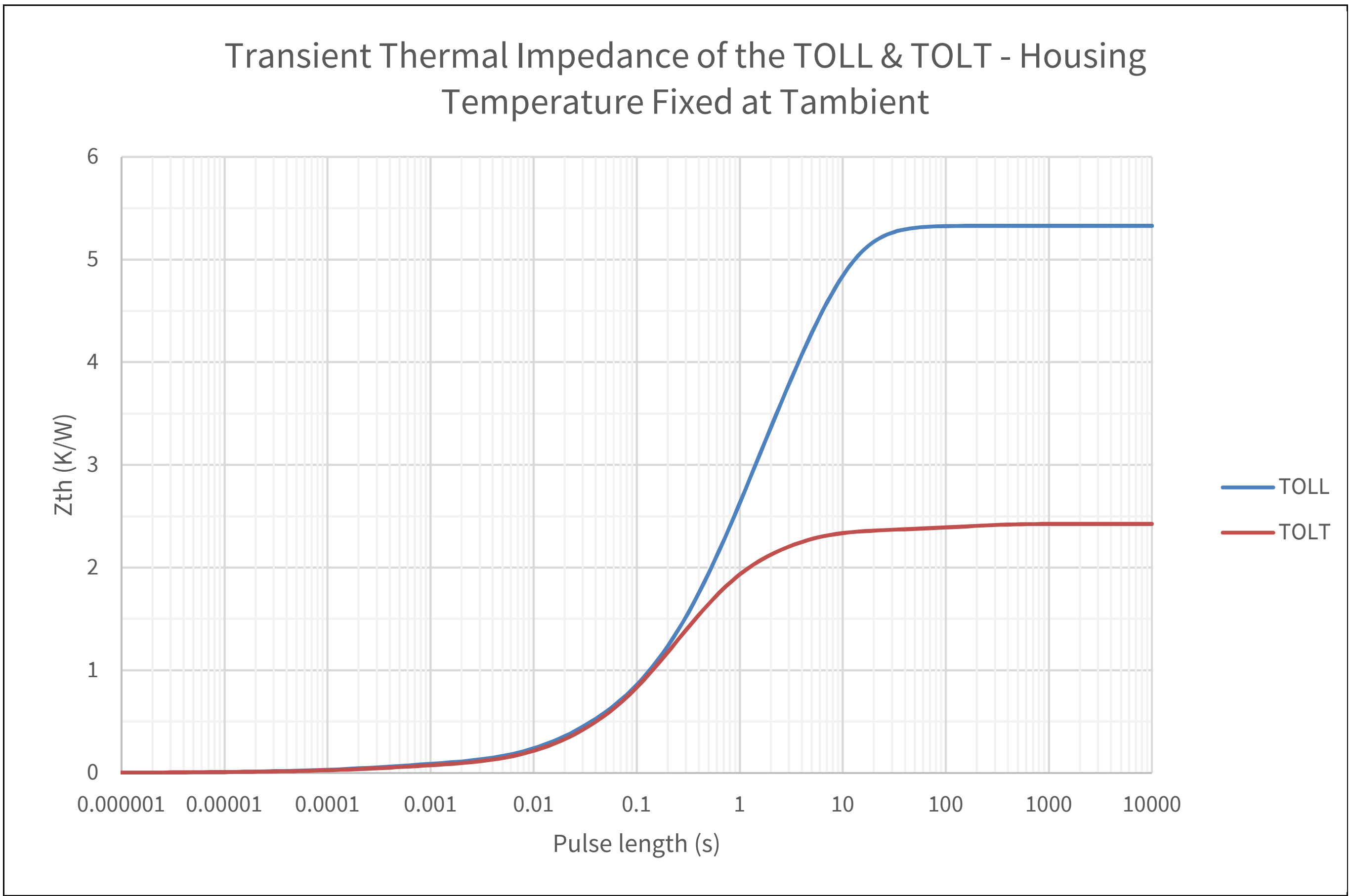


Figure 8 Transient thermal impedance (junction-ambient) of TOLL and TOLT with the housing fixed at ambient temperature

The chart shows that for pulse lengths under 0.01 s, both the TOLL and the TOLT have Zth values around 0.2 K/W. The two curves then ascend in unison up to 1 K/W for a pulse length of 0.16 s, beyond which the PCB starts having an impact on the heat flow for the TOLL and the two curves separate. The impedance curve of the TOLL continues to rise rapidly till it plateaus after about 40 s at 5.3 K/W. With the PCB taken out of the path of heat flow for the TOLT, the growth in Zth slows down much earlier than it does for the TOLL and the curve plateaus after 20 seconds at 2.4 K/W. This demonstrates that using the topside-cooled TOLT while cooling the heat sink allows reducing the Rth by over 50% compared to a similar setup with the back side-cooled TOLL.

Similar to figure 7, figure 9 below visually depicts the the TOLT's supreme thermal performance, with the heat sink fixed at ambient temperature. The enhanced thermal performance can be observed in the diagram below, with the TOLT chip barely rising 2 degrees in temperature, in contrast with the TOLL heating all the way up to 111 °C. The PCB underneath the TOLT experiences visibly less heat from the MOSFET than the the TOLL PCB does, with the TOLT enabling a 22% reduction in temperature as documented in table 2.

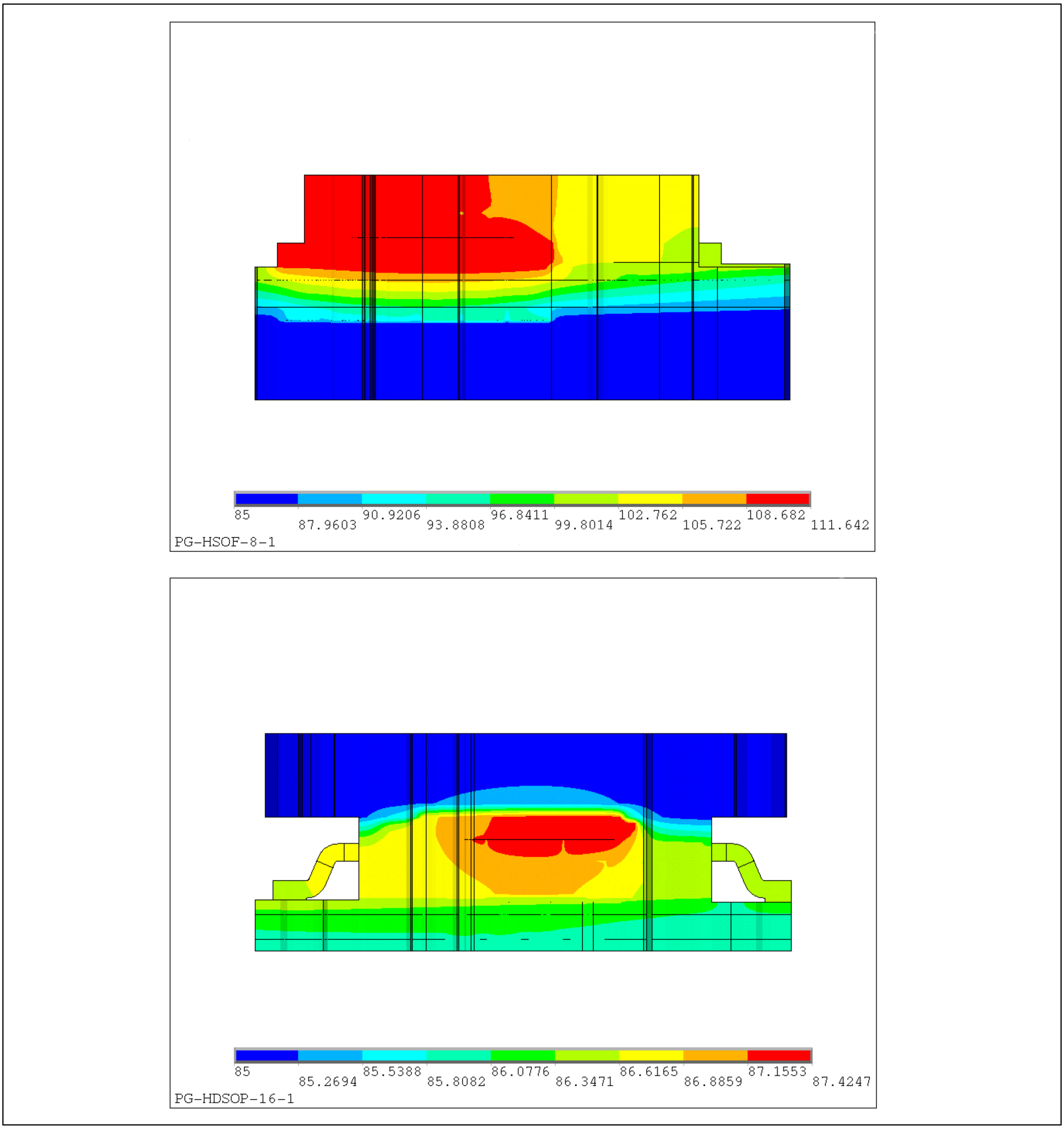


Figure 9 **Heat distribution plots for the TOLL (top) and the TOLT (bottom) with the housing fixed at ambient temperature**

Table 2 **Junction and PCB temperatures for each of the TOLL and TOLT with the housing fixed at ambient temperature**

	TOLL	TOLT	Percentage decrease
Junction temperature (°C)	111.6	87.4	22%
PCB temperature (°C)	111.1	86.6	22%

5 Afterword on impact of TIM on thermal resistance

For the TOLT results shown in sections 3 and 4, a 400 µm layer of 4 W/mK TIM is used in the simulation. The thermal performance of the TOLT depends on the thickness and the conductivity of the TIM layer chosen for the particular setup. Optimizing the TIM thickness is key for guaranteeing the best thermal performance and minimizing the thermal resistance. Typically, a thinner TIM layer means a lower Rth. Nevertheless, a more conductive TIM compensates the negative influence a thicker TIM layer may have on the Rth.

Figures 10 and 11 provide junction-ambient thermal resistance ($R_{th(ja)}$) values for the TOLT with 8 various TIM materials, ranging in conductivity from 0.7 W/mK to 15 W/mK, and with 7 different thicknesses investigated for each TIM. The power dissipated was 2 W.

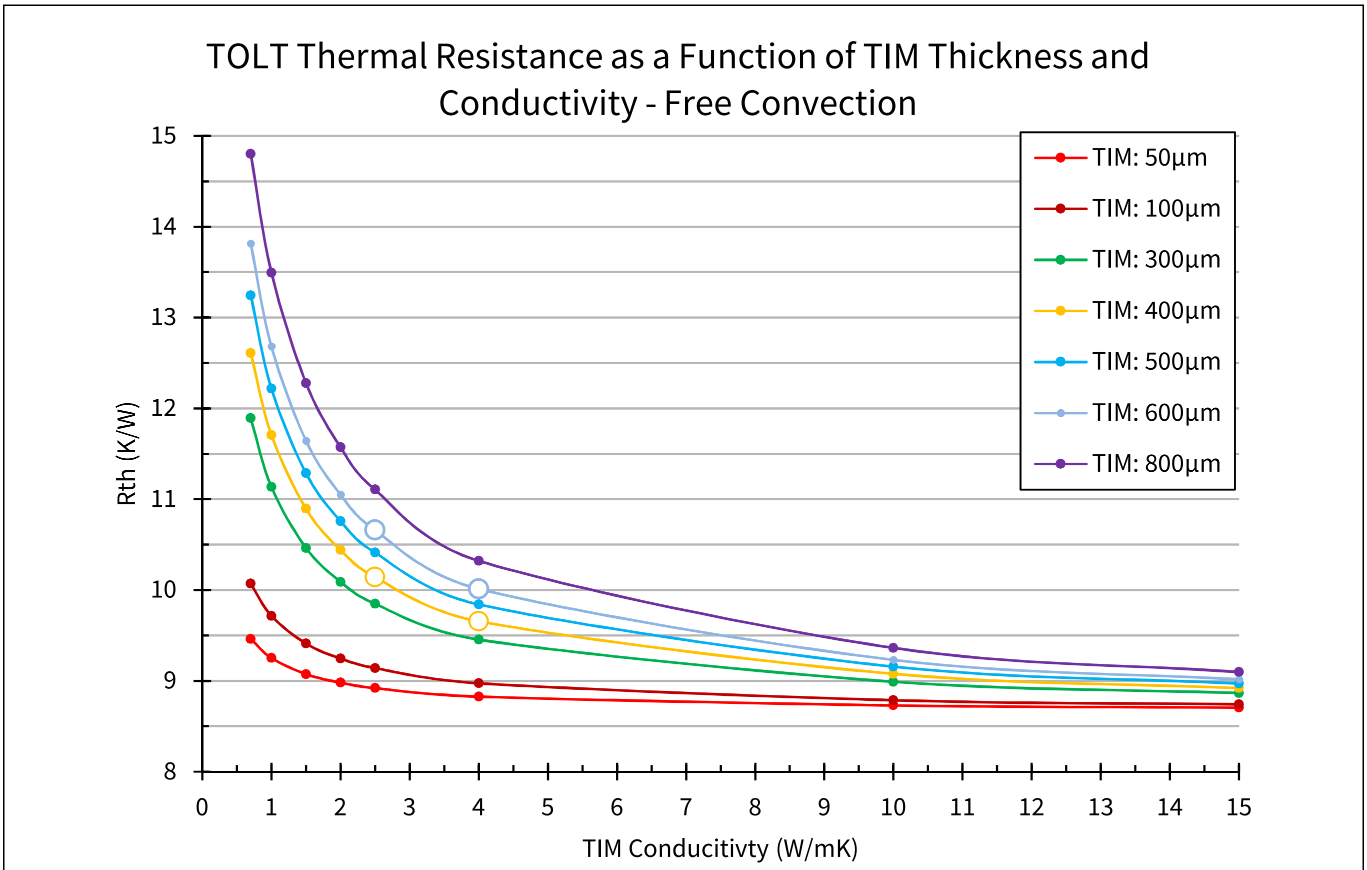


Figure 10 **Thermal ressitance (junction-ambient) of TOLT, for various TIM thicknesses and thermal conductivities, with the housing left at free convection**

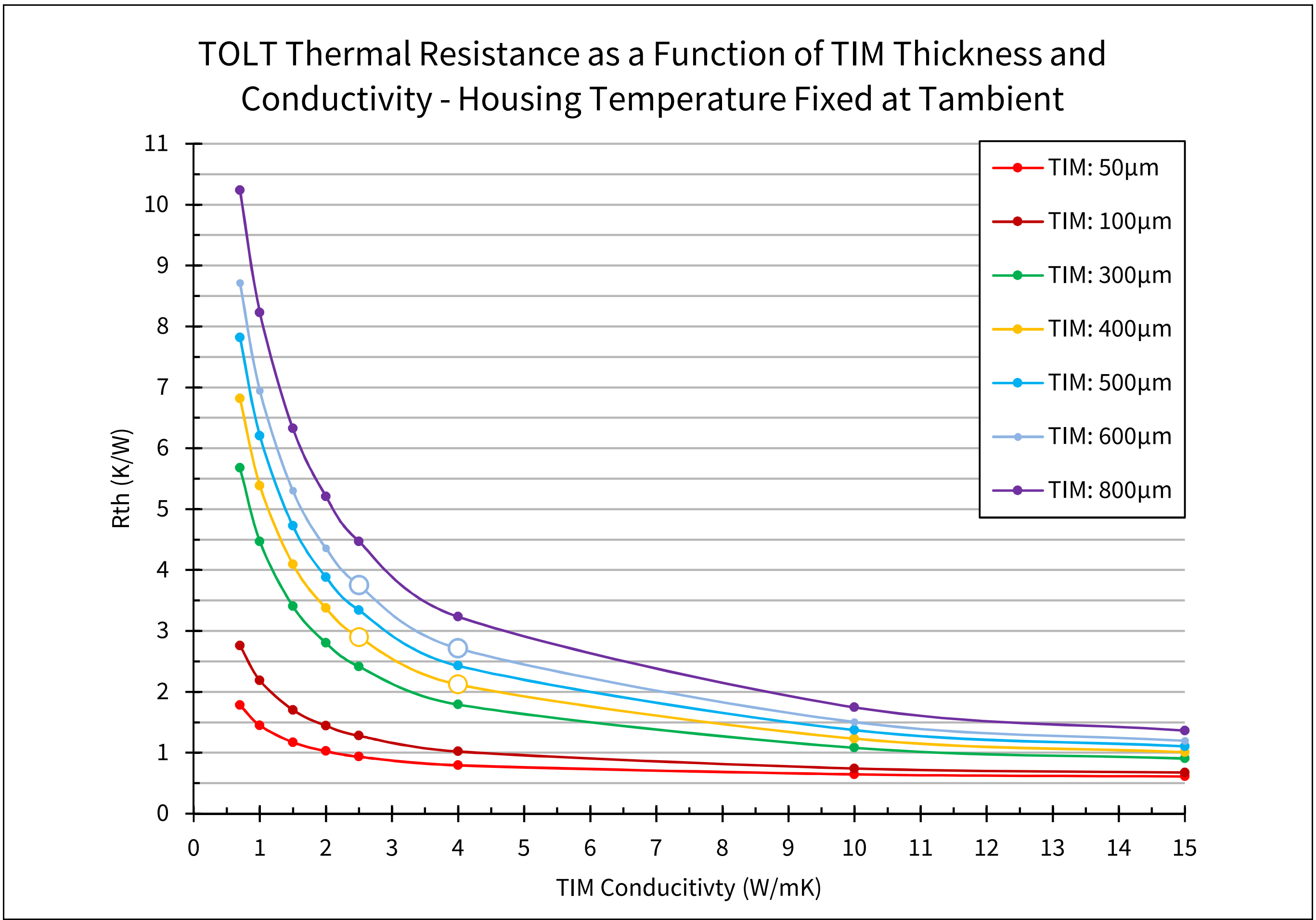


Figure 11 **Thermal resistance (junction-ambient) of TOLT, for various TIM thicknesses and thermal conductivities, with the housing fixed at ambient tempeature**

6 Conclusion

Infineon's new topside-cooled TOLT package has been specifically designed for Automotive MOSFETs to meet the demands of high-power automotive applications. The TOLT package offers a supreme thermal performance, and correspondingly an improved electrical performance, thanks to the reduced heat path from the MOSFET's chip to the heat sink. It has been shown that under similar conditions, the TOLT can achieve an $R_{th(ja)}$ reduction of up to 50% compared to the TOLL. The TOLT's enhanced performance makes it a great choice for modern, high-power automotive applications like the starter generator, the e-turbo, and the battery switch.

Revision history

Document version	Date of release	Description of changes
1.0	Aug. 16, 2021	Initial release
1.1	Jan. 10, 2022	Added heat distribution plots (figure 7, figure 9, table 1, table 2)

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