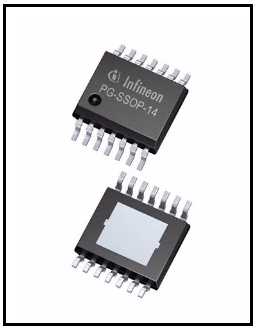
TLS820B2ELVSE

Low Dropout Linear Voltage Regulator

AEC Qualified   RoHS



Features

- Wide input voltage range from 3.0 V to 40 V
- Selectable output voltage 5 V or 3.3 V
- Output voltage precision ≤ ±2%
- Output current capability up to 200 mA
- Ultra low current consumption, typical 20 µA
- Very low dropout voltage, typical 100 mV at 100 mA
- Stable with ceramic output capacitor of 1 µF
- Enable
- Overtemperature shutdown
- Output current limitation
- Wide temperature range
- Green Product (RoHS compliant)

Potential applications

- Automotive or other supply systems that are connected to the battery permanently
- Automotive supply systems that need to operate in cranking condition

Product validation

Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

Description

The TLS820B2 is a linear voltage regulator with high performance, very low dropout linear voltage and very low quiescent current.

With an input voltage range of 3 V to 40 V and very low quiescent current of only 20 µA, this regulator is perfectly suitable for automotive or other supply systems permanently connected to the battery.

The new loop concept combines fast regulation and very high stability while requiring only one small ceramic capacitor of 1 µF at the output. At output currents below 100 mA the device will have a very low dropout voltage of only 100 mV (for 5 V output voltage) and 120 mV (for 3.3 V output voltage). The operating range starts at an input voltage of only 3 V (extended operating range). This makes the TLS820B2 suitable for automotive systems that need to operate during cranking condition.

The device can be switched on and off by the Enable feature.

The output voltage of TLS820B2ELVSE can be selected between 5 V and 3.3 V by connecting the SEL pin to V_Q or GND. When the SEL pin is connected to V_Q, the regulator's output is set to 5 V; when the SEL pin is connected to GND, the regulator's output is set to 3.3 V.

Internal protection features like output current limitation and overtemperature shutdown protect the device from immediate damage due to failures such as output shorted to GND, overcurrent and overtemperature.

External components

An input capacitor C_I is recommended to compensate line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. TLS820B2ELVSE is designed to be stable with low ESR ceramic capacitors.

Type	Package	Marking
TLS820B2ELVSE	PG-SSOP-14	820B2VSE

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1 Block diagram

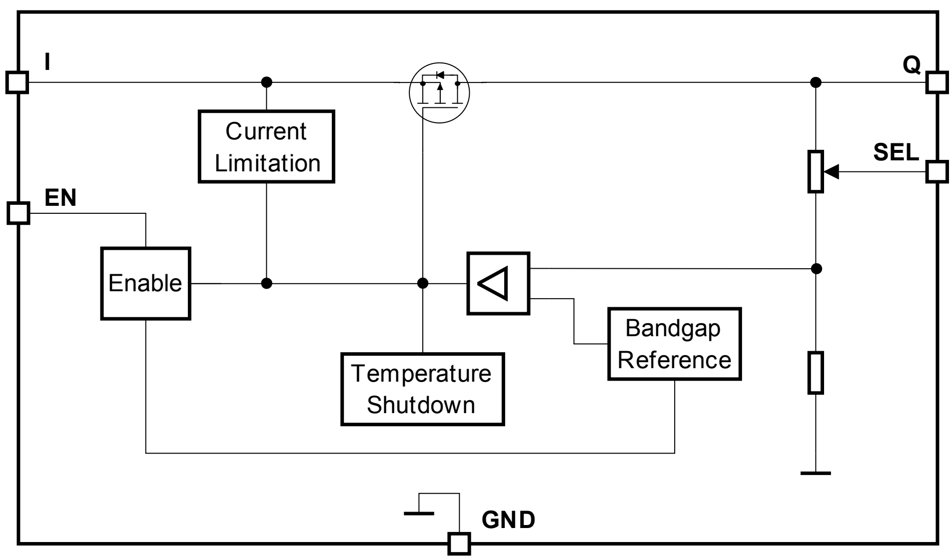


Figure 1 Block diagram TLS820B2

2 Pin configuration

2.1 Pin assignment TLS820B2ELVSE

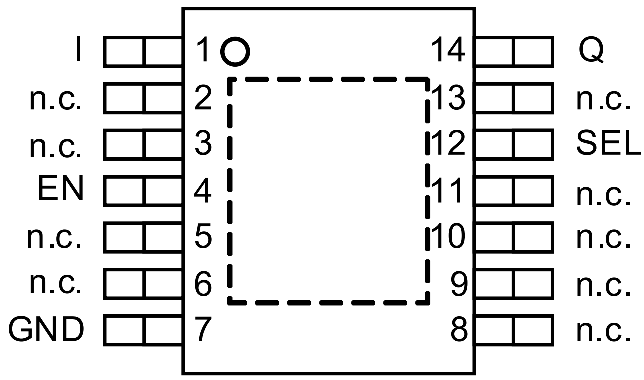


Figure 2 Pin configuration TLS820B2ELVSE

2.2 Pin definitions and functions TLS820B2ELVSE

Pin	Symbol	Function
1	I	**Input** It is recommended to place a small ceramic capacitor to GND, close to the pins, in order to compensate line influences.
2	n. c.	**Not connected** Leave open or connect to GND
3	n. c.	**Not connected** Leave open or connect to GND
4	EN	**Enable** (integrated pull-down resistor) Enable the IC with high level input signal; Disable the IC with low level input signal.
5	n. c.	**Not connected** Leave open or connect to GND
6	n. c.	**Not connected** Leave open or connect to GND
7	GND	**Ground**
8	n. c.	**Not Connected** Leave open or connect to GND
9	n. c.	**Not connected** Leave open or connect to GND
10	n. c.	**Not connected** Leave open or connect to GND
11	n. c.	**Not connected** Leave open or connect to GND

Pin configuration

Pin	Symbol	Function
12	SEL	**Output voltage selection** Connect to Q to select 5 V output voltage; Connect to GND to select 3.3 V output voltage.
13	n. c.	**Not connected** Leave open or connect to GND
14	Q	**Output voltage** Connect output capacitor C_Q to GND close to the pin, respecting the values specified for its capacitance and ESR in **“Functional range” on Page 8**.
Pad	–	**Exposed pad** Connect to heatsink area; Connect to GND

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I, Enable EN							
Voltage	V_I, V_{EN}	-0.3	–	45	V	–	P_4.1.1
Output Q							
Voltage	V_Q	-0.3	–	7	V	–	P_4.1.2
Select SEL							
voltage	V_{SEL}	-0.3	–	7	V	–	P_4.1.3
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.5
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.6
ESD absorption							
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	[2)] HBM	P_4.1.7
ESD susceptibility to GND	V_{ESD}	-750	–	750	V	[3)] CDM at all pins	P_4.1.8

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. *Exceeding the absolute max ratings may cause permanent damage to the device and affects the device’s reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 2 Functional range

T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage range	V_I	$V_{Q,nom} + V_{dr}$	–	40	V	[1] –	P_4.2.1
Extended input voltage range	$V_{I,ext}$	3.0	–	40	V	[2] –	P_4.2.2
Enable voltage range	V_{EN}	0	–	40	V	–	P_4.2.3
Capacitance of output capacitor for Stability	C_Q	1	–	–	µF	[3][4] –	P_4.2.4
Equivalent Series Resistance of output capacitor	$ESR(C_Q)$	–	–	50	Ω	[3] –	P_4.2.5
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.6

1) Output current is limited internally and depends on the input voltage, see Electrical Characteristics for more details.
2) If $V_{I,ext,min} \leq V_I \leq V_{Q,nom} + V_{dr}$, then $V_Q = V_I - V_{dr}$. If $V_I < V_{I,ext,min}$, then V_Q can drop to 0 V.
3) Not subject to production test, specified by design.
4) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Table 3 Thermal resistanceTLS820B2ELVSEPG-SSOP-14 Package

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	10	–	K/W	[1] –	P_4.3.1
Junction to ambient	R_{thJA}	–	41	–	K/W	[1][2] 2s2p board	P_4.3.2
Junction to ambient	R_{thJA}	–	125	–	K/W	[1][3] 1s0p board, footprint only	P_4.3.3
Junction to ambient	R_{thJA}	–	59	–	K/W	[1][3] 1s0p board, 300 mm² heatsink area on PCB	P_4.3.4
Junction to ambient	R_{thJA}	–	51	–	K/W	[1][3] 1s0p board, 600 mm² heatsink area on PCB	P_4.3.5

1) Not subject to production test, specified by design
2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 × 70 µm Cu).

4 Block description and electrical characteristics

4.1 Voltage regulation

The output voltage V_Q is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and the pass transistor is driven accordingly.

The control loop stability depends on the following factors:

- output capacitor C_Q
- load current
- chip temperature
- internal circuit design

Output capacitor

To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor (ESR) requirements given in **"Functional range" on Page 8** must be maintained. Because the output capacitor must buffer load steps, it should be sized according to the requirements of the application.

Input capacitors, reverse polarity protection diode

An input capacitor C_I is recommended to compensate line influences.

In order to block influences such as pulses and high frequency distortion at the input, an additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the component's terminals.

Smooth ramp up

In order to prevent overshoots during startup, a smooth ramp up function is implemented. This ensures almost no output voltage overshoots during startup, mostly independent from load and output capacitance.

Output current limitation

If the load current exceeds the specified limit, for example due to a short circuit, then the output current is limited and the output voltage decreases.

Overtemperature shutdown

The overtemperature shutdown circuit prevents the IC from immediate destruction in fault condition (for example a permanent short-circuit at the output) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the IC's life time.

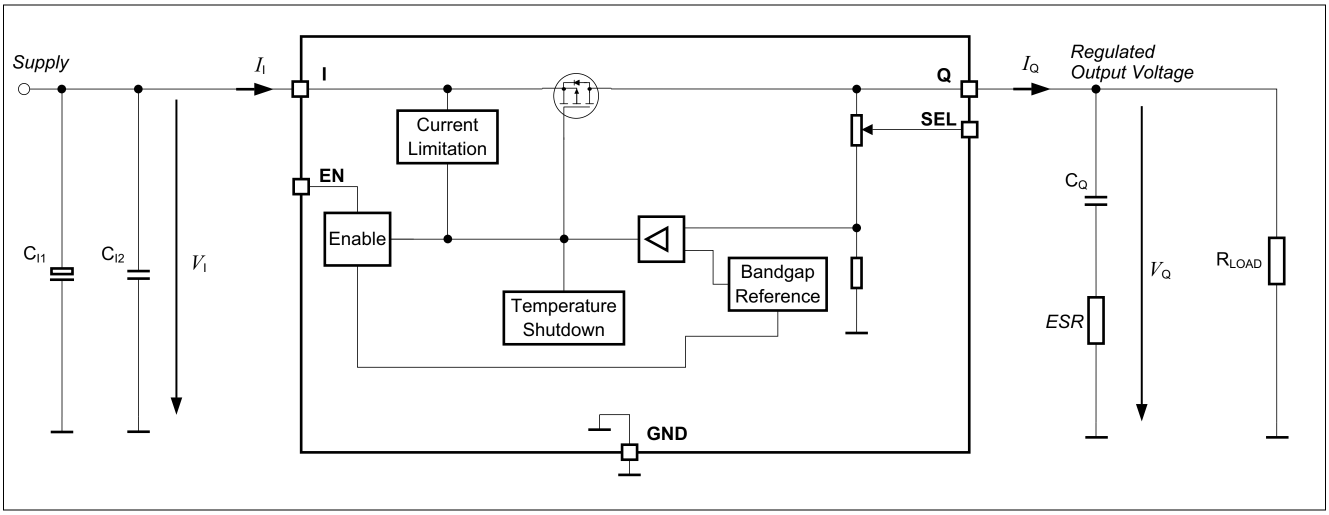


Figure 3 Voltager regulation

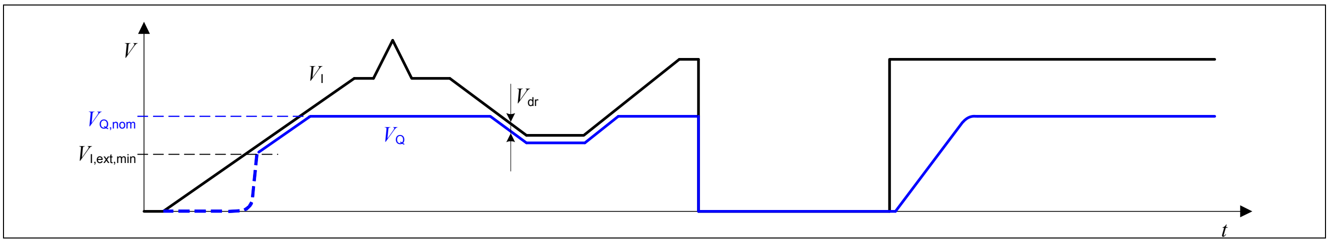


Figure 4 Output voltage vs. input voltage

Table 4 Electrical characteristics voltage regulator

T_j = -40°C to +150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
5V output voltage							
Output voltage accuracy	V_Q	4.9	5.0	5.1	V	0.05 mA ≤ I_Q ≤ 200 mA 5.5 V ≤ V_I ≤ 28 V SEL connected to Q	P_5.1.1
Output voltage accuracy	V_Q	4.9	5.0	5.1	V	0.05 mA ≤ I_Q ≤ 100 mA 5.3 V ≤ V_I ≤ 40 V SEL connected to Q	P_5.1.2
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	200	400	mV	[1] I_Q = 200 mA, SEL connected to Q	P_5.1.8
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	100	200	mV	[1] I_Q = 100 mA, SEL connected to Q	P_5.1.9
Power Supply Ripple Rejection	*PSRR*	–	60	–	dB	[2] f_{ripple} = 100 Hz V_{ripple} = 0.5 V_{pp} I_Q = 10 mA SEL connected to Q	P_5.1.10
3.3V output voltage							
Output voltage accuracy	V_Q	3.23	3.3	3.37	V	0.05 mA ≤ I_Q ≤ 200 mA 3.85 V ≤ V_I ≤ 28 V SEL connected to GND	P_5.1.12
Output voltage accuracy	V_Q	3.23	3.3	3.37	V	0.05 mA ≤ I_Q ≤ 100 mA 3.61 V ≤ V_I ≤ 40 V SEL connected to GND	P_5.1.13
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	240	480	mV	[1] I_Q = 200 mA, SEL connected to GND	P_5.1.19
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	120	240	mV	[1] I_Q = 100 mA, SEL connected to GND	P_5.1.20
Power Supply Ripple Rejection	*PSRR*	–	63	–	dB	[2] f_{ripple} = 100 Hz V_{ripple} = 0.5 V_{pp} I_Q= 10 mA SEL connected to GND	P_5.1.21
Other electrical characteristics							
Output current limitation	$I_{Q,max}$	201	350	550	mA	0 V < V_Q < $V_{Q,nom}$ - 0.1 V	P_5.1.23
Load regulation steady-state	$\Delta V_{Q,load}$	-15	-5	–	mV	I_Q = 0.05 mA to 200 mA V_I = 6.5 V	P_5.1.29
Line regulation steady-state	$\Delta V_{Q,line}$	–	1	10	mV	V_I = 8 V to 32 V I_Q = 5 mA	P_5.1.30

Table 4 Electrical characteristics voltage regulator (cont'd)

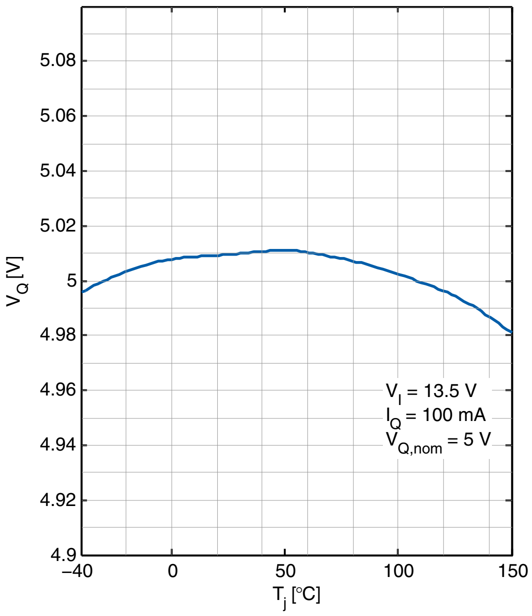
T_j = -40°C to +150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Overtemperature shutdown threshold	$T_{j,sd}$	151	175	200	°C	[2] T_j increasing	P_5.1.31
Overtemperature shutdown threshold hysteresis	$T_{j,sdh}$	–	15	–	K	[2] T_j decreasing	P_5.1.32

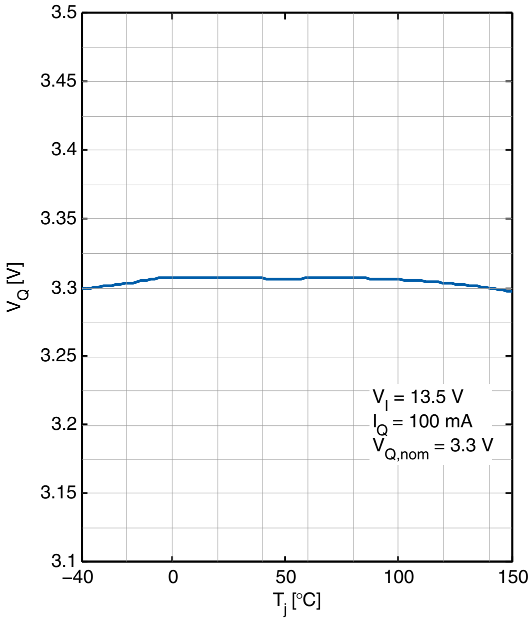
1) Measured when the output voltage V_Q has dropped by 100 mV while input voltage was gradually decreased.
2) Not subject to production test, specified by design

4.2 Typical performance characteristics voltage regulator

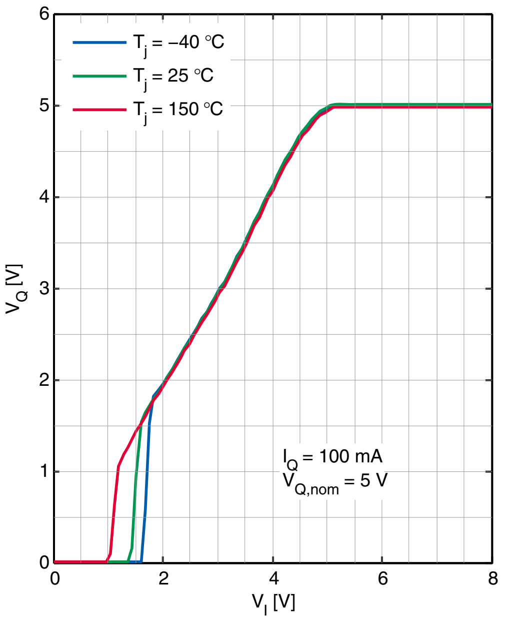
Output voltage V_Q versus junction temperature T_j



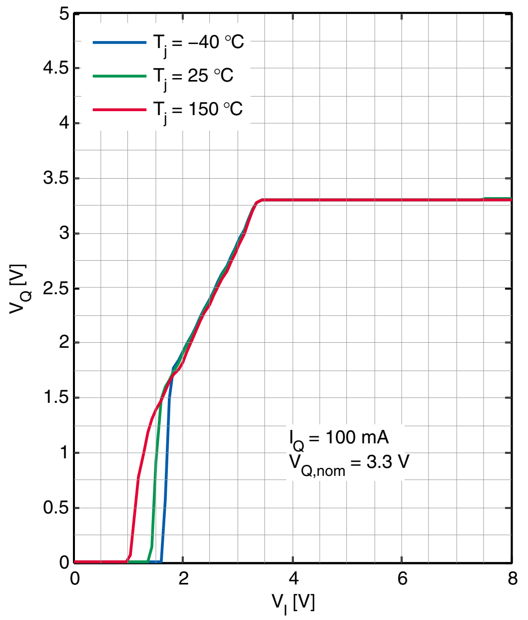
Output voltage V_Q versus junction temperature T_j



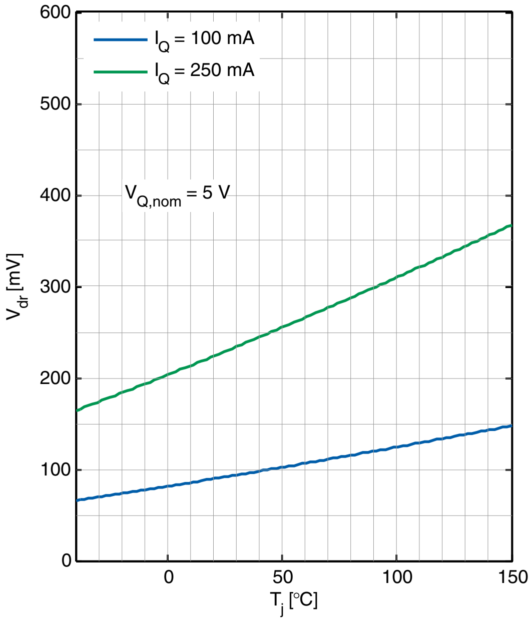
Output Voltage V_Q versus Input Voltage V_I



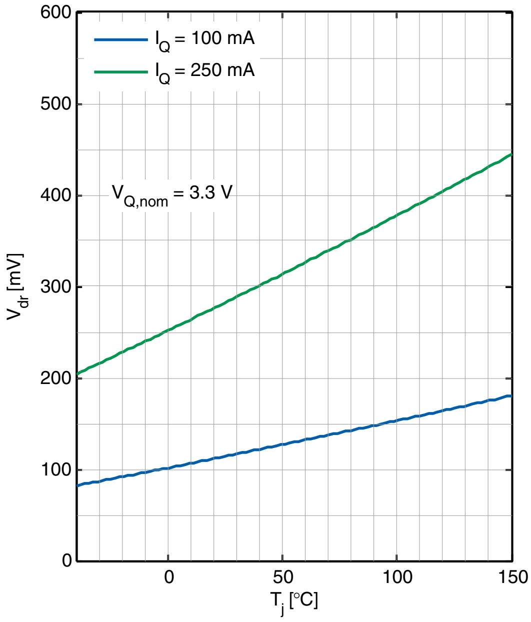
Output Voltage V_Q versus Input Voltage V_I



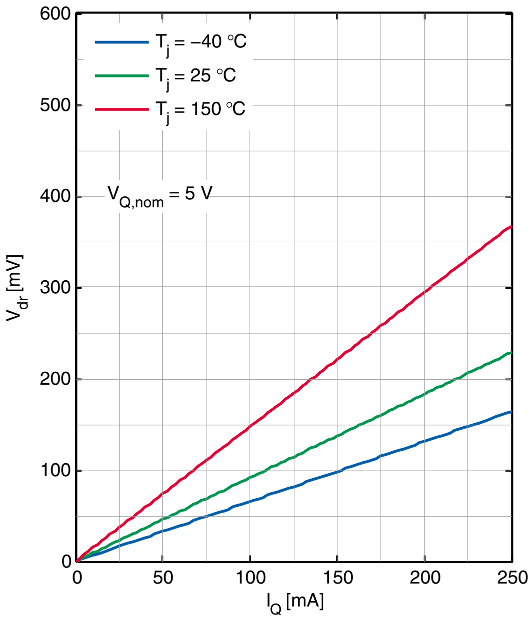
Dropout voltage V_{dr} versus junction temperature T_j



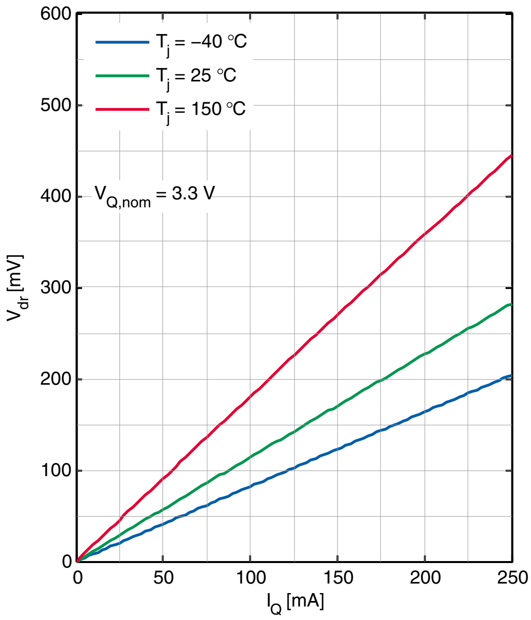
Dropout voltage V_{dr} versus junction temperature T_j



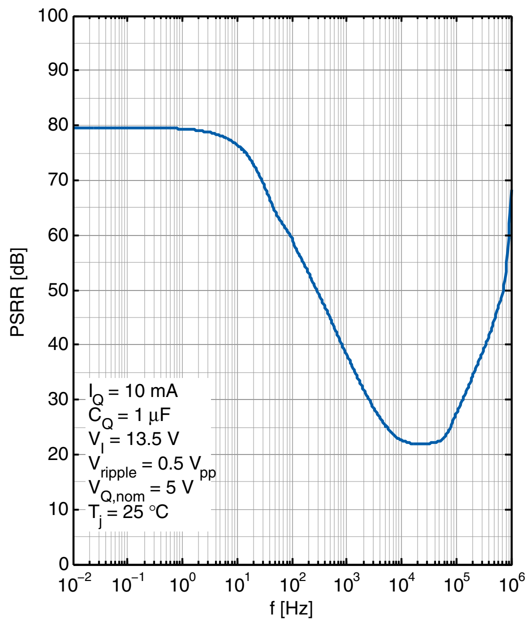
Dropout voltage V_{dr} versus Output Current I_Q



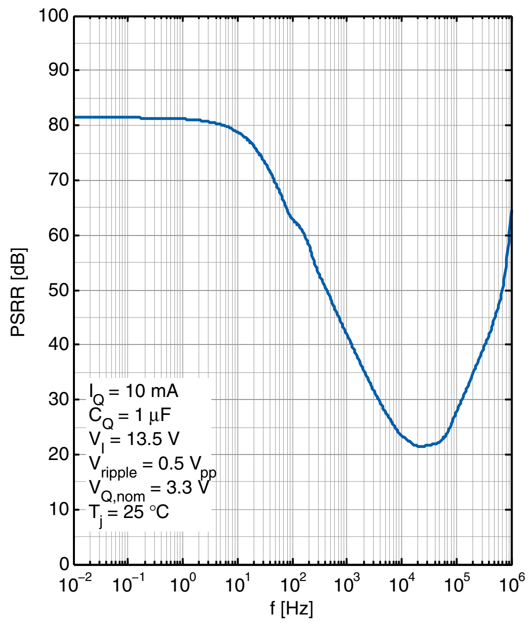
Dropout voltage V_{dr} versus Output Current I_Q



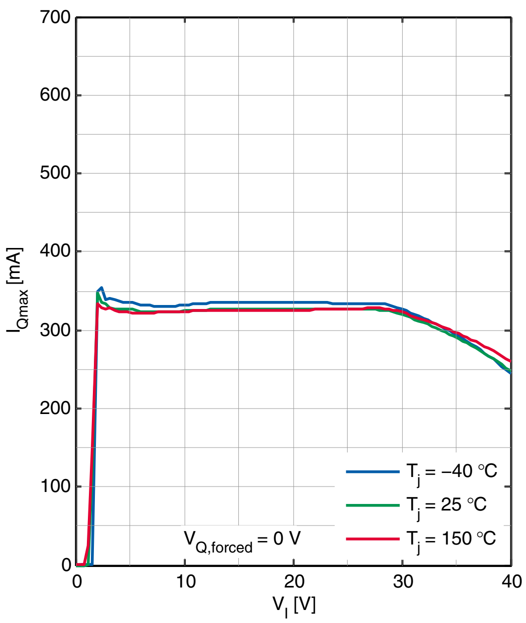
Power Supply Ripple Rejection *PSRR* versus ripple frequency *f*



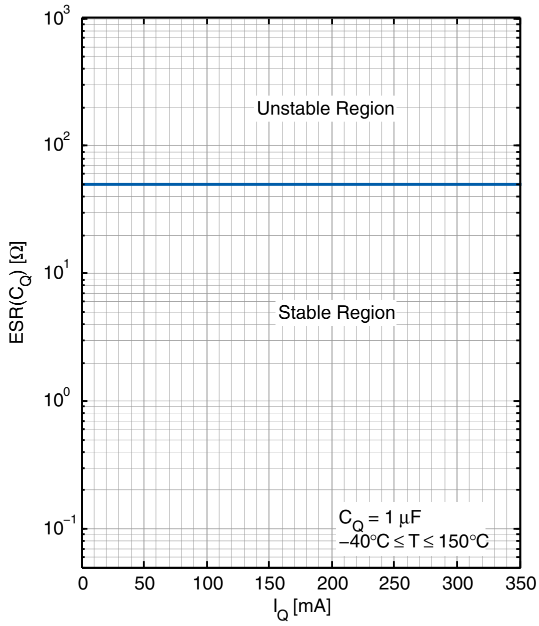
Power Supply Ripple Rejection *PSRR* versus ripple frequency *f*



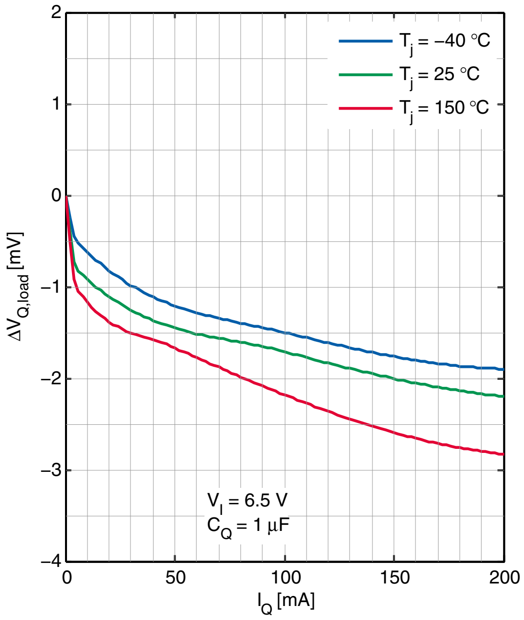
Maximum output current I_Q versus input voltage V_I



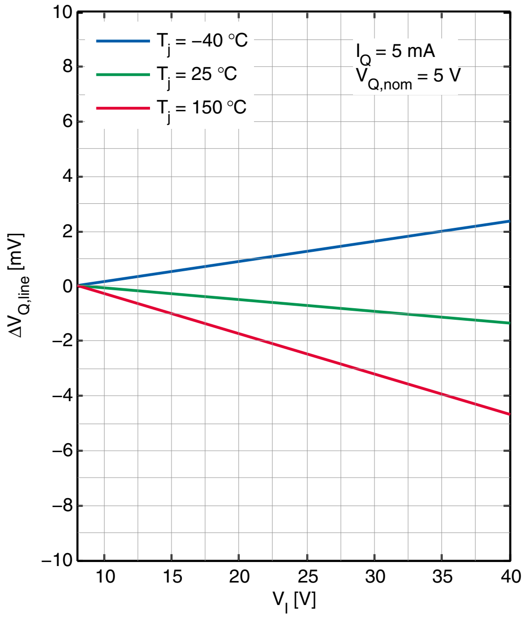
Equivalent Series Resistance of output capacitor $ESR(C_Q)$ versus output current I_Q



Load regulation $\Delta V_{Q,load}$ versus output current change I_Q



Line regulation $\Delta V_{Q,line}$ versus input voltage V_I



4.3 Current consumption

Table 5 Electrical characteristics current consumption

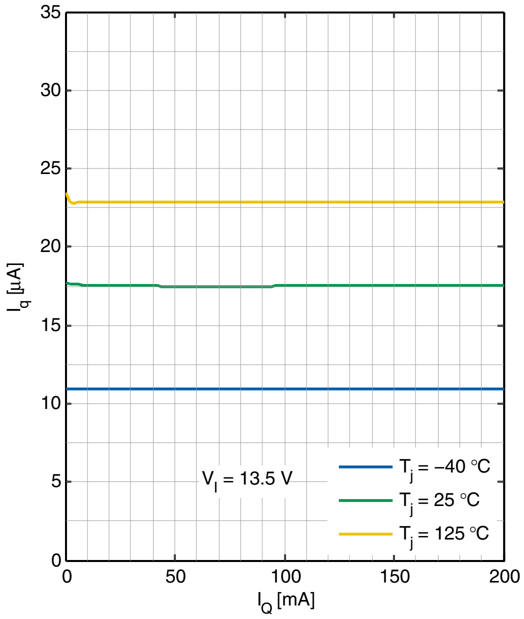
T_j = -40°C to +150°C, V_I = 13.5 V (unless otherwise specified)
Typical values are given at T_j = 25°C

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	1	µA	V_{EN} = 0 V; T_j < 105°C	P_5.3.1
Current consumption $I_q = I_I$	$I_{q,off}$	–	–	2	µA	V_{EN} = 0.4 V; T_j < 125°C	P_5.3.3
Current consumption $I_q = I_I - I_Q$	I_q	–	17	25	µA	I_Q = 0.05 mAT_j = 25°C	P_5.3.4
Current consumption $I_q = I_I - I_Q$	I_q	–	20	30	µA	I_Q = 0.05 mA T_j < 125°C	P_5.3.5
Current consumption $I_q = I_I - I_Q$	I_q	–	22	33	µA	[1] I_Q = 200 mA T_j < 125°C	P_5.3.6

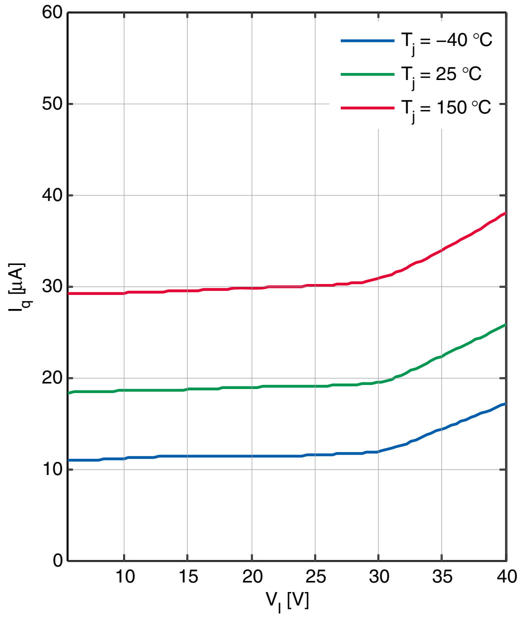
1) Not subject to production test, specified by design

4.4 Typical performance characteristics current consumption

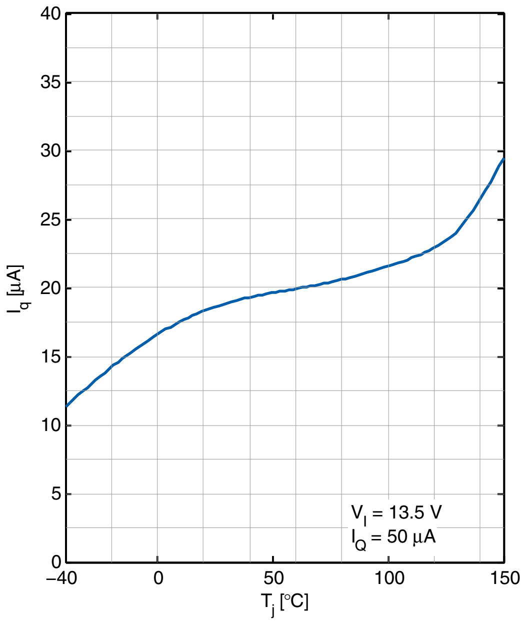
Current consumption I_q versus output current I_Q



Current consumption I_q versus input voltage V_I



Current consumption I_q versus junction temperature T_j



4.5 Enable

The TLS820B2 can be switched on and off by the enable feature. Applying a “high” level as specified below (V_{EN} ≥ 2 V) to the EN pin enables the device. Applying a “low” level as specified below (V_{EN} ≤ 0.8 V) shuts down the device. The enable feature has a built in hysteresis to avoid toggling between ON/OFF state, if a signal with slow slope is applied to the EN pin.

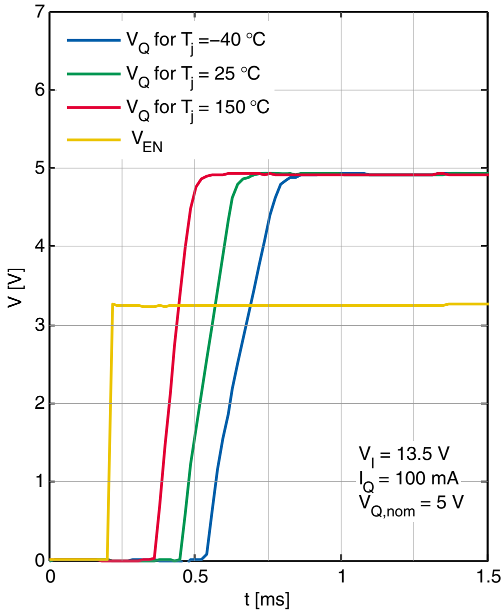
Table 6 Electrical characteristics Enable

T_j = -40°C to +150°C, V_I = 13.5 V, all voltages with respect to ground (unless otherwise specified)
Typical values are given at T_j = 25°C

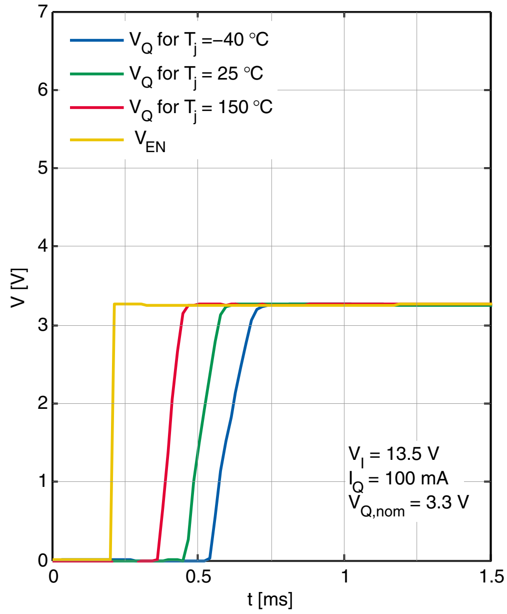
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable “high” input voltage	$V_{EN,H}$	2	–	–	V	–	P_5.5.1
Enable “low” input voltage	$V_{EN,L}$	–	–	0.8	V	–	P_5.5.2
Enable threshold hysteresis	$V_{EN,Hy}$	90	–	–	mV	–	P_5.5.3
Enable “high” input current	$I_{EN,H}$	–	–	1	µA	V_{EN} = 5 V	P_5.5.4
Enable “high” input current	$I_{EN,H}$	–	–	6	µA	V_{EN} ≤ 18 V	P_5.5.5
Enable internal pull-down resistor	R_{EN}	2.8	10	20	MΩ	–	P_5.5.6

4.6 Typical performance characteristics Enable

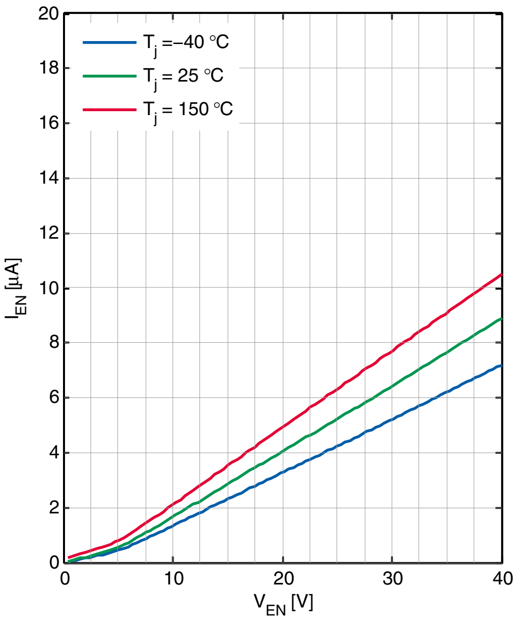
Output voltage V_Q versus time (EN switched on)



Output voltage V_Q versus time (EN switched on)



Enable input current I_{EN} versus Enable input voltage V_{EN}



4.7 Output voltage selection

The output voltage V_Q of TLS820B2ELVSE can be selected by the SEL pin:
SEL pin connected to Q: V_Q = 5 V;
SEL pin connected to GND: V_Q = 3.3 V.

5 Application information

5.1 Application diagram

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

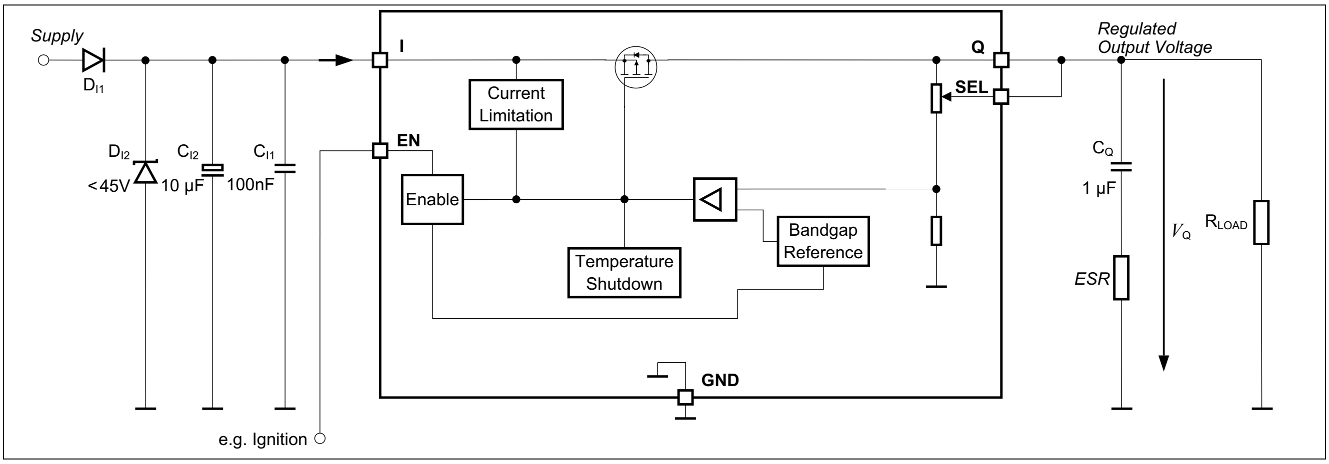


Figure 5 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

5.2 Selection of external components

5.2.1 Input pin

Figure 5 shows an exemplary input circuitry for a linear voltage regulator. A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line, for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor must be placed close to the input pin of the linear voltage regulator.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and to protect the device from damage due to overvoltage.

The external components at the input pin are optional, but they are recommended in case of possible external disturbances.

5.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators. Furthermore it serves as an energy buffer during load jumps, to compensate and maintain a constant output voltage potential. It must be dimensioned according to the applications requirements. The output capacitor's requirement is given in **"Functional range" on Page 8**.

TLS820B2 is designed to be also stable with low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the voltage regulator's output pin and GND pin and on the same side of the PCB as the regulator itself.

In case of transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

5.3 Thermal considerations

From the known input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q)I_Q + V_i I_q \tag{5.1}$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} is:

$$R_{th,JA} = \frac{T_{j,max-T_a}}{P_D} \tag{5.2}$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **"Thermal resistance" on Page 9**.

5.4 Reverse polarity protection

TLS820B2 is not protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is necessary. The absolute maximum ratings of the device as specified in **"Absolute maximum ratings" on Page 7** must be maintained.

5.5 Further application information

For further information you may contact **http://www.infineon.com/**

6 Package outlines

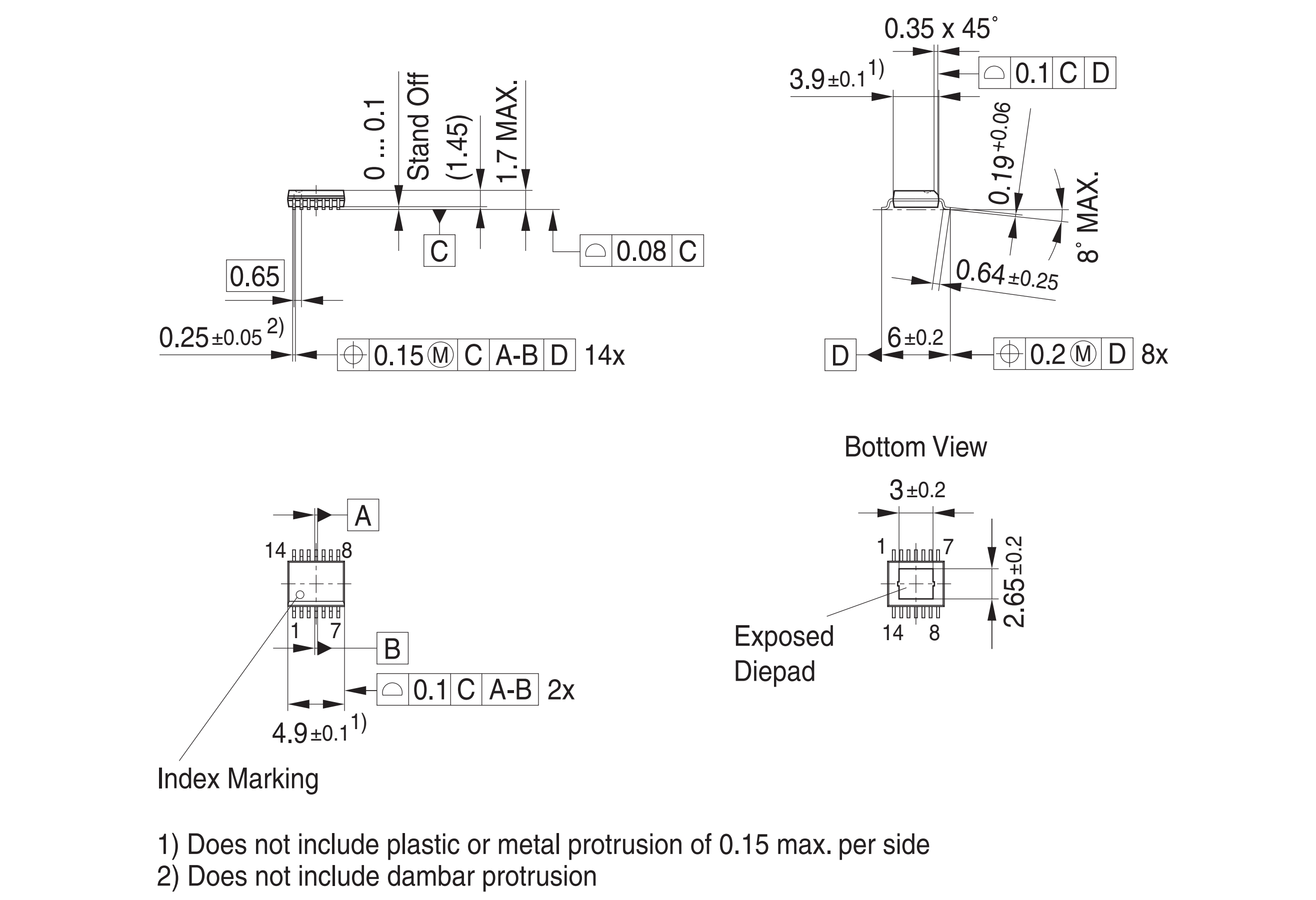


Figure 6 PG-SSOP-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

7 Revision history

Revision	Date	Changes
1.0	2018-03-20	Initial Version

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