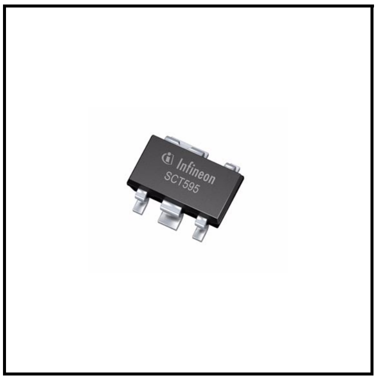
OPTIREG™ linear voltage regulator TLS202B1MBV33

Fixed linear voltage post regulator



Features

- Output voltage 3.3 V
- Output voltage accuracy of ± 3%
- Output currents up to 150 mA
- Extended input voltage operating range of 2.7 V to 18 V
- Enable functionality
- Low dropout voltage, typically 290 mV
- Very low current consumption, typically 50 µA
- Very low shutdown current, typically 0.01 µA
- Very high PSRR, typically 63 dB at 10 kHz
- Output current limitation
- Shortcircuit protected
- Overtemperature shutdown
- Wide temperature range from -40°C up to 150°C
- Suitable for use in automotive electronics as post regulator
- Green Product (RoHS-compliant)

Potential applications

Suitable for use in automotive electronics as post regulator.

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLS202B1MBV33 is a monolithic integrated fixed linear voltage post regulator for load currents up to 150 mA. The IC regulates an input voltage V_I up to 18 V to a fixed output voltage of 3.3 V with a precision of ± 3%. The TLS202B1MBV33 is especially designed for applications requiring very low standby currents, for example, with a permanent connection to the preregulators like DCDC converters. The regulator is not designed to operate with a direct connection to the battery. The component can be enabled/disabled via the Enable input. The device is available in a very small surface-mounted PG-SCT595 package. The device is designed for the harsh environment of automotive applications. Therefore, it is protected against overload, short circuit, and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLS202B1MBV33 can be also used in all other applications requiring a stabilized 3.3 V voltage.

The input capacitor C_I is recommended for compensating line influences. The output capacitor C_Q is necessary for the stability of the regulating circuit. Stability is guaranteed at values specified in **Table 3** within the whole operating temperature range.

Type	Package	Marking
TLS202B1MBV33	PG-SCT595	21

Table of contents

1 Block diagram

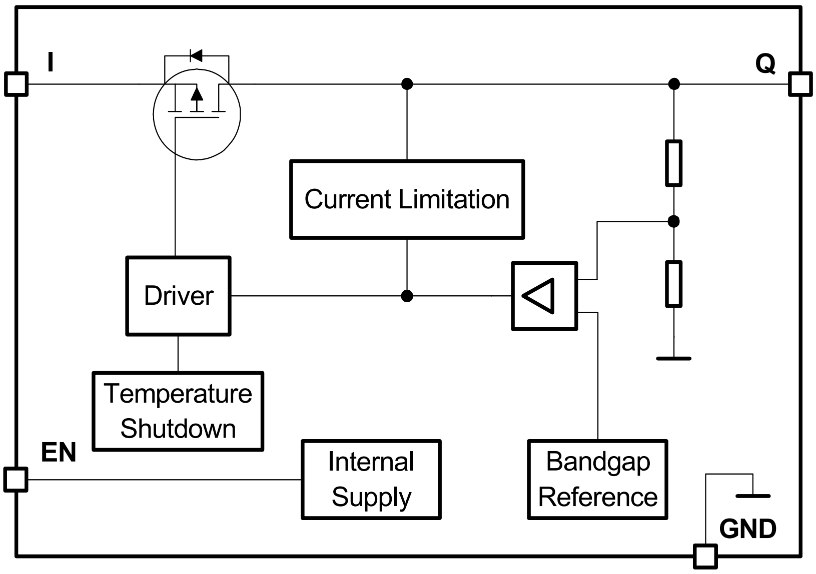


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

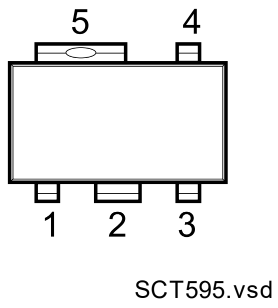


Figure 2 Pin configuration package PG-SCT595-5

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	I	**Input** IC supply. For compensating line influences, a capacitor of 220 nF close to the IC pin is recommended
2	GND	**Ground reference** Internally connected to pin 5. Connect to heatsink area. For thermal reasons, both ground pins 2 and 5 have to be soldered
3	Q	**Output** Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in **Table 3**
4	EN	**Enable** A low signal disables the IC. A high signal switches it on. Connect to the input I if the enable functionality is not required
5	GND	**Ground reference** Internally connected to pin 2. Connect to heatsink area. For thermal reasons, both ground pins 2 and 5 have to be soldered

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings [1)]

T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input I							
Voltage	V_I	-0.3	–	20	V	–	P_4.1.1
Output Q							
Voltage	V_Q	-0.3	–	5.5	V	–	P_4.1.2
Enable EN							
Voltage	V_{EN}	-0.3	–	20	V	–	P_4.1.3
Temperature							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.4
Storage temperature	T_{stg}	-50	–	150	°C	–	P_4.1.5
ESD susceptibility							
ESD absorption	$V_{ESD,HBM}$	-4	–	4	kV	[2)] Human body model (HBM)	P_4.1.6
ESD absorption	$V_{ESD,CDM}$	-750	–	750	V	[3)] Charged-device model (CDM) at all pins	P_4.1.7

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
3) ESD susceptibility, charged-device model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	2.7	–	18	V	–	P_4.2.1
Output capacitor requirements for stability	C_Q	1	–	–	µF	1)	P_4.2.2
Output capacitor requirements for stability	$ESR(C_Q)$	–	–	10	Ω	2)	P_4.2.3
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.4

1) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.
2) Relevant ESR value at f = 10 kHz.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the electrical characteristics table.

3.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to ambient	R_{thJA}	–	81	–	K/W	1) 2s2p board	P_4.3.1
Junction to ambient	R_{thJA}	–	217	–	K/W	2) Footprint only	P_4.3.2
Junction to ambient	R_{thJA}	–	117	–	K/W	2) 300 mm^2 PCB heatsink area	P_4.3.3
Junction to ambient	R_{thJA}	–	103	–	K/W	2) 600 mm^2 PCB heatsink area	P_4.3.4
Junction to soldering point	R_{thJSP}	–	30	–	K/W	Pins 2, 5 fixed to T_A	P_4.3.5

1) The specified R_{thJA} value is according to JESD51-2,-5,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array next to the package contacted to the first inner copper layer.
2) Package mounted on PCB FR4; 80 × 80 × 1.5 mm^3; 35 µm Cu, 5 µm Sn; horizontal position; zero airflow. Not subject to production test; specified by design.

4 Voltage regulator

4.1 Description voltage regulator

The output voltage V_Q is controlled as follows: It is divided by the resistor divider. This fraction is then compared to an internal reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor C_Q, the load current, the chip temperature, and the circuit design. To ensure stable operation, the requirements for output capacitance and equivalent series resistance ESR, given in **Table 3**, have to be maintained. For details see also the typical stability graph of **Output capacitor series resistance ESR(C_Q) versus output current I_Q**. As the output capacitor also has to buffer load steps, it should be sized according to the needs of the application.

An input capacitor C_I is recommended to compensate line influences. Connect the capacitors close to the terminals of the component.

In case the load current is above the specified limit, for example, in case of a short circuit, the output current limitation limits the current. The output voltage is therefore decreasing at the same time.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (for example, output continuously short-circuited) by switching off the power stage. After the chip has cooled down, the regulator restarts. This leads to an oscillatory behavior of the output voltage until the fault is removed. However, junction temperatures above 150°C are outside the maximum ratings and therefore significantly reduce the IC's lifetime.

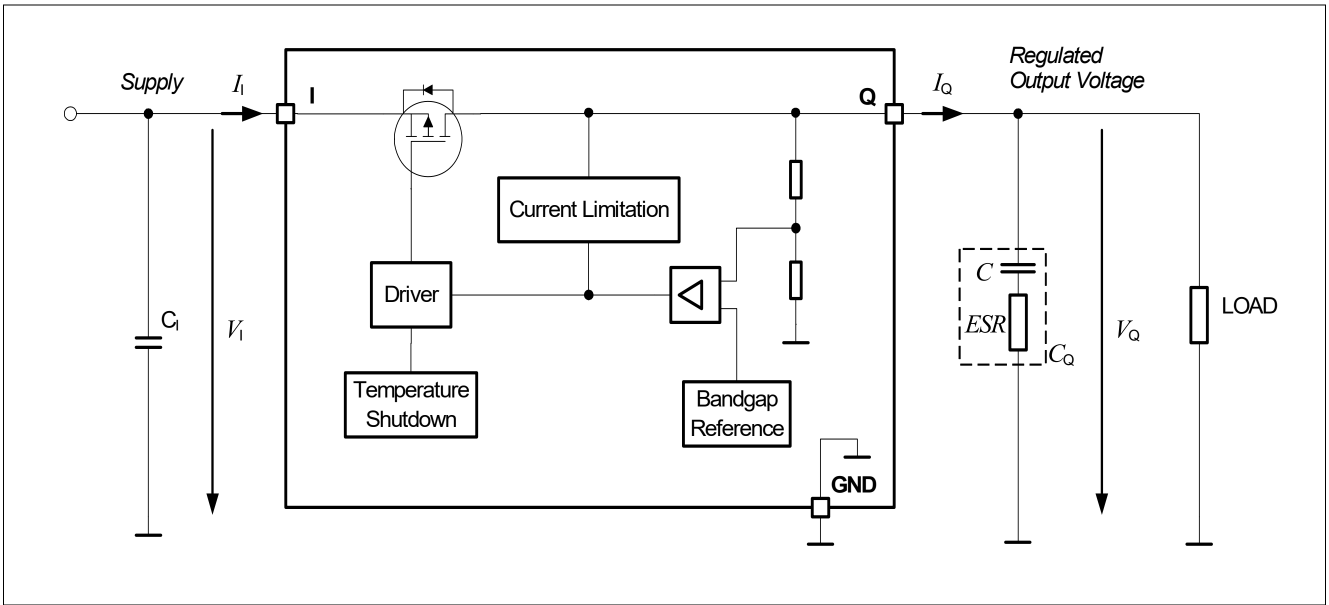


Figure 3 Block diagram voltage regulator circuit

4.2 Electrical characteristics voltage regulator

Table 5 Electrical characteristics

V_I = 4.3 V; T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage	V_Q	3.2	3.3	3.4	V	I_Q = 10 mA; T_j = 25°C	P_5.2.1
Output voltage	V_Q	3.17	3.3	3.43	V	I_Q = 10 mA	P_5.2.2
Dropout voltage	V_{dr}	–	290	570	mV	1) I_Q = 150 mA	P_5.2.3
Load regulation	ΔV_Q	-80	-25	–	mV	I_Q = 1 mA to 150 mA	P_5.2.4
Line regulation	ΔV_Q	–	1.88	37.6	mV	V_I = 4.3 V to 10 V; I_Q = 1 mA	P_5.2.5
Output current limitation	I_Q	151	300	–	mA	0 V ≤ V_Q ≤ 3.0 V	P_5.2.6
Power supply ripple rejection	PSRR	–	63	–	dB	2) f_f = 10 kHz; I_Q = 50 mA; T_j = 25°C; V_{in} = 4.3 V; ΔV_I = 1 V_{pp}; C_{out} = 1 µF (ceramic capacitor)	P_5.2.7
Overtemperature shutdown threshold	$T_{j,sd}$	151	170	190	°C	2)	P_5.2.8

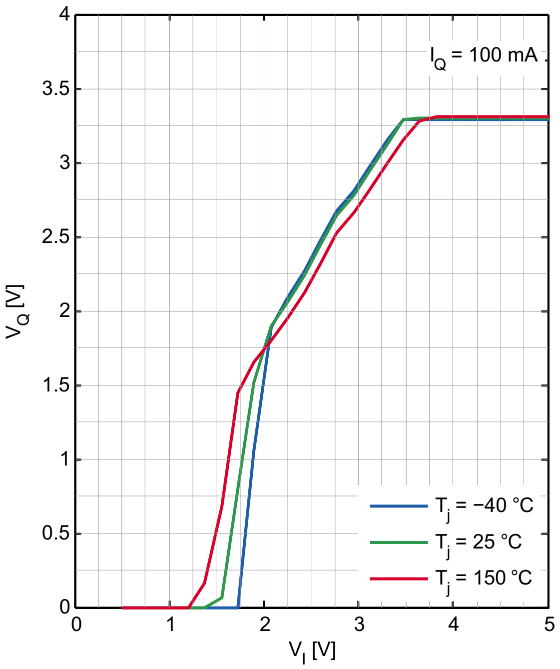
1) Dropout voltage is defined as the difference between input and output voltage when the output voltage decreases 100 mV from output voltage measured at $V_I = V_{Q,nom}$ + 1 V, I_{Load} = 150 mA.

2) Parameter is not subject to production test, specified by design.

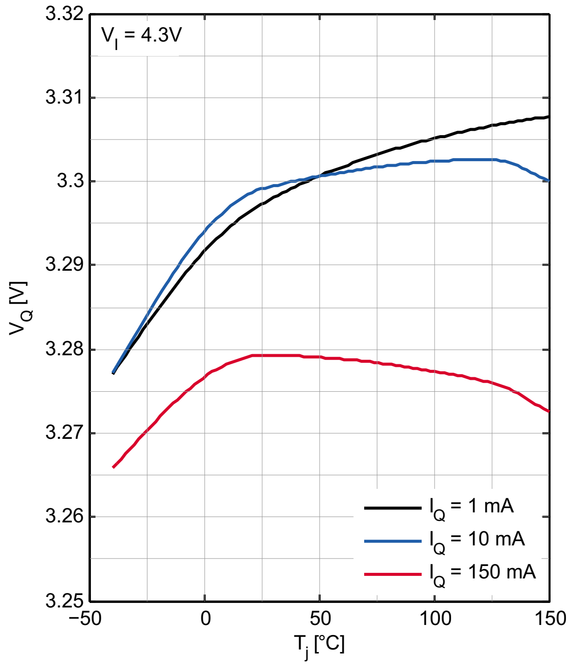
4.3 Typical performance characteristics voltage regulator

V_{EN} = 5 V (unless otherwise noted)

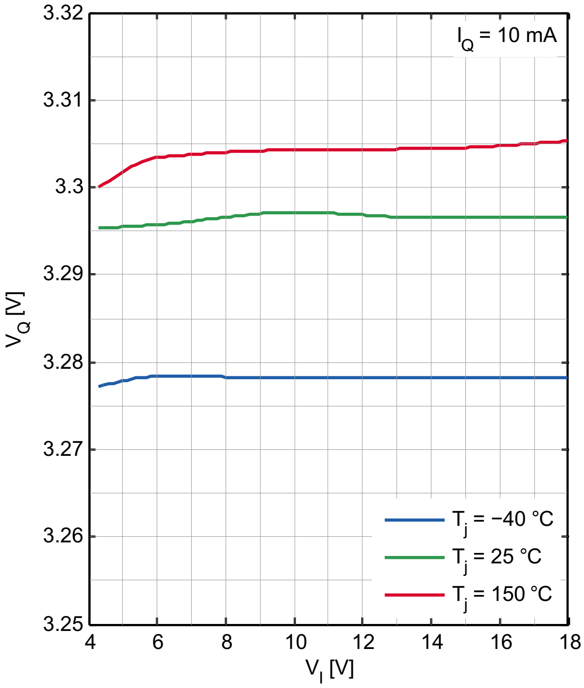
Output voltage V_Q versus input voltage V_I (



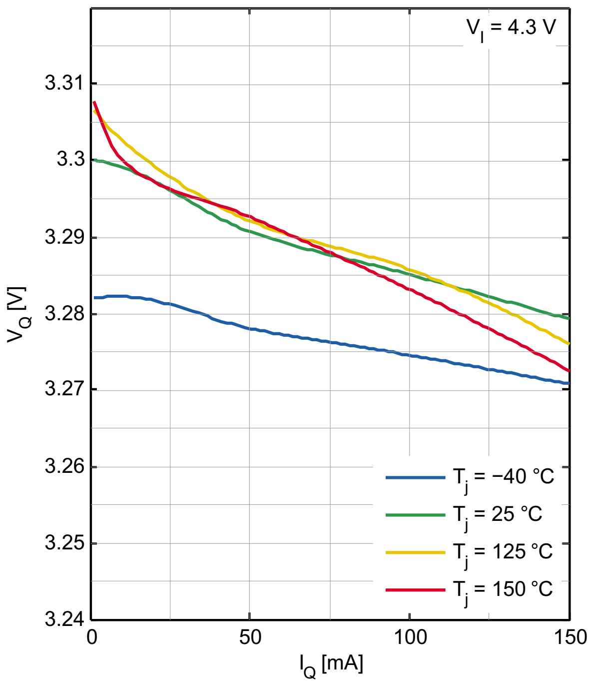
Output voltage V_Q versus junction temperature T_j



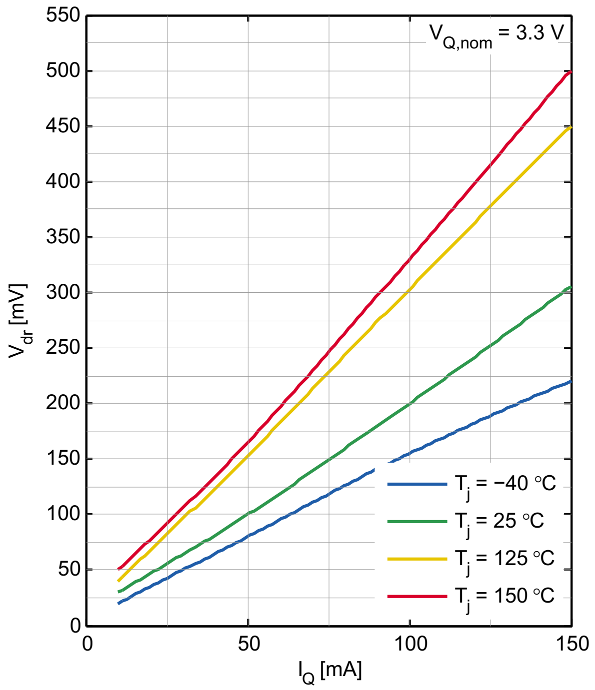
Line regulation output voltage V_Q versus input voltage V_I



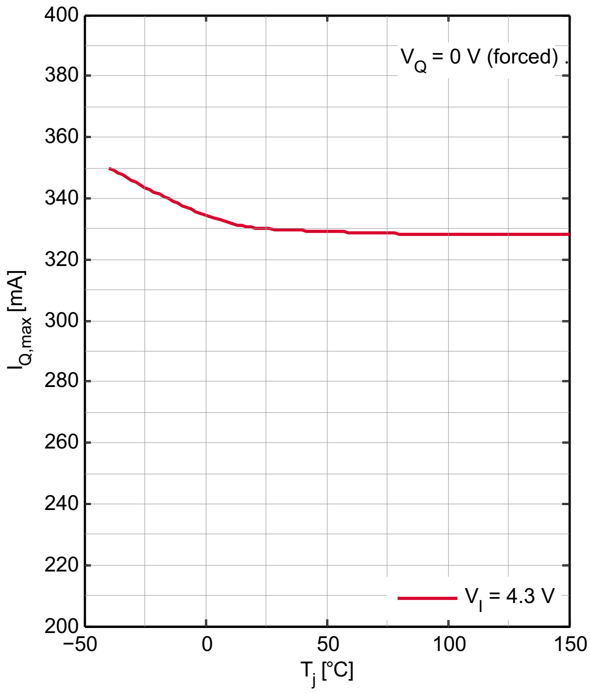
Load regulation output voltage V_Q versus load current I_Q



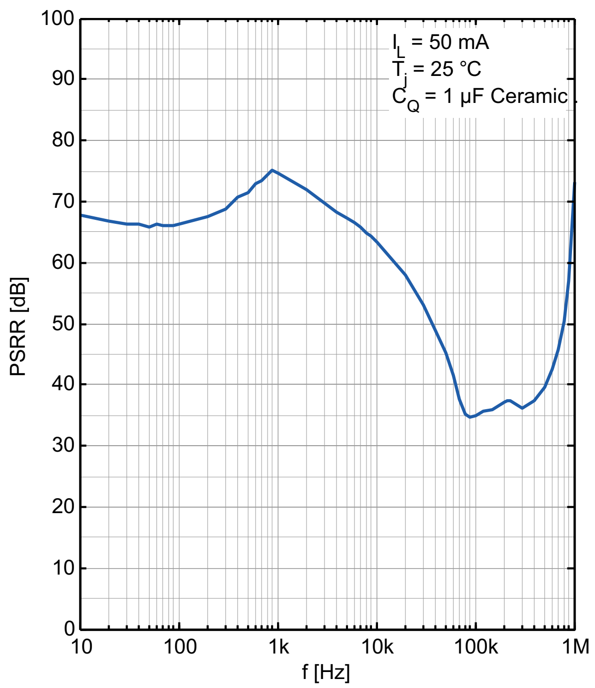
Dropout voltage V_{dr} versus load current I_Q



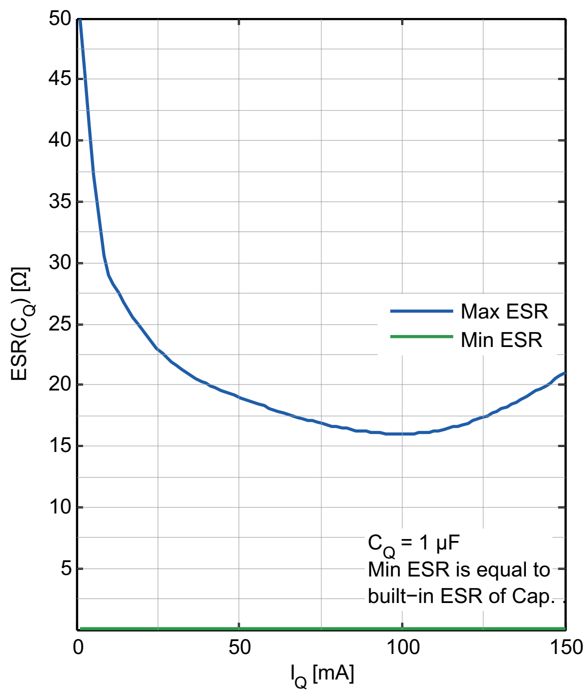
Output current limitation $I_{Q,max}$ versus junction temperature T_j



PSRR vs. frequency



Output capacitor series resistance ESR(C_Q) versus output current I_Q



5 Current consumption

5.1 Description current consumption

The current consumption of the device is characterizing the current the device needs to operate. The quiescent current is describing the current consumption in a very low load condition (for example, if the supplied microcontroller is in sleep mode). The TLS202B1MBV33 has an enable functionality to shutdown the device, in case it is not needed. During shutdown the device has a very low current consumption. The current consumption of the device can be determined by measuring the current flowing out of the GND pin and is defined as the delta between I_I and ($I_Q + I_{EN}$).

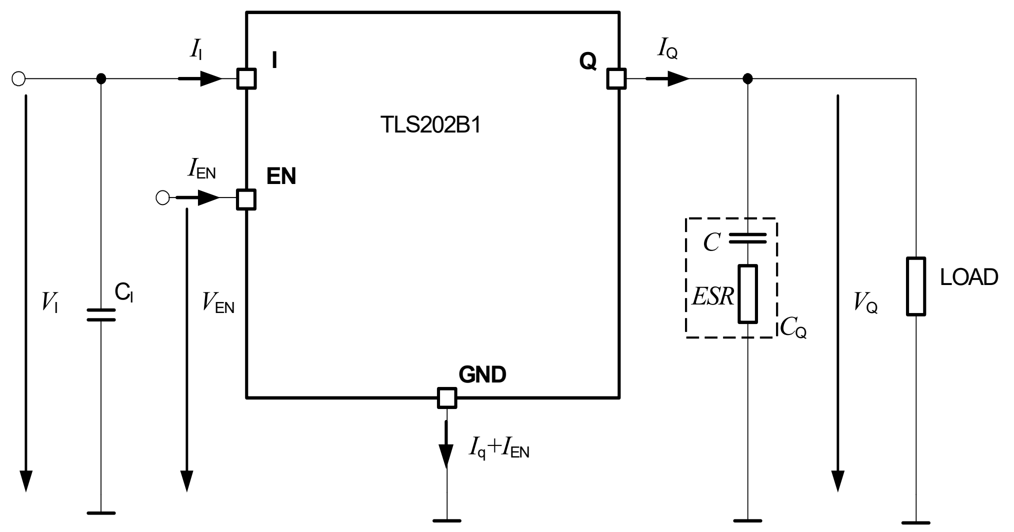


Figure 4 Parameter definitions of the current consumption

5.2 Electrical characteristics current consumption

Table 6 Electrical characteristics

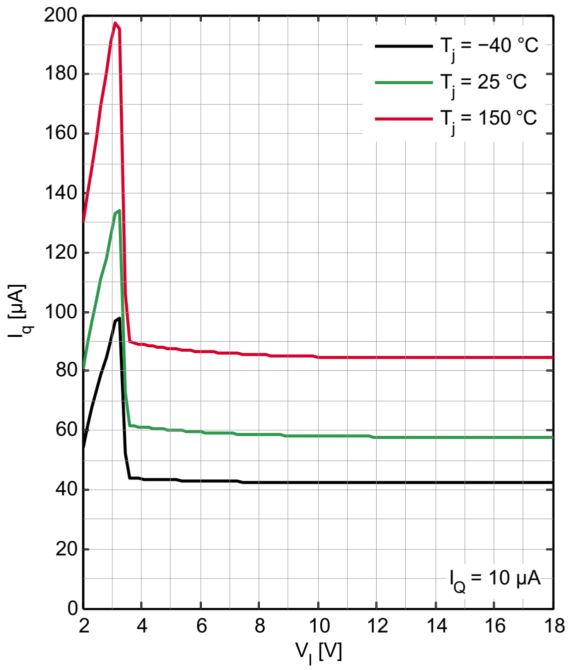
V_I = 4.3 V; T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Quiescent current $I_q = I_I - I_Q$	I_q	–	50	75	µA	I_Q = 10 µA; T_j = 25°C	P_6.2.1
Quiescent current $I_q = I_I - I_Q$	I_q	–	–	100	µA	I_Q = 10 µA; $T_j \leq$ 125°C	P_6.2.2
Current consumption $I_q = I_I - I_Q$	I_q	–	150	200	µA	I_Q = 50 mA	P_6.2.3
Quiescent current in shutdown	$I_{q,off}$	–	0.01	1	µA	V_I = 6 V; V_{EN} = 0 V; $T_j \leq$ 125°C; V_Q = 0 V	P_6.2.4

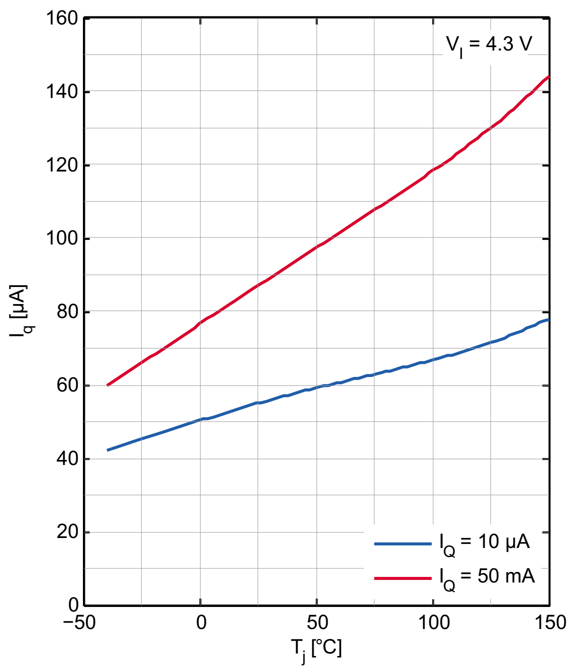
5.3 Typical performance characteristics current consumption

V_{EN} = 5 V (unless otherwise noted)

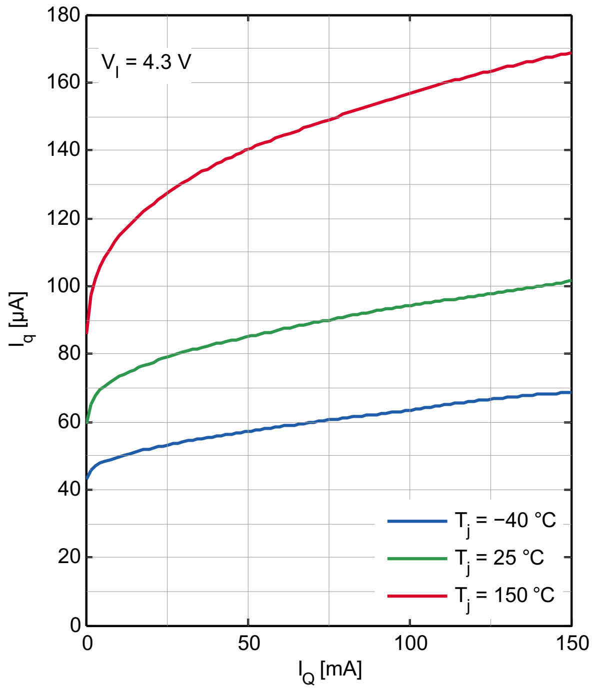
Quiescent current I_q versus input voltage V_I



Current consumption I_q versus junction temperature T_j



Current consumption I_q versus load current I_Q



6 Enable function

6.1 Description of the enable function

The TLS202B1MBV33 can be turned on or turned off by the EN input. The parameter V_{EN} is the voltage provided to the EN pin as shown in **Figure 4**.

With voltage levels lower than $V_{EN,Lo}$ applied to the EN input, the device will be turned off. During this state, the device is in shutdown with a very low current consumption $I_{q,off}$.

Changing the voltage at the EN input from $V_{EN,Hi}$ to $V_{EN,Lo}$ will trigger the start-up of the device. For voltages higher than $V_{EN,Hi}$, the device will regulate the output voltage to the nominal value as described in **Chapter 4**.

6.2 Electrical characteristics enable function

Table 7 Electrical characteristics

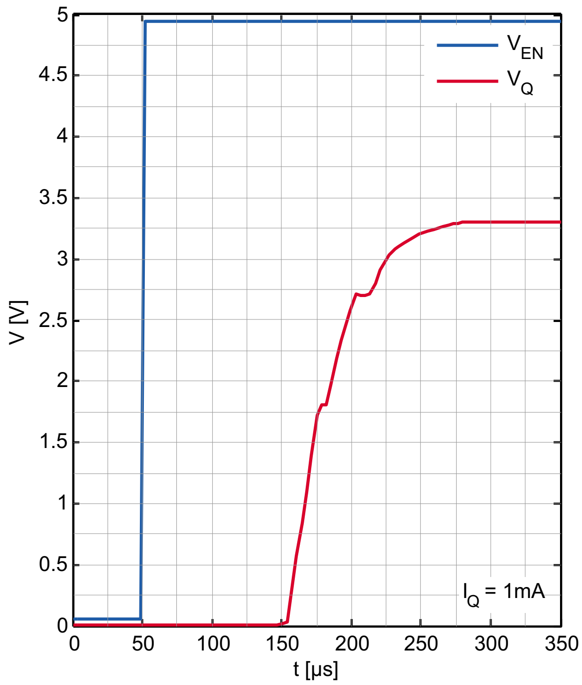
V_I = 4.3 V; T_j = -40°C to +150°C; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable high voltage level	$V_{EN,Hi}$	2	–	–	V	$V_{Q,on} \geq 3.135$ V	P_7.2.1
Enable low voltage level	$V_{EN,Lo}$	–	–	0.4	V	$V_{Q,off} \leq 200$ mV	P_7.2.2
Enable pin current	I_{EN}	–	–	5	µA	1) V_{EN} = 5 V	P_7.2.3

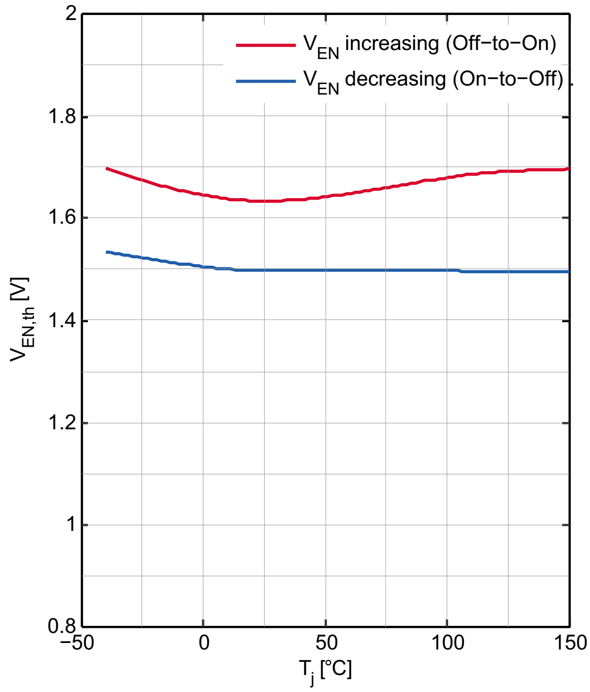
1) Enable pin current flows into the EN pin.

6.3 Typical performance characteristics enable function

Power-up timing



Enable thresholds V_{EN} versus junction temperature T_j



7 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

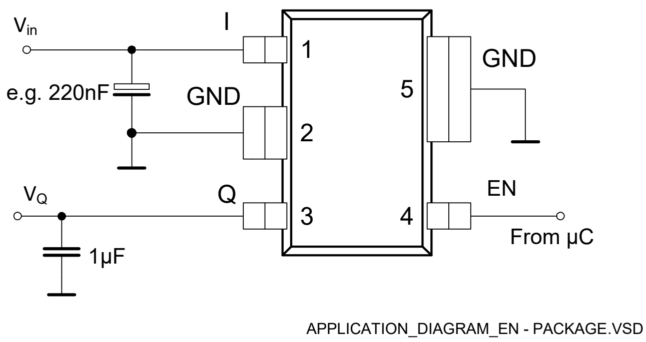


Figure 5 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

A typical application circuit of the TLS202B1MBV33 is shown in **Figure 5**. It shows a generic configuration of the voltage regulator, with the recommendable minimum number of components one should use. Theoretically, if there is no risk of high frequency noise at all, even the small input filter capacitor can be omitted. For a normal operation mode of the device only an output capacitor and a small ceramic input capacitor are needed. Depending on the application's environment, additional components like an input buffer capacitor or a reverse polarity protection diode can be considered as well.

Input filter capacitor C_I

A small ceramic capacitor (for example, 220 nF in **Figure 5**) at the device input helps filtering high frequency noise. To reach the best filter effect, this capacitor should be placed as close as possible to the input pin. The input filter capacitor does not have an influence on the stability of the regulation loop of the device, but in case of fast load changes an input capacitor can buffer the input voltage. Otherwise the parasitic inductance of the input line length can drop the input voltage at the IC terminals and influence the output voltage.

Output capacitor C_Q

The output capacitor is the external component that is required in any case as it is a part of the device's regulation loop. To maintain stability of this loop, the TLS202B1MBV33 requires at least an output capacitor respecting the values given in **Table 3**. The given parameters ensure a stable regulation loop in general, in case of fast load changes in the application, the output capacitance may have to be increased according to the requirements for load responses.

7.1 Further application information

For further information you may contact **https://www.infineon.com**.

8 Package outlines

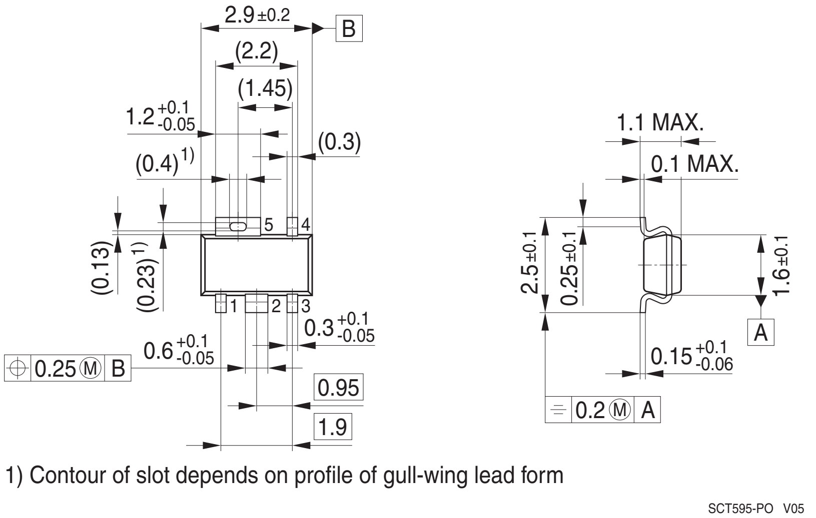


Figure 6 PG-SCT595 [1)]

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

9 Revision history

Revision	Date	Changes
1.01	2023-12-06	Editorial changes and template update
1.0	2015-06-23	Initial datasheet

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2023-12-06
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Z8F53680069