Current Sensor TLI4971

Programming Guide and User Manual

About this document

- This document describes how to program the TLI4971 with the Infineon proprietary one wire interface (SICI).
- Timing of the serial inspection interface.
- Command structure and commands for write/read and EEPROM access.
- A description of the user changeable EEPROM section.
- Details on the diagnosis mode.

For productive in circuit programming Infineon recommends to use a verified programmer which has been a coproduction development between Infineon and CGS. For further documentation please refer to Sensor – Programmer – CGS – Computer Gesteuerte Systeme GmbH (cgs-gruppe.de)

Further Infineon provides a programming board for laboratory usage.

Scope and purpose

TLI4971 Coreless Current Sensor Feature set, EEPROM and interface description.

Intended audience

- Users who use the high variety of the TLI4971 current sensor by programming the functionality like full scale or over current detection, operating modes etc. to their need.
- Current Sensor Module Developers.

Table of contents

1 Application and Programming circuit

The sensor has implemented a serial interface to set the EEPROM content. This chapter describes the hardware environment to program the device. Further, it shows the recommended circuit for a three-phase GPD application.

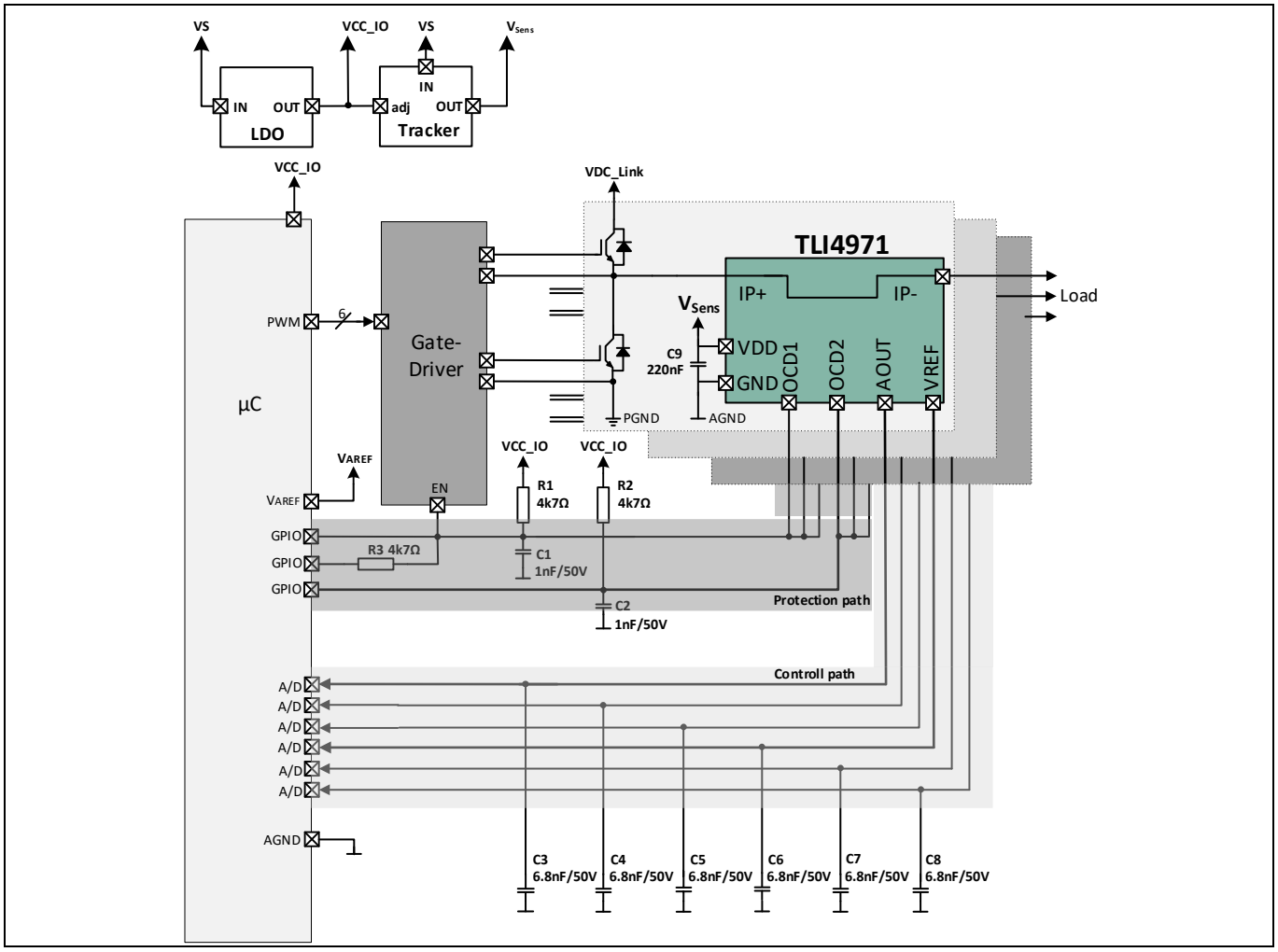

Figure 1 TLI4971 3-phase GPD application circuit for semi and or fully- differential mode

The protection functionality is covered by two open drain outputs (OCD1 and OCD2) to indicate an overload and to protect the system in case of an over current event. The OCD1 output shut down the HV gate-driver. The OCD2 connect to an interrupt input of the microcontroller.

1.1 Circuit / Precondition

Each device can be set separately via the SICI-one wire interface.
In order to communicate with the sensor via the SICI one wire interface the A_{OUT} lines of each sensor need to connect to a microcontroller.
As a first step of the programming procedure, the parameter set has to download into the volatile memory area of the sensor via the SICI interface.
In a second step, the parameter needs to get stored into the EEPROM by sending the programming command and applying the programming voltage on OCD2 pin.
OCD2 and V_{DD} need to be controlled by the programmer.

1.2 In-circuit programming

To program the EEPROM the digital interface sends a particular programming sequence and applies the programming voltage at pin OCD2. In a multiple sensor system the OCD2 can be connected together as each sensor will receive their individual data set via the separated A_{OUT} pin connection. The programming voltage can be applied to all sensors in parallel. Please find a detailed programming example in the chapter 3.

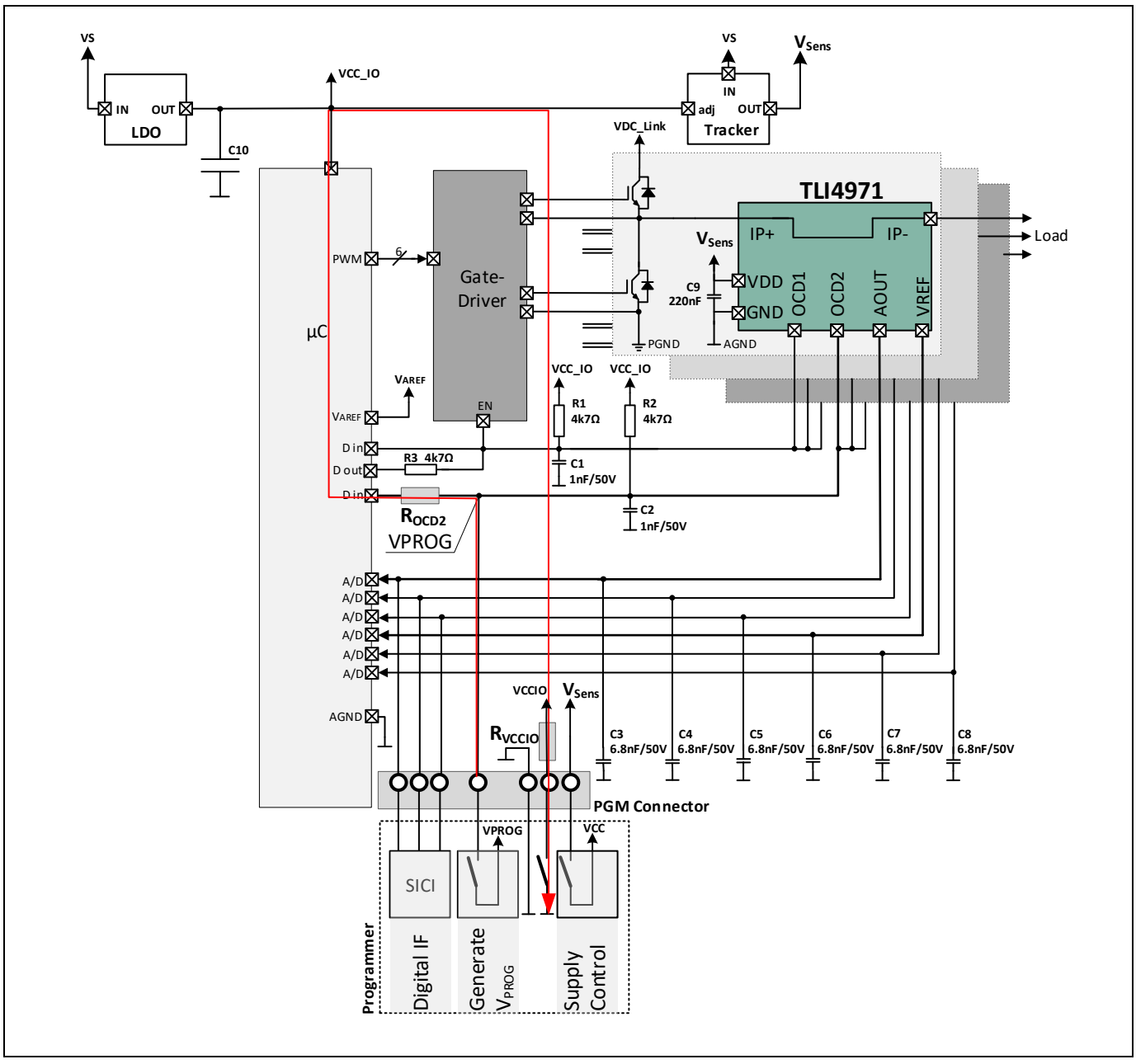

Figure 2 External Programmer connected to GPD application circuit (TLI4971 in-circuit-programming)

The recommended serial resistors R_{OCD2} and R_{VCCIO} are used to avoid a current feedback into the supply and to avoid possible high floating of the µC supply. The resistors R_{OCD2} and R_{VCCIO} have to be determined as described in following formula.

$$\frac{V_{CCIO}}{R_{VCCIO}} > \frac{V_{PROG} - V_{CCIO}}{R_{OCD2}} \mid R_{OCD2} = 10\text{k}\Omega \; \text{R}_{\text{VCCIO}} = 330\Omega$$

Alternatively, the OCD2 channel can be connected with a pull down resistor to GND while applying the programming voltage on the OCD2 pin as shown in Figure 4.

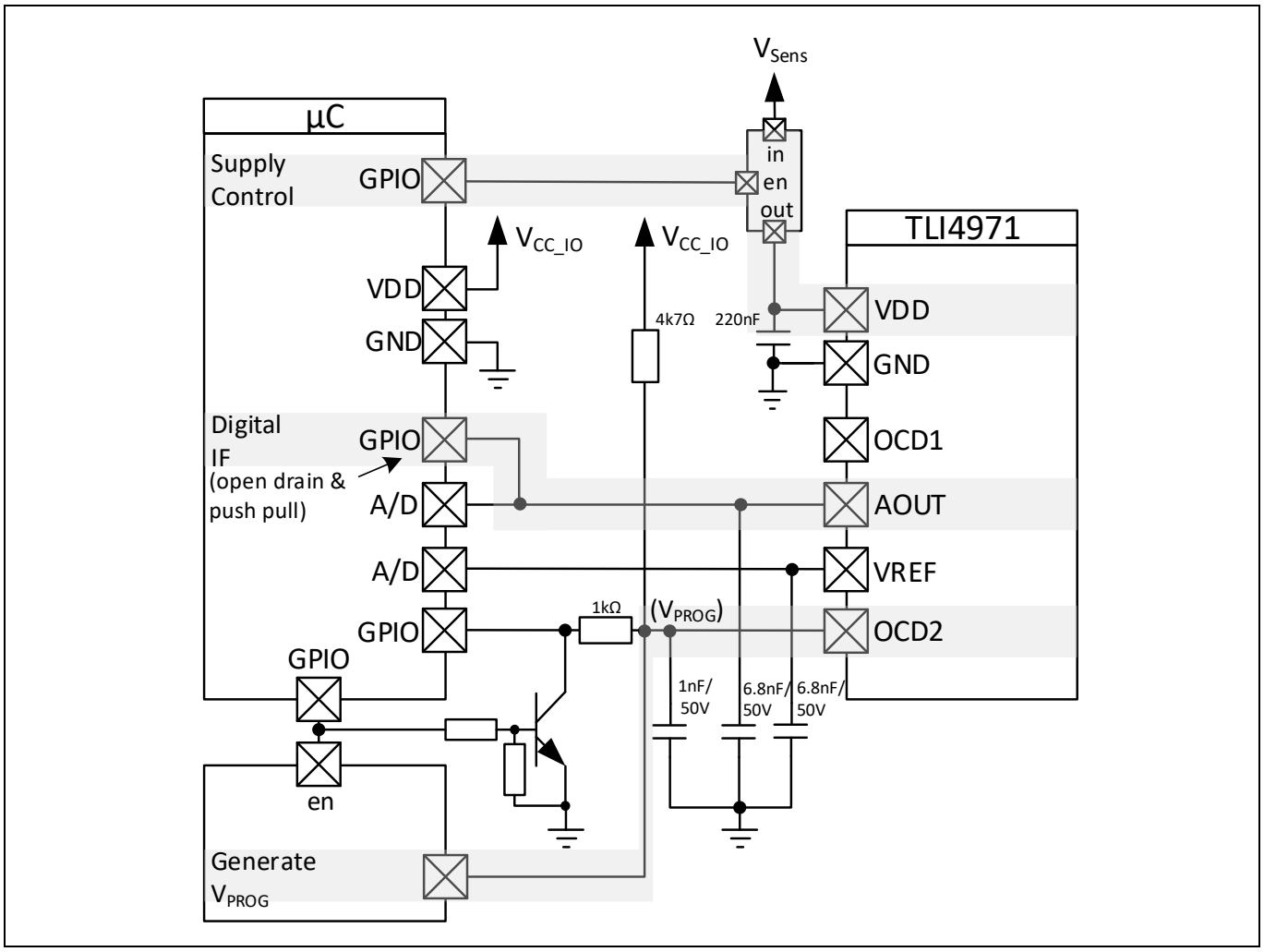

Figure 3: TLI4971 In-circuit programming without external programmer

2 Serial Inspection and Configuration Interface (SICI)

The sensor features a digital 16bit bidirectional one wire interface (SICI). Connect the A_{OUT} pin to a GPIO port in order to establish a communication between the sensor and the controller.

2.1 Hardware Implementation

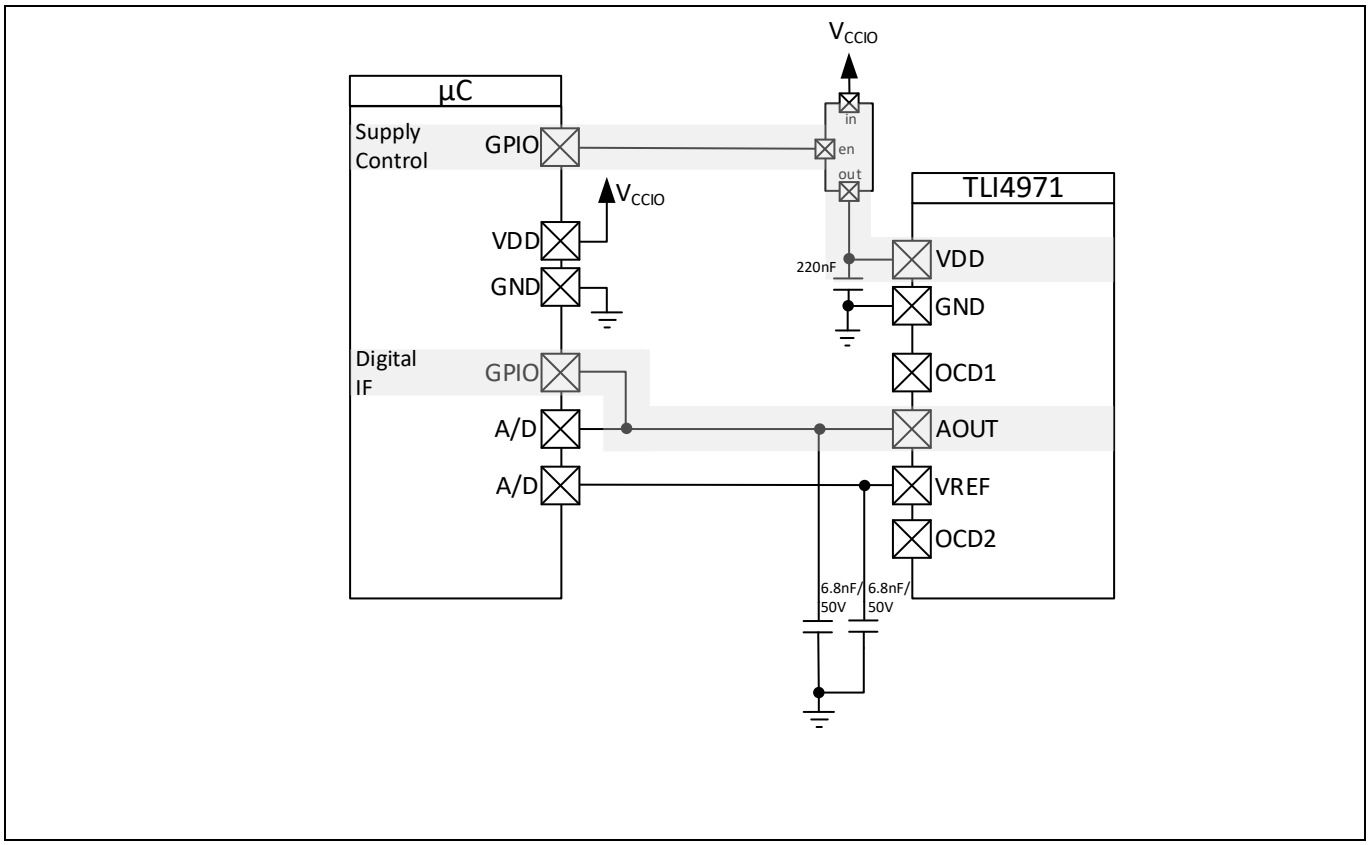

Figure 4 SICI application circuit

To activate the interface the AOUT shall be forced to GND during and after the sensor startup.
The communication is based on transmitting a bit stream to the sensor driven by an external controller. For this interface, the A_{OUT} pin is used as an I/O pin to read from the device and to write the registers of the device by driving the pin with a defined timing.
The interface timing specification is shown in Table 1 and described in Figure 6 and Figure 7.

2.2 Entering Communication Mode

After or while suppling the sensor, the A_{OUT} pin shall be forced to GND to enter the interface mode of the device. Figure 5 shows the “interface enable time” t_{IFen} which is the valid time window to enable the SICI interface. This low state has only to be present once after start up to allow the device to receive the 16 bit enter-interface-command. The activation will also work if the A_{OUT} stays at ground from the beginning. While sending the enter-interface-command, the device answers to each sent bit with logic “0” as shown in Figure 5.

After sending the enter-interface-command, the A_{OUT} pin will remain at V_{Sens} (open drain). If the interface activation is not successful the A_{OUT} pin will reflect the quiescent voltage.

To enable the access to the sensor memory the internal intelligent state machine (ISM) needs to be disabled with a dedicated command like described in chapter 3.

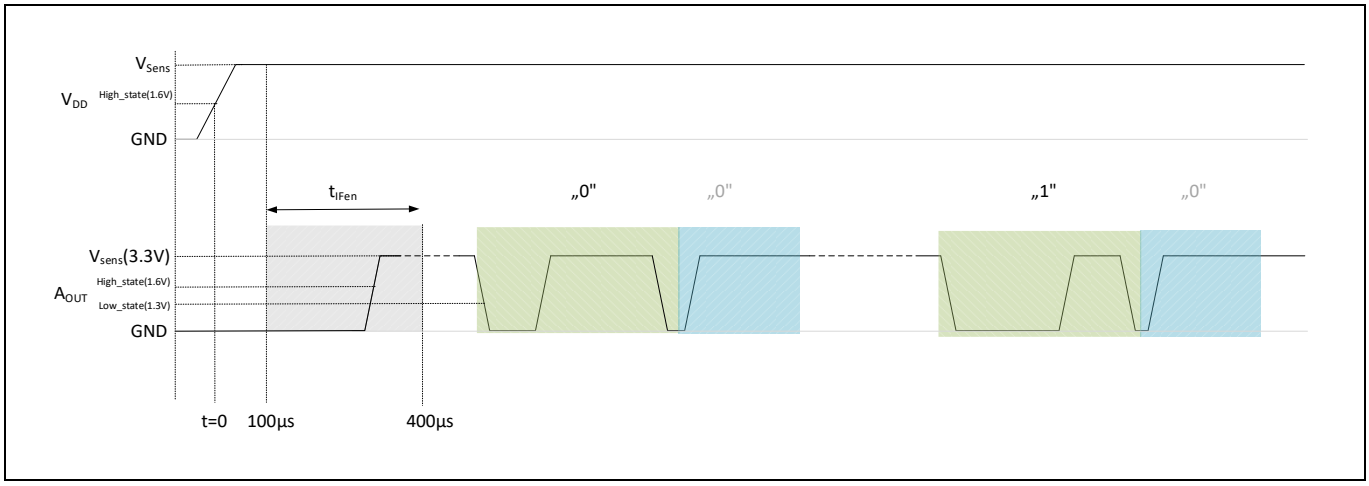

Figure 5 Enabling SICI interface after device start up

2.3 Communication timing

As communication runs in both direction the GPIO of the external controller shall support tri state. After releasing the A_{OUT} back to V_{Sens}, the 16-bit enter-interface-command with LSB first has to be send from the controller. Figure 5 shows the LSB and MSB of the enter-interface-command.

In the Figure 5, the green highlighted squares indicate the received bit while the blue highlighted squares indicate the bits sent by the sensor.

2.3.1 Single low/high PWM transmission

The initial pulse length t_1 & t_2 in Figure 6 and Figure 7 determines the write sequence.

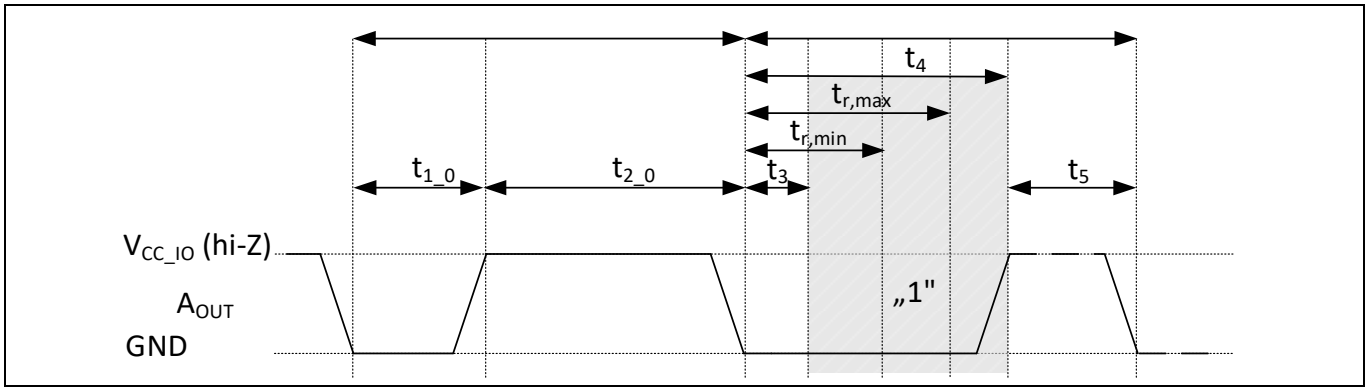

Figure 6 SICI duty cycle; sending logic '0' to the device; receiving logic '1' from the device

The read-out time t_4 is marked with a grey square. The timing of the read sequence t_4 is depending on the low time t_1 and high time t_2 as described in Table 1.

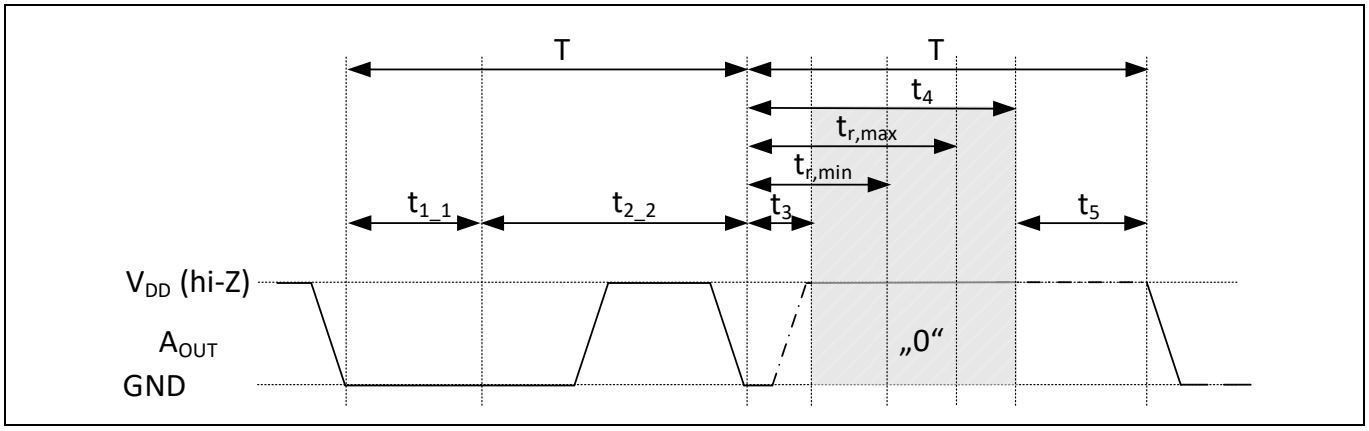

Figure 7 SICI duty cycle; sending logic '1' to the device; receiving logic '0' from the device

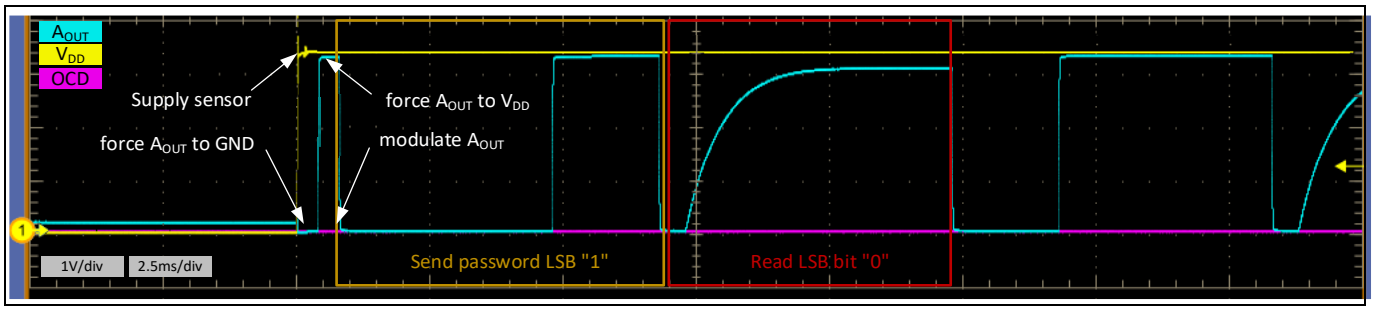

Figure 8 SICI enter interface sequence

Figure 8 describes the interface activation by modulating the AOUT after startup. The modulation of the first two bits can be seen in the picture.

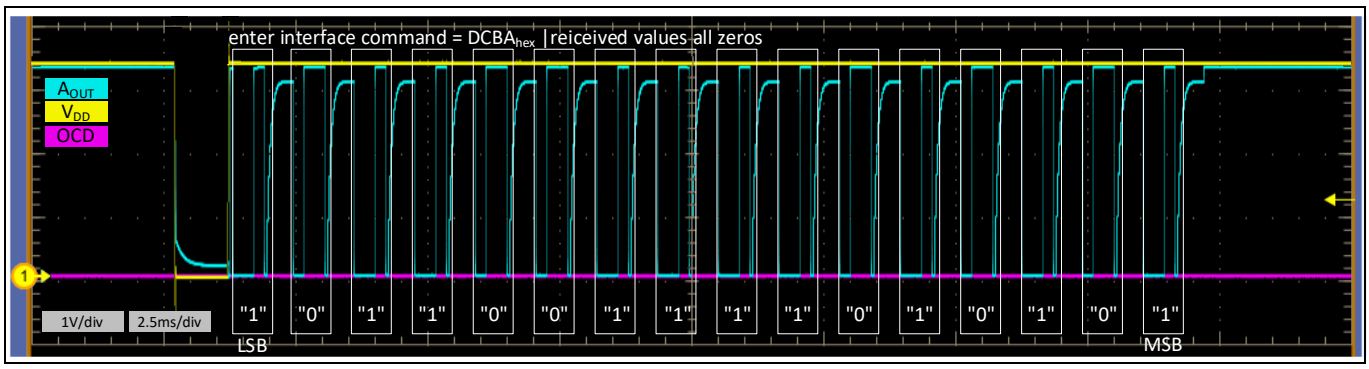

Figure 9 SICI enter interface command

Figure 9 shows the oscilloscope picture of the enter interface command to activate the sensor interface after performing the startup sequence.

2.4 Interface Timing Definition

Table 1 Interface timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Interface enable time	t_{IFen}	100	150	400	µs	Drive A_{OUT} to GND
Period time of 1 bit	T	40	t_1+t_2	7500	µs	One communication frame consist of 16 x 2 bits (16bits write / 16bits read)
Low time sending 0	t_{1_0}	28	33	38	% of T	Drive A_{OUT} to GND
Low time sending 1	t_{1_1}	62	67	72	% of T	Drive A_{OUT} to GND
High time sending 0	t_{2_0}		$T-t_{1\_0}$		µs	The device drives A_{OUT} to V_{DD} by default.
High time sending 1	t_{2_1}		$T-t_{1\_0}$		µs	The device drives A_{OUT} to V_{DD} by default.
Low time before read	t_3	10	-	30	% of t_4	Drive A_{OUT} to GND $t_4 = 2 * ABS(t_{1\_x} - t_{2\_x})$ t_3 can be set as applicable. Increase of t_3 will reduce sensor response time t_4. Therefore t_r has to be set accordingly
Reading time	t_r	50	-	80	% of t_4	The device drives A_{OUT} to V_{DD} by default. Set the external controller in tri state.
Response time	t_4	2 abs(t_{1_x}-t_{2_x})	-	-	µs	t_3 can be set as applicable. Increase of t_3 will reduce the response time t_4.
Time between 2 bits	t_5	1	$T-t_4$	5400	µs	
Max high time	t_{high}	1	-	5400	µs	Only valid for a single bit high time. There is no restriction in timing between two commands
Min low time	t_{low}	1	-	5400	µs	

- There is no timing restriction between two commands as long as the A_{OUT} pin is not driven to GND.
- The typical threshold level to detect a logic “0” during a high to low transition is 1.3V.
- The typical threshold level to detect a logic “1” during a low to high transition is 1.6V.

2.5 Definition of Voltage Levels

Table 2 SICI High and low level definition

Parameter	Symbol	Min.	Typ.	Max.	Unit	comment
Voltage level for SICI – High[1)]	V_{SICI_High}	1.6	3.3	3.5	V	high state
Voltage level for SICI – Low[2)]	V_{SICI_Low}	-0.3	0	1.3	V	low state

3 Interface description

3.1 Command Structure

A typical SICI communication consists in multiple input commands sent to the device via A_{OUT} voltage modulation, to which the sensor responds modulating the same A_{OUT} pin.

An input command is composed of 16 bits LSB first. One bit consists of a transmission sequence initiated by the master and a receiving sequence driven by the device. The reply data stream sent by the device starts with the LSB.

A typical communication consists of a command including the access information and address sent by the master to the device. The device replies with data from the former received command. The upper nibble of the command include the access information.

Table 3 SICI Command structure

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB
w/r	0	Ac1	Ac0	Ad7	Ad6	Ad5	Ad4	Ad3	Ad2	Ad1	Ad0	0	0	0	0

Table 4 Access bit description

w/r	Ac1	Ac0	description
1	0	X	Set ones and zeros like the sent 16 bit data word
1	1	0	Set only the sent zeros. The ones will not be set
1	1	1	Set only the sent ones. The zeros will not be set

3.2 Read / Write Command

There is always a delay of one command between the request command and the addressed data. When a new read command is sent to the sensor, the device replies with the data requested with the former command. The NOP command terminates a read sequence without initializing a new read or write sequence.

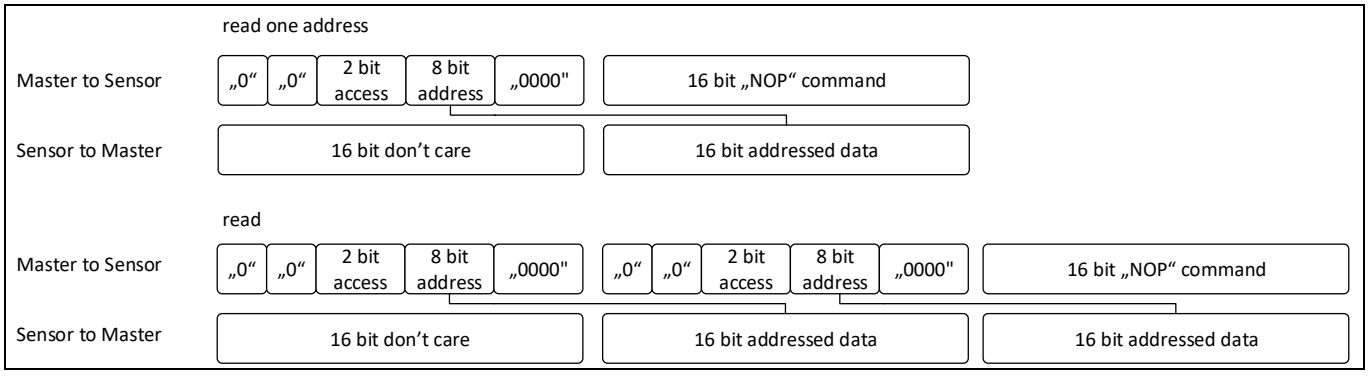

Figure 10 SICI read sequence

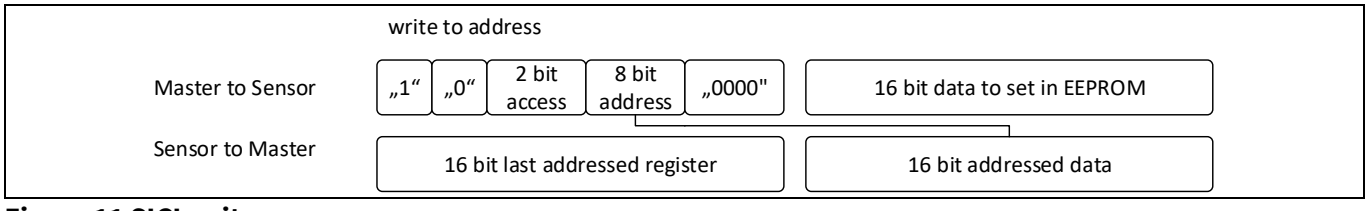

Figure 11 SICI write sequence

3.3 Interface Commands

Table 5 Available Commands

Command name	address$_{hex}$	command$_{hex}$	description
Enter Interface command	---	ABCD$_{hex}$	Activate communication as described in chapter Entering Communication Mode
Power down ISM	25$_{hex}$	8000$_{hex}$	reserve if-access to the EEPROM data bus to avoid that ISM is blocking the data bus
Disable failure indication	01$_{hex}$	0000$_{hex}$	Prevent unintended activation of the OCD2 output
Write command	40$_{hex}$ to 42$_{hex}$	8400$_{hex}$	Initialize Write command to address 40$_{hex}$
Send values		XYXY	send data XYXY to previous addressed line where XYXY stand for 16bit data placeholder
Read command	40$_{hex}$ to 51$_{hex}$	0400$_{hex}$	Initialize read command at address 40$_{hex}$
Read command	41$_{hex}$	0410$_{hex}$	Initialize read command at address 41$_{hex}$ read data from previous address 40$_{hex}$
Read command	51$_{hex}$	0510$_{hex}$	Initialize read command at address 51$_{hex}$ read data from previous address
NOP		FFFF$_{hex}$	No operation command, to read former addressed values.
EEPROM margin test ones	3E$_{hex}$	0044$_{hex}$	Compare cell voltages of programmed ones
EEPROM margin test zeros	3E$_{hex}$	0045$_{hex}$	Compare cell voltages of programmed zeros
EEPROM set zeros	3E$_{hex}$	0248$_{hex}$	Set EEPROM bits to zero
EEPROM set ones	3E$_{hex}$	024B$_{hex}$	Set EEPROM bits to one
EEPROM refresh	3E$_{hex}$	024C$_{hex}$	Refresh the all EEPROM lines
EEPROM program zeros	3E$_{hex}$	024E$_{hex}$	Program all set zeros into EEPROM
EEPROM program ones	3E$_{hex}$	024F$_{hex}$	Program all set ones into EEPROM

3.4 Write and programming sequence

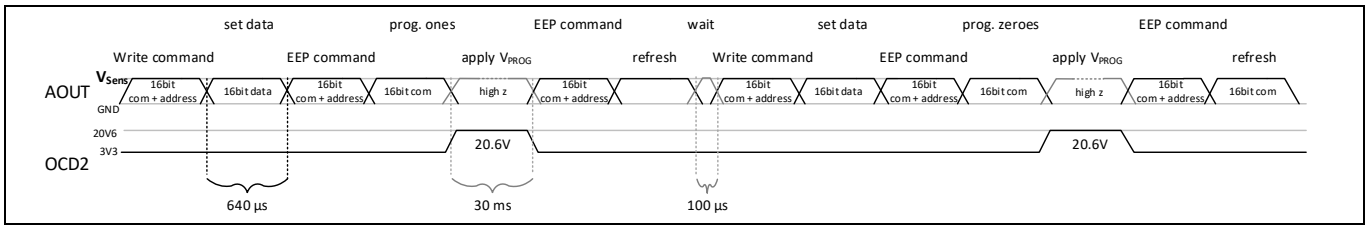

Figure 12 Programming Sequence

Figure 12 shows the command sequence for a write command and describes the sequence to program the EEPROM. After writing the values into the EEPROM, the programming voltage has to be applied for 30ms followed by a refresh command as shown.

3.5 Temporary register

For test purpose, it is possible to change the sensor settings in the temporary registers. This allows to test user settings without programming the EEPROM.

The addresses for the temporary registers are different from the EEPROM addresses. See Table 6 for details.

In order to access temporary registers send 0x8000 to address 25_{hex}. Set to 0x0000 to leave the interface mode and to change into normal operating mode until the next power down. The sensor uses the content of the temporary registers instead of the correlating EEPROM values until the next power down.

Table 6 Temporary register description

Temporary register address	EEPROM register address	Note
25_{hex}	-	Write 0x8000 to this address to get access to the register (otherwise the registers gets occupied / overwritten by the sensor)
01_{hex}	-	Write 0x0000 to temporary disables failure indications like CRC check.
11_{hex}	40_{hex}	Bit description and bit position same for both addresses
12_{hex}	41_{hex}	Bit description and bit position same for both addresses
13_{hex}	42_{hex}	Bit description and bit position same for both addresses

3.6 Read Example (temperature register read out)

The temperature value can be read out via the SICI interface. The following example describes the required command sequence to enter the interface and to read out the 16 bit temperature value. The temperature sensitivity is set to a sensitivity of 16 LSB_{16}/°C. The ADC value for 25°C corresponds to 1408 LSB_{16}. The following formula describes how to calculate the temperature dependent on the 16bit value.

$$Temperature = \frac{ADC_{value} - 2048}{16} + 65$$

Table 7 Command sequence example to read out the internal 16 bit temperature value

Command / sequence	minimum frame time	Description
$ABCD_{hex}$	0.64ms	Enter interface command (sending 16bit reading 16bit)
Write command to address 25_{hex}	0.64ms	Power down ISM (write to address 25_{hex})
8000_{hex}	0.64ms	Power down ISM (write data)
Read command at address 18_{hex}	0.64ms	Sending the address to read the temperature value
$FFFF_{hex}$	0.64ms	Reading the data.
Power on and off the device to activate normal operating mode. (1.5ms typical after power on) Alternatively set the device in normal operating mode by sending the following commands:		
Write command to address 25_{hex}	0.64ms	Power on ISM (write command to address)
0000_{hex}	0.64ms	Power on ISM (send data)
Wait until the A_{OUT} settles into calibrated mode. In calibrated mode, the A_{OUT} reflects the voltage level of the V_{REF} pin. Assumed no current flows through the primary current rail of the device.		

4 EEPROM

The sensor's non volatile memory (EEPROM) is organized in 16-bit (word) registers which can be addressed individually.

When content in the user area is re programmed, a CRC check register has to be updated. Since the EEPROM CRC is calculated covering the entire EEPROM storage space, the user is required to readout the entire EEPROM content, calculate the new CRC values and store it into the respective registers. An incorrect CRC value will be detected by the sensor and cause a transition to its safe state. In case of a CRC error the OCD open drain output will be set to GND.

All 18 lines of the EEPROM are readable because the CRC calculation has to be done with the complete data content of the EEPROM. The device is doing a cyclic redundancy check (CRC) of the EEPROM content while accessing the EEPROM and indicates an error on the OCD pin in case of a wrong programmed CRC.

Address	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
40_{hex}	Customer accessible settings								Customer accessible settings							
41_{hex}	Customer accessible settings								Customer accessible settings							
42_{hex}	Customer accessible settings								Customer accessible CRC							
43_{hex}	read only								read only							
...	read only								read only							
51_{hex}	read only								read only							

Figure 13 EEPROM overview

4.1 EEPROM Content

Table 8 EEPROM (address 40_{hex} – 42_{hex})

address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40_{hex}	$OCD2_{en}$	$OCD1_{en}$	$OCD2_{deglitch}$				$OCD1_{deglitch}$			OP_{mode}		$MEAS_{rng}$				
41_{hex}	$OCD2_{thrsh}$						$OCD1_{thrsh}$					OCD_{comp_hyst}				
42_{hex}	$RATIO_{Off}$	$RATIO_{Gain}$	$OCD2f_{only}$	$QV1V5_{sd}$	Empty	$VREF_{ext}$			CRC							

Table 9 Functional description Address 40_{hex}

Bit field name	Bit	Type	Bit field description	Default value
$MEAS_{rng}$	4:0	rw	The measurement range bits define the sensitivity in mV/A Symbol | Setting | Description / Full Scale setting S1 | 05_{hex} | ±120A Full Scale (FS) / 10mV/A S2 | 06_{hex} | ±100A / 12 mV/A S3 | 08_{hex} | ±75A / 16 mV/A S4 | $0C_{hex}$ | ±50A / 24 mV/A S5 | 10_{hex} | ±37.5A / 32 mV/A S6 | 18_{hex} | ±25A / 48 mV/A	xxx0x
OP_{mode}	6:5	rw	Symbol | Setting | Description SD bid | 0_{hex} | Semi-differential bidirectional V_{OQbid_1} : $V_{REF} = V_{DD} / 2$; V_{OQbid_2} : V_{REF} = 1.5 (QV1V5 = 1) FD | 1_{hex} | Fully-differential ($V_{OQ} = V_{DD}/2$) (doubled sensitivity) SD uni | 2_{hex} | Semi-differential unidirectional V_{OQuni} : $V_{REF} = V_{DD}/5.5$ SE | 3_{hex} | Single-ended $V_{OQ} = V_{REF} = V_{REF\_ext}$ The device standard setting is the semi-differential mode	00
$OCD1_{deglitch}$	9:7	rw	Symbol | Setting | Deglitch time in ns d0 | 0_{hex} | 0 (standard setting) d1 | 1_{hex} | 500 d2 | 2_{hex} | 1000 d3 | 3_{hex} | 1500 d4 | 4_{hex} | 2000 d5 | 5_{hex} | 2500 d6 | 6_{hex} | 3000 d7 | 7_{hex} | 3500	000
$OCD2_{deglitch}$	13:10	rw	Symbol | Setting | Deglitch time in ns d0 | 0 | 0 (standard setting) d1 | 1 | 500 d2 | 2 | 1000 d3 | 3 | 1500 d4 | 4 | 2000 d5 | 5 | 2500 d6 | 6 | 3000 d7 | 7 | 3500 d8 | 8 | 4000 d9 | 9 | 4500 d10 | 10 | 5000 d11 | 11 | 5500 d12 | 12 | 6000	0000

			d13	13	6500	
			d14	14	7000	
			d15	15	7500	
$OCD1_{en}$	14	rw	The over-current detection enable bit 1 activates the over-current functionality of channel 1. If this bit set to zero the OCD pin 1 will not indicate an internal failure or an over-current event. The standard setting is 1 = enabled			1
$OCD2_{en}$	15	rw	The over-current detection enable bit 2 activates the over-current functionality of channel 2. If this bit set to zero the OCD pin 2 will not indicate an internal failure or an over-current event. The standard setting is 1 = enabled			1

Table 10 Functional description Address 41_{hex}

<table>
<tr><th>Bit field name</th><th>Bit</th><th>Type</th><th>Bit field description</th><th>Default value</th></tr>
<tr><td>OCD_{comp_hyst}</td><td>3:0</td><td>rw</td><td>OCD release point: Standard setting out of range 0_{hex} .. F_{hex}:
• 3_{hex} for 25A- and 75A-full-scale-variant
• 6_{hex} for 50A- and 120A-full-scale-variant
Calculated thresholds for 120A-full-scale-variant:
$OCD1_{thresh}$ = 120 A * 1.25 = 150 A
$OCD1_{rel\_thresh}$ = $OCD1_{thresh}$ * (1 – ($OCD_{comp\_hyst\_setting}$ / $OCD1_{thrsh\_setting}$)) =
= 150 A * (1 – (6_{hex} / 13_{hex})) = 103 A
$OCD2_{thresh}$ = 120 A * 0.82 = 98 A
$OCD2_{rel\_thresh}$ = $OCD2_{thresh}$ * (1 – ($OCD_{comp\_hyst\_setting}$ / $OCD2_{thrsh\_setting}$)) =
= 98 A * (1 – (6_{hex} / $1B_{hex}$)) = 77 A
Calculated thresholds for 75A-full-scale-variant:
$OCD1_{thresh}$ = 75 A * 1.25 = 94 A
$OCD1_{rel\_thresh}$ = 94 A * (1 – (3_{hex} / $0A_{hex}$)) = 66 A
$OCD2_{thresh}$ = 75 A * 0.82 = 62 A
$OCD2_{rel\_thresh}$ = 62 A * (1 – (3_{hex} / $0F_{hex}$)) = 49 A
Calculated thresholds for 50A-full-scale-variant:
$OCD1_{thresh}$ = 50 A * 1.25 = 63 A
$OCD1_{rel\_thresh}$ = 63 A * (1 – (6_{hex} / 14_{hex})) = 44 A
$OCD2_{thresh}$ = 50 A * 0.82 = 41 A
$OCD2_{rel\_thresh}$ = 41 A * (1 – (6_{hex} / $1C_{hex}$)) = 32 A
Calculated thresholds for 25A-full-scale-variant:
$OCD1_{thresh}$ = 25 A * 1.25 = 31 A
$OCD1_{rel\_thresh}$ = 31 A * (1 – (3_{hex} / 07_{hex})) = 18 A
$OCD2_{thresh}$ = 25 A * 0.82 =21 A
$OCD2_{rel\_thresh}$ = 21 A * (1 – (3_{hex} / $0B_{hex}$)) = 15 A</td><td>0x1x</td></tr>
<tr><td>$OCD1_{thrsh}$</td><td>9:4</td><td>rw</td><td>Threshold level of OCD1
<table>
<tr><td>Symbol</td><td colspan="7">Setting</td></tr>
<tr><td>level</td><td>x FS</td><td>S1</td><td>S2</td><td>S3</td><td>S4</td><td>S5</td><td>S6</td></tr>
<tr><td>$I_{THR1.1}$</td><td>1.25</td><td>**13_{hex}**[*)]</td><td>$0F_{hex}$</td><td>**$0A_{hex}$**[*)]</td><td>**14_{hex}**[*)]</td><td>$0D_{hex}$</td><td>**07_{hex}**[*)]</td></tr>
<tr><td>$I_{THR1.2}$</td><td>1.39</td><td>16_{hex}</td><td>11_{hex}</td><td>$0B_{hex}$</td><td>17_{hex}</td><td>$0F_{hex}$</td><td>09_{hex}</td></tr>
<tr><td>$I_{THR1.3}$</td><td>1.54</td><td>19_{hex}</td><td>14_{hex}</td><td>$0D_{hex}$</td><td>$1A_{hex}$</td><td>12_{hex}</td><td>$0A_{hex}$</td></tr>
<tr><td>$I_{THR1.4}$</td><td>1.68</td><td>$1C_{hex}$</td><td>16_{hex}</td><td>$0F_{hex}$</td><td>$1D_{hex}$</td><td>14_{hex}</td><td>$0C_{hex}$</td></tr>
<tr><td>$I_{THR1.5}$</td><td>1.82</td><td>$1E_{hex}$</td><td>18_{hex}</td><td>11_{hex}</td><td>20_{hex}</td><td>16_{hex}</td><td>$0D_{hex}$</td></tr>
<tr><td>$I_{THR1.6}$</td><td>1.96</td><td>21_{hex}</td><td>$1B_{hex}$</td><td>12_{hex}</td><td>23_{hex}</td><td>18_{hex}</td><td>$0F_{hex}$</td></tr>
<tr><td>$I_{THR1.7}$</td><td>2.11</td><td>24_{hex}</td><td>$1D_{hex}$</td><td>14_{hex}</td><td>26_{hex}</td><td>$1B_{hex}$</td><td>10_{hex}</td></tr>
<tr><td>$I_{THR1.8}$</td><td>2.25</td><td>27_{hex}</td><td>$1F_{hex}$</td><td>16_{hex}</td><td>29_{hex}</td><td>$1D_{hex}$</td><td>12_{hex}</td></tr>
</table>
[*)] Standard setting datecode 2118 and later</td><td>xxxxxx</td></tr>
<tr><td>$OCD2_{thrsh}$</td><td>15:10</td><td>rw</td><td>Threshold level of OCD2</td><td>xxxxxx</td></tr>
</table>

			Symbol	Setting						
			level	x FS	S1	S2	S3	S4	S5	S6
			$I_{THR2.1}$	0.50	$0E_{hex}$	$0B_{hex}$	07_{hex}	$0E_{hex}$	09_{hex}	04_{hex}
			$I_{THR2.2}$	0.61	13_{hex}	$0F_{hex}$	$0A_{hex}$	13_{hex}	$0D_{hex}$	06_{hex}
			$I_{THR2.3}$	0.71	17_{hex}	12_{hex}	$0C_{hex}$	17_{hex}	10_{hex}	08_{hex}
			$I_{THR2.4}$	0.82	**$1B_{hex}$** *)	16_{hex}	**$0F_{hex}$** *)	**$1C_{hex}$** *)	13_{hex}	**$0B_{hex}$** *)
			$I_{THR2.5}$	0.93	$1F_{hex}$	$1A_{hex}$	12_{hex}	21_{hex}	17_{hex}	$0D_{hex}$
			$I_{THR2.6}$	1.04	24_{hex}	$1D_{hex}$	15_{hex}	25_{hex}	$1A_{hex}$	$0F_{hex}$
			$I_{THR2.7}$	1.14	28_{hex}	21_{hex}	17_{hex}	$2A_{hex}$	$1D_{hex}$	11_{hex}
			$I_{THR2.8}$	1.25	$2D_{hex}$	24_{hex}	$1A_{hex}$	$2E_{hex}$	21_{hex}	14_{hex}
			*) Standard setting datecode 2118 and later							

Table 11 Functional description Address 42_{hex}

Bit field name	Bit	Type	Bit field description	Default value
CRC	7:0	rw	CRC calculation is byte by byte, starting from address 42_{hex}. After reaching the end of the EEPROM (address 51_{hex}), the address 40_{hex} to 41_{hex} are append. The CRC calculation is based on the polynomial $x^8+x^4+x^3+x^2+1$	-
$VREF_{ext}$	10:8	rw	Symbol / Setting / Description 1V65 / 0_{hex} / V_{REF_nom} = 1.65 V (±10% if ratiometricity is enabled) standard setting 1V2 / 1_{hex} / V_{REF_nom} = 1.2 V (±10% if ratiometricity is enabled) 1V5 / 2_{hex} / V_{REF_nom} = 1.5 V (±10% if ratiometricity is enabled) 1V8 / 3_{hex} / V_{REF_nom} = 1.8 V (±10% if ratiometricity is enabled) Standard is set to 1.65V	000
Not used	11	rw	Not used	0
$QV1V5_{sd}$	12	rw	The bit enables the quiescent voltage to 1.5V in semi-differential. Default is 0 (=disabled)	0
$OCD2f_{only}$	13	rw	If the bit is set to one only failure indication is activated at the OCD2 channel. Over current detection is not activated if the bit is set to one. Default is 0 (= fault signal on both OCDs)	0
$RATIO_{Gain}$	14	rw	If the bit is set, the sensitivity is ratio metric to VDD respective to VREF in single-ended mode. Default is 0 (=disabled)	0
$RATIO_{Off}$	15	rw	The ratio-metric offset behavior of the quiescent voltage is activated if the bit is set to one. Default is 0 (=disabled)	0

4.2 Programming Example

Table 12 will guide the user through a complete programming sequence.

After activating the interface the integrated intelligent state machine (ISM) has to be powered down. To avoid unintended high current consumption during applying the programming voltage at the OCD2 pin, the error indication has to be disabled by writing the disable failure indication command to the device.

Programming requires two single commands followed by the programming pulse. One sequence is required to program the ones and one sequence to program the zeros into the EEPROM. All digital values are stored in the EEPROM. Figure 12 gives timing and an exemplary description of the programming sequence.

Table 12 EEPROM programming example

Command name	address$_{hex}$	command$_{hex}$	description
Enter Interface	---	DCBA$_{hex}$	Enter interface
Power down ISM	25$_{hex}$	8250$_{hex}$ 8000$_{hex}$	Write command: get access to the register Set data
Disable failure indication	01$_{hex}$	8010$_{hex}$ 0000$_{hex}$	Write command Set data
Read all register			Read data before modifying values
Read command (All EEPROM register)	40$_{hex}$ n 51$_{hex}$	0400$_{hex}$ 00n0 0510$_{hex}$	Read command at EEPROM line 0 Read command for address “n” Address last line in EEPROM
NOP	---	FFFF$_{hex}$	Read values from previous address
Write command Write data	40$_{hex}$	8400$_{hex}$ nnnn$_{hex}$	Write to EEPROM line 0: Access: set ones and zeros Write content to be programmed
EEPROM program zeros	3E$_{hex}$	83E0$_{hex}$ 024**E**$_{hex}$	Write to EEPROM command line Set EEPROM command program zeros
			Apply programming voltage
EEPROM refresh	3E$_{hex}$	83E0$_{hex}$ 024**C**$_{hex}$	Write to EEPROM command line Set EEPROM command refresh
			Wait 100 µs
Write command Write data	40$_{hex}$	8400$_{hex}$ nnnn$_{hex}$	Write to EEPROM line 0: Access: set ones and zeros Write content to be programmed
EEPROM program ones	3E$_{hex}$	83E0$_{hex}$ 024**F**$_{hex}$	Write to EEPROM command line Set EEPROM command program ones
			Apply programming voltage
EEPROM refresh	3E$_{hex}$	83E0$_{hex}$	Write to EEPROM command line
		024C$_{hex}$	Set EEPROM command refresh
			Wait 100 µs

Table 13 EEPROM voltage and timing parameter

Parameter	Symbol	Min	Typ	Max	Unit	Note
Programming Voltage	V_{PROG}	20.5	20.6	21.0	V	EEPROM designed to write under specified condition on the first shot. In case of lower voltage (i.e. 15V) Infineon recommends a margin test to proof quality of EEPROM content and repeat the programming-sequence if needed.
EEPROM threshold margin level at start of lifetime[1)]	V_{TH_0h}	3.55	3.8	4.15	V	“1” programmed cells
				0.25	V	“0” programmed cells
EEPROM threshold margin level after lifetime	V_{TH_LT}	1.9			V	“1” programmed cells
				1.1	V	“0” programmed cells
Margin voltage sweep range, test of “1” bits	V_{margin}	1.3		4.3	V	25mV step size recommended
Margin voltage sweep range, test of “0” bits		0		1.7	V	
EEPROM Programming time	$t_{EEPvprog}$		30		ms	Time to apply programming voltage V_{PROG} on OCD2 pin
EEPROM wait time	$t_{EEPwait}$		100		µs	Wait time after EEPROM refresh command
Programming Current consumption	I_{PROG}		6	10	mA	Current consumption of OCD2 while applying the programming voltage

1) Limits for EEPROM programming and margin level test at the same temperature. Alternatively the temperature characteristic of the margin level test needs to be considered: VTH(T)=VTH(WRITE_ERASE)+0.0016V/K*(TPROG-T). Please note that only a typical temperature coefficient is used.

4.3 Margin Test

The margin test command is used in order to check the threshold voltages of the programmed EEPROM cells. For reliable sensor EEPROM operation the threshold level of the cells have to be kept within the specification (Table 13). After sending the margin test command an external margin voltage can be switched to the control gates while refreshing the EEPROM-registers by an external trigger, so that the switching threshold of the EEPROM cells can be identified (Table 13). EEPROM cells programmed to '0' or to '1' need to be tested separately. For the '1' programmed cells a threshold voltage smaller than the applied margin voltage a '0' will be stored to the EEPROM registers, for those with a higher threshold a '1'. Vice versa the procedure when testing '0' programmed cells, for a margin voltage smaller than the threshold a '1' and for those higher than the

threshold a '0' is stored in the EEPROM registers. By sweeping the external margin voltage the effective threshold voltages of each EEPROM cell can be identified. The threshold voltages of cells programmed to '1' can be found in this way. The smallest possible margin voltage is 0V, it is therefore not possible to determine the threshold voltages below 0V for the cells programmed to '0'.

Table 14 EEPROM margin test

Command name	**address$_{hex}$**	**command$_{hex}$**	**description**
Enter Interface	---	DCBA$_{hex}$	Enter interface
Power down ISM	25$_{hex}$	8250$_{hex}$ 8000$_{hex}$	Write command: get access to the register Set data
Disable failure indication	01$_{hex}$	8010$_{hex}$ 0000$_{hex}$	Write command Set data
Read all register			Read data before modifying values
Read all EEPROM for reference	40$_{hex}$ n 51$_{hex}$	0400$_{hex}$ 00n0 0510$_{hex}$	Read command at EEPROM line 0 Read command for address “n” Address last line in EEPROM
NOP	---	FFFF$_{hex}$	Read values from previous address
Loop reference voltage on OCD2:			Sweep voltage from start voltage till end voltage in defined step-size
Send “margin” command	3E$_{hex}$	83E0$_{hex}$ 004**5**$_{hex}$	Write to EEPROM command line Set margin test “zeros” (004**4**$_{hex}$ = “ones”)
			Apply actual reference voltage for comparison and wait 2ms
Send “margin stop”	3E$_{hex}$	83E0$_{hex}$ 0080$_{hex}$	Write to EEPROM command line Stop margin test
			Wait 100 µs
Read all EEPROM for comparison	40$_{hex}$ n 51$_{hex}$	0400$_{hex}$ 00n0 0510$_{hex}$	Read command at EEPROM line 0 Read command for address “n” Address last line in EEPROM
LoopEnd			
Find threshold-voltage when EEPROM cell flipped			Compare all EEPROM-content at each voltage to reference

4.4 Cyclic Redundancy Check

The CRC calculation is based on the polynomial x8+x4+x3+x2+1. Table 15 describes the CRC calculation. The seed word is defined as 0xAAhex. The CRC calculation of the EEPROM is performed byte by byte, starting from the EEPROM line three (address 43_{hex}). After reaching the end of the EEPROM the line 0 (address 40_{hex}) to line 2 are appended. The CRC byte is not used for the calculation. The end word is defined as 0xFFhex.

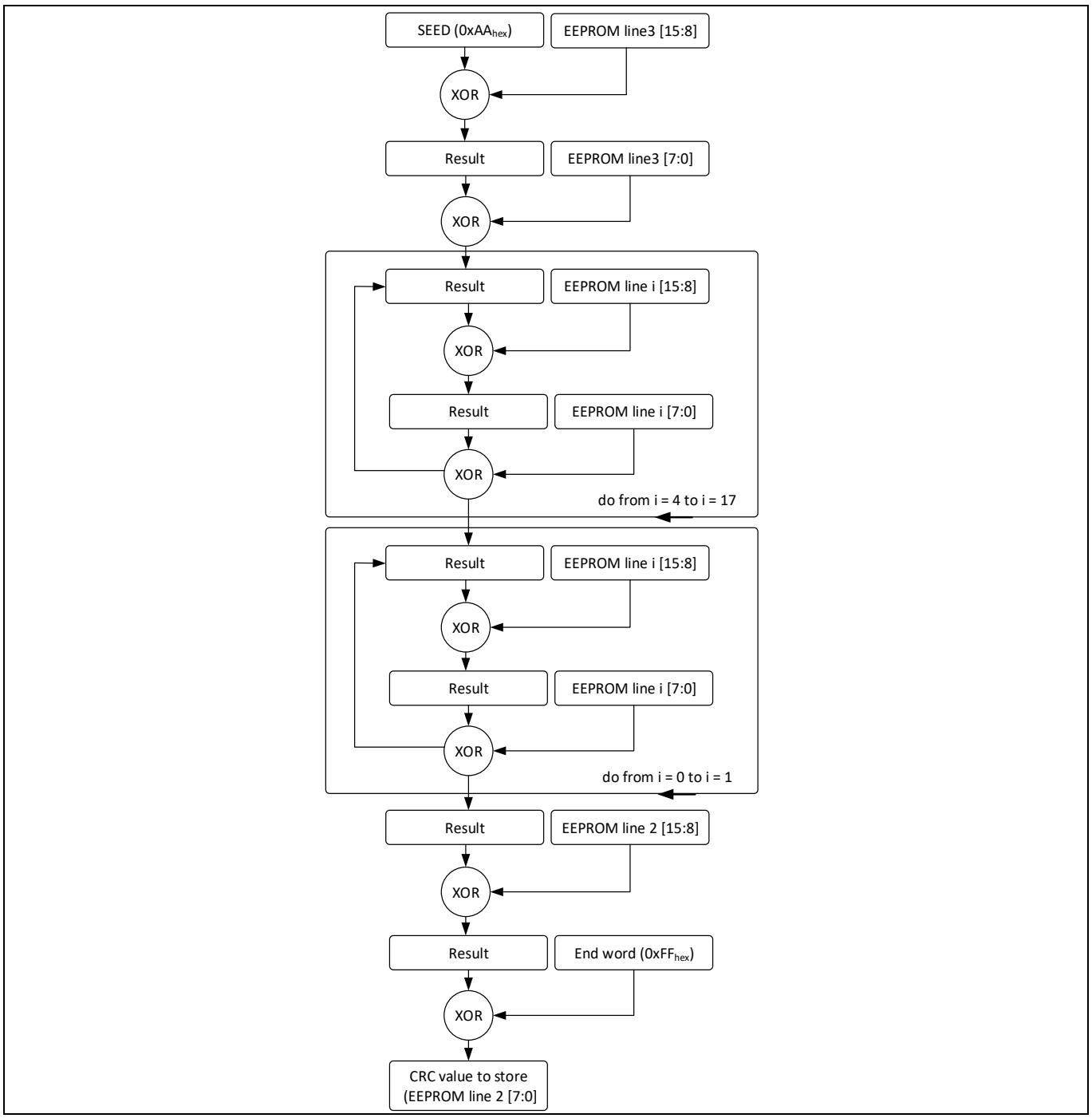

Figure 14 flow chart CRC calculation

Table 15 CRC calculation specification

CRC value	operation	comment
CRC_3_1	[$0xAA_{hex}$] XOR [EEPROM_line_03_bit15_downto_bit8]	The CRC calculation starts with the content of the upper 8 bits in the EEPROM line 3
CRC_3_2	CRC_3_1 XOR [EEPROM_line_03_bit07_downto_bit0]	Continue calculating the CRC with the lower 8 bits stored in the EEPROM line 3
CRC_4_1	CRC_3_2 XOR [EEPROM_line_04_bit15_downto_bit8]	
CRC_4_2	CRC_4_1 XOR [EEPROM_line_04_bit07_downto_bit0]	
. . .	. . .	Proceed calculation until EEPROM line 17
CRC_n_2	CRC_n_1 XOR [EEPROM_line_17_bit07_downto_bit0]	CRC_n stands for CRC_17 to represent the CRC calculation with the content of the last line (17) of the EEPROM
CRC_0_1	CRC_n_2 XOR [EEPROM_line_00_bit15_downto_bit8]	Continue calculating the CRC with the content of EEPROM line 0
. . .	. . .	Proceed calculation until EEPROM line 2
CRC_k_1	CRC_k-1_2 XOR [EEPROM_line_02_bit15_downto_bit8]	CRC_k represents the CRC value calculated with the EEPROM content of the third EEPROM line (line 2).
CRC	CRC_k XOR [$0xFF_{hex}$]	The CRC has to be stored into the lower 8 bits of the EEPROM line 2.

4.5 Code example CRC calculation

```
//CRC calculation example for Infineon TLI4971 current sensor
//CRC 8 (SAE - J1850) CRC polynomial: x^8 + x^4 + x^3 + x^2 + 1
// len = 18 (EEPROM line 0-17)
#define CRC_POLYNOMIAL 0x1D
#define CRC_SEED 0xAA

//check CRC
bool checkCRC (uint16_t* data, int len) {
 uint8_t checkSum = data[2]&0xFF;//CRC lower byte in EEPROM line2
 return checkSum == crcCalc(data, len);
}

//read data beginning in EEPROM line 3 to line 17, append line 0 to line 2
uint8_t crcCalc(uint16_t* data, int len) {
 uint8_t crcData8[len*2];
 for(int i = 0; i < len; i++) {
  crcData8[i*2] =     ( data[(i+3)%18] >>8 ) & 0xFF;//read upper 8 bit
  crcData8[i*2+1] = ( data[(i+3)%18]       ) & 0xFF;//read lower 8 bit
 }
return crc8(crcData8, len*2-1); //do not include last byte (line 2 lower byte)
}

// CRC calculation
uint8_t crc8(uint8_t *data, uint8_t length) {
 uint32_t crc;
 int16_t i, bit;
 crc = CRC_SEED;
  for (i = 0; i < length; i++) {
   crc ^= data[i];
   for (bit = 0; bit < 8; bit++) {
    if ((crc & 0x80) != 0) {
    crc <<= 1;
    crc ^= CRC_POLYNOMIAL;
    } else {
    crc <<= 1;
  }
  }
 }
 return ~crc;  // ~crc = crc^0xFF;
}
```

5 Operation Mode

The default output mode is semi-differential mode $V_{OQ} = V_{OQbid1}$.

5.1 Single-Ended Mode

The sensors reference voltage pin is set as input and supplied by an external reference voltage generation circuit. The V_{REF} input leakage current of up to 20µA has to be considered in the design of the reference voltage generation circuit.

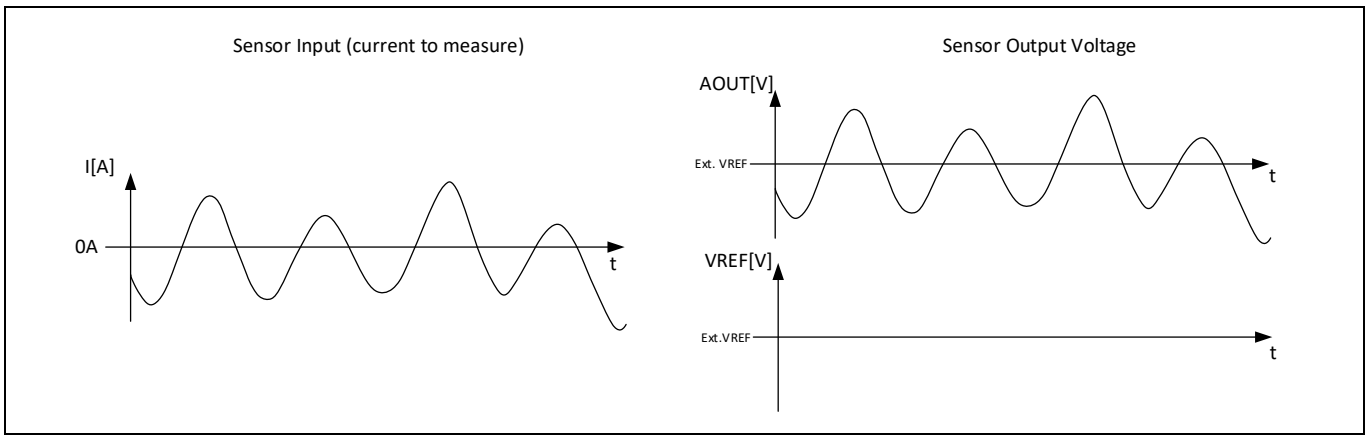

Figure 15 Sensor output signal dependent on input signal waveform in single-ended mode

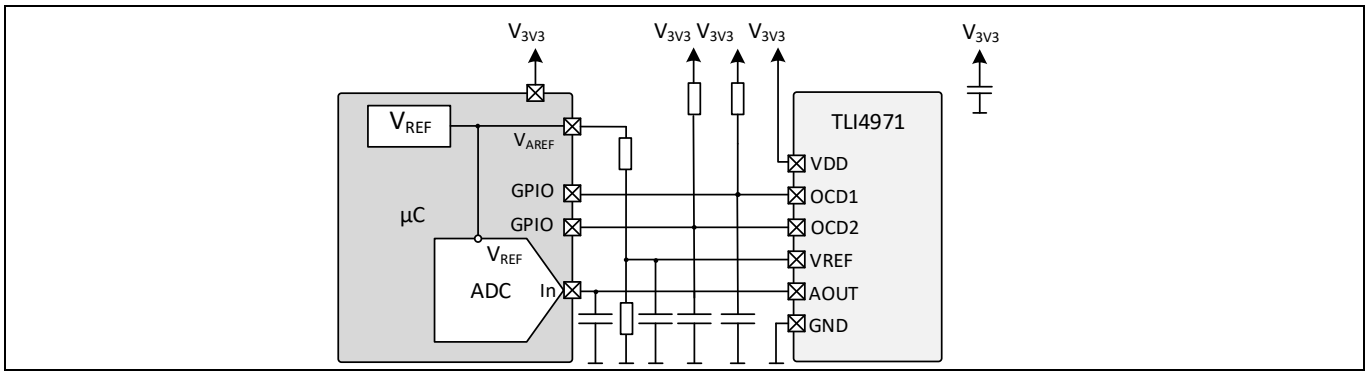

Figure 16 TLI4971 connected to µC in single-ended mode

5.2 Fully-differential Mode

In fully differential output mode, both V_{REF} and A_{OUT} are analog outputs to achieve double voltage swing.

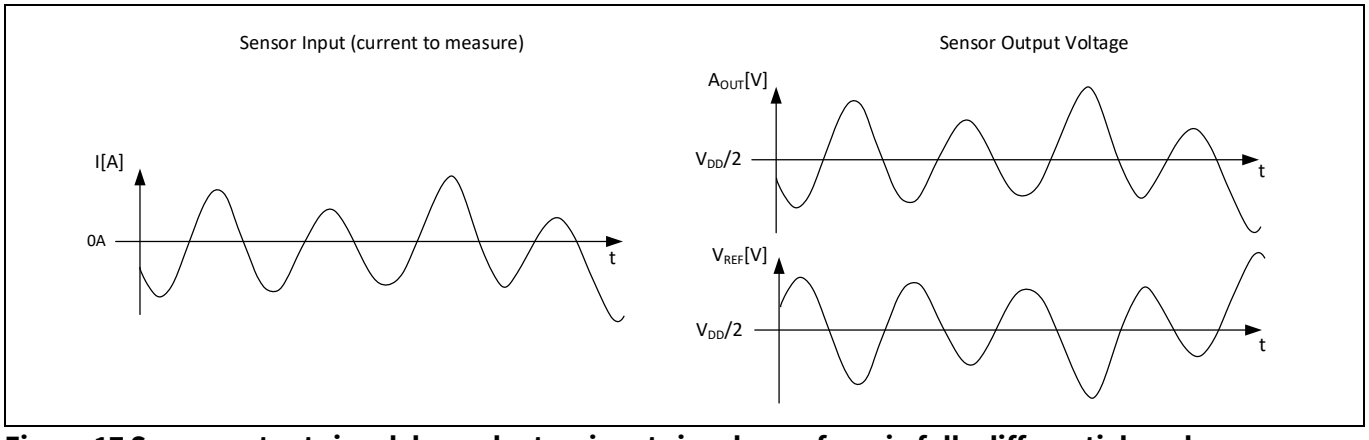

Figure 17 Sensor output signal dependent on input signal waveform in fully differential mode

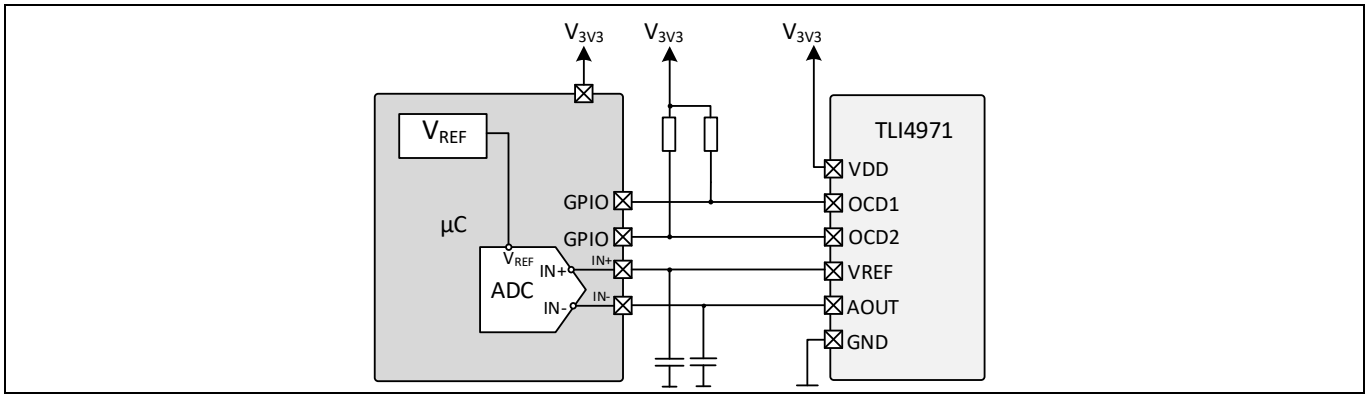

Figure 18 TLI4971 (fully-differential mode) connected to differential ADC

5.3 Semi-differential Mode

In Semi-Differential Output Mode, the sensor is using a chip-internal reference voltage. This reference voltage is then provided on the VREF. Therefore, the reference voltage can be monitored by the microcontroller and/or used for other devices as a reference voltage (cascade setup). The current-dependent output signal is provided as single-ended signal on AOUT.

The Quiescent Voltage will be set to a value in the middle of the voltage range or at 1.5V (V_{OQbid}) to measure bidirectional current values, whereas when the direction of the current is already known by the application, the quiescent voltage can be set to a lower value (V_{OQuni}) in order to better exploit the full voltage range.

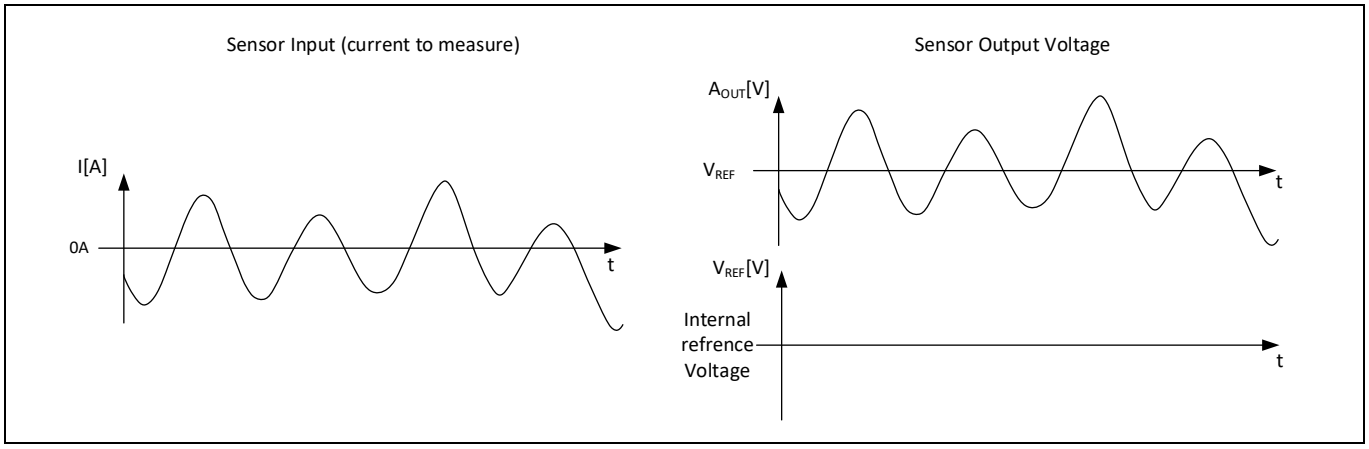

Figure 19 Sensor output signal dependent on input signal waveform in semi-differential mode

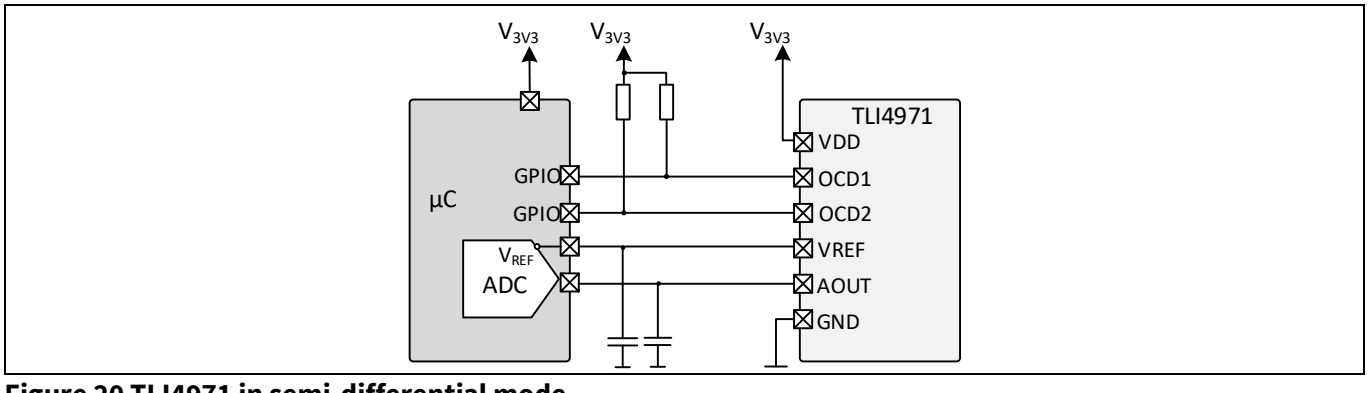

Figure 20 TLI4971 in semi-differential mode

6 How to connect the sensor in a 5V domain

This chapter gives a proposal how to connect the 3.3V sensor device with a 5V microcontroller.

Table 16 Electric parameter for application circuit

Name	Value	Unit
Capacitor on VDD	220	nF
Capacitor on analog outputs	6.8	nF
Pull up resistor on OCDs	4.7	kΩ

6.1 Single-Ended Mode

The open drain output of the OCD2 can be connected via the pull up resistor to the 5V.
The OCD1 has to be separated from the 5V with a level shifter since the maximum voltage is limited to 3.6V.

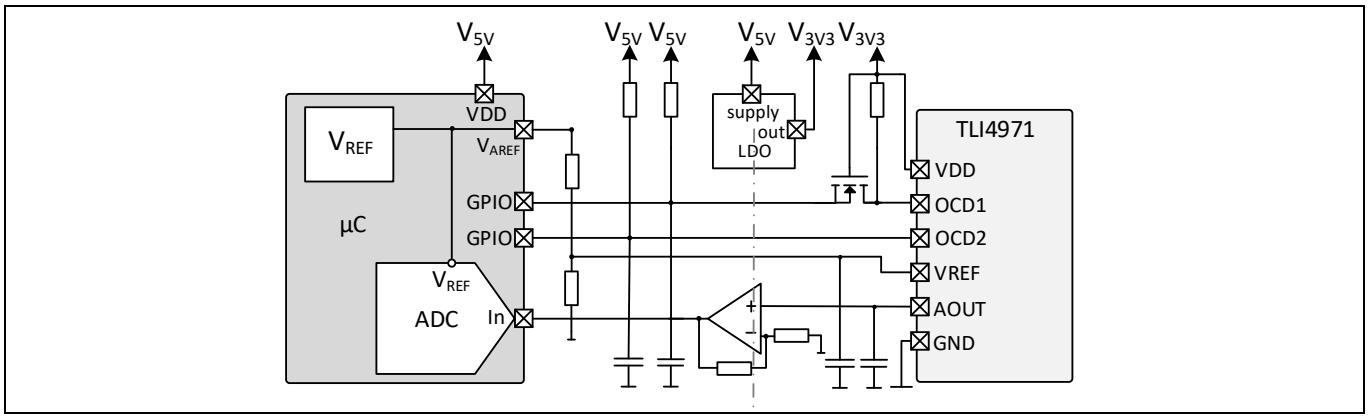

Figure 21 TLI4971 3.3 to 5V topology approach for single-ended mode

6.2 Semi and or Fully-differential Mode

In order to connect the sensor within a 5V environment an amplifier for each analog output can be part of the signal conditioning circuit as shown Figure 22.

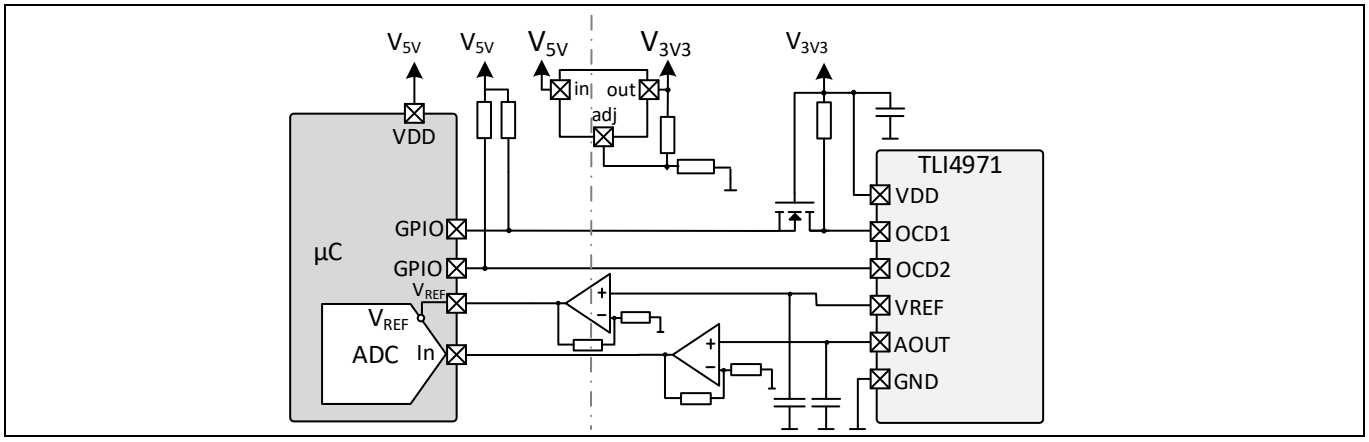

Figure 22 TLI4971 in fully differential mode (using two ADC input)

7 Diagnosis Mode

General Description

The TLI4971 current sensor is equipped with an internal self-diagnosis mode. It can be enabled by setting bit 14 at address 0x51 to logical one.

In order to verify the full functionality of the device signal path and the external signal conditioning circuit the diagnosis mode can be activated externally.

The diagnosis mode can be activated at any time after start up by forcing the OCD2 for at least 100µs to GND. The programmed threshold limits for the OCD channels are modified during the diagnosis test is activated. It is recommended to run the diagnosis mode as an initial test after startup.

The sensor converts the magnetic flux density to output voltage, which is linearly proportional to the current through the sensor package. In diagnosis mode, an additional known test voltage will be add at the Hall probes to the current depending output voltage.

The voltage caused by the test signal is equivalent to a primary current of 40A. The output voltage at A_{OUT} is dependent on the sensitivity range.

The threshold voltage of the OCD comparators is set to fixed values (V_{TEST} x 1.2, V_{TEST} x 0.8) as seen in Figure 24.

How to Operate

Ensure the OCD2 are not pull together in a multiple sensor setup. If connect together and Diagnosis Mode is enabled there will be interaction between the sensors: In an overcurrent event one sensor can trigger the diagnosis of the other sensor. The diagnosis event of the other sensor will trigger the diagnosis of the first sensor. A deadlock exist.

Force OCD2 to GND for at least 100µs to activate the diagnosis mode.

Observe the voltage on the A_{OUT} and V_{REF} pin according to the timing shown in Figure 24.

- The additional output voltage caused by the test mode corresponds to an input current of about 40A.
- The A_{OUT} voltage will change accordingly to the set sensitivity range.

The current sensor operates in normal mode after 4 times 250 µs = 1 ms.

Recommendation

To avoid unintended activation, the minimum pulse width of the activation pulse applied at OCD2 has to meet the minimum timing constraint of 100µs.

Since the OCD2 is kept to GND after startup by the sensor, the capacitance on the OCD2 pin shall be low to avoid unintended activation of the diagnosis mode because of a to slow release of the OCD2 level. This can happen if the threshold level for a logic “1” (1.6V) is not reached within 100µs.

If all OCD2 in a multiple current sensor system are connected together the OCD2 fault indication might activate an unintended activation of the diagnosis mode by forcing the pin to ground due to an over current event.

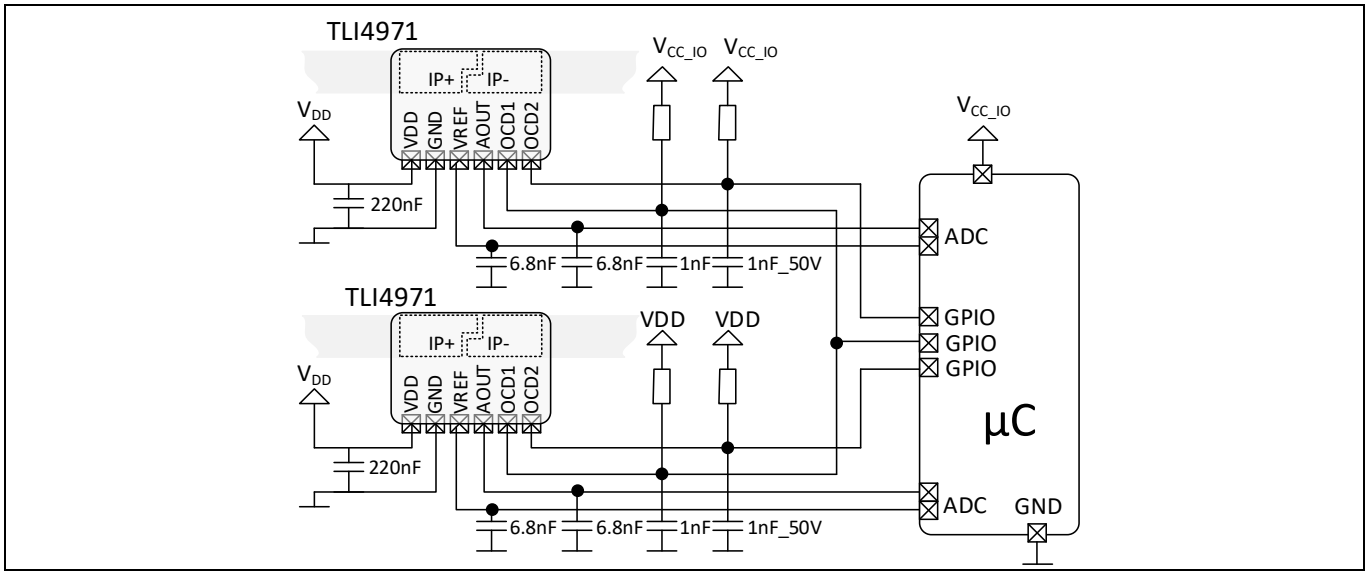

Figure 23 Application Circuit for diagnosis mode, OCD2 are wired separately

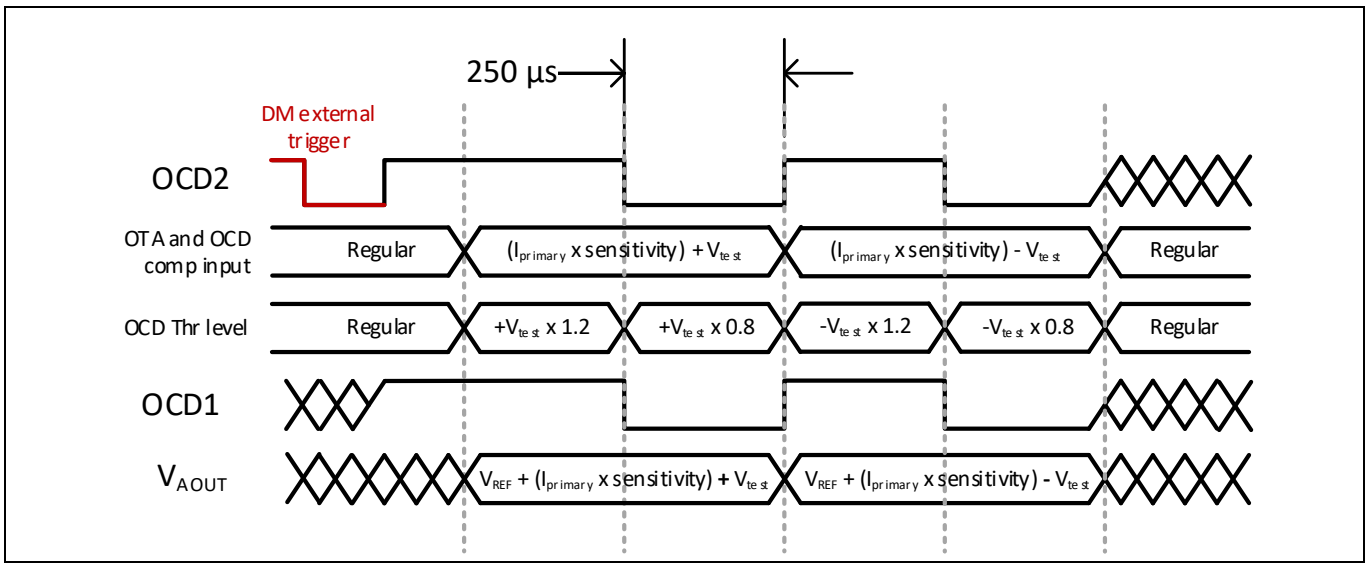

Figure 24 Diagnosis mode timing if 0A applied in the primary current path

8 Glossary

FS	Full Scale
SICI	Serial Inspection and Configuration Interface
EEPROM	Electrically Erasable Programmable Read-Only Memory
CRC	Cyclic Redundancy Check
VDD	Supply voltage
ISM	Intelligent State Machine
A/D	Analog Digital Converter Input
ADC	Analog to Digital Converter
FSR	Full Scale Range
CGS	Computer Gesteuerte Systeme GmbH……..
NI	National Instruments™
PC	Personal Computer
USB	Universal Serial Bus
OCD	Over Current Detection
VREF	Reference Voltage
AOUT	Analog Output
GND	Ground
GPIO	General Purpose Input Output
I/O	Input / Output
PWM	Pulse Width Modulation
NOP	No Operation
MSB	Most Significant Bit
LSB	Least Significant Bit
AC	Alternating Current
IGBT	Insulated Gate Bipolar Transistor
µC	Micro Controller
GPD	General Purpose Drive
IFX	Infineon

Revision history

Document version	Date of release	Description of changes
Rev. 1.30	2022-03-01	Updated typo in note (table 1) Updated register address (table 5)
		Added position of Diagnosis_mode_enable_bit in chapter 7
		Combine table 12..14 into Table 9..11 and renumber all later tables
		Delete chapter 8 (OCD-Settings Overview)
		Added chapter 4.3 (Margin test)
		Shorten chapter 5 and remove table 16
		Editorial changes
		Changed to revision V1.3
Rev. 1.20	2021-03-01	Updated “Enter Interface Sequence” Updated OCD-settings Updated programming voltage
		Editorial changes
Rev. 1.10	2020-03-01	Change OCD setting
		Updated OCD example
Rev. 1.00	2019-12-20	Initial version

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2022-03-01

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference
AppNote_TLI4971_ProgGuide

IMPORTANT NOTICE

The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.