# Table of Contents

1. **Overview** ......................................................... 3
2. **Block Diagram** .................................................. 4
3. **Pin Configuration** ................................................ 5
   3.1 Pin Assignment PG-DSO8-EP .................................... 5
   3.2 Pin Definitions and Functions PG-DSO8-EP ..................... 5
4. **General Product Characteristics** ................................. 6
   4.1 Absolute Maximum Ratings ..................................... 6
   4.2 Functional Range ................................................ 7
   4.3 Thermal Resistance .............................................. 7
5. **Block Description and Electrical Characteristics** ............. 8
   5.1 Voltage Regulation ............................................... 8
   5.2 Typical Performance Characteristics Voltage Regulator ...... 10
   5.3 Current Consumption ............................................ 13
   5.4 Typical Performance Characteristics Current Consumption ... 14
6. **Application Information** ......................................... 15
   6.1 Application Diagram ............................................ 15
   6.2 Selection of External Components ............................... 15
     6.2.1 Input Pin .................................................. 15
     6.2.2 Output Pin ................................................ 15
   6.3 Thermal Considerations .......................................... 16
   6.4 Reverse Polarity Protection .................................... 17
   6.5 Further Application Information ............................... 17
7. **Package Outlines** ............................................... 18
   7.1 Further Application Information ............................... 18
8. **Revision History** ................................................ 19
Low Dropout Linear Fixed Voltage Regulator

1 Overview

Features
- Output Voltage 5 V and 3.3 V
- Output Voltage Precision ±2 %
- Output Current up to 400 mA
- Ultra Low Current Consumption 38 µA
- Very Low Dropout Voltage: 100 mV at 100 mA Output Current
- Extended Operating Range Starting at 3.3 V
- Small Output Capacitor 1 µF
- Output Current Limitation
- Overtemperature Shutdown
- Suitable for Use in Automotive Electronics
- Wide Temperature Range from -40 °C up to 150 °C
- Green Product (RoHS compliant)
- AEC Qualified

Description
The TLF80511EJ is a linear low dropout voltage regulator for load currents up to 400 mA. An input voltage of up to 40 V is regulated to \( V_{Q,nom} = 5 \text{ V} \) (TLF80511EJV50) or \( V_{Q,nom} = 3.3 \text{ V} \) (TLF80511EJV33) with ±2 % precision. The TLF80511EJ with a typical quiescent current of 38 µA, is the ideal solution for systems requiring very low operating currents, such as those permanently connected to a battery.

It features a very low dropout voltage of 100 mV, when the output current is less than 100 mA. In addition, the dropout region begins at input voltages of 3.3 V (extended operating range). This makes the TLF80511EJ suitable to supply automotive systems.

In addition, the TLF80511’s new fast regulation concept requires only a single, 1 µF output capacitor to maintain stable regulation.

The device is designed for the harsh environment of automotive applications. Therefore standard features like output current limitation and overtemperature shutdown are implemented and protect the device against failures like output short circuit to GND, over-current and over-temperatures. The TLF80511EJ can be also used in all other applications requiring a stabilized 5 V or 3.3 V supply voltage.

<table>
<thead>
<tr>
<th>Type</th>
<th>Package</th>
<th>Marking</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLF80511EJV50</td>
<td>PG-DSO8-EP</td>
<td>80511V5</td>
</tr>
<tr>
<td>TLF80511EJV33</td>
<td>PG-DSO8-EP</td>
<td>80511V3</td>
</tr>
</tbody>
</table>
2 Block Diagram

Figure 1  Block Diagram
3 Pin Configuration

3.1 Pin Assignment PG-DSO8-EP

![Pin Configuration Diagram](image)

<table>
<thead>
<tr>
<th>Pin Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>I</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>n.c.</td>
</tr>
<tr>
<td>4</td>
<td>Q</td>
</tr>
<tr>
<td>5, 6, 7, 8</td>
<td>n.c.</td>
</tr>
<tr>
<td>Pad</td>
<td>-</td>
</tr>
</tbody>
</table>
4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings  
$T_j = -40 \, ^\circ\text{C}$ to $+150 \, ^\circ\text{C}$; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input I</td>
<td>$V_I$</td>
<td>-0.3 – 45</td>
<td>V</td>
<td>–</td>
</tr>
<tr>
<td>Output Q</td>
<td>$V_Q$</td>
<td>-0.3 – 7</td>
<td>V</td>
<td>–</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_j$</td>
<td>-40 – 150</td>
<td>°C</td>
<td>–</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>$T_{stg}$</td>
<td>-55 – 150</td>
<td>°C</td>
<td>–</td>
</tr>
<tr>
<td>ESD Susceptibility</td>
<td>$V_{ESD}$</td>
<td>-4 – 4</td>
<td>kV</td>
<td>HBM$^2$</td>
</tr>
<tr>
<td>ESD Susceptibility</td>
<td>$V'_{ESD}$</td>
<td>-1.5 – 1.5</td>
<td>kV</td>
<td>CDM$^3$</td>
</tr>
</tbody>
</table>

1) Not subject to production test, specified by design.  
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k Ω, 100 pF)  
3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101  

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.  

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.
4.2 Functional Range

Table 2 Functional Range

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range for Normal Operation</td>
<td>$V_i$</td>
<td>$V_{Q,nom} + V_{dr}$</td>
<td>–</td>
<td>40 V</td>
<td>–</td>
</tr>
<tr>
<td>Extended Input Voltage Range</td>
<td>$V_{I,ext}$</td>
<td>3.3</td>
<td>–</td>
<td>40 V</td>
<td>$T_j &gt; 25 ^\circ C$ 1)</td>
</tr>
<tr>
<td>Output Capacitor’s Requirements for Stability</td>
<td>$C_Q$</td>
<td>1</td>
<td>–</td>
<td>–</td>
<td>μF 2)</td>
</tr>
<tr>
<td>Output Capacitor’s Requirements for Stability</td>
<td>$ESR(C_Q)$</td>
<td>–</td>
<td>–</td>
<td>5 Ω</td>
<td>3)</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>$T_j$</td>
<td>–40</td>
<td>–</td>
<td>150 °C</td>
<td>–</td>
</tr>
</tbody>
</table>

1) Between min. value and $V_{Q,nom} + V_{dr}$: $V_Q = V_I - V_{dr}$. Below min. value: $V_Q = 0$ V
2) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%
3) relevant ESR value at $f = 10$ kHz

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

Table 3 Thermal Resistance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Case 1)</td>
<td>$R_{i,jc}$</td>
<td>–</td>
<td>–</td>
<td>41</td>
<td>K/W</td>
</tr>
<tr>
<td>Junction to Ambient 1)</td>
<td>$R_{i,ja}$</td>
<td>–</td>
<td>–</td>
<td>152</td>
<td>K/W</td>
</tr>
<tr>
<td>Junction to Ambient 1)</td>
<td>$R_{i,ja}$</td>
<td>–</td>
<td>–</td>
<td>67</td>
<td>K/W</td>
</tr>
<tr>
<td>Junction to Ambient 1)</td>
<td>$R_{i,ja}$</td>
<td>–</td>
<td>–</td>
<td>56</td>
<td>K/W</td>
</tr>
</tbody>
</table>

1) Not subject to production test, specified by design
2) Specified $R_{i,ja}$ value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 2 inner copper layers (2 x 70μm Cu, 2 x 35μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.
3) Specified $R_{i,ja}$ value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm³ board with 1 copper layer (1 x 70μm Cu).
5 Block Description and Electrical Characteristics

5.1 Voltage Regulation

The output voltage $V_Q$ is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor $C_Q$, the load current, the chip temperature and the internal circuit design. To ensure stable operation, the output capacitor’s capacitance and its equivalent series resistor ESR requirements given in Table 2 “Functional Range” on Page 7 must be maintained. For details see the typical performance graph “Stability Region: Equivalent Serial Resistor ESR versus Output Current $I_Q$ (TLF80511EJV50)” on Page 11. Since the output capacitor is used to buffer load steps, it should be sized according to the application’s needs.

An input capacitor $C_I$ is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the regulator terminals.

Whenever the load current exceeds the specified limit, e.g. in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled, the regulator restarts. This oscillatory thermal behaviour causes the junction temperature to exceed the 150° C maximum and significantly reducing the IC’s life.

![Block Diagram Voltage Regulation](ApplicationDiagram.vsd)
### Table 4  Electrical Characteristics Voltage Regulator 5 V and 3.3 V version

\( V_i = 13.5 \, V; \ T_j = -40 \, ^\circ C \) to +150 \, ^\circ C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Precision</td>
<td>( V_Q )</td>
<td>4.9</td>
<td>5.0</td>
<td>5.1</td>
<td>V</td>
</tr>
<tr>
<td>TLF80511EJV50</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Precision</td>
<td>( V_Q )</td>
<td>4.9</td>
<td>5.0</td>
<td>5.1</td>
<td>V</td>
</tr>
<tr>
<td>TLF80511EJV50</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Precision</td>
<td>( V_Q )</td>
<td>3.23</td>
<td>3.3</td>
<td>3.37</td>
<td>V</td>
</tr>
<tr>
<td>TLF80511EJV33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage Precision</td>
<td>( V_Q )</td>
<td>3.23</td>
<td>3.3</td>
<td>3.37</td>
<td>V</td>
</tr>
<tr>
<td>TLF80511EJV33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Current Limitation</td>
<td>( I_{Q,\text{max}} )</td>
<td>401</td>
<td>600</td>
<td>900</td>
<td>mA</td>
</tr>
<tr>
<td>Load Regulation steady-state</td>
<td>(</td>
<td>\Delta V_{Q,\text{load}}</td>
<td>)</td>
<td>–</td>
<td>20</td>
</tr>
<tr>
<td>Line Regulation steady-state</td>
<td>(</td>
<td>\Delta V_{Q,\text{line}}</td>
<td>)</td>
<td>–</td>
<td>10</td>
</tr>
<tr>
<td>Dropout Voltage 1) ( V_{dr} = V_i - V_Q )</td>
<td>( V_{dr} )</td>
<td>–</td>
<td>250</td>
<td>500</td>
<td>mV</td>
</tr>
<tr>
<td>TLF80511EJV50</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dropout Voltage 1) ( V_{dr} = V_i - V_Q )</td>
<td>( V_{dr} )</td>
<td>–</td>
<td>100</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>TLF80511EJV50</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dropout Voltage 1) ( V_{dr} = V_i - V_Q )</td>
<td>( V_{dr} )</td>
<td>–</td>
<td>320</td>
<td>650</td>
<td>mV</td>
</tr>
<tr>
<td>TLF80511EJV33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dropout Voltage 1) ( V_{dr} = V_i - V_Q )</td>
<td>( V_{dr} )</td>
<td>–</td>
<td>130</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>TLF80511EJV33</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Ripple Rejection 2)</td>
<td>( PSRR )</td>
<td>–</td>
<td>55</td>
<td>–</td>
<td>dB</td>
</tr>
<tr>
<td>TLF80511EJV50</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Overtemperature Shutdown Threshold</td>
<td>( T_{J,\text{sd}} )</td>
<td>151</td>
<td>175</td>
<td>200</td>
<td>°C</td>
</tr>
<tr>
<td>Overtemperature Shutdown Threshold Hysteresis</td>
<td>( T_{J,\text{sdh}} )</td>
<td>–</td>
<td>15</td>
<td>–</td>
<td>K</td>
</tr>
</tbody>
</table>

1) Measured when the output voltage \( V_Q \) has dropped 100 mV from the nominal value obtained at \( V_i = 13.5 \, V \)
2) Not subject to production test, specified by design
5.2 Typical Performance Characteristics Voltage Regulator

Typical Performance Characteristics

Output Voltage $V_O$ versus Junction Temperature $T_j$ (TLF80511EJV50)

Dropout Voltage $V_{dr}$ versus Junction Temperature $T_j$ (TLF80511EJV50)

Dropout Voltage $V_{dr}$ versus Output Current $I_O$ (TLF80511EJV50)

Maximum Output Current $I_O$ versus Input Voltage $V_I$ (TLF80511EJV50)
Load Regulation $\Delta V_{Q,\text{load}}$ versus Output Current Change $\Delta I_Q$ (TLF80511EJV50)

Line Regulation $\Delta V_{Q,\text{line}}$ versus Input Voltage $\Delta V_I$ (TLF80511EJV50)

Power Supply Ripple Rejection versus Frequency (TLF80511EJV50)

Stability Region: Equivalent Serial Resistor $ESR$ versus Output Current $I_Q$ (TLF80511EJV50)
Output Voltage $V_O$ versus Input Voltage $V_I$ (TLF80511EJV50)

$V_I$ [V]  $V_O$ [V]

$I_O = 100$ mA  
$T_J = 25^\circ C$
### 5.3 Current Consumption

**Table 5 Electrical Characteristics Current Consumption**

$V_i = 13.5 \text{ V}; \ T_j = -40 \degree \text{C to } +150 \degree \text{C};$ all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
<th>Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current Consumption</td>
<td>$I_q$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_q = I_i - I_Q$</td>
<td></td>
<td>–</td>
<td>38</td>
<td>46 µA</td>
<td>$I_Q = 0.05 \text{ mA}$ $T_j &lt; 25 \degree \text{C}$</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>$I_q$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_q = I_i - I_Q$</td>
<td></td>
<td>–</td>
<td>–</td>
<td>75 µA</td>
<td>$I_Q = 0.05 \text{ mA}$ $T_j &lt; 125 \degree \text{C}$</td>
</tr>
<tr>
<td>Current Consumption</td>
<td>$I_q$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_q = I_i - I_Q$</td>
<td></td>
<td>–</td>
<td>67</td>
<td>80 µA</td>
<td>$I_Q = 400 \text{ mA}$ $T_j &lt; 125 \degree \text{C}^{1)$}</td>
</tr>
</tbody>
</table>

1) Not subject to production test, specified by design.
5.4 Typical Performance Characteristics Current Consumption

Typical Performance Characteristics

Current Consumption $I_q$ versus Output Current $I_Q$ (TLF80511EJV50)

![Graph showing $I_q$ vs $I_Q$ at $T_j = 25°C$, $V_I = 13.5V$, $R_{LOAD} = 100Ω$]  

Current Consumption $I_q$ versus Input Voltage $V_I$ (TLF80511EJV50)

![Graph showing $I_q$ vs $V_I$ at $T_j = -40°C$, $-25°C$, $150°C$, $R_{LOAD} = 100Ω$]
6 Application Information

6.1 Application Diagram

Figure 4 Application Diagram

6.2 Selection of External Components

6.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100nF to 470nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10µF to 470µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

6.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in “Functional Range” on Page 7. The graph “Stability Region: Equivalent Serial Resistor ESR versus Output Current I_Q (TLF80511EJV50)” on Page 11 shows the stable operation range of the device.

TLF80511EJ is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator’s output and GND pins and on the same side of the PCB as the regulator itself.
In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

### 6.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

\[
P_D = (V_i - V_Q) \times I_Q + V_i \times I_q\]

with

- \(P_D\): continuous power dissipation
- \(V_i\): input voltage
- \(V_Q\): output voltage
- \(I_Q\): output current
- \(I_q\): quiescent current

The maximum acceptable thermal resistance \(R_{thJA}\) can then be calculated:

\[
R_{thJA,max} = \frac{(T_{j,max} - T_a)}{P_D}
\]

with

- \(T_{j,max}\): maximum allowed junction temperature
- \(T_a\): ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in “Thermal Resistance” on Page 7.

### Example

Application conditions:

\(V_i = 13.5V\)
\(V_Q = 5V\)
\(I_Q = 120mA\)
\(T_a = 85^\circ C\)

Calculation of \(R_{thJA,max}\):

\[
P_D = (V_i - V_Q) \times I_Q + V_i \times I_q\]
\(= (13.5V - 5V) \times 120mA\)
\(= 1.02W\)

\[
R_{thJA,max} = \frac{(T_{j,max} - T_a)}{P_D}
\]
\(= \frac{(150^\circ C - 85^\circ C)}{1.02W} = 63.73K/W\)

As a result, the PCB design must ensure a thermal resistance \(R_{thJA}\) lower than 63.73 K/W. According to “Thermal Resistance” on Page 7, at least 600 mm\(^2\) heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.
6.4 Reverse Polarity Protection

TLF80511EJ is not self protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is needed. The absolute maximum ratings of the device as specified in “Absolute Maximum Ratings” on Page 6 must be kept.

6.5 Further Application Information

- For further information you may contact http://www.infineon.com/
7 Package Outlines

![Package Outlines Diagram](image)

7.1 Further Application Information

- For further information you may contact [http://www.infineon.com/](http://www.infineon.com/)
8 Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>2014-11-17</td>
<td>Data Sheet - Initial version</td>
</tr>
</tbody>
</table>
Legal Disclaimer

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Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.