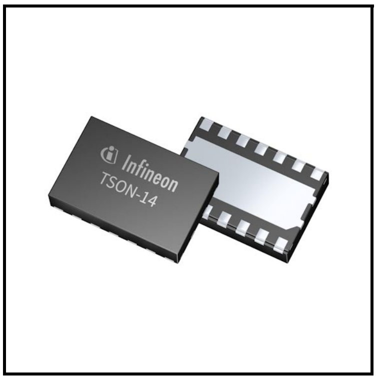
OPTIREG™ linear TLF4477-3LA

Dual-channel low drop out linear voltage regulator



Features

- Integrated current monitor
- Overvoltage, overtemperature and overcurrent detection
- Adjustable output voltage
- Output current up to 300 mA
- Adjustable output current limitation
- Very low current consumption
- Very low dropout voltage
- Stable with ceramic output capacitor of 1 µF
- Wide input voltage range up to 40 V
- Reverse current protection
- Reverse polarity protection
- Short circuit protection
- Overtemperature shutdown
- Automotive temperature range -40°C ≤ T_j ≤ 150°C
- Green Product (RoHS compliant)

Potential applications

- Infotainment active antenna power supply
- Surround view camera power supply
- Automotive applications that are permanently connected to the battery

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear TLF4477-3LA is a monolithic integrated dual channel low drop out voltage regulator capable of supplying loads up to 300 mA. For an input voltage up to 40 V the TLF4477-3LA provides an adjustable output voltage in the range from 3 V up to 20 V in a thermally enhanced PG-TSON-14 package.

The channel specific current monitors of the TLF4477-3LA provide access to unique diagnostic and protection features. They measures the output currents and translate them to a proportional voltage at the current sense output CSOx. The output current limits for each channel can be manually set by via an external resistor.

Overtemperature, overcurrent and output overvoltage fault conditions can be detected as an analogue voltage level at the current sense output CSOx above the current sensing range.

Separate digital status pins ST1 and ST2 for each channel can indicate the presence of one or multiple of the aforementioned faults.

The outputs of the device can be disabled independently via the enable signals on EN1 and EN2 to reduce power consumption.

The CSOxSel selects the channel monitored at the CSOx pin. CSOxSel can also set the monitor pin CSOx into a high impedance state. This allows the CSOx signals of multiple devices to be monitored by a single ADC connected.

Type	Package	Marking
TLF4477-3LA	PG-TSON-14	44773

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1 Block diagram

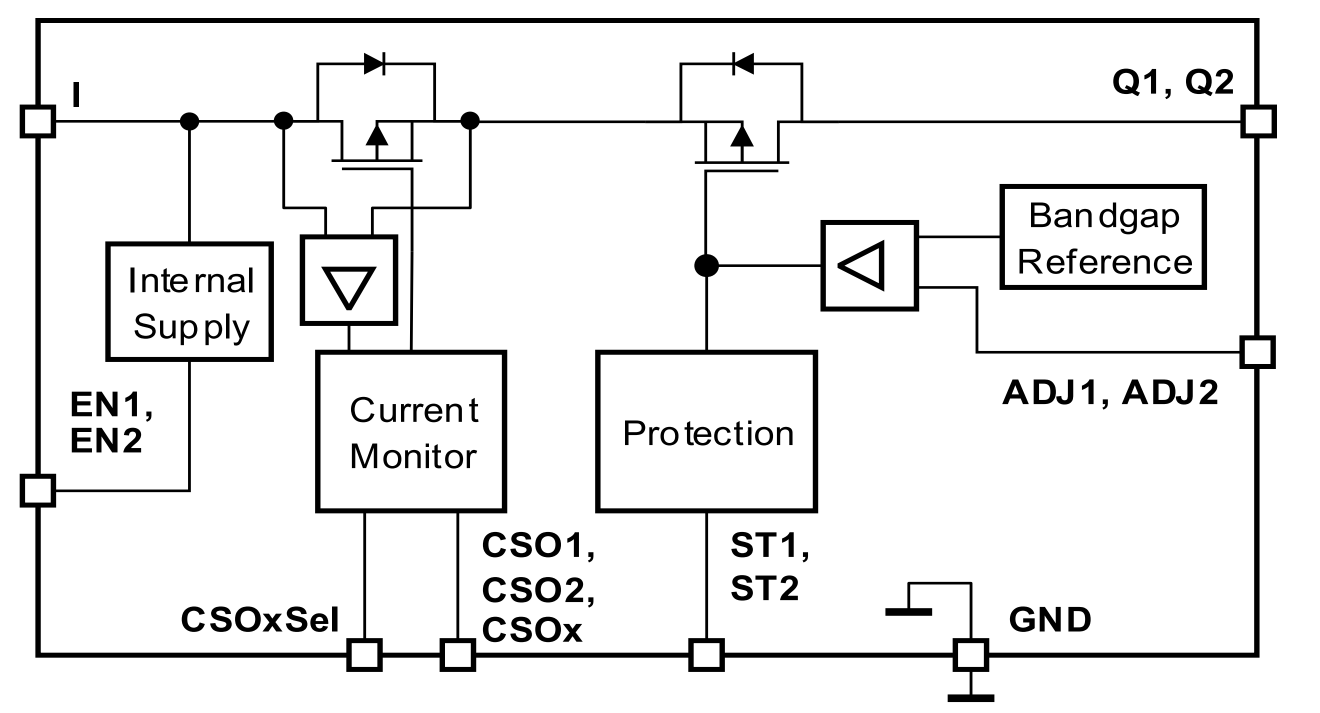


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

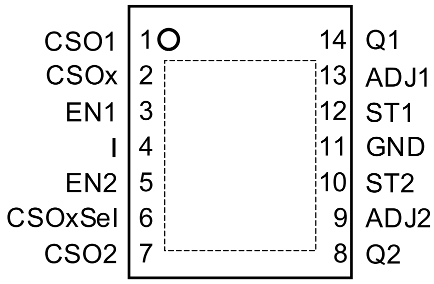


Figure 2 Pin configuration (top view)

2.2 Pin definitions and functions

Pin	Symbol	Function
1	CSO1	**Current sense output** Current monitor and status output for Q1. Connect a capacitor C_{CSO1} and resistor R_{CSO1} between CSO1 and GND close to the IC pins.
2	CSOx	**Current sense output** Current monitor and status for Q2, if CSOxSel is "high" ($V_{CSOxSel} = V_{CSOxSel,H}$). Current monitor and status for Q1, if CSOxSel is "low" ($V_{CSOxSel} = V_{CSOxSel,L}$). High impedance (HZ), if $V_{CSOxSel} = V_{CSOxSel,T}$ or if $V_{EN1} = V_{EN2} = V_{EN1,2,low}$.
3	EN1	**Enable** "High" signal ($V_{EN1} = V_{EN1,2,high}$) enables regulator output Q1. "Low" signal ($V_{EN1} = V_{EN1,2,low}$) disables regulator output Q1. Connect to I to permanently enable the output Q1. Internal pull-down (R_{EN1}), leave floating when Q1 permanently disabled.
4	I	**IC supply** It is recommended to place a capacitor from this pin to GND, close to the pins, in order to compensate for line influences.
5	EN2	**Enable** "High" signal ($V_{EN2} = V_{EN1,2,high}$) enables regulator output Q2. "Low" signal ($V_{EN2} = V_{EN1,2,low}$) disables regulator output Q2. Connect to I to permanently enable the output Q2. Internal pull-down (R_{EN2}), leave floating when Q2 permanently disabled.
6	CSOxSel	**Current sense output selection** "High" signal ($V_{CSOxSel} = V_{CSOxSel,H}$) CSOx is the current monitor and status for Q2. "Low" signal ($V_{CSOxSel} = V_{CSOxSel,L}$) CSOx is the current monitor and status for Q1. $V_{CSOxSel} = V_{CSOxSel,T}$ sets CSOx to high impedance (HZ).
7	CSO2	**Current sense output** Current monitor and status output for Q2. Connect a capacitor C_{CSO2} and resistor R_{CSO2} between CSO2 and GND close to the IC pins.

Pin	Symbol	Function
8	Q2	**Regulator output** Connect a capacitor between Q2 and GND close to the IC pins, respecting the values given for its capacitance C_{Q2} and ESR in **Functional range**.
9	ADJ2	**Voltage adjust** Connect an external voltage divider to configure the nominal output voltage Q2.
10	ST2	**Status output** Digital output signal with open drain output. A “low” signal ($V_{ST2} = V_{ST1,2,low}$) indicates fault conditions at the regulator‘s output Q2.
11	GND	**Ground**
12	ST1	**Status output** Digital output signal with open drain output. A “low” signal ($V_{ST1} = V_{ST1,2,low}$) indicates fault conditions at the regulator‘s output Q1.
13	ADJ1	**Voltage adjust** Connect an external voltage divider to configure the nominal output voltage Q1.
14	Q1	**Regulator output** Connect a capacitor between Q1 and GND close to the IC pins, respecting the values given for its capacitance C_{Q1} and ESR in **Functional range**.
Pad	–	**Exposed pad** Connect the exposed pad to a heat sink area. Connect the exposed pad to GND.

3 General product characteristics

3.1 Absolute maximum ratings

Table 1 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
IC supply I	V_I	-40	–	45	V	$\|V_I - V_{Q1,2}\|$ < 35 V	P_4.1.1
Enable input EN	$V_{EN1,2}$	-40	–	45	V	$\|V_{EN1,2} - V_I\|$ < 60 V	P_4.1.2
CSOxSel	$V_{CSOxSel}$	-0.3	–	5	V	–	P_4.1.3
Voltage adjust input ADJ	$V_{ADJ1,2}$	-0.3	–	24	V	–	P_4.1.4
Regulator output Q	$V_{Q1,2}$	-0.3	–	45	V	–	P_4.1.5
Current monitor out CSO	$V_{CSO1,2,x}$	-0.3	–	5	V	–	P_4.1.6
Status output	$V_{ST1,2}$	-0.3	–	45	V	[2)] see also **"Status output signal ST1, ST2"**	P_4.1.7
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.8
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.9
ESD susceptibility							
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	[3)] HBM	P_4.1.10
ESD susceptibility to GND	V_{ESD}	-500	–	500	V	[4)] CDM	P_4.1.11
ESD susceptibility pin 1, 7, 8, 14 (corner pins) to GND	$V_{ESD1,7,8,14}$	-750	–	750	V	[4)] CDM	P_4.1.12

1) Not subject to production test, specified by design.
2) Special care must be taken to control (for by optical inspection) the proper handling of ST pin with an external resistor and not connecting directly to a higher voltage level, which allows an uncontrolled current flowing into the pin.
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
4) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101.

Notes

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as outside normal operating range. Protection functions are not designed for continuous repetitive operation.*
2. *Stresses above the ones listed her may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

3.2 Functional range

Table 2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	$V_{Q1,2}$ + V_{dr}	–	40	V	$(V_I - V_{Q1,2}) < 35$ V $V_I > 5.5$ V	P_4.2.1
Enable voltage	$V_{EN1,2}$	0		40	V	–	P_4.2.2
Output voltage range	$V_{Q1,2}$	3	–	20	V	–	P_4.2.3
Current sense output resistor	$R_{CSO1,2}$	1.7	–	10.2	kΩ	–	P_4.2.4
Current sense output capacitor requirements	$C_{CSO1,2}$	1	–	4.7	µF	1)	P_4.2.5
Current sense output capacitor requirements	$ESR_{CSO1,2}$	–	–	10	Ω	1)	P_4.2.6
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.7
Output capacitor requirements	C_Q	1	–	–	µF	1)2)	P_4.2.8
Output capacitor requirements	ESR_{CQ}	–	–	10	Ω	1)3)	P_4.2.9

1) Not subject to production test, specified by design.
2) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.
3) Relevant ESR value at f = 10 kHz.

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

Table 3 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case bottom	R_{thJC}	–	9.5	–	K/W	Measured to the exposed pad	P_4.3.1
Junction to ambient	R_{thJA}	–	137	–	K/W	[2)] Footprint only	P_4.3.2
Junction to ambient	R_{thJA}	–	67	–	K/W	[2)] 300 mm^2 PCB heat sink area	P_4.3.3
Junction to ambient	R_{thJA}	–	57	–	K/W	[2)] 600 mm^2 PCB heat sink area	P_4.3.4
Junction to ambient	R_{thJA}	–	45	–	K/W	[3)] 2s2p PCB	P_4.3.5

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 1 copper layer (1 × 70 µm Cu).

3) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm^3 board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4 Voltage regulator

4.1 Description voltage regulator

The output voltage (V_{Q1}, V_{Q2}) is divided by an external resistor network and applied to the ADJ1 and ADJ2 pins as (V_{ADJ1}, V_{ADJ2}). The device compares the voltage V_{ADJ1}, V_{ADJ2} with an internal reference voltage and drives the pass transistor of each channel accordingly.

The following factors determine the stability of the control loop:

- Output capacitor
- Load currents I_{Q1}, I_{Q1}
- Chip temperature T_j
- Internal circuit design

Output capacitor

To ensure stable operation, the capacitance of the output capacitors (C_{Q1}, C_{Q2}) and its equivalent series resistors (ESR_{CQ1}, ESR_{CQ2}) requirements must be maintained, see **Functional range**. The output capacitor must be sized according to the requirements of the application.

Input capacitor

An input capacitor C_I is recommended to compensate line influences. Connect the capacitors close to the component's terminals.

Reverse polarity protection

A secondary PMOS detects and limits potential reverse current flow. An external reverse polarity protection diode is not needed. The reverse current must be taken into consideration for thermal design, since the thermal protection circuit does not operate in reverse polarity condition. For details on the reverse current see **Electrical characteristics: voltage regulator**.

Output current limitation

In addition to the channel specific and user-configurable current limitation on the CSO1 and CSO2 pins, an internal current limitation protects the device from destruction in case of catastrophic events. The internal current limitation is always active as a secondary protection feature. For details on how to set the user-configurable current limitation see **Adjustable output current limitation**.

Overtemperature shutdown

The overtemperature shutdown circuit prevents the device from immediate destruction in case of a fault condition, for example due to a permanent short circuit at the output. In such condition the overtemperature shutdown circuit switches off the power stage. After the device cools down again, the regulator restarts. This leads to an oscillatory behavior of the output voltages V_{Q1}, V_{Q2}. However, any junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the lifetime of the device.

Since the device allows for negative supply voltages, small currents can flow through the device in reverse direction increasing its junction temperature. This reverse current must be taken into account, since the overtemperature shutdown circuit does not mitigate its heating effects.

Voltage regulator

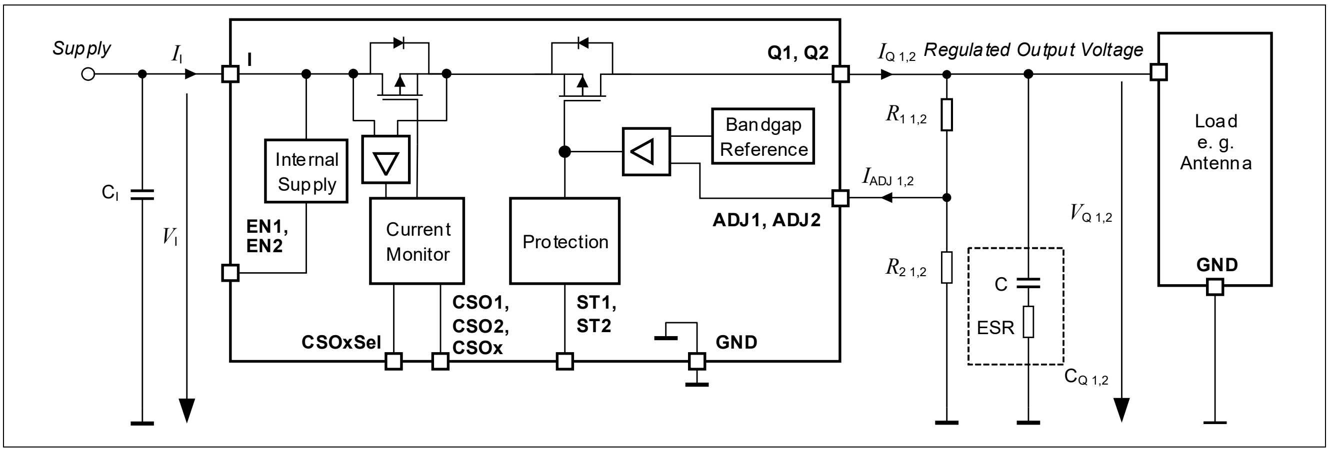


Figure 3 **Functional block diagram voltage regulator circuit**

4.2 Electrical characteristics voltage regulator

Table 4 Electrical characteristics: voltage regulator

V_I = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 8 "Application diagram" on Page 27** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference voltage	$V_{REF,int}$	–	1.2	–	V	[1]	P_5.2.1
Output voltage tolerance	$V_{Q1,2}$	-2	–	2	%	[2] 1 mA ≤ $I_{Q1,2}$ ≤ 300 mA; 9 V ≤ V_I ≤ 16 V; 3 V ≤ $V_{Q1,2}$ ≤ 14 V with $V_I > V_{Q1,2} + V_{dr}$ + 0.5 V	P_5.2.2
Output voltage tolerance	$V_{Q1,2}$	-2	–	2	%	1 mA ≤ $I_{Q1,2}$ ≤ 150 mA; 6 V ≤ V_I ≤ 16 V; 5 V ≤ $V_{Q1,2}$ ≤ 15 V with $V_I > V_{Q1,2} + V_{dr}$ + 0.5 V	P_5.2.3
Output voltage tolerance	$V_{Q1,2}$	-2	–	2	%	1 mA ≤ $I_{Q1,2}$ ≤ 100 mA; 16 V ≤ V_I ≤ 32 V; 3 V ≤ $V_{Q1,2}$ ≤ 15 V	P_5.2.4
Output voltage tolerance	$V_{Q1,2}$	-2	–	2	%	1 mA ≤ $I_{Q1,2}$ ≤ 10 mA; 32 V ≤ V_I ≤ 40 V; 3 V ≤ $V_{Q1,2}$ ≤ 16 V	P_5.2.5
Output voltage tolerance	$V_{Q1,2}$	-1.5	–	1.5	%	100 mA ≤ $I_{Q1,2}$ ≤ 300 mA; 8 V ≤ V_I ≤ 16 V; -40°C ≤ T_j ≤ 85°C; 7 V ≤ $V_{Q1,2}$ ≤ 9 V; $V_I > V_{Q1,2} + V_{dr}$ + 0.5 V	P_5.2.6
Load regulation steady state	$\Delta V_{Q1,2\ load}$	-30	-5	–	mV	$I_{Q1,2}$ = 1 mA to 250 mA; V_I = 6 V; $V_{Q1,2}$=5 V	P_5.2.7
Line regulation steady state	$\Delta V_{Q1,2,line}$	–	5	20	mV	V_I = 6 V to 32 V; $I_{Q1,2}$ = 5 mA; $V_{Q1,2}$ = 5 V	P_5.2.8
Power supply ripple rejection	*PSRR*	60	65	–	dB	[1] f_{ripple} = 100 Hz; V_{ripple} = 1 V_{pp}; $V_{Q1,2}$ = 5 V; $I_{Q1,2}$ < 100 mA	P_5.2.10
Dropout voltage $V_{dr} = V_I - V_{Q1,2}$	V_{dr}	–	200	350	mV	[3] $I_{Q1,2}$ = 100 mA; $V_{Q1,2}$ = 5 V	P_5.2.12
Dropout voltage $V_{dr} = V_I - V_{Q1,2}$	V_{dr}	–	350	650	mV	[3] $I_{Q1,2}$ = 200 mA; $V_{Q1,2}$ = 5 V	P_5.2.13
Output current limitation	$I_{Q1,2,lim}$	301	–	500	mA	0 V ≤ $V_{Q1,2}$ ≤ 0.95 × $V_{Q1,2,nom}$	P_5.2.15
Reverse current	$I_{Q1,2rev}$	-2	-1	–	mA	V_I =0 V; $V_{Q1,2}$ = 5 V	P_5.2.16
Reverse current at negative input voltage	I_{Irev}	-2.6	-0.1	–	mA	V_I = -16 V; $V_{Q1,2}$ = 0 V	P_5.2.17

Table 4 Electrical characteristics: voltage regulator (cont'd)

V_I = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 8 "Application diagram" on Page 27** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reverse current at output short to battery	$I_{QtoVbat}$	-40	–	–	µA	V_I = 5.8 V; $V_{Q1,2}$ = 16 V	P_5.2.18
Overtemperature shutdown threshold	$T_{j,sd}$	151	165	180	°C	[1] T_j increasing	P_5.2.19
Overtemperature shutdown threshold hysteresis	$T_{j,hy}$	5	10	15	K	[1] T_j decreasing	P_5.2.20

1) Not subject to production test, specified by design.
2) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation.
3) Measured when the output voltage $V_{Q1,2}$ has dropped 100 mV from its nominal value.

4.3 Application information for setting the variable output voltage

The output voltages of both outputs Q1, Q2 can be adjusted between 3 V and 20 V independently via an external output voltage divider, closing the control loops to their respective voltage adjust pins ADJ1, ADJ2.

The device compares the voltages at ADJ1, ADJ2 pins to the internal reference of typical 1.2 V with channel specific error amplifiers. Each error amplifier drives the channel's pass transistor accordingly to control the output voltage.

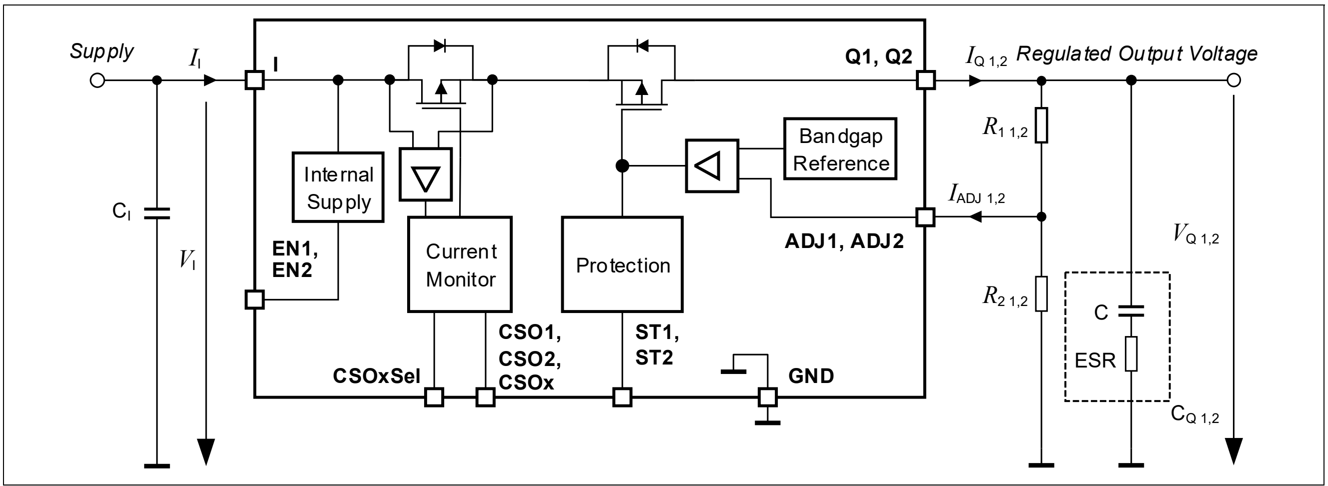


Figure 4 Application detail external components at output for variable voltage regulator

The output voltage is calculated according to **Equation (4.1)**:

$$V_{Q1,2} = (R_{1\,1,2} + R_{2\,1,2})/R_{2\,1,2} \times V_{REF,int}, \text{ neglecting } I_{ADJ1,2} \quad (4.1)$$

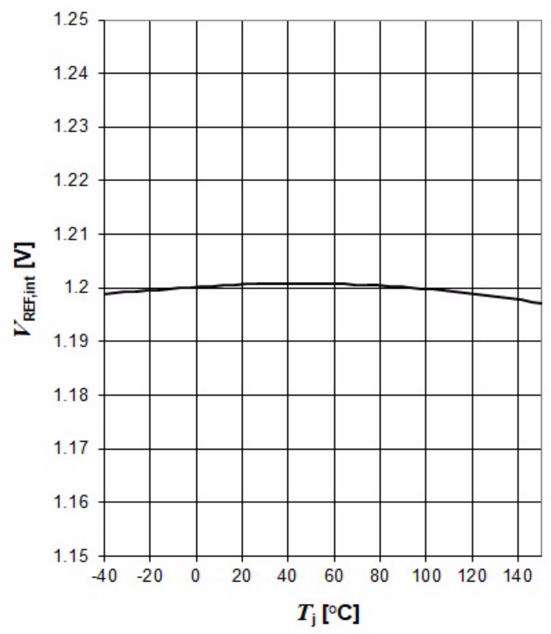
$V_{REF,int}$ is typically 1.2 V.

To avoid errors caused by the leakage current $I_{ADJ1,2}$, we recommend to choose the resistor value for $R_{2\,1,2} <$ 27 kΩ.

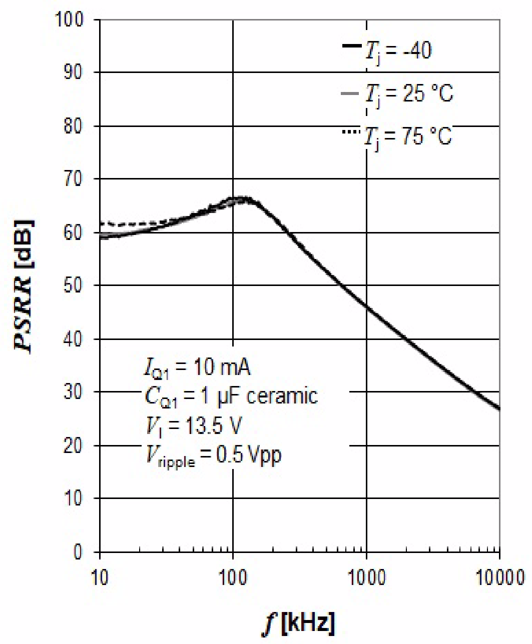
The accuracy of the resistors for the external voltage divider also influence the output voltage tolerance. To achieve a reasonable accuracy resistors with a tolerance of 1% or less are recommended for the feedback divider.

4.4 Typical performance characteristics voltage regulator

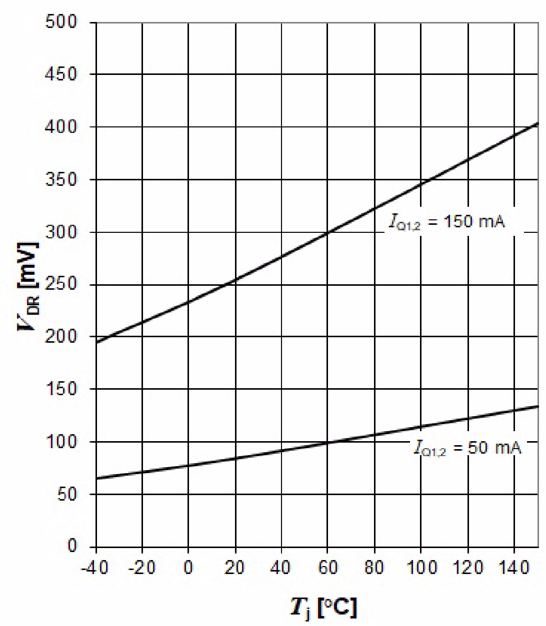
Reference voltage $V_{REF,int}$ versus junction temperature T_j



Power supply ripple rejection *PSRR*



Dropout voltage V_{dr} versus junction temperature T_j



5 Current consumption

5.1 Electrical characteristics current consumption

Table 5 Electrical characteristics: current consumption

V_I = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground; direction of currents as shown in **Figure 7 “Application diagram” on Page 27** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption	$I_{q1,on}$	–	–	815	µA	$I_{Q1} \leq 200$ µA; $T_j \leq 25$°C; $V_{EN1} = 5$ V; $V_{EN2} = 0$ V; $I_{q1} = I_I - I_{Q1} - I_{CSO1}$	P_6.1.1
Current consumption	$I_{q1,on}$	–	–	835	µA	$I_{Q1} \leq 200$ µA; $T_j \leq 85$°C; $V_{EN1} = 5$ V; $V_{EN2} = 0$ V; $I_{q1} = I_I - I_{Q1} - I_{CSO1}$	P_6.1.2
Current consumption	$I_{q1,on}$	–	–	1	mA	$I_{Q1} = 200$ mA; $V_{EN1} = 5$ V; $V_{EN2} = 0$ V; $I_{q1} = I_I - I_{Q1} - I_{CSO1}$	P_6.1.3
Current consumption	$I_{q2,on}$	–	–	815	µA	$I_{Q2} \leq 200$ µA; $T_j \leq 25$°C; $V_{EN2} = 5$ V; $V_{EN1} = 0$ V; $I_{q2} = I_I - I_{Q2} - I_{CSO2}$	P_6.1.6
Current consumption	$I_{q2,on}$	–	–	835	µA	$I_{Q2} \leq 200$ µA; $T_j \leq 85$°C; $V_{EN2} = 5$ V; $V_{EN1} = 0$V; $I_{q2} = I_I - I_{Q2} - I_{CSO2}$	P_6.1.7
Current consumption	$I_{q2,on}$	–	–	1	mA	$I_{Q2} = 200$ mA; $V_{EN2} = 5$ V; $V_{EN1} = 0$ V; $I_{q2} = I_I - I_{Q2} - I_{CSO1}$	P_6.1.8
Current consumption	$I_{q1,2,on}$	–	–	1.5	mA	$I_{Q1} = I_{Q2} = 50$ mA; $V_{EN1} = 5$ V; $V_{EN2} = 5$ V; $I_{q1,2on} = I_I - I_{Q2} - I_{Q1} - I_{CSO1} - I_{CSO2}$	P_6.1.9
Current consumption	$I_{q1,2,on}$	–	–	1.6	mA	$I_{Q1} = I_{Q2} = 200$ mA; $V_{EN1} = 5$ V; $V_{EN2} = 5$ V; $I_{q1,2on} = I_I - I_{Q2} - I_{Q1} - I_{CSO1} - I_{CSO2}$	P_6.1.10
Current consumption	$I_{q1,2,off}$	–	–	3	µA	$T_j \leq 25$°C; $V_{EN1} = 0$ V; $V_{EN2} = 0$ V	P_6.1.11
Current consumption	$I_{q1,2,off}$	–	–	5	µA	$T_j \leq 85$°C $V_{EN1} = 0$ V; $V_{EN2} = 0$ V	P_6.1.12

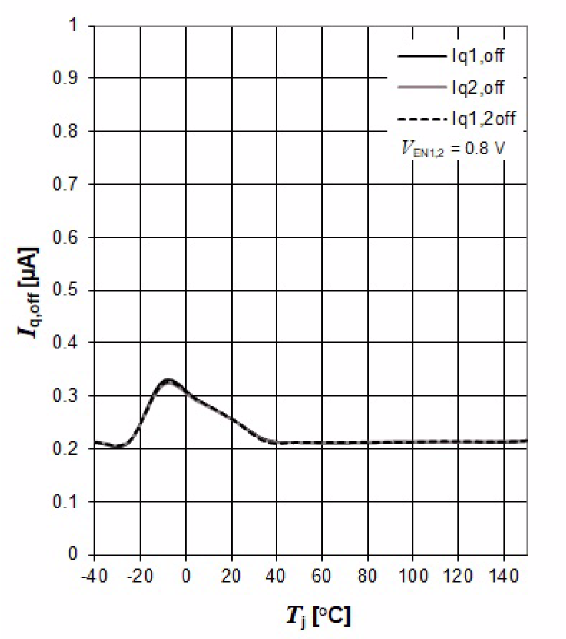
Table 5 Electrical characteristics: current consumption (cont'd)

V_I = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground; direction of currents as shown in **Figure 7 "Application diagram" on Page 27** (unless otherwise specified)

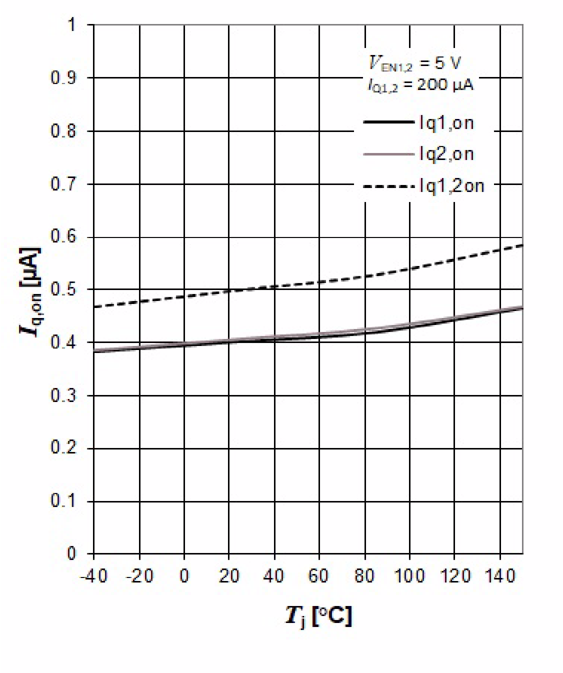
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption	$I_{q1,2,off}$	–	–	15	µA	$T_j \leq 85°C$; V_{EN1} = 0.8 V; V_{EN2} = 0.8 V	P_6.1.13
Current consumption	$I_{q1,2,off}$	–	–	15	µA	$T_j \leq 85°C$; V_{EN1} = 0.8 V; V_{EN2} = 0 V	P_6.1.14
Current consumption	$I_{q1,2,off}$	–	–	15	µA	V_{EN1} = 0 V; V_{EN2} = 0 V	P_6.1.15

5.2 Typical performance graphs current consumption

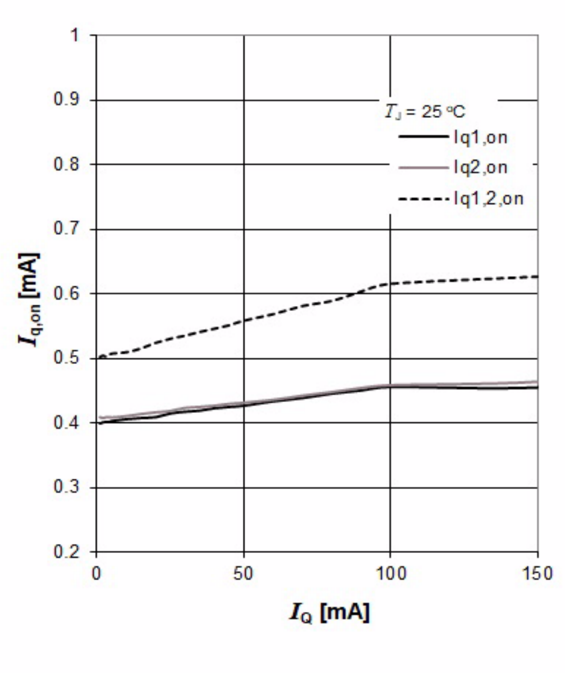
Current consumption $I_{q1,off}$, $I_{q2,off}$, $I_{q1,2,off}$ versus junction temperature T_j



Current consumption $I_{q1,on}$, $I_{q2,on}$, $I_{q1,2,on}$ versus junction temperature T_j



Current consumption $I_{q1,on}$, $I_{q2,on}$, $I_{q1,2,on}$ versus output current $I_{Q1,2}$



6 Current and protection monitor functions

The device provides a set of advanced monitoring functions to support system analysis and failure identification.

Current and failure monitor

The output currents of the power stages (I_{Q1}, I_{Q2}) are scaled down by the current monitor factor $F_{IQ/ICSO1,2,x}$ and flow out of the respective pins CSO1 and CSO2, causing a voltage drop at the external resistors R_{CSO1}, R_{CSO2}. By choosing the size of (R_{CSO1}, R_{CSO2}) the current limit can be programmed, see **Adjustable output current limitation**. The voltage on the CSO1 and CSO2 pin can be sampled by an ADC to measure the respective power stage currents I_{Q1}, I_{Q2}. Hereby the ratios between R_{CSO1}, R_{CSO2} and $F_{IQ/ICSO1,2,x}$ must be taken into account accordingly. The capacitors C_{CSO1}, C_{CSO2} are required for loop stability and must be sized as given in **Functional range**.

Voltage levels on the CSO1 and CSO2 pin above the linear current sensing range indicate fault conditions, see **Figure 6**. This includes an active current limit, overtemperature and overvoltage.

In addition the presence of either of the three fault conditions can also be detected on the channel specific digital pins ST1 and ST2, see **Status output signal**.

By applying $V_{CSOxSel,L}$ from **Electrical characteristics: current monitor** to the CSOxSel pin, CSOx can be internally connected to CSO1. When applying $V_{CSOxSel,H}$ to CSOxSel it is internally connected to CSO2. The voltage $V_{CSOxSel,T}$ on CSOxSel puts CSOx into a high impedance state. This feature allows the CSOx signal to be shared between multiple channels and devices that are connected to a single ADC for monitoring, see **Application information**. Any additional current drawn from CSOx influences the voltage levels on the CSO1 and CSO2 pins due to the internal current sources driving I_{CSO1} and I_{CSO2} respectively.

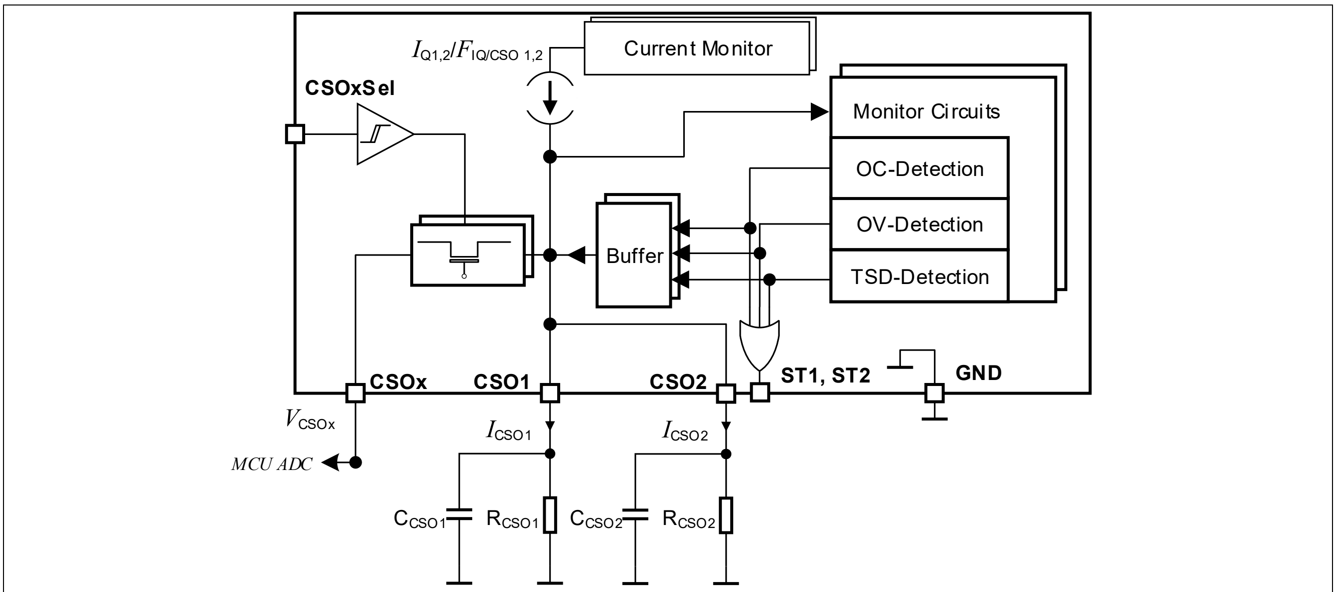


Figure 5 Functional block diagram current and protection monitor

To reduce possible effects from the supply voltage V_I additional filtering of the supply voltage is recommended. Place a 100 nF capacitor as close a possible to the IC terminal, which is connected to V_I.

Figure 6 shows the output voltage level at the CSO output (CSO1, CSO2, CSOx pin) versus the operation or fault condition. The graph is valid for the following set up of external components:

$C_{CSO1,2}$ = 2.2 µF

$R_{CSO1,2}$ = 3 kΩ

Note: In case of high junction temperature (T_j > 151°C) and with any of the CSO pins (CSO1, CSO2) directly connected to GND, the return to normal operation from the thermal shutdown mode cannot be ensured.

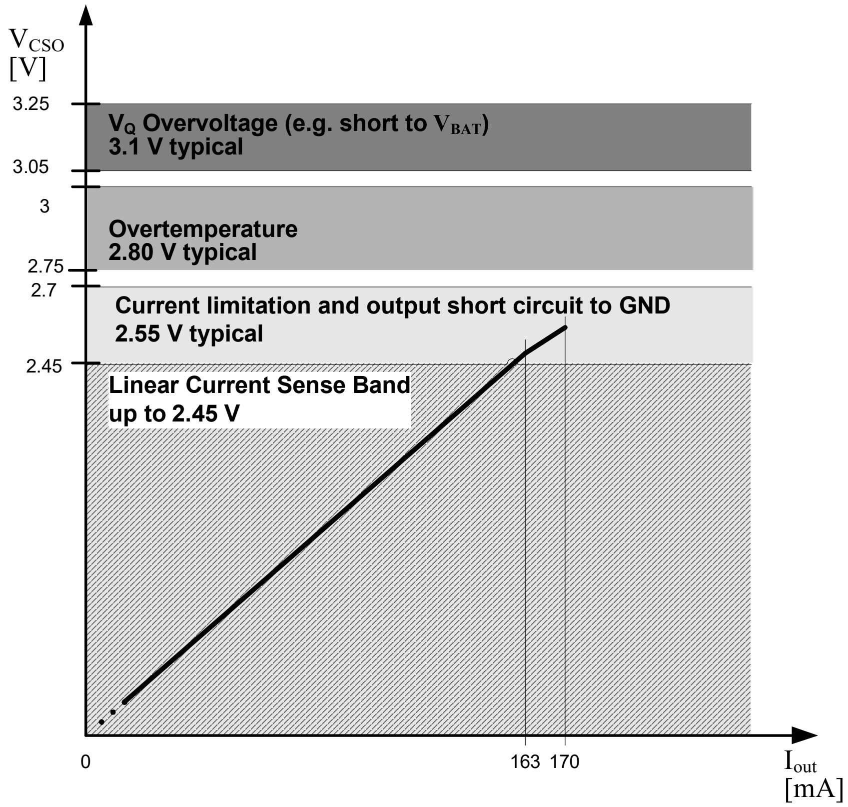


Figure 6 Output levels and functionality of the CSO output

Note: The graph is just an example and only valid for a certain configuration of the external components.

6.1 Linear current monitor

Inside the linear current monitor area of **Figure 6** the current driven out of the CSO1 or CSO2 pin is directly proportional to the corresponding output load I_{Q1}, I_{Q2}.

The level of the current $I_{CSO\,1,2}$ can be calculated according to **Equation (6.1)**:

(6.1)

$$I_{\mathrm{CSO\,1,2}} = \frac{I_{\mathrm{Q1,2}}}{F_{\mathrm{IQ/ICSO\,1,2}}}$$

6.2 Adjustable output current limitation

The device has a channel specific and adjustable current limitation for the current flowing out of the respective power stage. If the level of the output current exceeds its defined current limit threshold $I_{Q,lim}$, then the device limits the output current.

Setting the adjustable current limitation: (6.2)

$$I_{Q\ 1,2,\mathrm{lim}} = \frac{2.55\mathrm{V} \cdot F_{\mathrm{IQ/ICSO}\ 1,2}}{R_{\mathrm{CSO}\ 1,2}}$$

A voltage level as defined in **CSO voltage level Overvoltage detected** is applied at the CSO output pins. In addition the ST1, ST2 pins are set to ”low.”

*Note: During power up of the device, the regulator current limit is according to **CSO current at no load condition**. If an adjustable current limit is set, the status output pin ST is set to "low" as long as the adjustable current limitation is active during the power up sequence.*

For example, use the following configuration to set the current limitation at 170 mA:

$$I_{Q\ 1,2,\mathrm{lim}} = \frac{2.55\mathrm{V} \cdot 200}{3\mathrm{k}\Omega}$$

FIQ/ICSO = 200

R_{CSO} = 3 kΩ

6.3 Overvoltage detection

To detect a possible short circuit of the output to a higher supply rail the device has an overvoltage detection. If the voltage level at the ADJ1 pin is 20% higher than the internal reference voltage $V_{REF,int}$ defined in **Reference voltage**, then the device detects overvoltage.

If the device detects an overvoltage event at one of the outputs Q1, Q2, then it sets the respective CSO output CSO1, CSO2 to a voltage level defined in **CSO voltage level Overvoltage detected**. In addition, the device sets the corresponding digital status output ST1, ST2 to "low".

6.4 Thermal shutdown detection

If the junction temperature exceeds the limits defined in the **Overtemperature shutdown threshold**, then the device disables the output. In this case the device applies a voltage level defined in **CSO voltage level Current limitation** at the respective pins CSO1 and CSO2. In addition, the device sets the corresponding pins ST1 and ST2 to "low".

6.5 Status output signal

The status condition pins ST1, ST2 are open drain outputs. An external pull-up resistor must be applied for functionality. The current into the pin must be limited by sizing the resistor according to **Status output digital signal sink current**. Do not connect the ST1 pin nor the ST2 pin directly to a supply voltage, as this can damage the device.

If one or more of the monitored protection functions (overcurrent, overvoltage and temperature shutdown) are active for Q1, then the device sets the digital status output pin ST1 to “low”.

If one or more of the monitored protection functions (overcurrent, overvoltage and temperature shutdown) are active for Q2, then the device sets the digital status output pin ST2 to “low”.

6.6 Electrical characteristics current monitor

Table 6 Electrical characteristics: current monitor

V_I = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7 “Application diagram” on Page 27** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Linear current monitor CSO1, CSO2							
Current monitor factor I_Q / I_{CSO}	$F_{IQ/ICSO\ 1,2}$	194	200	206	–	[1] T_j = -40°C to 125°C; 5.5 V ≤ V_I ≤ 16 V; 3 V ≤ $V_{Q1,2}$ ≤ 15 V; V_I > $V_{Q1,2}$ + 0.5 V; 100 mA ≤ $I_{Q1,2}$ ≤ 300 mA	P_7.1.1
Current monitor factor I_Q / I_{CSO}	$F_{IQ/ICSO\ 1,2}$	190	200	210	–	T_j = -40°C to 125°C; 5.5 V ≤ V_I ≤ 16 V; 3 V ≤ $V_{Q1,2}$ ≤ 15 V; V_I > $V_{Q1,2}$ + 0.5 V; 40 mA ≤ $I_{Q1,2}$ ≤ 100 mA	P_7.1.2
Current monitor factor I_Q / I_{CSO}	$F_{IQ/ICSO\ 1,2}$	190	200	210	–	T_j = -40°C to 125°C; 5.5 V ≤ V_I ≤ 16 V; 3 V ≤ $V_{Q1,2}$ ≤ 15 V; V_I > $V_{Q1,2}$ + 0.5 V; 5 mA ≤ $I_{Q1,2}$ ≤ 40 mA	P_7.1.3
Current monitor factor I_Q / I_{CSO}	$F_{IQ/ICSO\ 1,2}$	176	200	224	–	T_j = -40°C to 125°C; 5.5 V ≤ V_I ≤ 16 V; 3 V ≤ $V_{Q1,2}$ ≤ 15 V; V_I > $V_{Q1,2}$ + 0.5 V; 2 mA ≤ $I_{Q1,2}$ ≤ 5 mA	P_7.1.4
Current monitor factor I_Q / I_{CSO}	$F_{IQ/ICSO\ 1,2}$	160	200	240	–	T_j = -40°C to 125°C; 5.5 V ≤ V_I ≤ 16 V; 3 V ≤ $V_{Q1,2}$ ≤ 15 V; V_I < $V_{Q1,2}$ + 0.5 V; 1 mA ≤ $I_{Q1,2}$ ≤ 300 mA	P_7.1.6
CSO current at no load condition	$I_{CSO1,2,off}$	–	–	550	nA	No load connected at Q1, Q2; R_{21} = 27 kΩ, R_{22} = 27 kΩ; $V_{Q1,2}$ = 5 V	P_7.1.7

Table 6 Electrical characteristics: current monitor (cont'd)

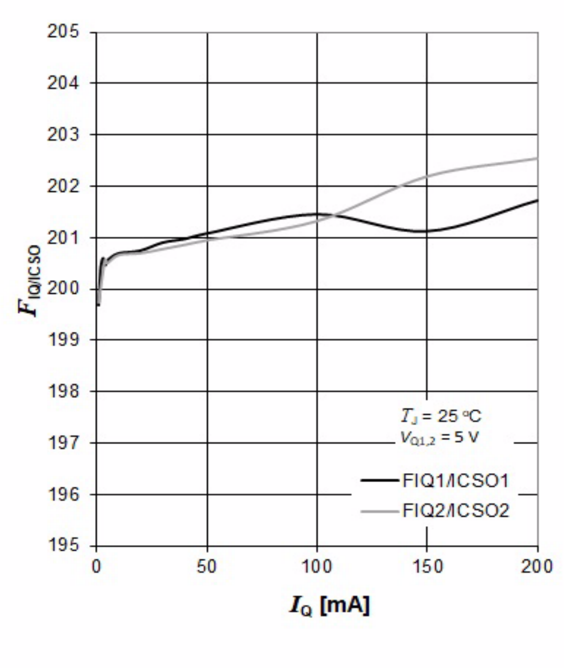
V_I = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7 "Application diagram" on Page 27** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Linear current monitor CSOx							
CSOx current	$I_{CSOx,off}$	–50	–	50	nA	CSOx set to high impedance	P_7.1.8
Adjustable current limitation							
Adjustable current limit	$I_{Qlim1,2}$	50	–	300	mA	1) 1.7 kΩ < $R_{CSO1,2}$ < 10.2 kΩ; $V_{Q1,2} < 0.95 \times V_{Q,nom}$	P_7.1.9
Adjustable current limit Tolerance	$I_{QlimTOL1,2}$	-10	–	10	%	50 mA ≤ $I_{Qlim1,2}$ ≤ 300 mA T_j = -40°C to 125°C; $0.95 \times V_{Q,nom} > V_{Q1,2} >$ 3.0 V	P_7.1.10
Adjustable current limit Tolerance	$I_{QlimTOL1,2}$	-10	–	25	%	50 mA ≤ $I_{Qlim1,2}$ ≤ 300 mA T_j = -40°C to 125°C; $0.95 \times V_{Q,nom} > V_{Q1,2} >$ 0 V	P_7.1.11
CSO voltage level Current limitation	$V_{CSOlim1,2}$	2.45	2.55	2.7	V	1) $V_{Q1,2} \leq 0.95 \times V_{Q,nom}$	P_7.1.12
Output level overvoltage detected CSO1, CSO2, CSOx							
CSO voltage level Overvoltage detected	$V_{CSO,OV1,2}$	3.05	3.1	3.25	V	1) $V_{ADJ} > 1.2 \times V_{REF,nom}$	P_7.1.13
Over voltage threshold level	$V_{ADJ,OV1,2}$	1.44 - 0.04 $V_{Q1,2,nom}$	1.44	1.44 + 0.04 $V_{Q1,2,nom}$	V	1)	P_7.1.14
Output level overtemperature detected CSO1, CSO2, CSOx							
CSO voltage level overtemperature detected	$V_{CSO,TSD}$	2.75	2.8	3	V	2) 151°C < T_j < 180°C	P_7.1.15
Status output signal ST1, ST2							
Status output digital signal "low" voltage	$V_{ST1,2,low}$	–	0.2	0.4	V	$I_{ST1,2}$ ≤ 1.8 mA	P_7.1.16
Status output digital signal sink current	$I_{ST1,2}$	–	–	1.8	mA	–	P_7.1.17
CSOxSel							
CSOxSel digital signal "low" voltage	$V_{CSOxSel,L}$	–	–	0.8	V	Sets CSOx to CSO1	P_7.1.18
CSOxSel digital signal third state	$V_{CSOxSel,T}$	1.1	–	1.7	V	Sets CSOx to high impedance	P_7.1.19
CSOxSel digital signal "high" voltage	$V_{CSOxSel,H}$	2	–	–	V	Sets CSOx to CSO2	P_7.1.20

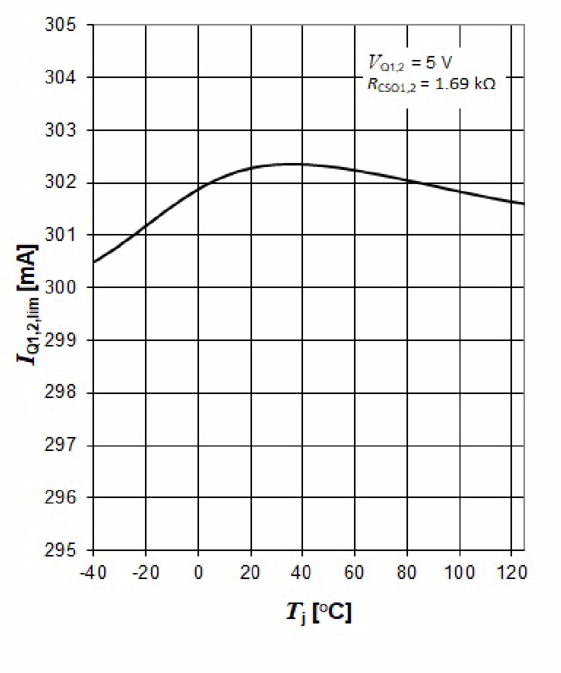
1) Referring to the device tolerance only, the tolerance of the external components can cause additional deviation.
2) Not subject to production test, specified by design.

6.7 Typical performance characteristics current monitor

Current monitor factor $F_{IQ/ICSO\ 1,2,x}$ versus output current $I_{Q1,2}$



External current limitation $I_{Q,lim1,2}$ versus junction temperature T_j



7 Enable

7.1 Functional description enable

Each outputs of the device Q1, Q2 can be switched on or switched off individually via EN1, EN2 input respectively. By applying voltage levels within $V_{EN1,2,high}$ applied to the EN1 and EN2 inputs the device switches on completely. A voltage level of $V_{EN1,2,low}$ applied to the EN1 and EN2 inputs sets the device to low quiescent current mode. In this state the device is switched off and is not functional. The enable input has a hysteresis to avoid toggling between on-state and off-state due to signals with slow slope at the input. The enable input pins EN1 and EN2 provide separate internal pull-down resistors.

7.2 Electrical characteristics enable

Table 7 Electrical characteristics: enable

V_I = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7 "Application diagram" on Page 27** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable "low" signal valid	$V_{EN1,2,low}$	–	–	0.8	V	–	P_8.2.1
Enable "high" signal valid	$V_{EN1,2,high}$	2	–	–	V	See also startup time P_8.2.7	P_8.2.2
Enable threshold hysteresis	$V_{EN1,2,hyst}$	50	–	–	mV	–	P_8.2.3
Enable input current	$I_{EN1,2,high}$	–	–	5.3	µA	$V_{EN1,2}$ = 5 V	P_8.2.4
Enable input current	$I_{EN1,2,high}$	–	–	20	µA	$V_{EN1,2}$ < 18 V	P_8.2.5
Enable internal pull-down resistor	$R_{EN1,2}$	0.94	1.5	9	MΩ	$V_{EN1,2}$ < 5 V	P_8.2.6
Startup time	$t_{EN1,2}$	–	1	–	ms	$C_{Q1,2}$ = 1 µF; $V_{Q1,2,nom}$ = 5 V; $I_{Q1,2,load}$ = 150 mA; $R_{CSO1,2}$ = 2.83 kΩ; time from V_{EN} > 2 V; (0 V to 5 V transition) until V_Q = 90% of $V_{Q,nom}$	P_8.2.7

8 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

8.1 Application diagram

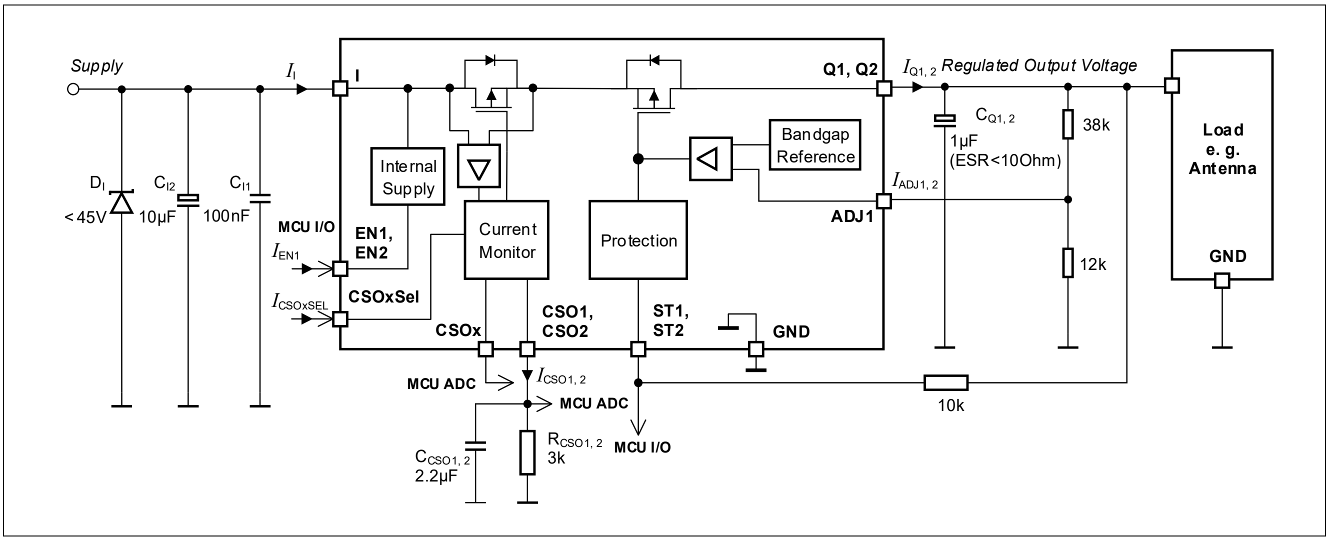


Figure 7 Application diagram

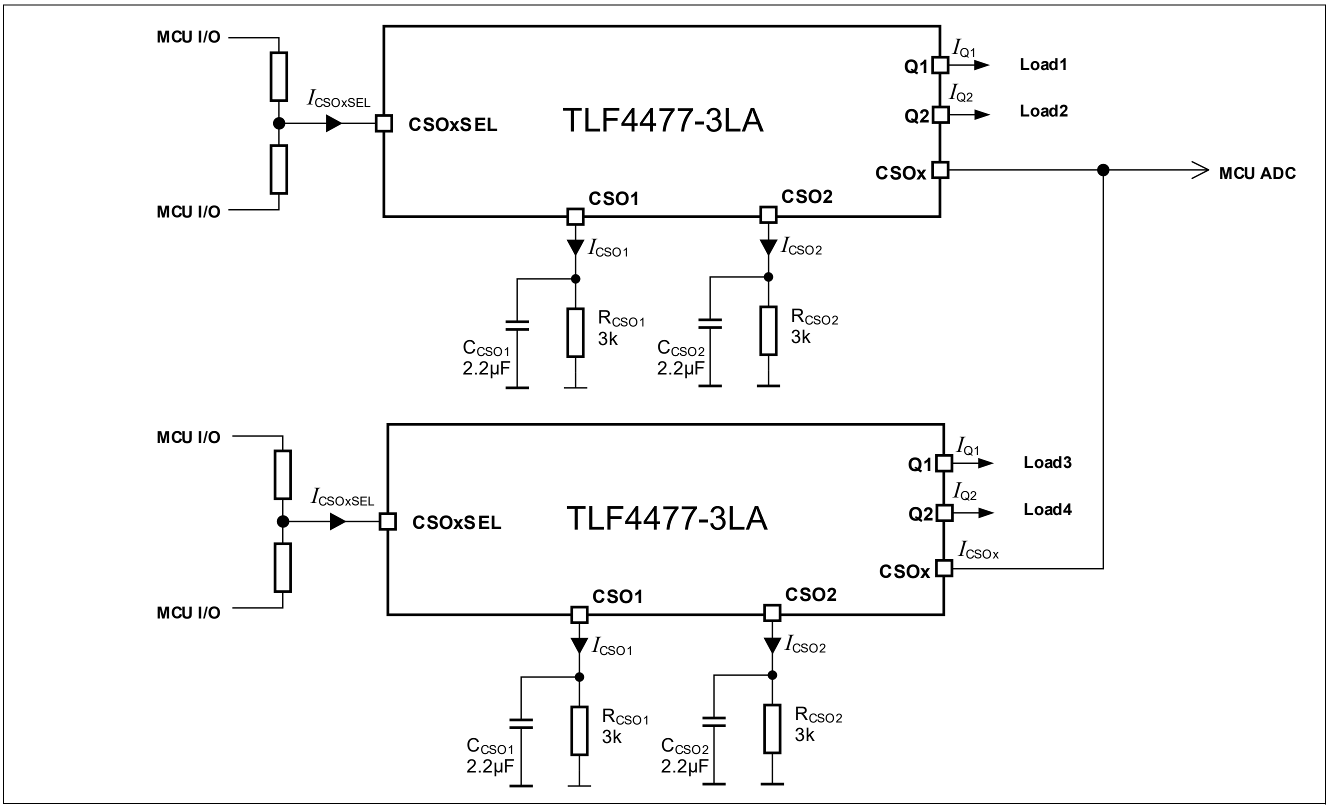


Figure 8 Application diagram

8.2 Selection of external components

8.2.1 Input pin

Figure 7 shows the typical input circuitry for a linear voltage regulator.

A ceramic capacitor at the input, in the range of 100 nF to 470 nF, is recommended to filter out the high frequency disturbances imposed by the line for example ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against damage due to overvoltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

8.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

For the requirements for the output capacitor see **Functional range**.

The device is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator output and GND pins and on the same side of the PCB as the regulator.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application in order to fulfill the output stability requirements.

8.3 Thermal considerations

From the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_{Q1}) \times I_{Q1} + (V_I - V_{Q2}) \times I_{Q2} + V_I \times (I_{q1}+I_{q2}) \quad (8.1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_{Q1}, V_{Q2}: output voltage
- I_{Q1}, I_{Q2}:output current
- I_{q1}, I_{q2}: quiescent current

The maximum acceptable thermal resistance R_{thJA} can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \tag{8.2}$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **Thermal resistance**.

Example

Application conditions:

$V_I = 13.5$ V

$V_{Q1} = 5$ V

$I_{Q1} = 50$ mA

$V_{Q2} = 5$ V

$I_{Q2} = 50$ mA

$T_a = 85°C$

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_{Q1}) \times I_{Q1} + (V_I - V_{Q2}) \times I_{Q2} + V_I \times (I_{q1}+I_{q2})$

$= (13.5\ V - 5\ V) \times 50\ mA + (13.5\ V - 5\ V) \times 50\ mA + 13.5\ V \times (1.5\ mA)$

$= 0.850\ W + 0.021\ W$

$= 0.871\ W$

$R_{thJA,max} = (T_{j,max} - T_a) / P_D$

$= (150°C - 85°C) / 0.871\ W = 74.62\ K/W$

As a result, the PCB design must ensure a thermal resistance R_{thJA} lower than 74.62 K/W. According to **Thermal resistance**, at least 300 mm^2 heatsink area is necessary on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

8.4 Reverse polarity protection

The device is self protected against reverse polarity faults and allows negative supply voltage. An external reverse polarity diode is not needed. However, the **Absolute maximum ratings** of the device must be maintained.

Reverse voltage causes several small currents to flow into the IC the increase its junction temperature.

Application design must consider that the thermal shut down circuitry does not work in reverse polarity condition.

8.5 Further application information

- For further information you may contact **http://www.infineon.com/**

9 Package information

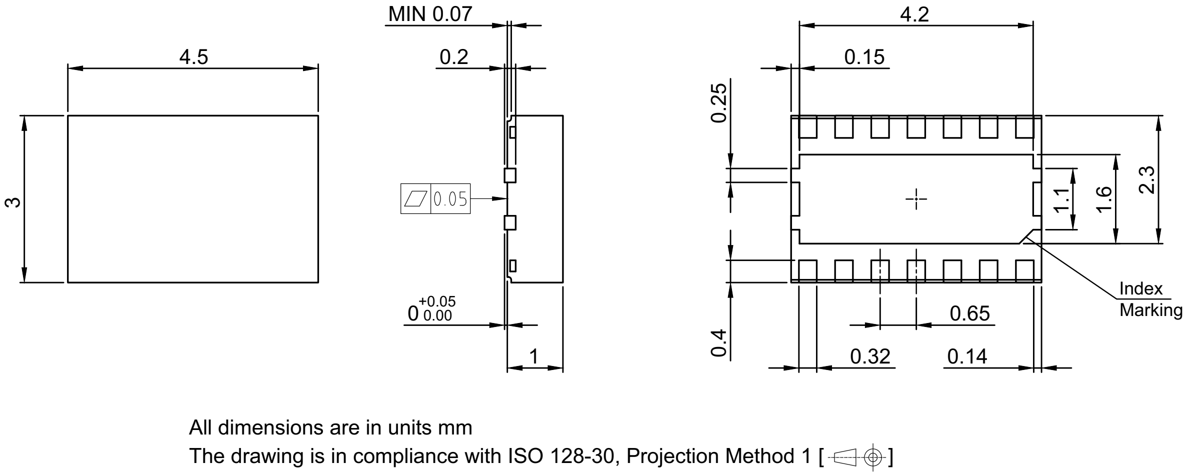


Figure 9 PG-TSON-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

10 Revision history

Revision	Date	Changes
1.0	2020-11-11	Datasheet created

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Edition 2020-11-11

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference
Z8F66321558