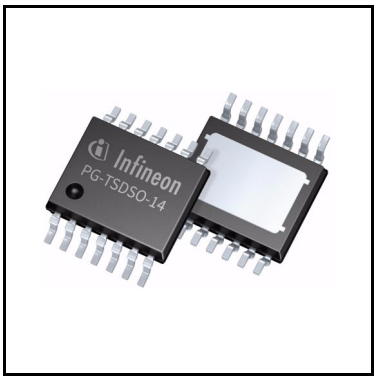
OPTIREG™ linear voltage regulator TLF4277-2EP

Low dropout linear voltage regulator with integrated current monitor



Features

- Integrated current monitor
- Overvoltage, overtemperature, and overcurrent detection
- Adjustable output voltage
- Output current up to 400 mA
- Adjustable output current limitation
- Very low current consumption
- Very low dropout voltage
- Stable with ceramic output capacitor of 1 µF
- Wide input voltage range up to 40 V
- Reverse-polarity protection
- Short-circuit protection
- Overtemperature shutdown
- Automotive temperature range -40°C ≤ T_j ≤ 150°C
- Green Product (RoHS-compliant)

Potential applications

- Automotive sensor supply
- Automotive telematics systems
- Camera and radar supply

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The OPTIREG™ linear voltage regulator TLF4277-2EP is the ideal companion IC to supply critical applications requiring tight current limitation and diagnostics. It provides monitoring and protection features as well as a high-side power switch.

The TLF4277-2EP is a monolithic integrated low dropout voltage regulator that can supply loads up to 400 mA. For an input voltage up to 40 V, the TLF4277-2EP provides an adjustable output voltage from 3 V to 16 V. The

integrated current monitor is a unique feature that provides diagnosis and system protection functionality. The TLF4277-2EP monitors fault conditions such as overtemperature and output overvoltage and indicates that at the current-sense output. The maximum output current limit of the TLF4277-2EP is adjustable to provide additional protection to the connected load.

Via the enable function, the TLF4277-2EP can be disabled to reduce power consumption. The PG-TSDSO-14 package provides enhanced thermal performance within an SO8 body size.

Type	Package	Marking
TLF4277-2EP	PG-TSDSO-14	TLF42772

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1 Block diagram

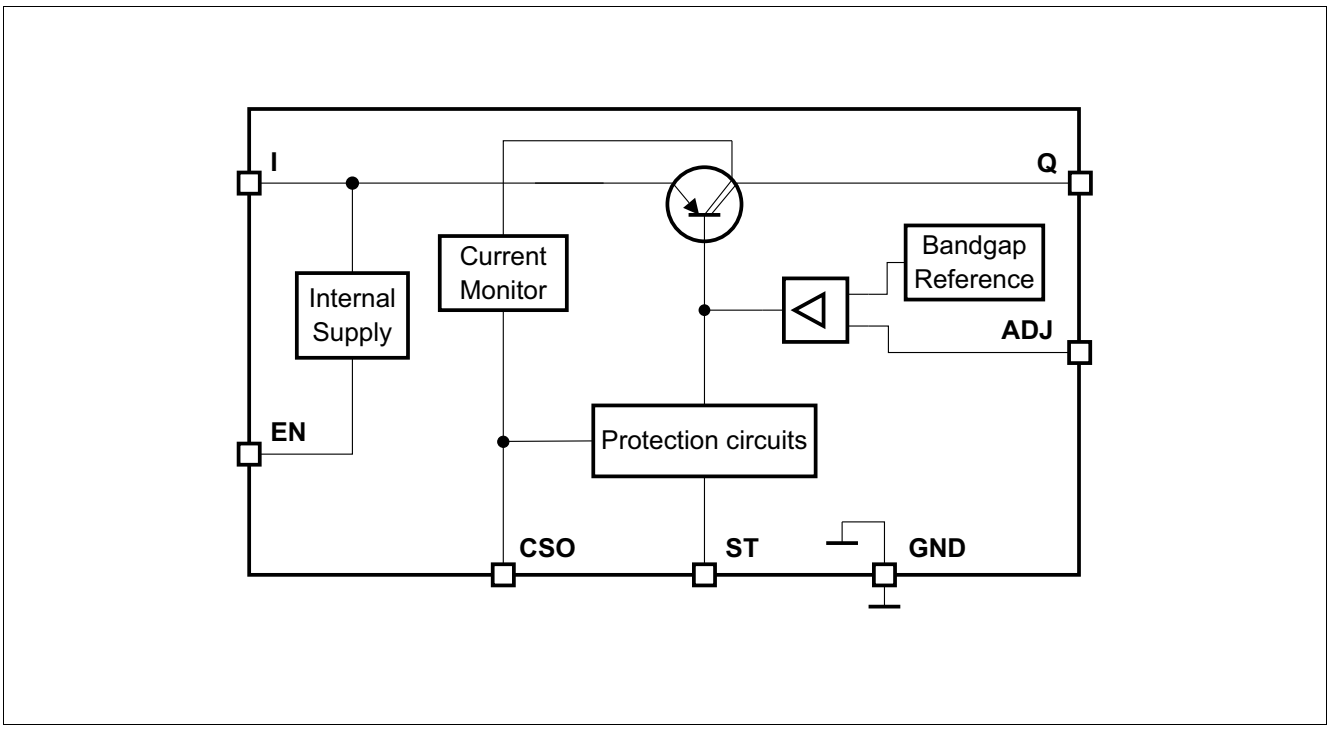


Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

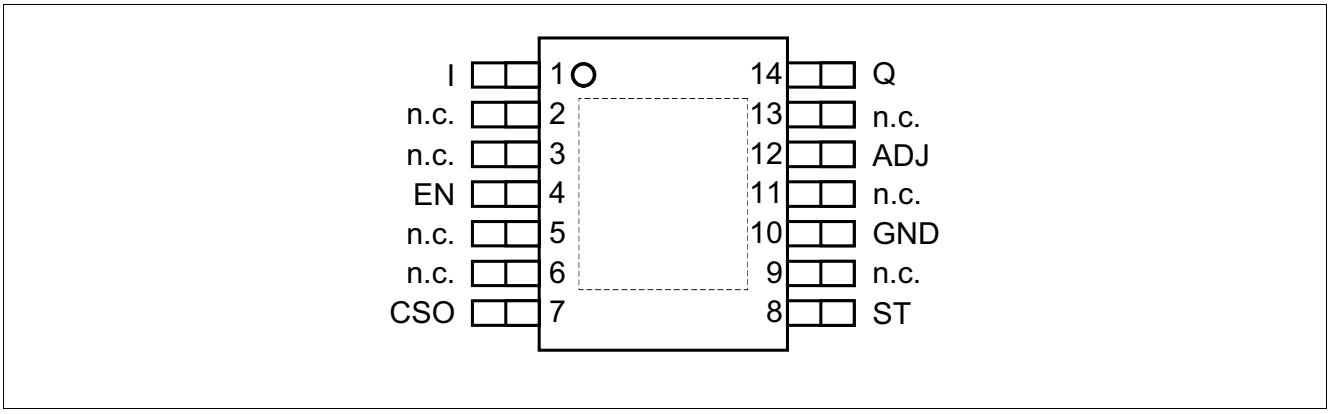


Figure 2 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin	Symbol	Function
1	I	**IC supply** Place a capacitor from I to GND close to the IC pins to compensate line influences
4	EN	**Enable** High signal enables the regulator Low signal disables the regulator If the enable function is not needed, then connect EN to I
7	CSO	**Current-sense out** Current monitor and status output
8	ST	**Status output** Digital output signal with open-collector output A low signal indicates fault conditions at the regulator's output
10	GND	**Ground**
12	ADJ	**Voltage adjust** Connect an external voltage divider to adjust the output voltage
14	Q	**Regulator output** Connect a capacitor between Q and GND close to the IC pins, respecting the values given for its capacitance C_Q and $ESR(C_Q)$, see **Table 3**
–	Exposed pad	**Heat sink** Connect the exposed pad to GND. It is recommended to connect the exposed pad to a heat sink

Pin configuration

Table 1 Pin definitions and functions (cont'd)

Pin	Symbol	Function
2, 3, 5, 6	n.c.	**Not connected** Not connected internally Connect to PCB GND
9, 11, 13	n.c.	**Not connected** Not connected internally Connect to PCB GND

3 General product characteristics

3.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltage ratings							
IC supply I	V_I	-16	–	45	V	–	P_4.1.1
Enable input EN	V_{EN}	-16	–	45	V	–	P_4.1.2
Voltage adjust input ADJ	V_{ADJ}	-0.3	–	16	V	–	P_4.1.3
Regulator output Q	V_Q	-0.3	–	45	V	$V_Q < V_I + 5$ V	P_4.1.4
Current monitor out CSO	V_{CSO}	-0.3	–	5	V	–	P_4.1.5
Status output	V_{ST}	-0.3	–	45	V	[2)] See also **Status output signal**	P_4.1.6
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_4.1.7
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.8
ESD susceptibility							
ESD susceptibility to GND	V_{ESD}	-2	–	2	kV	[3)] Human body model (HBM)	P_4.1.9
ESD susceptibility to GND	V_{ESD}	-500	–	500	V	[4)] Charge device model (CDM)	P_4.1.10
ESD susceptibility to GND, pin 1, 7, 8, 14 (corner pins)	$V_{ESD1,7,8,14}$	-750	–	750	V	[4)] Charge device model (CDM)	P_4.1.11

1) Not subject to production test, specified by design.
2) In order to prevent uncontrolled current from flowing into the ST pin, use a resistor to connect to higher voltage level. Check proper soldering of the ST pin, for example, by optical inspection.
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
4) ESD susceptibility, charged device model (CDM) according to JEDEC JESD22-C101.

Notes

1. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*
2. *Stresses above the ones listed her may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

3.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	V_I	$V_Q + V_{dr}$	–	40	V	–	P_4.2.1
Output voltage	V_Q	3	–	16	V	–	P_4.2.2
Current sense output resistor	R_{CSO}	637	–	25.5	kΩ	–	P_4.2.3
Current sense output capacitor	C_{CSO}	1	–	4.7	µF	1)	P_4.2.4
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.5
Output capacitor capacitance	C_Q	1	–	–	µF	1)2)	P_4.2.6
Output capacitor equivalent series resistance	$ESR(C_Q)$	–	–	10	Ω	1)3)	P_4.2.7

1) Not subject to production test, specified by design.
2) The minimum output capacitance requirement is applicable for a worst-case capacitance tolerance of 30%.
3) Relevant *ESR* value at f = 10 kHz.

Note: Within the functional range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

3.3 Thermal resistance

Table 4 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	10	–	K/W	Measured to the exposed pad	P_4.3.1
Junction to ambient	R_{thJA}	–	142	–	K/W	2) Footprint only	P_4.3.2
Junction to ambient	R_{thJA}	–	62	–	K/W	2) 300 mm² PCB heat sink area	P_4.3.3
Junction to ambient	R_{thJA}	–	52	–	K/W	2) 600 mm² PCB heat sink area	P_4.3.4
Junction to ambient	R_{thJA}	–	41	–	K/W	3) 2s2p PCB	P_4.3.5

1) Not subject to production test, specified by design.
2) The specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on an FR4 1s0p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with one copper layer (1 × 70 µm Cu).
3) The specified R_{thJA} value is according to JEDEC JESD51-2,-5,-7 at natural convection on an FR4 2s2p board. The product (chip and package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable, a thermal via array under the exposed pad contacted the first inner copper layer.

4 Voltage regulator

4.1 Description of the voltage regulator

The TLF4277-2EP controls the output voltage V_Q by comparing the feedback voltage V_{ADJ} to an internal reference voltage and driving a PNP pass transistor accordingly.

The control loop stability depends on the following factors:

- Output capacitor C_Q
- Output capacitor *ESR*
- Load current
- Chip temperature

To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the **Table 3** must be maintained. For stability details. please refer to the typical performance graph **Output capacitor ESR(C_Q) versus output current I_Q**. In addition, the output capacitor may need to be sized larger to buffer load transients.

An input capacitor C_I is not needed for the control loop stability, but recommended to buffer line influences. Connect the capacitors close to the IC terminals. In general, a buffered supply voltage is recommended for the device, see **Chapter 8.1**.

Protection circuitry prevents the IC as well as the application from destruction in case of catastrophic events with the integrated safeguards:

- Output current limitation
- Reverse polarity protection
- Thermal shutdown

Output current limitation

In order to avoid excessive power dissipation by the pass element and the package, an integrated safe operation monitor reduces the maximum output current for input voltages above V_{BAT} = 22 V.

Reverse polarity protection

The TLF4277-2EP allows a negative supply voltage. However, several small currents flowing into the IC increase its junction temperature. This reverse current must be considered in thermal design, respecting that the thermal protection circuit is not operational in reverse polarity condition.

Thermal shutdown

The thermal shutdown circuit prevents the IC from immediate destruction in fault condition (for example permanent short circuit at the output) by switching off the power stage. After the chip cools down, the regulator restarts. This leads to oscillations of the output voltage until the fault is removed. However, a junction temperature above 150°C is outside the maximum ratings and therefore significantly reduces the IC lifetime.

Voltage regulator

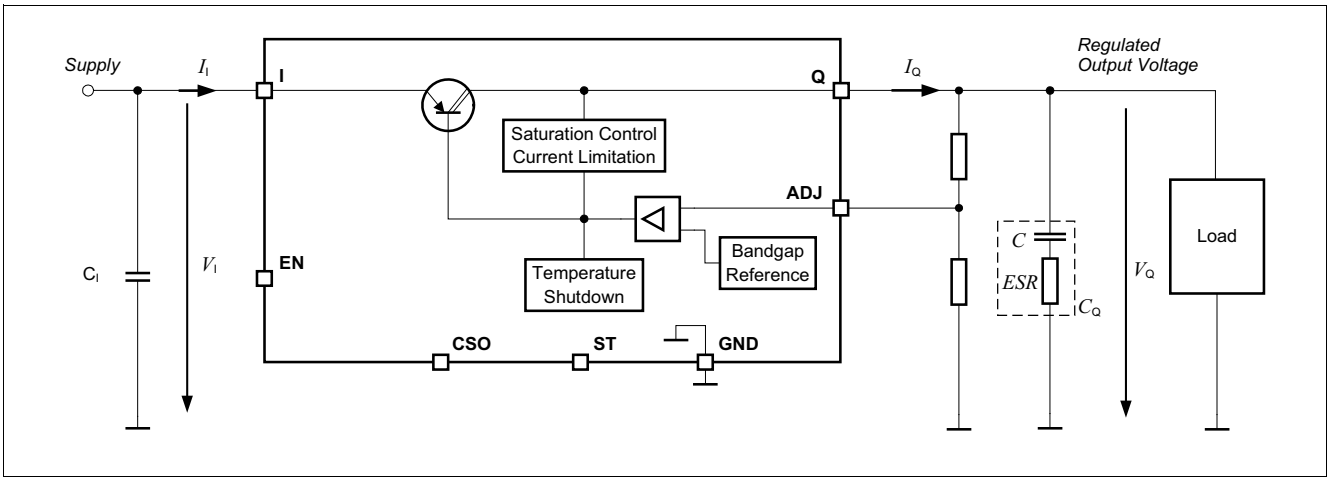


Figure 3 Functional block diagram voltage regulator circuit

4.2 Electrical characteristics of the voltage regulator

Table 5 Electrical characteristics of the voltage regulator

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reference voltage	$V_{REF,int}$	–	1.19	–	V	1)	P_5.2.1
Output voltage tolerance	V_Q	-2	–	2	%	2) 1 mA ≤ I_Q ≤ 300 mA; 9 V ≤ V_{BAT} ≤ 16 V; 3 V ≤ V_Q ≤ 14 V with V_{BAT} > V_Q + 2 V	P_5.2.2
Output voltage tolerance	V_Q	-2	–	2	%	1 mA ≤ I_Q ≤ 150 mA; 6 V ≤ V_{BAT} ≤ 16 V; 5 V ≤ V_Q ≤ 15 V with V_{BAT} > V_Q + 1 V	P_5.2.3
Output voltage tolerance	V_Q	-2	–	2	%	3) 1 mA ≤ I_Q ≤ 100 mA; 16 V ≤ V_{BAT} ≤ 32 V; 3 V ≤ V_Q ≤ 15 V with V_{BAT} > V_Q + 1 V	P_5.2.4
Output voltage tolerance	V_Q	-2	–	2	%	3) 1 mA ≤ I_Q ≤ 10 mA; 32 V ≤ V_{BAT} ≤ 40 V; 3 V ≤ V_Q ≤ 16 V	P_5.2.5
Output voltage tolerance	V_Q	-2	–	2	%	3) 1 mA ≤ I_Q ≤ 100 mA; 5.5 V ≤ V_{BAT} ≤ 16 V; 3 V ≤ V_Q ≤ 14 V with V_{BAT} > V_Q + 2 V	P_5.2.6
Output voltage tolerance	V_Q	-2	–	2	%	3) 300 mA ≤ I_Q ≤ 400 mA; 9 V ≤ V_{BAT} ≤ 16 V; 5 V ≤ V_Q ≤ 13.5 V with V_{BAT} > V_Q + 2.5 V	P_5.2.12
Load regulation steady-state	$dV_{Q,load}$	-30	-5	–	mV	I_Q = 1 mA to 250 mA; V_{BAT} = 6 V; V_Q = 5 V	P_5.2.7
Load regulation steady-state	$dV_{Q,load}$	-30	-5	–	mV	I_Q = 1 mA to 100 mA; V_{BAT} = 5.5 V; V_Q = 3 V	P_5.2.18
Line regulation steady-state	$dV_{Q,line}$	–	5	20	mV	V_{BAT} = 6 V to 32 V; I_Q = 5 mA; V_Q = 3 V	P_5.2.8
Line regulation steady-state	$dV_{Q,line}$	–	5	20	mV	V_{BAT} = 5.5 V to 32 V; I_Q = 5 mA; V_Q = 3 V	P_5.2.19

Table 5 Electrical characteristics of the voltage regulator (cont'd)

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Power supply ripple rejection	*PSRR*	65	70	–	dB	f_{ripple} = 100 Hz; V_{ripple} = 1 Vpp; V_Q = 5 V; I_Q < 100 mA	P_5.2.9
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	100	250	mV	4) I_Q = 100 mA; V_Q = 5 V	P_5.2.10
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	200	500	mV	4) I_Q = 200 mA; V_Q = 5 V	P_5.2.11
Dropout voltage $V_{dr} = V_I - V_Q$	V_{dr}	–	400	1000	mV	4) I_Q = 400 mA; V_Q = 8.5 V	P_5.2.20
Output current limitation	$I_{Q,max}$	401	–	700	mA	0 V ≤ V_Q ≤ 0.95 × $V_{Q,nom}$	P_5.2.13
Reverse current	I_Q	-2	-1	–	mA	V_{BAT} = 0 V; V_Q = 5 V; V_Q = 3 V	P_5.2.14
Reverse current at negative input voltage	I_{BAT}	-10	-6	–	mA	V_{BAT} = -16 V; V_Q = 0 V	P_5.2.15
Overtemperature shutdown threshold	$T_{j,sd}$	151	–	200	°C	1) T_j increasing	P_5.2.16
Overtemperature shutdown threshold hysteresis	$T_{j,hy}$	–	15	–	K	1) T_j decreasing	P_5.2.17

1) Not subject to production test, specified by design.
2) Referring to the device tolerance only, the tolerance of the resistor divider can cause additional deviation.
3) See typical performance graph for details.
4) Measured when the output voltage V_Q has dropped 100 mV from its nominal value.

4.3 Application information for setting the adjustable output voltage

The output voltage of the TLF4277-2EP can be adjusted between 3 V and 16 V by an external output voltage divider, closing the control loop to the voltage adjust pin ADJ.

The TLF4277-2EP compares the voltage at pin ADJ to the internal reference voltage of typically 1.19 V in an error amplifier to control the output voltage.

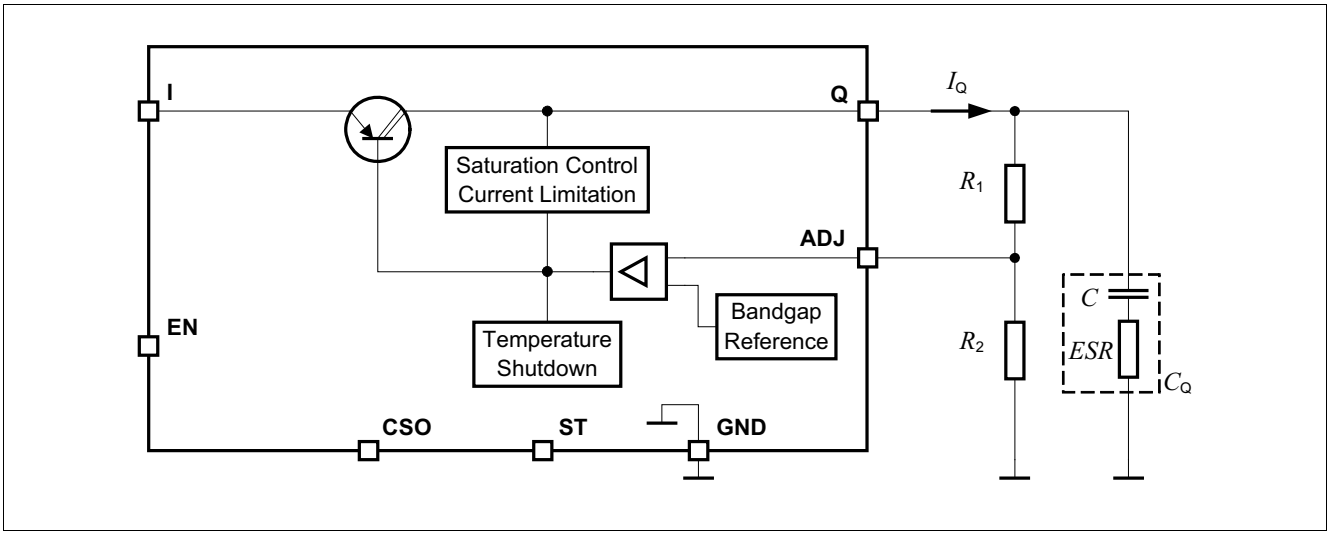


Figure 4 Application detail: external components at the output for adjustable voltage regulator

The output voltage is calculated according to **Equation (4.1)**:

$$V_Q = (R_1 + R_2)/R_2 \times V_{REF,int}, \text{ neglecting } I_{ADJ} \quad (4.1)$$

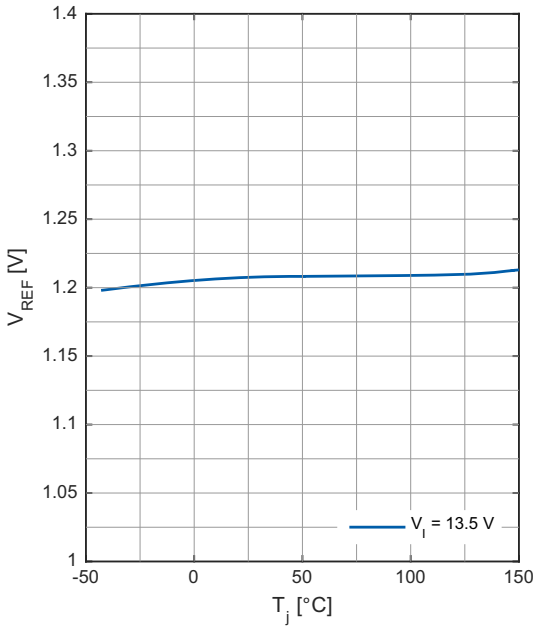
$V_{REF,int}$ is typically 1.19 V.

To avoid errors caused by leakage current I_{ADJ}, choose a resistor value for $R_2 < 27$ kΩ.

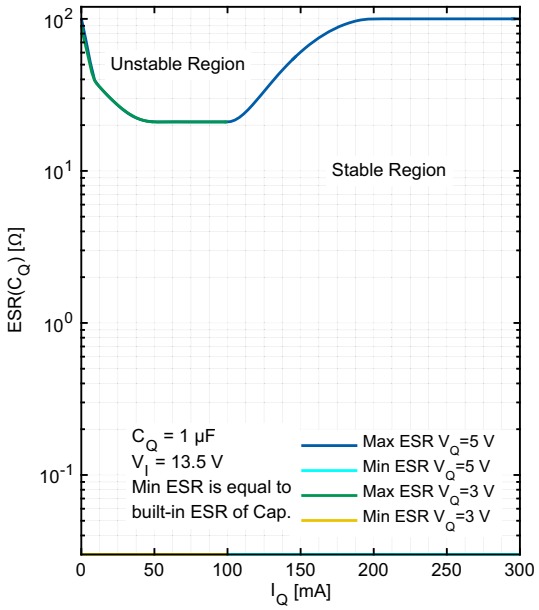
The tolerance of the resistors can reduce the accuracy of the output voltage. For good accuracy, use resistors with a tolerance of 1% or less for the feedback voltage divider.

4.4 Typical performance characteristics of the voltage regulator

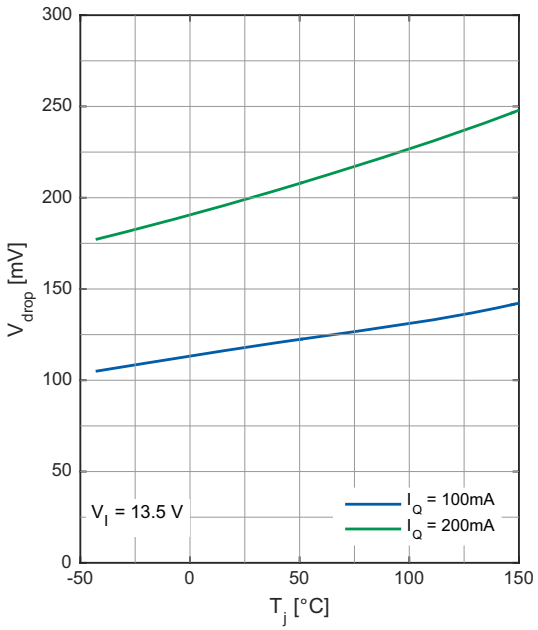
Reference voltage $V_{REF,int}$ versus junction temperature T_j



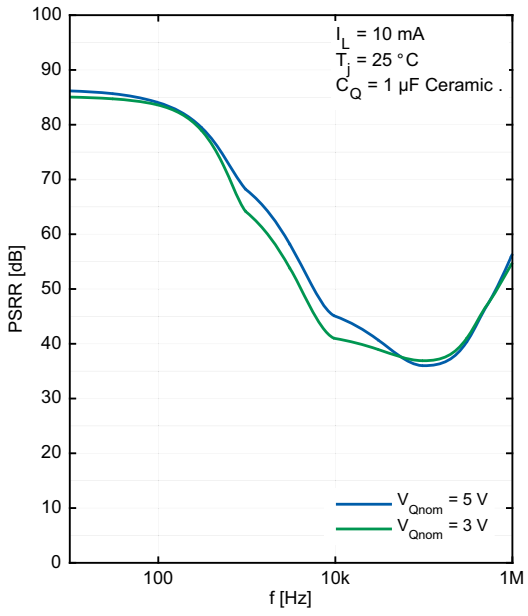
Output capacitor $ESR(C_Q)$ versus output current I_Q



Dropout voltage V_{dr} versus junction temperature T_j



Power supply ripple rejection *PSRR* versus frequency *f*



5 Current consumption

5.1 Electrical characteristics of the current consumption

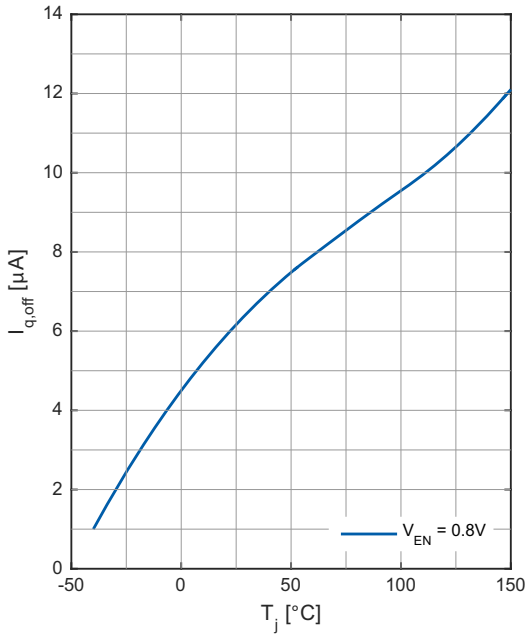
Table 6 Electrical characteristics of the current consumption

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground; direction of currents as shown in **Figure 7** (unless otherwise specified)

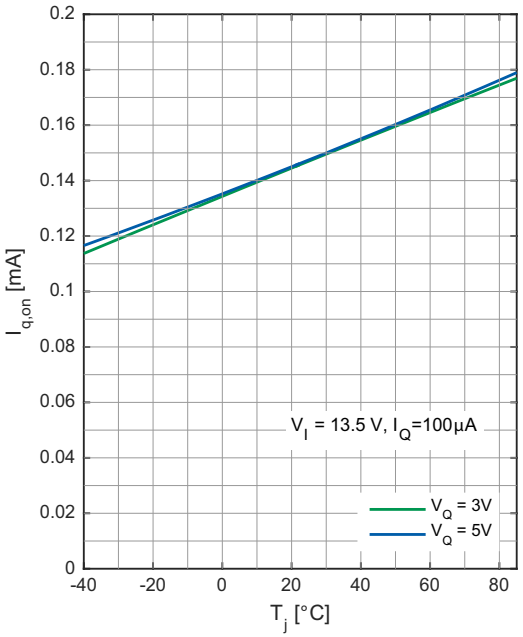
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption	$I_{q,on}$	–	150	200	µA	$I_Q \leq 200$ µA; $T_j \leq 25$°C; V_{EN} = 5 V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.1
Current consumption	$I_{q,on}$	–	–	250	µA	$I_Q \leq 200$ µA; $T_j \leq 85$°C; V_{EN} = 5 V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.2
Current consumption	$I_{q,on}$	–	1.2	2.6	mA	I_Q = 50 mA; V_{EN} = 5 V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.3
Current consumption	$I_{q,on}$	–	5.5	11	mA	I_Q = 200 mA; V_{EN} = 5 V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.4
Current consumption	$I_{q,on}$	–	10	24	mA	I_Q = 300 mA; $V_{EN} > 2$ V; $I_q = I_I - I_Q - I_{CSO}$	P_6.1.8
Current consumption	$I_{q,off}$	–	–	3	µA	$T_j \leq 25$°C; V_{EN} = 0 V; $I_q = I_I - I_Q$	P_6.1.5
Current consumption	$I_{q,off}$	–	–	5	µA	$T_j \leq 85$°C; V_{EN} = 0 V; $I_q = I_I - I_Q$	P_6.1.6
Current consumption	$I_{q,off}$	–	–	15	µA	$T_j \leq 85$°C; V_{EN} = 0.8 V; $I_q = I_I - I_Q$	P_6.1.7

5.2 Typical performance graphs of the current consumption

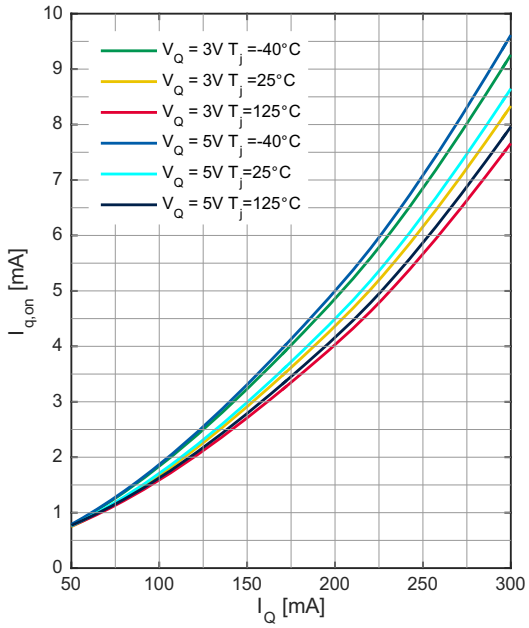
Current consumption $I_{q,off}$ versus junction temperature T_j



Current consumption $I_{q,on}$ versus junction temperature T_j



Current consumption $I_{q,on}$ versus output current I_Q



6 Current monitor and protection monitor functions

6.1 Functional description current and protection monitors

The TLF4277-2EP provides a set of advanced monitoring features.

The CSO output offers monitoring of the current flowing out of the power stage.

In addition, the current limitation can be adjusted via an external resistor. Via dedicated voltage levels, the CSO output reports events that the implemented protection functions detect. An external microcontroller can evaluate this information for system analysis and failure identification.

The TLF4277-2EP monitors the following events:

- Overcurrent
- Overvoltage
- Temperature shutdown

The TLF4277-2EP indicates each of these fault conditions at the digital output pin ST.

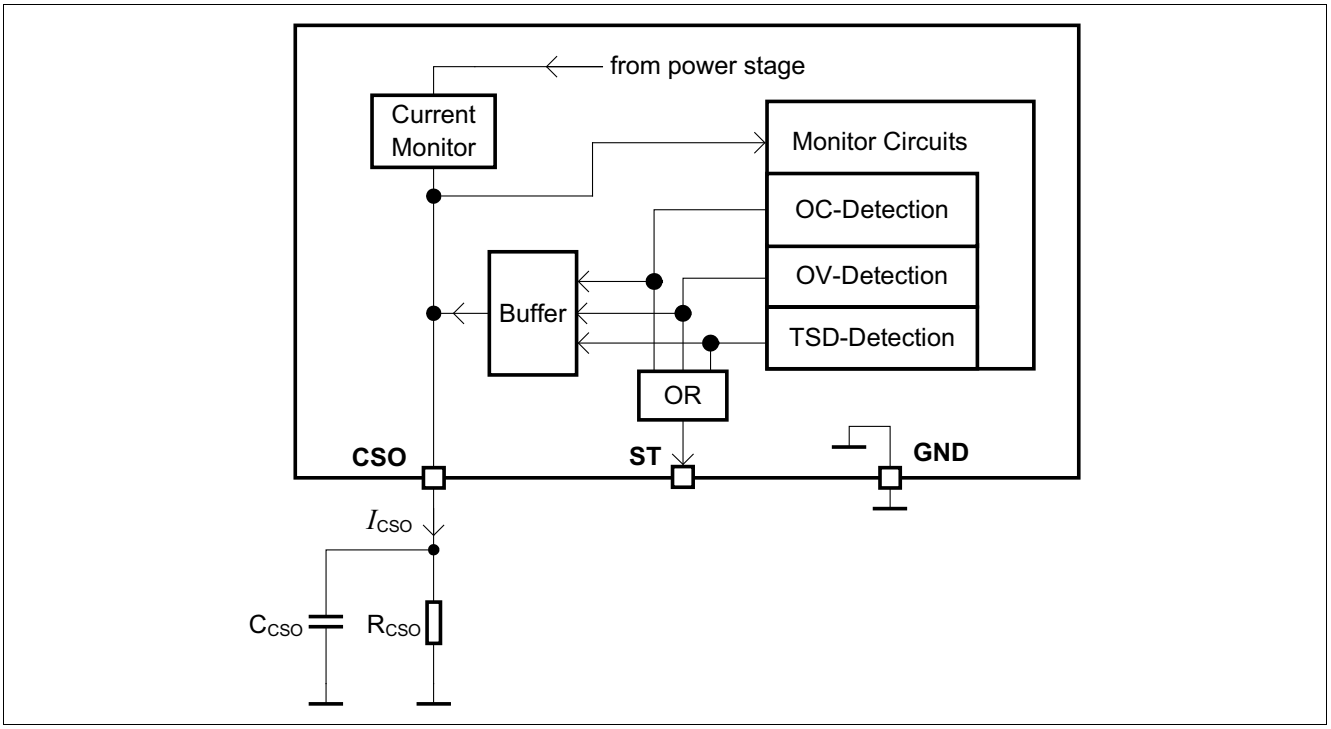


Figure 5 Functional block diagram current monitor and protection monitor

To reduce potential side effects from the supply voltage V_{BAT}, additional filtering of the supply voltage is recommended. Place a 100 nF capacitor as close a possible to the IC terminal connected to V_{BAT}.

Figure 6 shows the output level at the CSO pin versus the operation or fault condition. The graph is valid for the following setup of external components:

C_{CSO} = 2.2 µF

R_{CSO} = 1.5 kΩ

Note: In case of high input voltage (V_I > 20 V), high junction temperature (T_j > 151°C), and the CSO pin directly connected to GND, the return to normal operation from the thermal shutdown mode is not ensured.

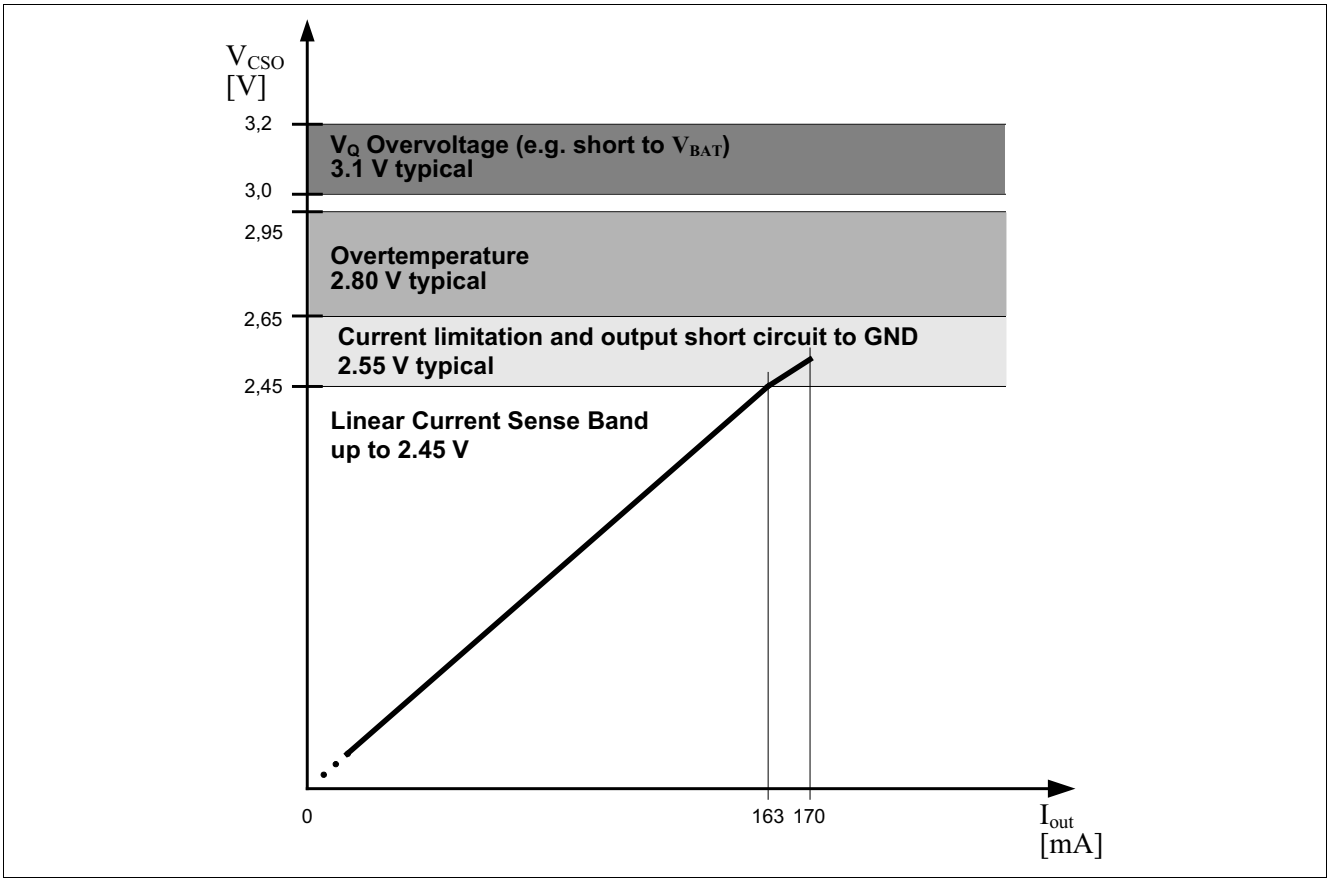


Figure 6 Output levels and functionality of the CSO output

Note: The graph is just an example and only valid for the set up of external components described above.

6.1.1 Linear current monitor

Inside the linear current sense band the TLF4277-2EP drives the current at the CSO directly proportional to the output current I_Q.

The level of the current I_{CSO} can be calculated according to **Equation (6.1)**:

(6.1)

$$I_{CSO} = \frac{I_Q}{F_{IQ/ICSO}}$$

6.1.2 Adjustable output current limitation

The TLF4277-2EP has an adjustable current limitation for the current flowing out of the power stage. If the level of the output current exceeds the defined current limit threshold ($I_{Q,lim}$), then the TLF4277-2EP limits the output current.

Setting of the adjustable current limitation: (6.2)

$$I_{Q,lim} = \frac{2.55V \times F_{IQ/ICSO}}{R_{CSO}}$$

The TLF4277-2EP applies a voltage level defined in **CSO voltage level current limitation** at the CSO pin. In addition the TLF4277-2EP sets the ST pin to low.

*Note: During power up of the device, the regulator works in output current limitation, regardless of the protection function according to **Output current limitation**, limiting the output current or the adjustable output current limitation according to **Adjustable current-limit range**. If an adjustable current limit is set, then the TLF4277-2EP sets the status output pin ST to low as long as the adjustable current limitation is active during power up sequence.*

To achieve a current limitation of for example 170 mA the following configuration can be used:

$$I_{Q,lim} = \frac{2.55V \times 100}{1.5k\Omega} = 170mA$$

$F_{IQ/ICSO}$ = 100
R_{CSO} = 1.5 kΩ

6.1.3 Overvoltage detection

To detect a possible short circuit of the output to a higher supply rail the TLF4277-2EP has an overvoltage detection implemented. If the voltage level at the ADJ pin is 20% above the internal reference voltage $V_{REF,int}$ defined in **Reference voltage**, then the TLF4277-2EP detects overvoltage.

In case of overvoltage the TLF4277-2EP sets the CSO pin to a voltage level defined in **CSO voltage level overvoltage detected**. In addition the TLF4277-2EP sets the ST pin to low.

6.1.4 Thermal shutdown detection

If the junction temperature exceeds the limits defined in the **Overtemperature shutdown threshold**, then the TLF4277-2EP disables the output voltage. In this case the TLF4277-2EP sets the CSO pin to a voltage level defined in **CSO voltage level overtemperature detected**. In addition the TLF4277-2EP sets the ST pin to low.

6.1.5 Status output signal

The ST pin is an open-collector output. An external pull-up resistor must be placed for functionality and to limit the current into the pin (for example, connect via a resistor to Q). Do not connect the ST pin directly to a supply voltage, because this may damage the device.

Current monitor and protection monitor functions

If at least one of the monitored protection functions (overcurrent, overvoltage and temperature shutdown) is active, then the TLF4277-2EP sets the ST pin to low.

Table 7 Electrical characteristics current monitor function

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Linear current monitor							
Current monitor factor $F_{IQ/ICSO} = I_Q/I_{CSO}$	$F_{IQ/ICSO}$	95	100	105	–	1) T_j = -40°C to 125°C; 10 mA ≤ I_Q ≤ 150 mA; V_{IN} = 9 V to 16 V; V_Q = 5 V to 14 V; V_{IN} > V_Q + 2.0 V	P_7.1.1
Current monitor factor $F_{IQ/ICSO} = I_Q/I_{CSO}$	$F_{IQ/ICSO}$	95	100	105	–	1) T_j = -40°C to 125°C; 10 mA ≤ I_Q ≤ 100 mA; V_{IN} = 9 V to 16 V; V_Q = 3 V to 14 V; V_{IN} > V_Q + 2.0 V	P_7.1.2
Current monitor factor $F_{IQ/ICSO} = I_Q/I_{CSO}$	$F_{IQ/ICSO}$	90	100	110	–	1 mA ≤ I_Q ≤ 400 mA; V_{IN} = 9 V to 16 V; V_Q = 5 V	P_7.1.5
Current monitor factor $F_{IQ/ICSO} = I_Q/I_{CSO}$	$F_{IQ/ICSO}$	90	100	110	–	1 mA ≤ I_Q ≤ 300 mA; V_{IN} = 9 V to 16 V; V_Q = 3 V	P_7.1.3
CSO current at no-load condition	$I_{CSO,off}$	–	–	550	nA	No load connected at Q; R_2 = 27 kΩ; V_Q = 5 V	P_7.1.6
Adjustable current limitation							
Adjustable current-limit range	$I_{Q,lim}$	10	–	400	mA	1) 637 Ω < R_{CSO} < 25.5 kΩ; V_Q ≥ 5 V; V_Q < 0.95 × $V_{Q,nom}$	P_7.1.7
Adjustable current-limit range	$I_{Q,lim}$	10	–	300	mA	1) 850 < R_{CSO} < 25.5 kΩ; 5 V > V_Q ≥ 3 V; V_Q < 0.95 × $V_{Q,nom}$	P_7.1.11
Adjustable current-limit tolerance	$I_{Q,lim}$	-10	–	10	%	10 mA ≤ $I_{Q,lim}$ ≤ 300 mA; T_j = -40°C to 125°C; 0.95 × $V_{Q,nom}$ > V_Q > 2.85 V	P_7.1.8
Adjustable current-limit tolerance	$I_{Q,lim}$	-10	–	10	%	300 mA ≤ $I_{Q,lim}$ ≤ 400 mA; T_j = -40°C to 125°C; 0.95 × $V_{Q,nom}$ > V_Q > 4.5 V	P_7.1.4
Adjustable current-limit tolerance	$I_{Q,lim}$	-10	–	25	%	10 mA ≤ $I_{Q,lim}$ ≤ 400 mA; T_j = -40°C to 125°C; 0.95 × $V_{Q,nom}$ > V_Q > 0 V	P_7.1.15
CSO voltage level current limitation	V_{CSO,cur_lim}	2.45	2.55	2.65	V	1) V_Q < 0.95 × $V_{Q,nom}$	P_7.1.9

Table 7 Electrical characteristics current monitor function (cont'd)

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

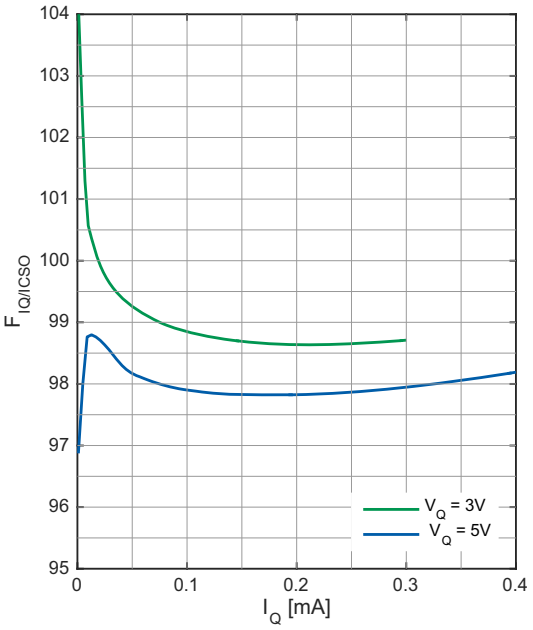
Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output level, overvoltage							
CSO voltage level overvoltage detected	$V_{CSO,OV}$	3.0	3.1	3.2	V	1) $V_{ADJ} > 1.2 \times V_{REF,nom}$	P_7.1.10
Output level, overtemperature							
CSO voltage level overtemperature detected	$V_{CSO,TSD}$	2.65	2.8	2.95	V	2) 151°C < T_j < 180°C	P_7.1.12
Status output signal							
Status-output digital signal low voltage	$V_{ST,low}$	–	0.2	0.4	V	$I_{ST} \leq 1.8$ mA	P_7.1.13
Status-output digital signal sink current	I_{ST}	–	–	1.8	mA	–	P_7.1.14

1) Referring to the device tolerance only. The tolerance of the external components can cause additional deviation.

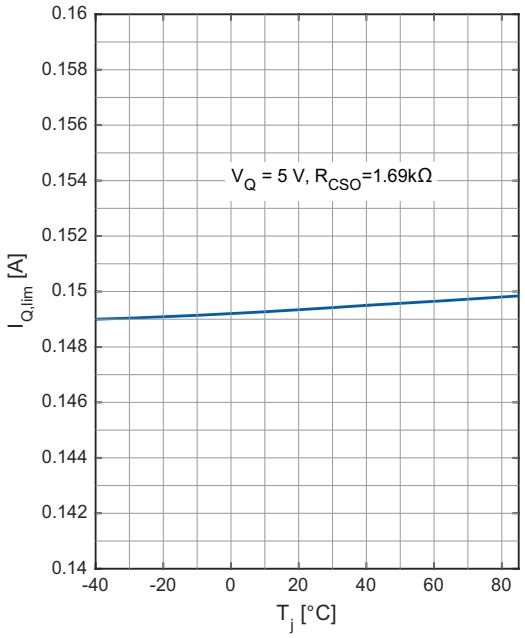
2) Not subject to production test, specified by design.

6.1.6 Typical performance graphs of the current monitor

Current monitor factor $F_{IQ/ICSO}$ versus output current I_Q



External current limitation $I_{Q,lim}$ versus junction temperature T_j



7 Enable function

7.1 Description enable function

The EN input can switch on or switch off the device. A voltage level above $V_{EN,high}$ applied to the EN input switches the device on completely. A voltage level below $V_{EN,low}$ sets the device to low quiescent current mode. In low-quiescent current mode, the device is turned off and is not functional. The EN input has a built-in hysteresis to avoid toggling between on-state and off-state when signals with slow slope are applied to the input. The EN input has an internal pull-down resistor.

7.2 Electrical characteristics enable function

Table 8 Electrical characteristics enable function

V_{BAT} = 13.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, direction of currents as shown in **Figure 7** (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Enable low signal valid	$V_{EN,low}$	–	–	0.8	V	–	P_8.2.1
Enable high signal valid	$V_{EN,high}$	2	–	–	V	See startup time P_8.2.7	P_8.2.2
Enable threshold hysteresis	$V_{EN,hyst}$	50	–	–	mV	–	P_8.2.3
Enable input current	$I_{EN,high}$	–	–	5	µA	V_{EN} = 5 V	P_8.2.4
Enable input current	$I_{EN,high}$	–	–	20	µA	V_{EN} < 18 V	P_8.2.5
Enable internal pull-down resistor	R_{EN}	0.94	1.5	2.5	MΩ	V_{EN} < 5 V	P_8.2.6
Startup time	t_{EN}	–	180	–	µs	C_Q = 1 µF; $V_{Q,nom}$ = 5 V; $I_{Q,load}$ = 150 mA; time from V_{EN} > 2 V; (0 V to 5 V transition) until V_Q = 0.9 × $V_{Q,nom}$	P_8.2.7

8 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

8.1 Application diagram

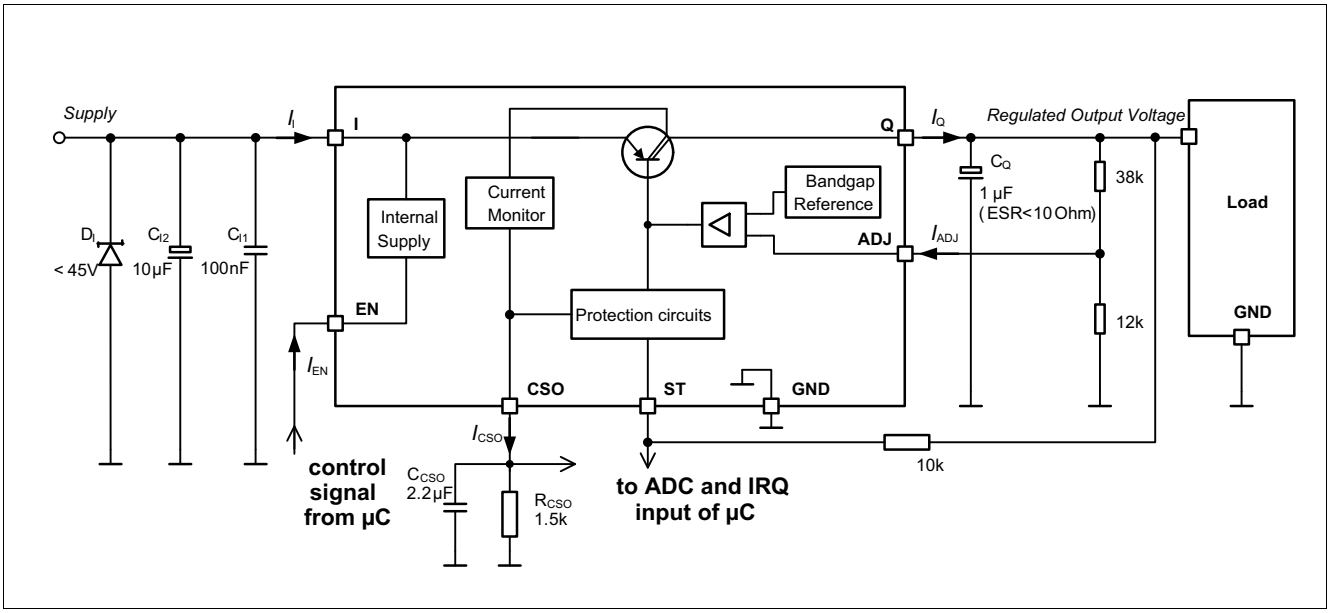


Figure 7 Application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

8.2 Selection of external components

8.2.1 Input pin

Figure 7 shows the typical input circuitry for a linear voltage regulator.

A ceramic capacitor at the input in the range of 100 nF to 470 nF is recommended to filter the high frequency disturbances imposed from the line, such as ISO pulses 3a/b. Place this capacitor as close as possible to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10 µF to 470 µF is recommended as an input buffer to damp high-energy pulses, such as ISO pulse 2a. Place this capacitor close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to overvoltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator from external disturbances and damages.

8.2.2 Output pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **Table 3**. The graph **Output capacitor ESR(C_Q) versus output current I_Q** shows the stable operation range of the device.

The TLF4277-2EP is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator's output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

8.3 Thermal considerations

The total power dissipation can be calculated from the known input voltage, the output voltage and the load profile of the application:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (8.1)$$

with

- P_D: continuous power dissipation
- V_I: input voltage
- V_Q: output voltage
- I_Q: output current
- I_q: quiescent current

The maximum acceptable thermal resistance R_{thJA} is:

$$R_{thJA,max} = (T_{j,max} - T_a)/P_D \quad (8.2)$$

with

- $T_{j,max}$: maximum allowed junction temperature
- T_a: ambient temperature

Based on the above calculation, the proper PCB type and the necessary heat sink area can be determined with reference to the specification in **Table 4**.

Example

Application conditions:

V_I = 13.5 V

V_Q = 5 V

I_Q = 100 mA

T_a = 85°C

Calculation of $R_{thJA,max}$:

$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q$

$= (13.5\ V - 5\ V) \times 100\ mA + 13.5\ V \times 5.0\ mA$

$= 0.850\ W + 0.068\ W$

$= 0.918\ W$

$R_{thJA,max} = (T_{j,max} - T_a)/P_D$

$= (150°C - 85°C)/0.918\ W = 70.8\ K/W$

As a result, the PCB design must ensure a thermal resistance R_{thJA} of less than 70.8 K/W. According to **Table 4**, at least 300 mm^2 heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.

8.4 Reverse-polarity protection

TLF4277-2EP is self protected against reverse-polarity faults and allows negative supply voltage. An external reverse polarity diode is not needed. However, the absolute maximum ratings of the device as specified in **Table 2** must be maintained.

The reverse voltage causes several small currents to flow into the IC, which increase its junction temperature. As the thermal shutdown circuitry does not work in reverse-polarity conditions, the application design must consider this in the thermal design.

8.5 Further application information

For further information you may contact **http://www.infineon.com/**

9 Package information

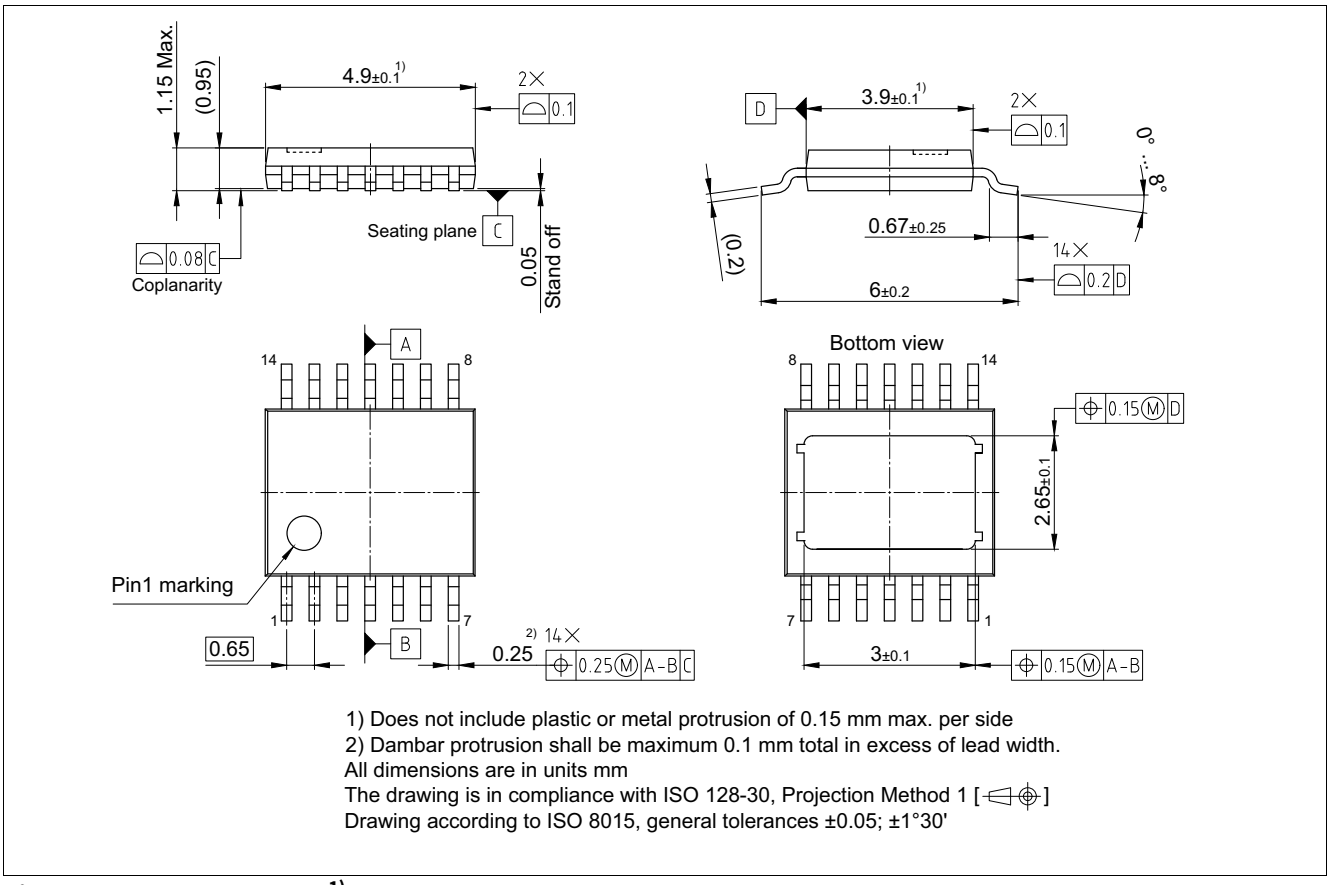


Figure 8 PG-TSDSO-14[1)]

Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Further information on packages

https://www.infineon.com/packages

1) Dimensions in mm

10 Revision history

Revision	Date	Changes
1.01	2024-03-26	Template update and editorial changes
1.0	2021-07-23	Datasheet created

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