

# OPTIREG™ PMIC TLF35585QUS01

## Functional safety PMIC



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Technical documents



Simulation



Family overview



Support



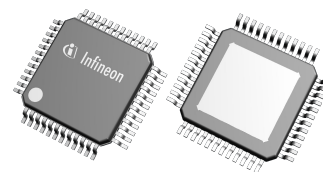
RoHS



ISO 26262 compliant

## Features

- High efficient power management integrated circuit (PMIC)
- Serial step up and step down pre-regulator for wide input voltage range from 3.0 V to 40 V with full performance and low overall power loss
- Low drop post regulator 5.0 V/600 mA for microcontroller main supply (QUC)
- Low drop post regulator 5.0 V/200 mA for communication supply (QCO)
- Voltage reference ( $\pm 1\%$ ) 5.0 V/150 mA for ADC supply (QVR)
- Two trackers for sensor supply following voltage reference 150 mA current capability each (QT1 and QT2)
- Standby regulator 5.0 V/10 mA (QST)
- Enable, sync out signal and voltage monitoring of an optional external post regulator for core supply
- Independent voltage monitoring block and error pin monitoring
- Configurable window watchdog and functional watchdog
- Safe State Control with two safe state signals with programmable delay
- 16-bit SPI, interrupt and reset function
- High junction temperature operation up to 175°C
- PRO-SIL™ Features:
  - ISO 26262 Safety Element out of Context for requirements up to ASIL D
  - Safety documentation for ISO 26262 compliant system integration
- Green Product (RoHS compliant)



## Potential applications

- Electric power steering
- Battery management
- Engine management
- Domain control
- Traction inverter

## Product validation

Qualified for automotive applications with higher temperature requirements. Product validation according to AEC-Q100, Grade 0.

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**Description**

## Description

The OPTIREG™ PMIC TLF35585QUS01 is a highly efficient Functional Safety PMIC (Power management integrated circuit) for safety-relevant applications.

The power supply includes a boost-buck pre-regulator supplying post regulator rails for microcontroller supply, communication supply and a precise voltage reference. In addition, two trackers following the voltage reference are available to supply off-board sensors.

The OPTIREG™ PMIC TLF35585QUS01 comes with a configurable window watchdog (time based trigger) and functional watchdog (question and answer based trigger), error pin monitoring and voltage monitoring functions as major supervision functions. For microcontroller interaction a 16-bit SPI, interrupt and reset function are provided.

The device has been developed according to ISO 26262 targeting systems up to ASIL D and supports an extended junction temperature range of up to 175°C.

| Type          | Package       | Marking (Line1 / Line2) |
|---------------|---------------|-------------------------|
| TLF35585QUS01 | PG-TQFP-48-10 | TLF35585 / S01 R0       |

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**1 General product characteristics**

**1 General product characteristics**

**1.1 Absolute maximum ratings**

**Table 1 Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $175^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                                 | Symbol    | Values |      |      | Unit | Note or condition  | Number   |
|---|-----------|--------|------|------|------|--|----------|
|   |           | Min.   | Typ. | Max. |      |  |          |
| <b>Voltages</b>                           |           |        |      |      |      |  |          |
| Boost driver ground                       | $V_{BSG}$ | -0.3   | -    | 0.3  | V    | -  | P_4.1.1  |
| Input standby supply                      | $V_{VST}$ | -0.3   | -    | 40   | V    | 2) 3)  | P_4.1.2  |
| Input voltage pin 1 (pre-regulator)       | $V_{VS1}$ | -0.3   | -    | 40   | V    | 2) 3)<br>Exception for SLEEP state: $V_{VS1}$ is limited to max. 20 V) | P_4.1.3  |
| External step up power stage, gate        | $V_{DRG}$ | -0.3   | -    | 40   | V    | 2)   | P_4.1.4  |
| External power stage, sense resistor high | $V_{RSH}$ | -0.3   | -    | 40   | V    | 2)   | P_4.1.5  |
| External power stage, sense resistor low  | $V_{RSL}$ | -0.3   | -    | 2.5  | V    | -  | P_4.1.6  |
| Enable input                              | $V_{ENA}$ | -0.3   | -    | 40   | V    | 2)   | P_4.1.7  |
| Enable input                              | $I_{ENA}$ | -5     | -    | -    | mA   | 4)   | P_4.1.8  |
| Wake input                                | $V_{WAK}$ | -0.3   | -    | 40   | V    | 2)   | P_4.1.9  |
| Wake input                                | $I_{WAK}$ | -5     | -    | -    | mA   | 4)   | P_4.1.10 |
| Reset output                              | $V_{ROT}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.11 |
| SPI chip select input                     | $V_{SCS}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.12 |
| SPI clock input                           | $V_{SCL}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.13 |
| SPI data in (MOSI) input                  | $V_{SDI}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.14 |
| SPI data out (MISO output)                | $V_{SDO}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.15 |
| Interrupt output                          | $V_{INT}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.16 |
| Window watchdog trigger input             | $V_{WDI}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.17 |
| Error pin input                           | $V_{ERR}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.18 |
| Safe state 1 output                       | $V_{SS1}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.19 |
| Safe state 2 output                       | $V_{SS2}$ | -0.3   | -    | 40.0 | V    | -  | P_4.1.20 |
| Output voltage reference supply           | $V_{QVR}$ | -0.3   | -    | 6.0  | V    | -  | P_4.1.21 |

**(table continues...)**  
 Datasheet (excerpt)

**1 General product characteristics**

**Table 1 (continued) Absolute maximum ratings<sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $175^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                            | Symbol    | Values |      |      | Unit | Note or condition | Number   |
|--------------------------------------|-----------|--------|------|------|------|-------------------|----------|
|                                      |           | Min.   | Typ. | Max. |      |                   |          |
| Output tracker 2                     | $V_{QT2}$ | -1.0   | –    | 40   | V    | –                 | P_4.1.22 |
| Output tracker 1                     | $V_{QT1}$ | -1.0   | –    | 40   | V    | –                 | P_4.1.23 |
| Output communication supply          | $V_{QCO}$ | -0.3   | –    | 6.0  | V    | –                 | P_4.1.24 |
| Output microcontroller main supply   | $V_{QUC}$ | -0.3   | –    | 6.0  | V    | –                 | P_4.1.25 |
| External core voltage monitor input  | $V_{VCI}$ | -0.3   | –    | 6.0  | V    | –                 | P_4.1.26 |
| HW config: ext. core voltage monitor | $V_{SEC}$ | -0.3   | –    | 6.0  | V    | –                 | P_4.1.27 |
| Synchronization output               | $V_{SYN}$ | -0.3   | –    | 40.0 | V    | –                 | P_4.1.28 |
| Enable output for ext. core supply   | $V_{EVC}$ | -0.3   | –    | 40.0 | V    | –                 | P_4.1.29 |
| Step down feedback input 2           | $V_{FB2}$ | -0.3   | –    | 8.0  | V    | –                 | P_4.1.30 |
| Step down feedback input 1           | $V_{FB1}$ | -0.3   | –    | 8.0  | V    | –                 | P_4.1.31 |
| Step down power ground 2             | $V_{PG2}$ | -0.3   | –    | 0.3  | V    | –                 | P_4.1.32 |
| Step down power ground 1             | $V_{PG1}$ | -0.3   | –    | 0.3  | V    | –                 | P_4.1.33 |
| Step down switching node             | $V_{SW1}$ | -0.3   | –    | 40   | V    | <sup>3)</sup>     | P_4.1.34 |
| HW config: step up pre-regulator     | $V_{STU}$ | -0.3   | –    | 6.0  | V    | –                 | P_4.1.35 |
| HW config: step down frequency       | $V_{FRE}$ | -0.3   | –    | 6.0  | V    | –                 | P_4.1.36 |
| Output standby supply                | $V_{QST}$ | -0.3   | –    | 6.0  | V    | –                 | P_4.1.37 |
| Input MPS                            | $V_{MPS}$ | -0.3   | –    | 20   | V    | –                 | P_4.1.38 |

**Temperatures**

|                      |           |     |   |     |    |   |          |
|----------------------|-----------|-----|---|-----|----|---|----------|
| Junction temperature | $T_j$     | -40 | – | 175 | °C | – | P_4.1.39 |
| Storage temperature  | $T_{stg}$ | -55 | – | 175 | °C | – | P_4.1.40 |

**ESD susceptibility**

|                                     |                  |      |   |     |    |                   |          |
|-------------------------------------|------------------|------|---|-----|----|-------------------|----------|
| ESD robustness to GND               | $V_{ESD}$        | -2   | – | 2   | kV | HBM <sup>5)</sup> | P_4.1.41 |
| ESD robustness to GND               | $V_{ESD}$        | -500 | – | 500 | V  | CDM <sup>6)</sup> | P_4.1.42 |
| ESD robustness (corner pins) to GND | $V_{ESD,Corner}$ | -750 | – | 750 | V  | CDM <sup>6)</sup> | P_4.1.43 |

1) Not subject to production test, specified by design.

2) Maximum rating is 60 V, if rising slewrate of voltage at the pin is lower than 6 V/ms, for an overall time of 1 hour during the lifetime of the product

## **1 General product characteristics**

- 3) Maximum rating is 43.5 V, for an overall time of 10 s (in the range of 40 V to 43.5 V) during the lifetime of the product independent from the rise time.
  - 4) Consider external series resistor for negative voltages < -0.3 V to ensure maximum rating of current
  - 5) Human body model (HBM) robustness according to ANSI/ESDA/JEDEC JS-001 (1.5 k $\Omega$ , 100 pF).
  - 6) Charged device model (CDM) robustness according to ESDA STM5.3.1 or ANSI/ESD S.5.3.1.
- 

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information visit [www.jedec.org](http://www.jedec.org).*

## **2 Application information**

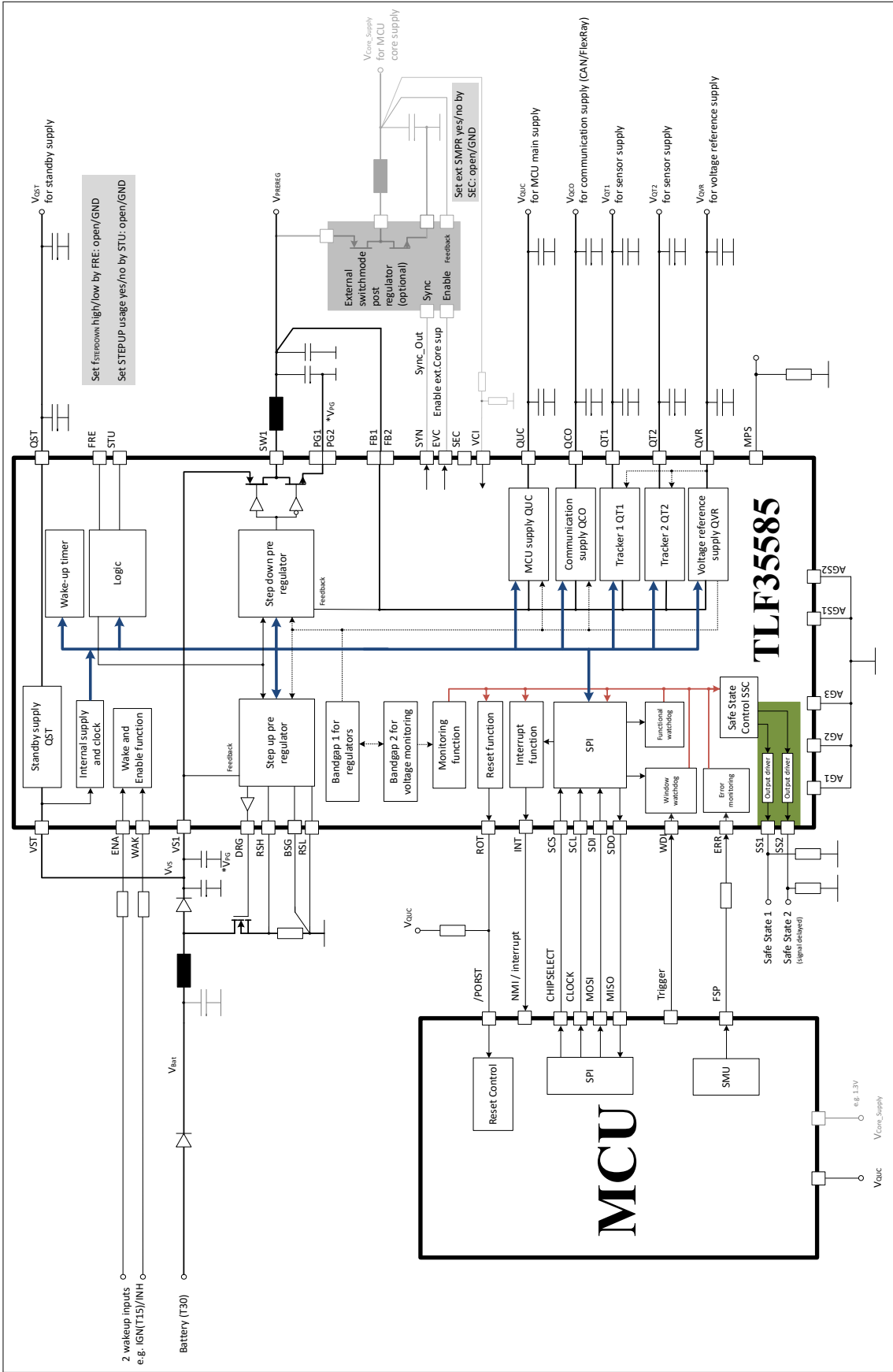
The following figure describes how the IC is used in its environment.

*Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

- Please contact us for additional supportive documentation.
- For further information you may contact <http://www.infineon.com/>

*Note: This figure is a simplified example of an application circuit. The function must be verified in the application.*

**2 Application information**

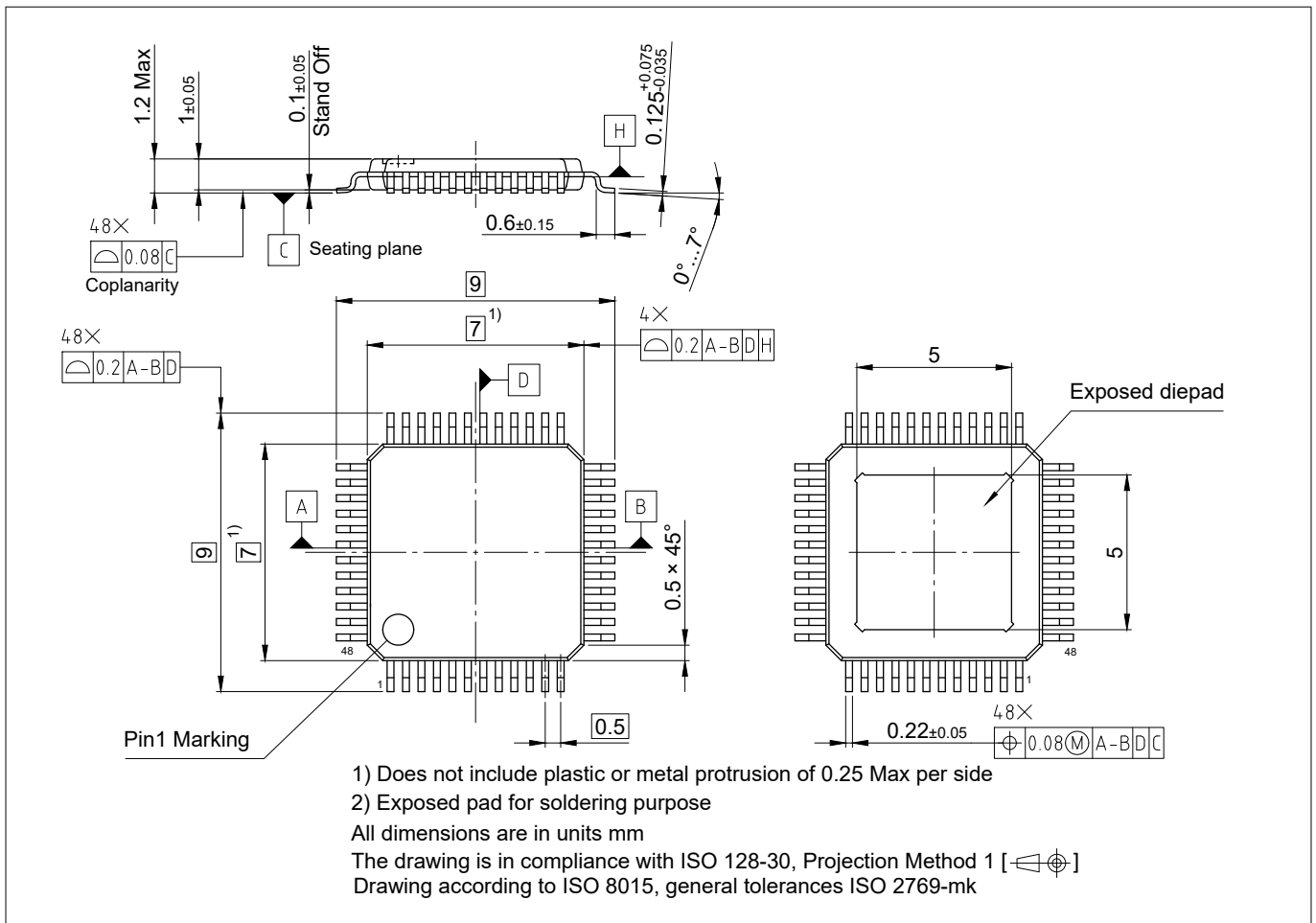


**Figure 1** Application diagram



**3 Package information**

**3 Package information**



**Figure 2 PG-TQFP-48-10**

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

**Information on alternative packages**

Please visit [www.infineon.com/packages](http://www.infineon.com/packages).

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