

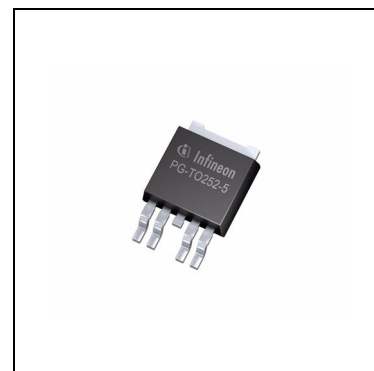
# OPTIREG™ linear TLF1963TE

## Low dropout voltage post regulator



### Features

- Adjustable output voltage
- Output voltage tolerance at small loads of  $\pm 1.5\%$
- Output current capability up to 1.5 A
- Very low dropout voltage of 340 mV
- Extended operating range starting at 1.7 V
- Low noise of typ.  $40 \mu\text{V}_{\text{RMS}}$  (10 Hz to 100 kHz)
- Small output capacitor for stability 10  $\mu\text{F}$
- Suitable for ceramic output capacitors
- Enable functionality
- Overtemperature shutdown
- Reverse polarity protection
- Output current limitation
- Wide temperature range from  $-40^\circ\text{C}$  up to  $150^\circ\text{C}$
- Green Product (RoHS compliant)



### Potential applications

- Suitable for use in automotive electronics as post regulator.

### Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

### Description

The OPTIREG™ linear TLF1963TE is a low dropout voltage regulator available in a PG-T0252-5 SMD package. The IC regulates an input voltage  $V_I$  in the range of  $2.5 \text{ V} < V_I < 20 \text{ V}$  to an adjustable output voltage of  $1.21 \text{ V} < V_{Q,\text{nom}} < V_I - V_{\text{dr}}$ . The device is capable to supply loads up to 1.5 A. The regulator can be enabled and disabled via the Enable input. The integrated output current limitation and the overtemperature shutdown will protect the device against failures like output short circuit to GND, overcurrent and overtemperature.

The TLF1963TE provides the ideal solution for systems requiring several supply voltages. With its adjust feature the regulator can provide all supply voltages between 1.21 V and the available input voltage, this offers a high flexibility to the system designer.

The input capacitor  $C_I$  is necessary for compensating line influences. The output capacitor  $C_O$  is necessary for the stability of the regulating circuit. Stability is guaranteed at values specified in **Functional range** within the whole operating temperature range.

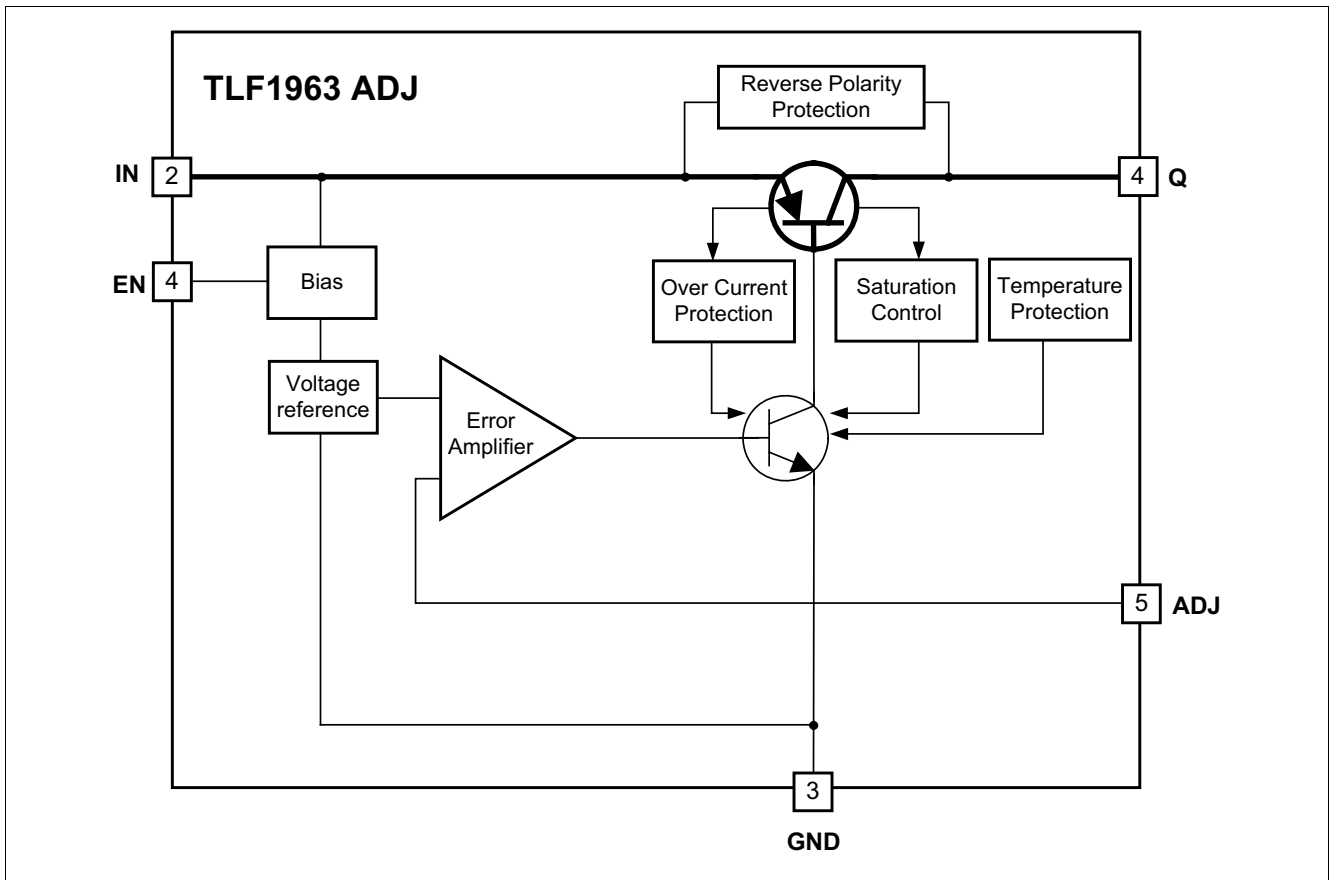
<b>Type</b>	<b>Package</b>	<b>Marking</b>
TLF1963TE	PG-TO252-5	T1963V

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**Block diagram**

**1 Block diagram**

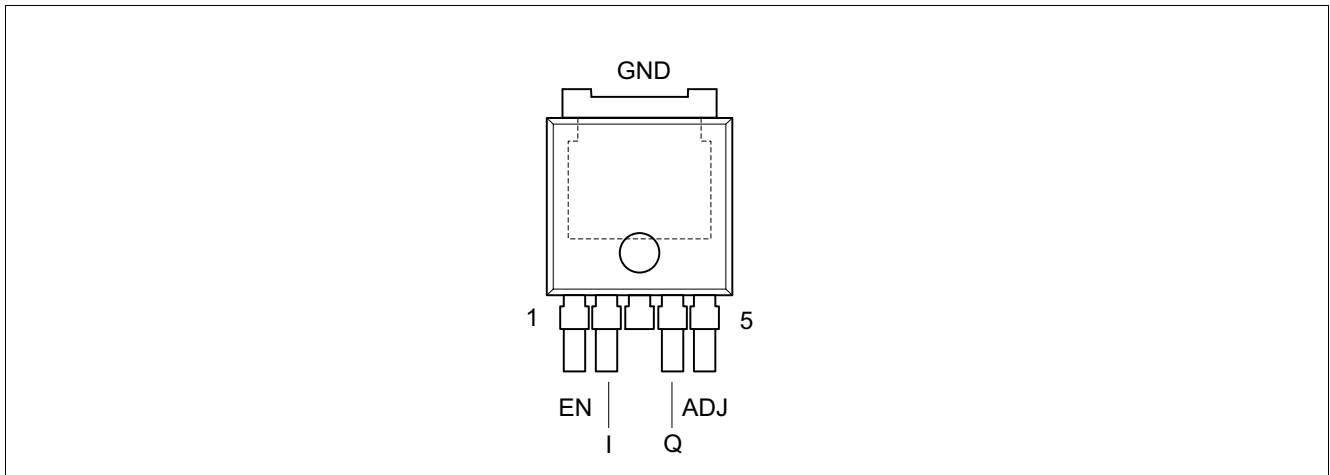


**Figure 1 Block diagram**

**Pin configuration**

## 2 Pin configuration

### 2.1 Pin assignment



**Figure 2 Pin configuration**

### 2.2 Pin definitions and functions

**Table 1 Pin definitions and functions**

Pin	Symbol	Function
1	EN	<b>Enable;</b> A low signal disables the IC. A high signal switches it on. Connect to the input I, if enable functionality is not required.
2	I	<b>Input voltage;</b> IC supply. For compensating line influences, a capacitor close to the IC pins is recommended.
3	GND	<b>Ground</b>
4	Q	<b>Output voltage;</b> Connect a capacitor between Q and GND close to the IC terminals, respecting the values given for its capacitance $C_Q$ and ESR given in the table <a href="#">“Functional range” on Page 7</a>
5	ADJ	<b>Adjust Input;</b> Connect an external voltage divider from Q to GND to determine the output voltage. By connecting the output pin Q directly to the adjust pin ADJ without resistors an output voltage equal to the reference voltage $V_{ADJ} = 1.21\text{ V}$ is determined.
TAB	GND	<b>Ground</b>

**General product characteristics**

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings <sup>1)</sup>**

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
<b>Input, enable</b>							
Voltage	$V_I, V_{EN}$	-20	-	20	V	-	P_4.1.1
<b>Adjust</b>							
Voltage	$V_{ADJ}$	-7	-	7	V	-	P_4.1.2
<b>Output</b>							
Voltage	$V_Q$	-20	-	20	V	-	P_4.1.3
<b>Temperatures</b>							
Junction temperature	$T_j$	-40	-	150	°C	-	P_4.1.4
Storage temperature	$T_{stg}$	-50	-	150	°C	-	P_4.1.5
<b>ESD susceptibility</b>							
ESD resistivity	$V_{ESD,HBM}$	-2	-	2	kV	HBM <sup>2)</sup>	P_4.1.6
ESD resistivity	$V_{ESD,CDM}$	-750	-	750	V	CDM <sup>3)</sup>	P_4.1.7

1) Not subject to production test, specified by design.

2) ESD susceptibility, human body model “HBM” according AEC-Q100-002 - JESD22-A114 (1.5 kΩ, 100 pF).

3) ESD susceptibility, charged device model “CDM” according to EIA/JESD22-C101 or ESDA STM5.3.1.

#### Notes

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

**General product characteristics**

**3.2 Functional range**

**Table 3 Functional range**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	$V_I$	2.5	–	20	V	–	P_4.2.1
Output capacitor's requirements for stability	$C_Q$	10	–	–	$\mu\text{F}$	1)	P_4.2.2
Output capacitor's requirements for stability	$\text{ESR}(C_Q)$	–	–	3	$\Omega$	2)	P_4.2.3
Junction temperature	$T_j$	-40	–	150	$^{\circ}\text{C}$	–	P_4.2.4

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

2) Relevant ESR value at  $f = 10$  kHz.

*Note:* Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

**3.3 Thermal resistance**

*Note:* This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 4 Thermal resistance**

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	$R_{\text{thJC}}$	–	0.78	–	K/W	1) measured to heat slug	P_4.3.6
Junction to ambient	$R_{\text{thJA}}$	–	24	–	K/W	1) 2)	P_4.3.7
Junction to ambient	$R_{\text{thJA}}$	–	95	–	K/W	1)3) footprint only	P_4.3.8
Junction to ambient	$R_{\text{thJA}}$	–	50	–	K/W	1)3) 300 mm <sup>2</sup> heatsink area	P_4.3.9
Junction to ambient	$R_{\text{thJA}}$	–	38	–	K/W	1)3) 600 mm <sup>2</sup> heatsink area	P_4.3.10

1) Not subject to production test, specified by design.

2) Specified  $R_{\text{thJA}}$  value is according to JEDEC JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 × 70  $\mu\text{m}$  Cu, 2 × 35  $\mu\text{m}$  Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified  $R_{\text{thJA}}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm<sup>3</sup> board with 1 copper layer (1 × 70  $\mu\text{m}$  Cu).

**Electrical characteristics**

**4 Electrical characteristics**

**4.1 Electrical characteristics voltage regulator**

**Table 5 Electrical characteristics:**

$V_I = 2.5\text{ V} - 20\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing out of the pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Min. input voltage	$V_{I,\text{min}}$	–	1.7	–	V	<sup>1)2)</sup> $I_Q = 0.5\text{ A}$ ; $T_j = 25^\circ\text{C}$	P_5.1.1
Min. input voltage	$V_{I,\text{min}}$	–	2.1	2.5	V	<sup>1)2)</sup> $I_Q = 1.5\text{ A}$	P_5.1.2
Adjustable pin voltage	$V_{\text{ADJ}}$	1.192	1.21	1.228	V	<sup>1)3)</sup> $V_I = 2.21$ to $20\text{ V}$ ; $I_Q = 1\text{ mA}$ ; $T_j = 25^\circ\text{C}$	P_5.1.3
Adjustable pin voltage	$V_{\text{ADJ}}$	1.174	1.21	1.246	V	<sup>1)3)</sup> $I_Q = 1\text{ mA}$ to $1.5\text{ A}$	P_5.1.4
Line regulation	$\Delta V_{Q,\text{line}}$	–	1.0	3	mV	<sup>1)</sup> $V_I = 2.21$ to $20\text{ V}$ ; $I_Q = 1\text{ mA}$	P_5.1.5
Load regulation	$\Delta V_{Q,\text{load}}$	–	2	8	mV	<sup>1)</sup> $I_Q = 1\text{ mA}$ to $1.5\text{ A}$ ; $V_I = 2.5\text{ V}$ ; $T_j = 25^\circ\text{C}$	P_5.1.6
Load regulation	$\Delta V_{Q,\text{load}}$	–	–	12	mV	<sup>1)</sup> $I_Q = 1\text{ mA}$ to $1.5\text{ A}$ ; $V_I = 2.5\text{ V}$	P_5.1.7
Dropout voltage $V_I = V_{Q,\text{nom}}$	$V_{\text{dr}}$	–	0.01	0.03	V	<sup>2)4)5)</sup> $I_Q = 1\text{ mA}$ ; $T_j = 25^\circ\text{C}$	P_5.1.8
Dropout voltage $V_I = V_{Q,\text{nom}}$	$V_{\text{dr}}$	–	–	0.04	V	<sup>2)4)5)</sup> $I_Q = 1\text{ mA}$	P_5.1.9
Dropout voltage $V_I = V_{Q,\text{nom}}$	$V_{\text{dr}}$	–	0.03	0.05	V	<sup>2)4)5)</sup> $I_Q = 100\text{ mA}$ ; $T_j = 25^\circ\text{C}$	P_5.1.10
Dropout voltage $V_I = V_{Q,\text{nom}}$	$V_{\text{dr}}$	–	–	0.09	V	<sup>2)4)5)</sup> $I_Q = 100\text{ mA}$	P_5.1.11
Dropout voltage $V_I = V_{Q,\text{nom}}$	$V_{\text{dr}}$	–	0.13	0.25	V	<sup>2)4)5)</sup> $I_Q = 500\text{ mA}$ ; $T_j = 25^\circ\text{C}$	P_5.1.12
Dropout voltage $V_I = V_{Q,\text{nom}}$	$V_{\text{dr}}$	–	–	0.27	V	<sup>2)4)5)</sup> $I_Q = 500\text{ mA}$	P_5.1.13
Dropout voltage $V_I = V_{Q,\text{nom}}$	$V_{\text{dr}}$	–	0.34	0.45	V	<sup>2)4)5)</sup> $I_Q = 1.5\text{ A}$ ; $T_j = 25^\circ\text{C}$	P_5.1.14
Dropout voltage $V_I = V_{Q,\text{nom}}$	$V_{\text{dr}}$	–	–	0.55	V	<sup>2)4)5)</sup> $I_Q = 1.5\text{ A}$	P_5.1.15
GND pin current $V_I = V_{Q,\text{nom}} + 1\text{ V}$	$I_q$	–	1.0	1.5	mA	<sup>4)6)</sup> $I_Q = 0\text{ mA}$	P_5.1.16
GND pin current $V_I = V_{Q,\text{nom}} + 1\text{ V}$	$I_q$	–	1.1	1.7	mA	<sup>4)6)</sup> $I_Q = 1\text{ mA}$	P_5.1.17



**Electrical characteristics**

**Table 5 Electrical characteristics: (cont'd)**

$V_I = 2.5\text{ V} - 20\text{ V}$ ,  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ , all voltages with respect to ground, positive current flowing out of the pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
GND pin current $V_I = V_{Q,nom} + 1\text{ V}$	$I_q$	–	3.8	5.0	mA	<sup>4)6)</sup> $I_Q = 100\text{ mA}$	P_5.1.18
GND pin current $V_I = V_{Q,nom} + 1\text{ V}$	$I_q$	–	15	22	mA	<sup>4)6)</sup> $I_Q = 500\text{ mA}$	P_5.1.19
GND pin current $V_I = V_{Q,nom} + 1\text{ V}$	$I_q$	–	80	130	mA	<sup>4)6)</sup> $I_Q = 1.5\text{ A}$	P_5.1.20
Output voltage noise	$V_{Q,noise}$	–	40	–	$\mu\text{V}_{RMS}$	$C_Q = 10\text{ }\mu\text{F}$ ; $I_Q = 1.5\text{ A}$ ; BW = 10 Hz to 100 kHz	P_5.1.21
ADJ pin bias current	$I_{ADJ}$	–	1	2	$\mu\text{A}$	<sup>1)7)</sup>	P_5.1.22
Enable threshold	$V_{EN,LH}$	–	1.4	2	V	$V_Q = \text{Off to On}$	P_5.1.23
Enable threshold	$V_{EN,HL}$	0.8	1.3	–	V	$V_Q = \text{On to Off}$	P_5.1.24
EN Pin current	$I_{EN}$	–	0	0.2	$\mu\text{A}$	<sup>8)</sup> $V_{EN} = 0\text{ V}$	P_5.1.25
EN Pin current	$I_{EN}$	–	2.5	20	$\mu\text{A}$	<sup>8)</sup> $V_{EN} \leq 20\text{ V}$	P_5.1.26
Quiescent current in Shutdown	$I_{q,off}$	–	0.01	1	$\mu\text{A}$	<sup>9)</sup> $V_I = 6\text{ V}$ ; $V_{EN} = 0\text{ V}$ ; $T_j \leq 85^\circ\text{C}$	P_5.1.27
Power supply ripple rejection	$PSRR$	55	67	–	dB	<sup>10)</sup> $T_j = 25^\circ\text{C}$ ; $f_r = 120\text{ Hz}$ ; $I_Q = 0.75\text{ A}$ ; $V_I - V_Q = 1.5\text{ V}$ ; $V_r = 0.5\text{ }V_{pp}$	P_5.1.28
Output current limitation	$I_Q$	–	2	–	A	$T_j = 25^\circ\text{C}$ ; $V_I = 7\text{ V}$ ; $V_Q = 0\text{ V}$	P_5.1.29
Output current limitation	$I_Q$	1.6	–	–	A	$V_I = V_{Q,nom} + 1\text{ V}$ ; $\Delta V_Q = -0.1\text{ V}$	P_5.1.30
Input reverse leakage current	$I_{I,rev}$	–	–	2	mA	$V_I = -20\text{ V}$ ; $V_Q = 0\text{ V}$	P_5.1.31
Reverse output current	$I_{Q,rev}$	–	300	600	$\mu\text{A}$	<sup>11)</sup> $T_j = 25^\circ\text{C}$ ; $V_Q = 1.21\text{ V}$ ; $V_I < 1.21\text{ V}$	P_5.1.32
Reverse output current	$I_{Q,rev}$	–	–	1	mA	<sup>11)</sup> $V_Q = 1.21\text{ V}$ ; $V_I < 1.21\text{ V}$	P_5.1.33

1) The TLF1963TE is tested and specified for these conditions with the ADJ pin connected to the Q pin.

2) For TLF1963TE dropout voltage will be limited by the minimum input voltage specification under some output voltage/load conditions.

3) Operating conditions are limited by maximum junction temperature. The regulated output voltage specification will not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current range must be limited. When operating at maximum output current, the input voltage range must be limited.

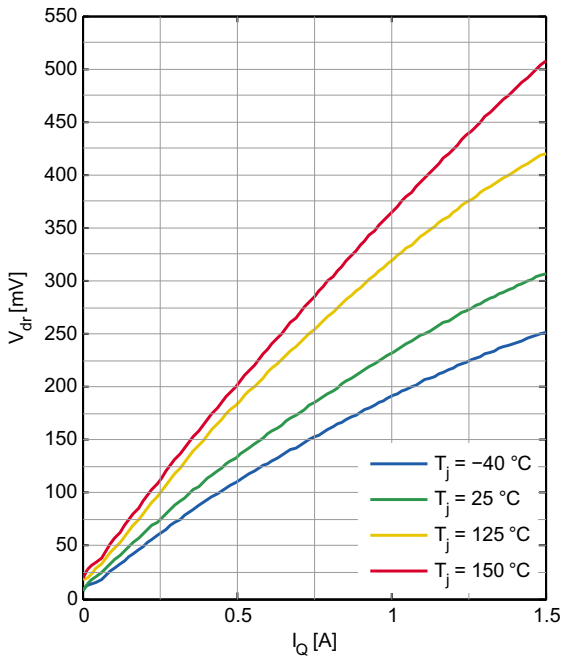
### Electrical characteristics

- 4) To satisfy requirements for minimum input voltage, the TLF1963TE is tested and specified for these conditions with an external resistor divider (two 4.12 kΩ resistors) for an output voltage of 2.4 V. The external resistor divider will add a 300 μA DC load on the output.
- 5) Dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to:  $V_I - V_{dr}$
- 6) GND pin current is tested with  $V_I = V_{Q,nom} + 1\text{ V}$  and a current source load.
- 7) ADJ pin bias current flows into the ADJ pin.
- 8) EN pin current flows into the EN pin.
- 9) Specified by design, tested at  $T_{amb} = 25\text{ °C}$
- 10) Not subject to production test, specified by design.
- 11) Reverse output current is tested with the IN pin grounded and the Q pin forced to the rated output voltage. This current flows into the Q pin and out the GND pin

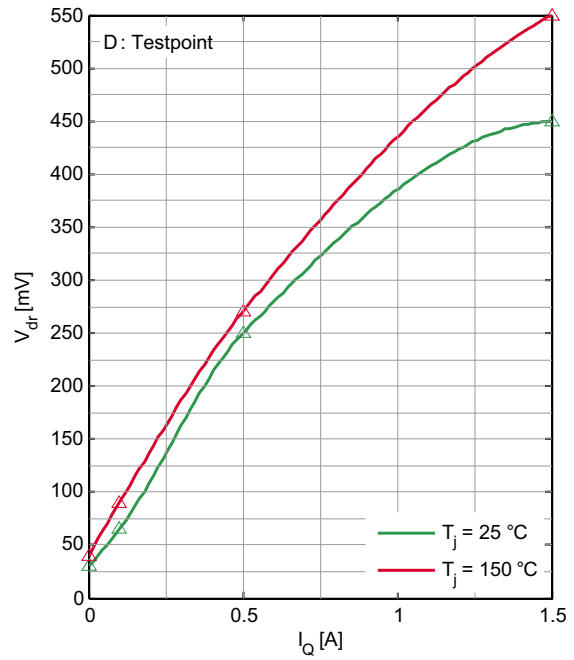
**Electrical characteristics**

**4.2 Typical performance graphs**

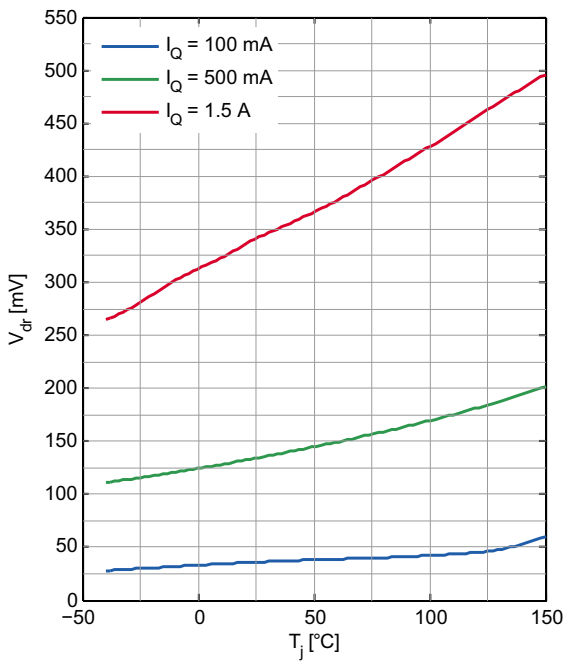
**Dropout voltage  $V_{DR}$  versus output current  $I_Q$**



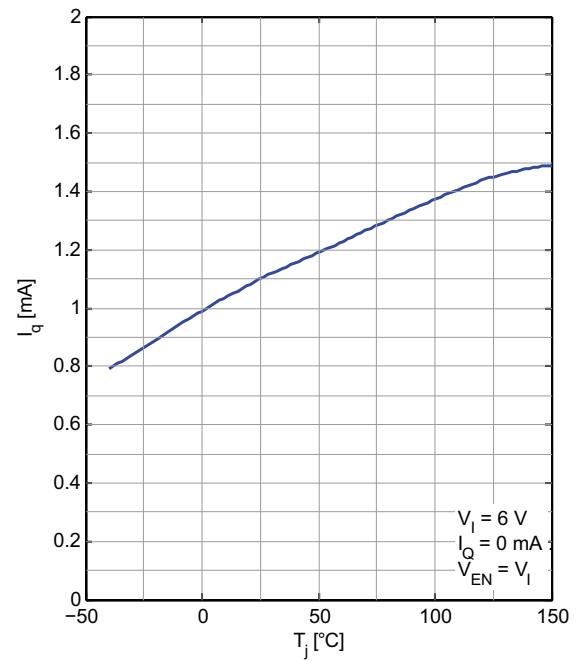
**Specified dropout voltage  $V_{dr}$  versus output current  $I_Q$**



**Dropout voltage  $V_{dr}$  versus temperature  $T_j$**

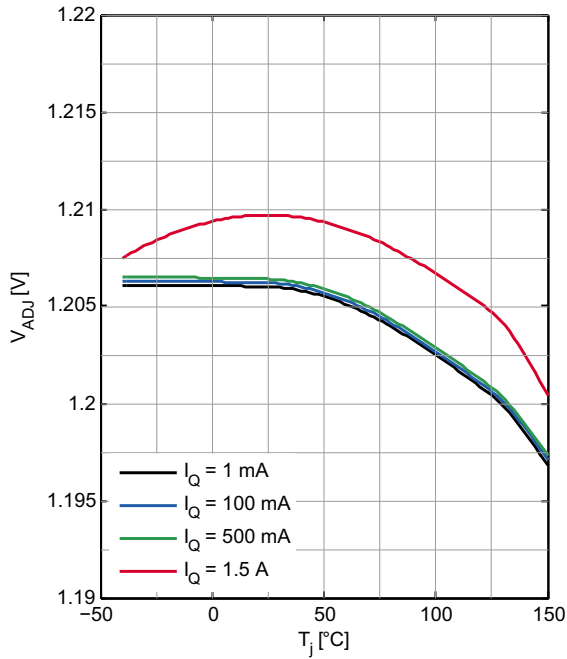


**Quiescent current  $I_q$  versus temperature  $T_j$**

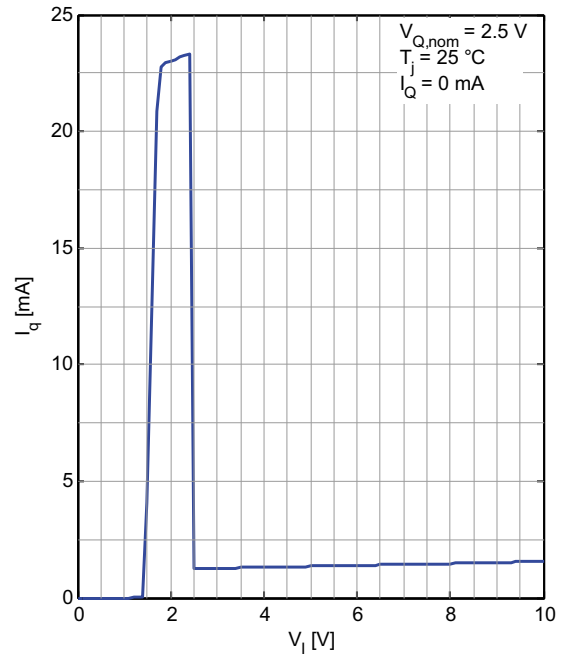


**Electrical characteristics**

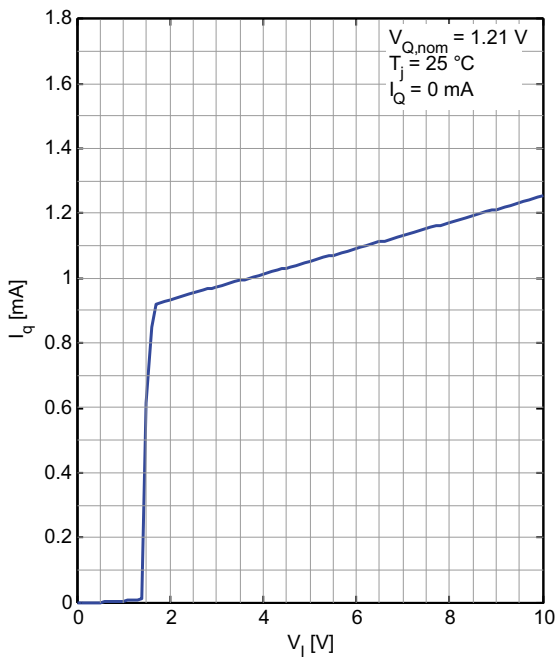
**Adjustable voltage  $V_{ADJ}$  versus temperature  $T_j$**



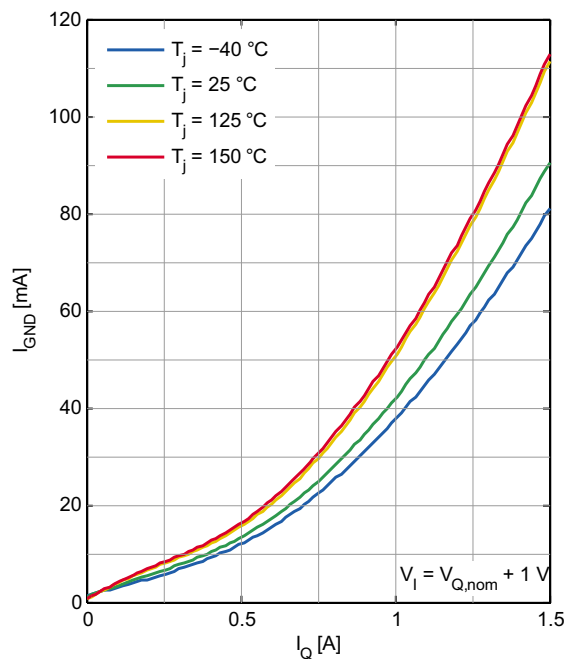
**Quiescent current  $I_q$  versus input voltage  $V_I$  ( $V_{Q,nom} = 2.5 V$ )**



**Quiescent current  $I_q$  versus input voltage  $V_I$  ( $V_{Q,nom} = 1.21 V$ )**

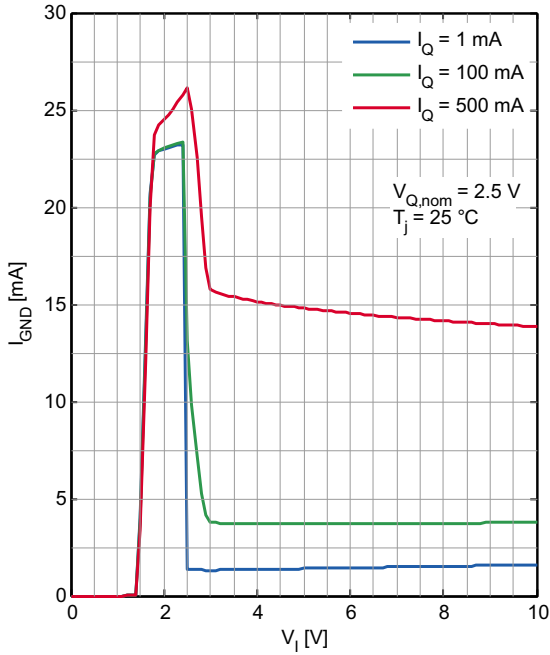


**GND Pin current  $I_{GND}$  versus output current  $I_Q$**

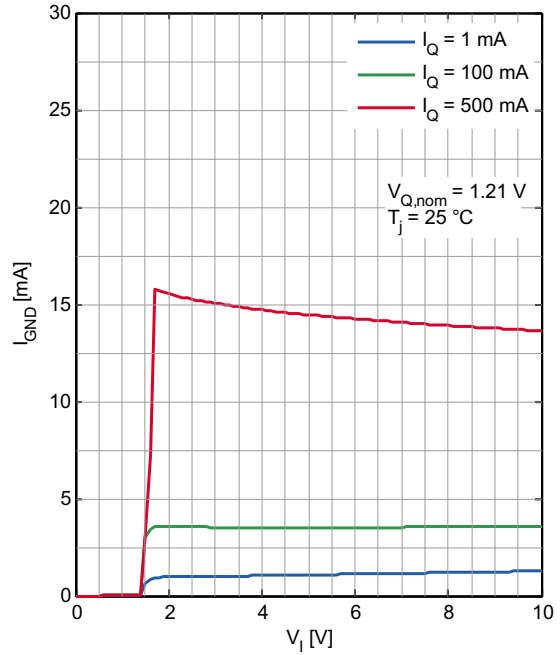


**Electrical characteristics**

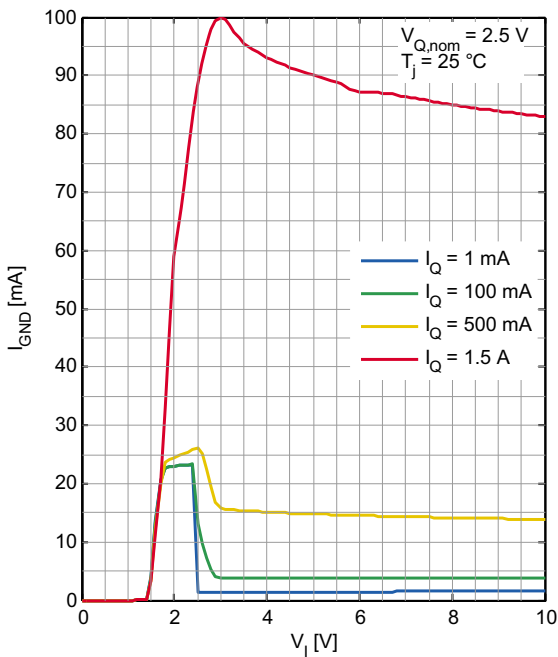
**GND pin current  $I_{GND}$  versus input voltage  $V_I$  ( $V_{Q,nom} = 2.5 V$ )**



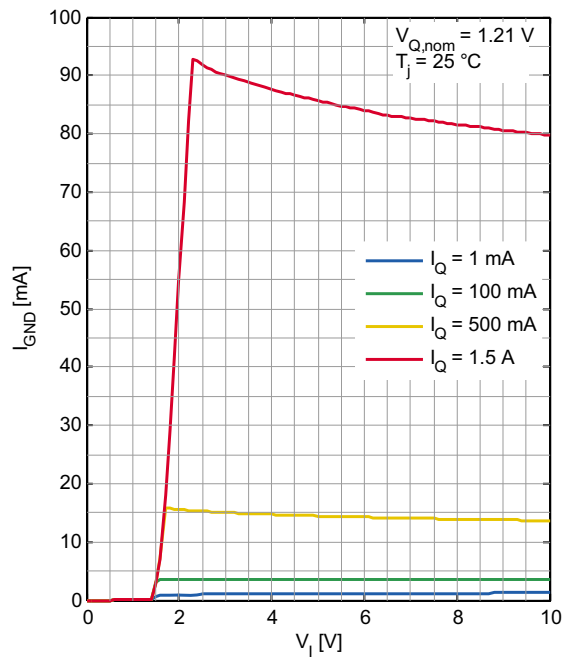
**GND pin current  $I_{GND}$  versus input voltage  $V_I$  ( $V_{Q,nom} = 1.21 V$ )**



**GND pin current  $I_{GND}$  versus input voltage  $V_I$  ( $V_{Q,nom} = 2.5 V$ )**

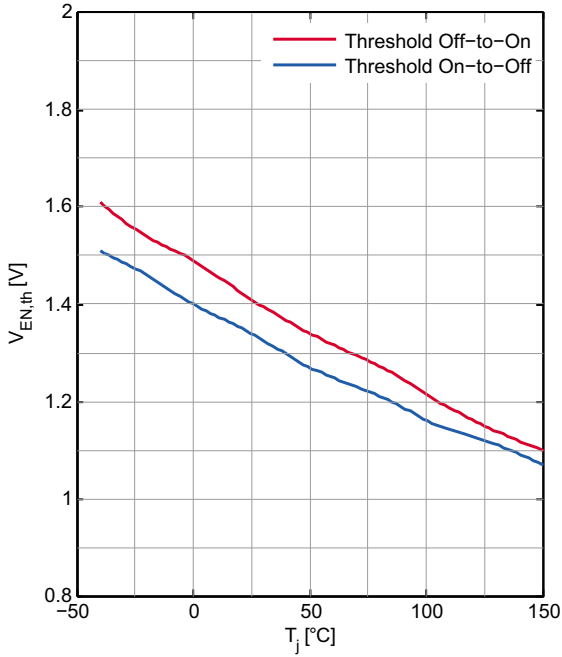


**GND pin current  $I_{GND}$  versus input voltage  $V_I$  ( $V_{Q,nom} = 1.21 V$ )**

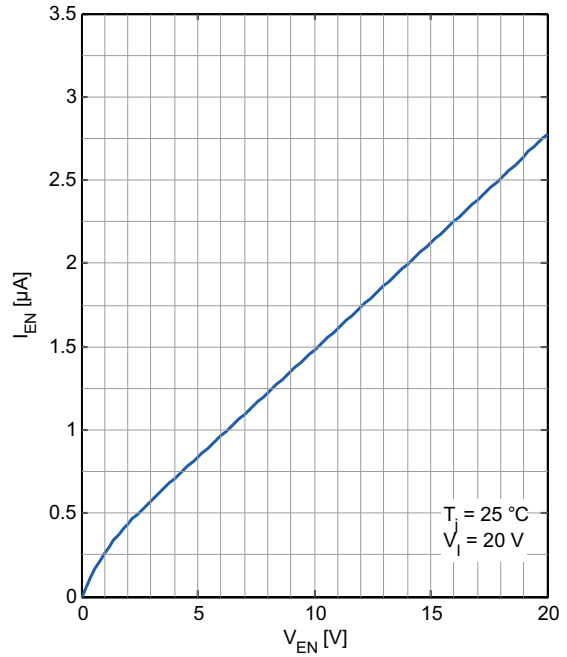


**Electrical characteristics**

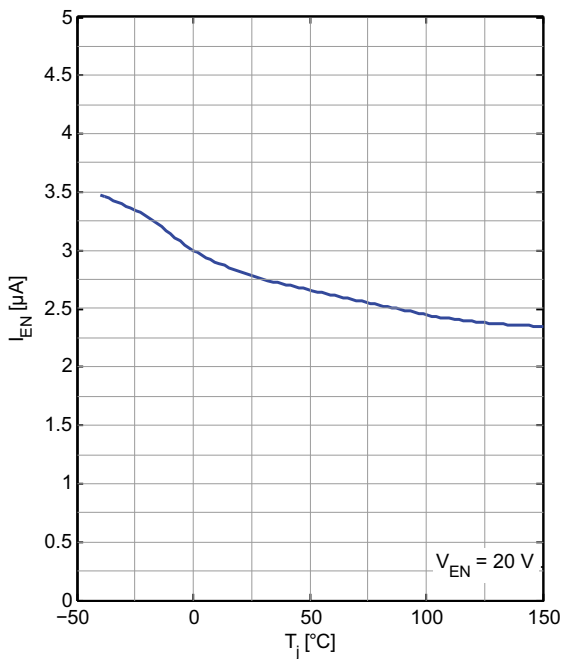
**EN pin thresholds  $V_{EN,th}$  versus temperature  $T_j$**



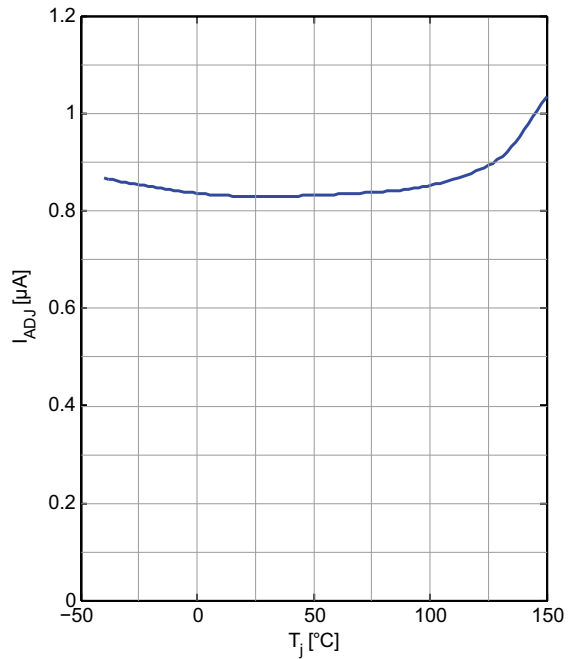
**EN pin input current  $I_{EN}$  versus EN pin voltage  $V_{EN}$**



**EN pin input current  $I_{EN}$  versus temperature  $T_j$**

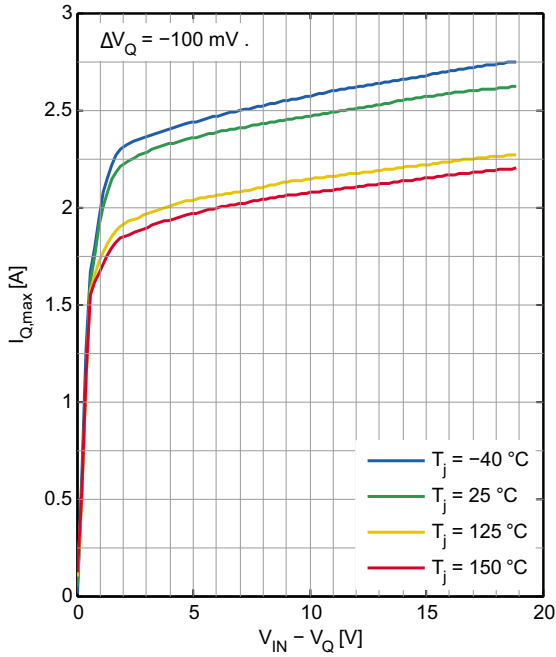


**Adjustable pin bias current  $I_{ADJ}$  versus temperature  $T_j$**

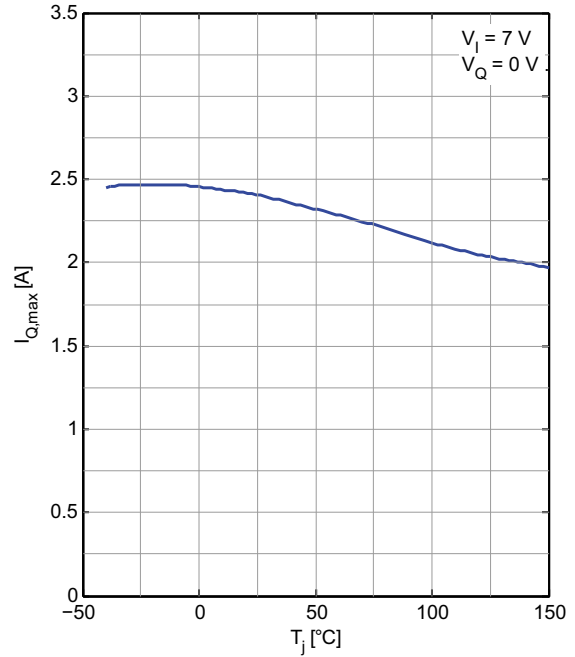


**Electrical characteristics**

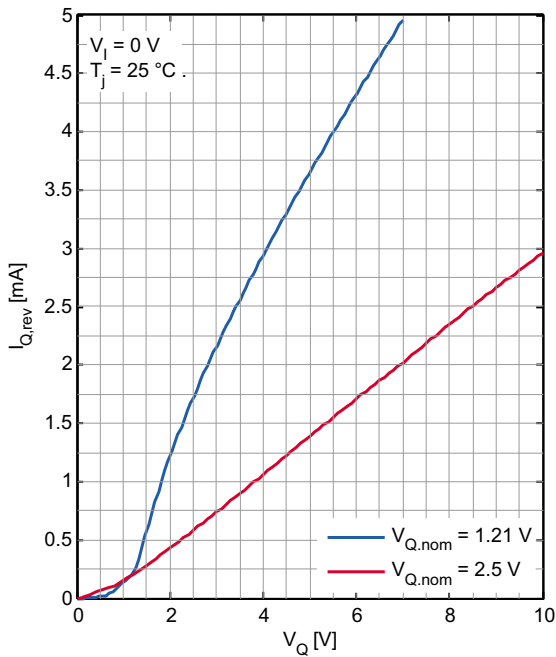
**Current limit  $I_{Q,max}$  versus input / output differential  $V_{IN} - V_Q$**



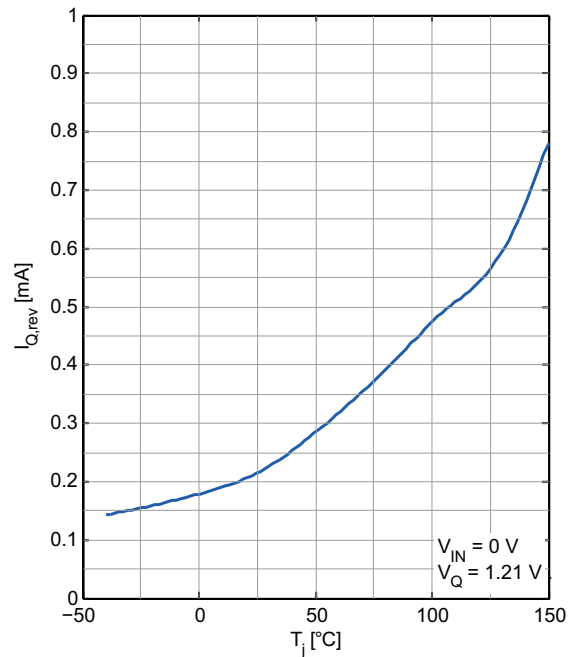
**Current limit  $I_{Q,max}$  versus temperature  $T_j$**



**Reverse output current  $I_{Q,rev}$  versus output voltage  $V_Q$**

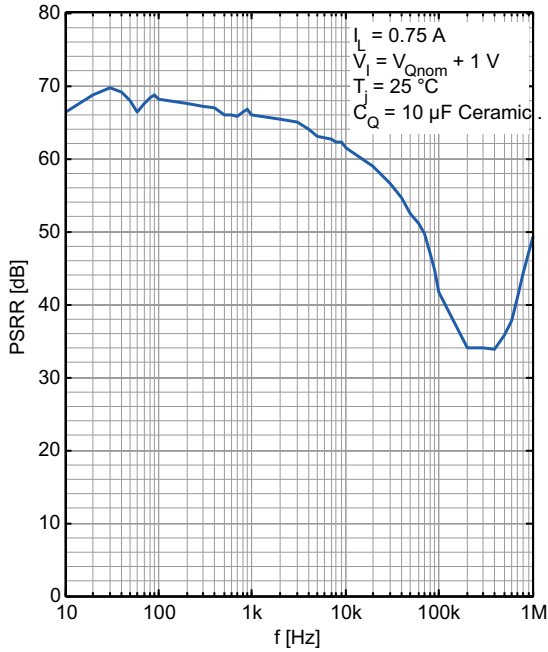


**Reverse output current  $I_{Q,rev}$  versus temperature  $T_j$**

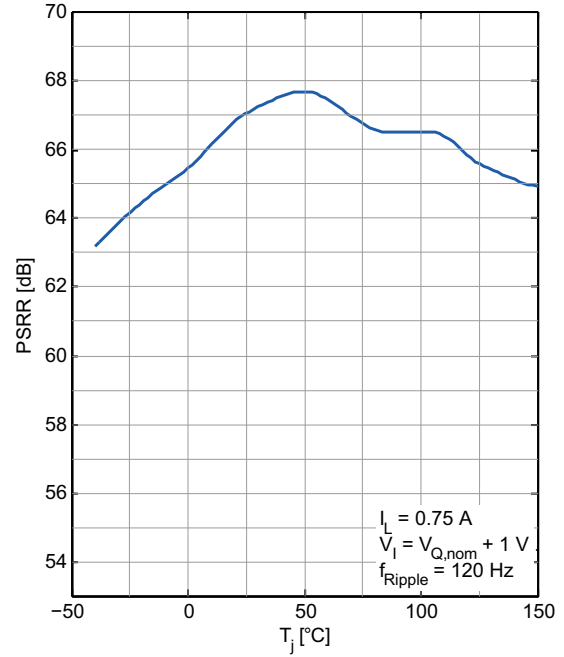


**Electrical characteristics**

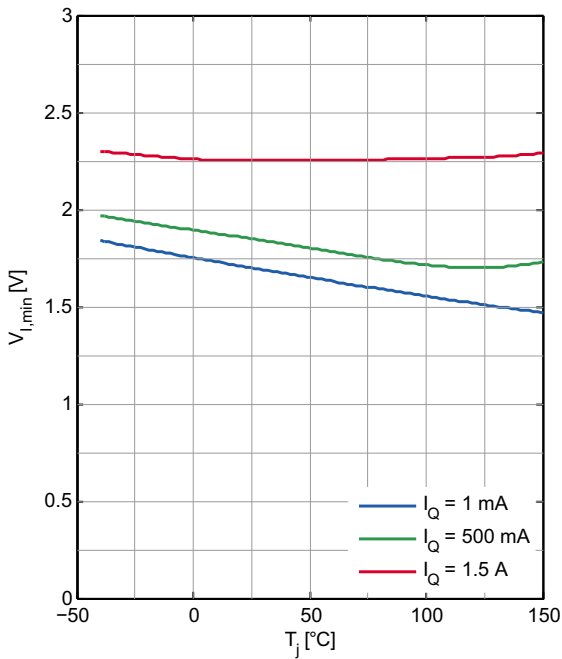
**Ripple rejection PSRR versus frequency  $f$**



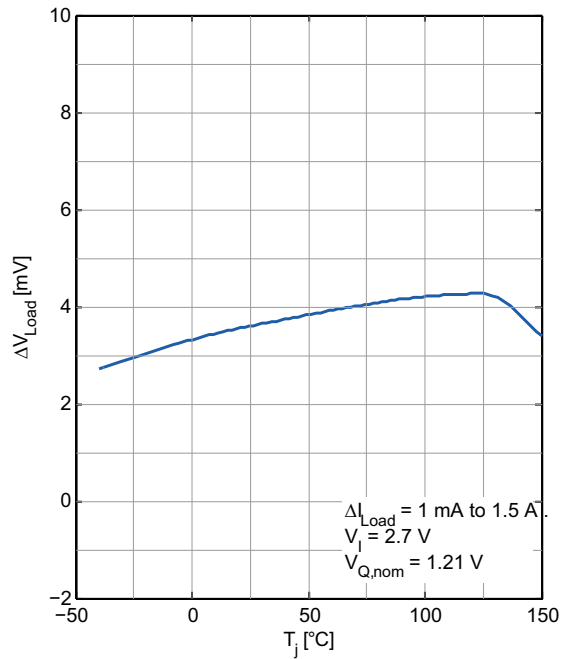
**Ripple rejection PSRR versus temperature  $T_j$**



**Minimum input voltage  $V_{I,min}$  versus temperature  $T_j$**



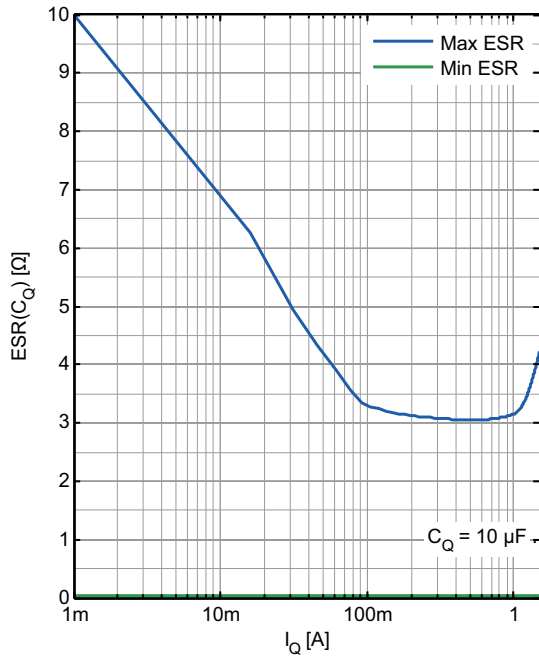
**Load regulation  $dV_{Load}$  versus temperature  $T_j$**





**Electrical characteristics**

**Equivalent series resistance  $ESR(C_Q)$  versus load current  $I_Q$**



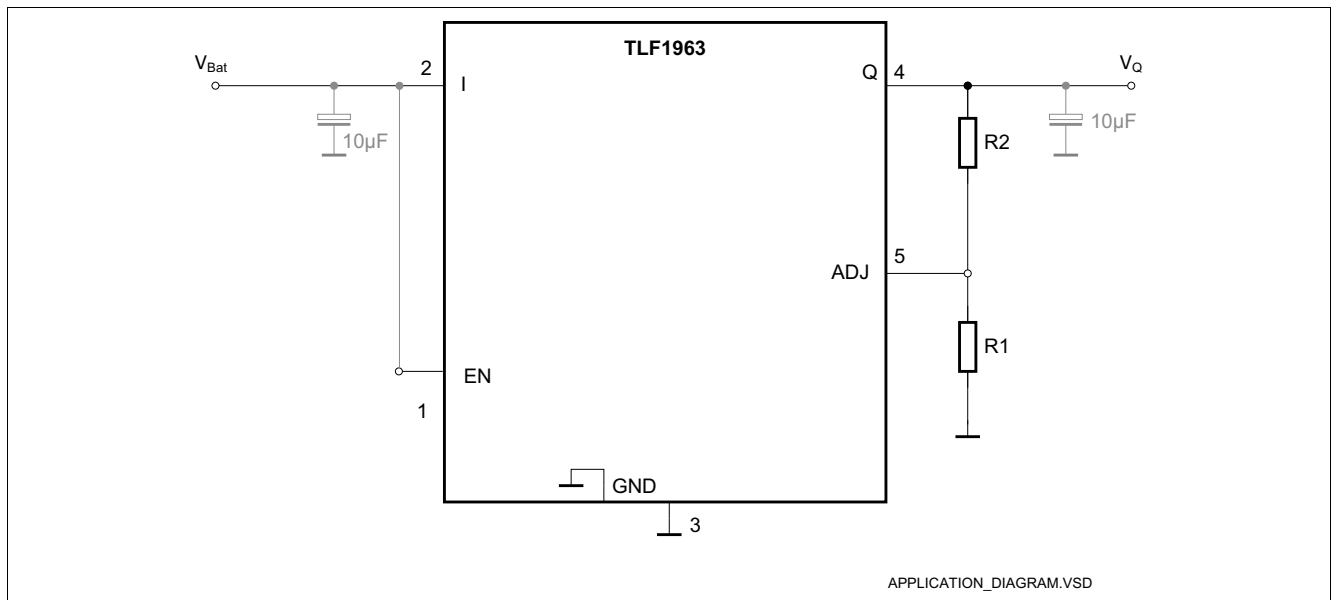
**Application information**

**5 Application information**

*Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

The TLF1963TE is an 1.5 A low dropout regulator optimized for fast transient response. The device is capable of supplying 1.5 A at a very low dropout voltage up to a junction temperature of 150 °C. The low operating quiescent current of 1 mA drops to less than 1 µA in case the device is disabled. In addition to the low quiescent current, the TLF1963TE incorporates several protection features which make them ideal for use in battery-powered systems. The device is protected against both reverse input and reverse output voltages.

*Note: This is a very simplified example of an application circuit. The function must be verified in the real application.*



**Figure 3 Application Diagram**

**5.1 Adjustable operation**

The TLF1963TE has an output voltage range of 1.21 V to  $V_I - V_{dr} < 20$  V. The output voltage is set by the ratio of two external resistors as shown in **Figure 3**. The device serves the output to maintain the voltage at the ADJ pin at 1.21 V referenced to ground. The current in R1 is then equal to  $1.21 \text{ V} / R_1$  and the current in R2 is the current in R1 plus the ADJ pin bias current. The ADJ pin bias current, 1 µA at 25 °C, flows through R2 into the ADJ pin. The output voltage can be calculated using the formula in **Equation (5.1)**.

(5.1)

$$V_Q = V_{ADJ} \cdot \left(1 + \frac{R_2}{R_1}\right) + I_{ADJ} \cdot R_2$$

$V_{ADJ} = 1.21 \text{ V typical}$

$I_{ADJ} = 1 \text{ µA at } 25 \text{ °C}$

The value of R1 is recommended to be smaller than 12 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. Note that in shutdown the output is turned off and the divider current will be zero.

## Application information

The adjustable device is mainly tested and specified with the ADJ pin connected to the Q pin for an output voltage of 1.21 V. Specifications for output voltages adjusted to greater values than 1.21 V will be proportional to the ratio of the desired output voltage to 1.21 V. For example, load regulation for an output current change of 1 mA to 1.5 A is  $\Delta V_{Q,load} = 2 \text{ mV}$  typical at  $V_{Q,nom} = 1.21 \text{ V}$ .

At  $V_{Q,nom} = 5 \text{ V}$ , load regulation is:  $\Delta V_{Qload,5V} = (5 \text{ V} / 1.21 \text{ V}) \times (2 \text{ mV}) = 8.3 \text{ mV}$

### 5.2 Output capacitance and transient response

The TLF1963TE is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 10  $\mu\text{F}$  with an ESR in the range of 10 m $\Omega$  to 3  $\Omega$  is recommended to prevent oscillations. Larger values of output capacitance can decrease the peak deviations and provide improved transient response for larger load current changes.

### 5.3 Overload recovery

The TLF1963TE has a safe operating area protection. The device protects itself by limiting the output current to a maximum and prevent it self against destruction due to overload or short circuits conditions. In this cases the current is limited and the resulting output voltage decreases according to the load down to 0V in a short circuit condition.

The TLF1963TE can supply the application for all input voltages between 2.5 V up to 20V with currents up to 1.5 A. Of course it needs to be ensured, that the junction temperature stays within the operating range up to 150 °C. For startup conditions with a high load current the TLF1963TE is able to start up properly without exceeding the safe operating area. Even immediately after removal of a short circuit failure case the device is able to start if the load current is very high. The characteristic of the current limitation can be seen in the typical performance graphs on [Page 15](#).

### 5.4 Output voltage noise

The TLF1963TE has been designed to provide low output voltage noise over the 10 Hz to 100 kHz bandwidth while operating at full load. Output voltage noise is typically 40  $\mu\text{V}_{\text{RMS}}$  over this frequency bandwidth. For higher output voltages (generated by using a resistor divider), the output voltage noise will be gained up accordingly.

Higher values of output voltage noise may be measured when care is not exercised with regards to circuit layout and testing. Crosstalk from nearby traces can induce unwanted noise onto the output of the TLF1963TE. Power supply ripple rejection must also be considered, because the TLF1963TE does not have unlimited power supply ripple rejection and will pass a small portion of the input noise through to the output.

### 5.5 Protection features

The TLF1963TE has several protection features which makes him ideal for use in battery-powered circuits. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device is protected against reverse input voltages and reverse output voltages.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation, the junction temperature should not exceed 150 °C.

The input of the device will withstand reverse voltages of 20 V. Current flow out of the device will be limited to less than 2 mA in case of an input voltage of -20 V at the Input and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries that can be plugged in backward.

## **Application information**

The output of the TLF1963TE can be pulled below ground without damaging the device. If the input is left open circuit or grounded, the output can be pulled below ground by 20 V. The output will act like an open circuit, no current will flow out of the pin. If the input is powered by a voltage source, the output will source the short-circuit current of the device and will protect itself by thermal limiting. In this case, grounding the EN pin will turn off the device and stop the output from sourcing the short-circuit current.

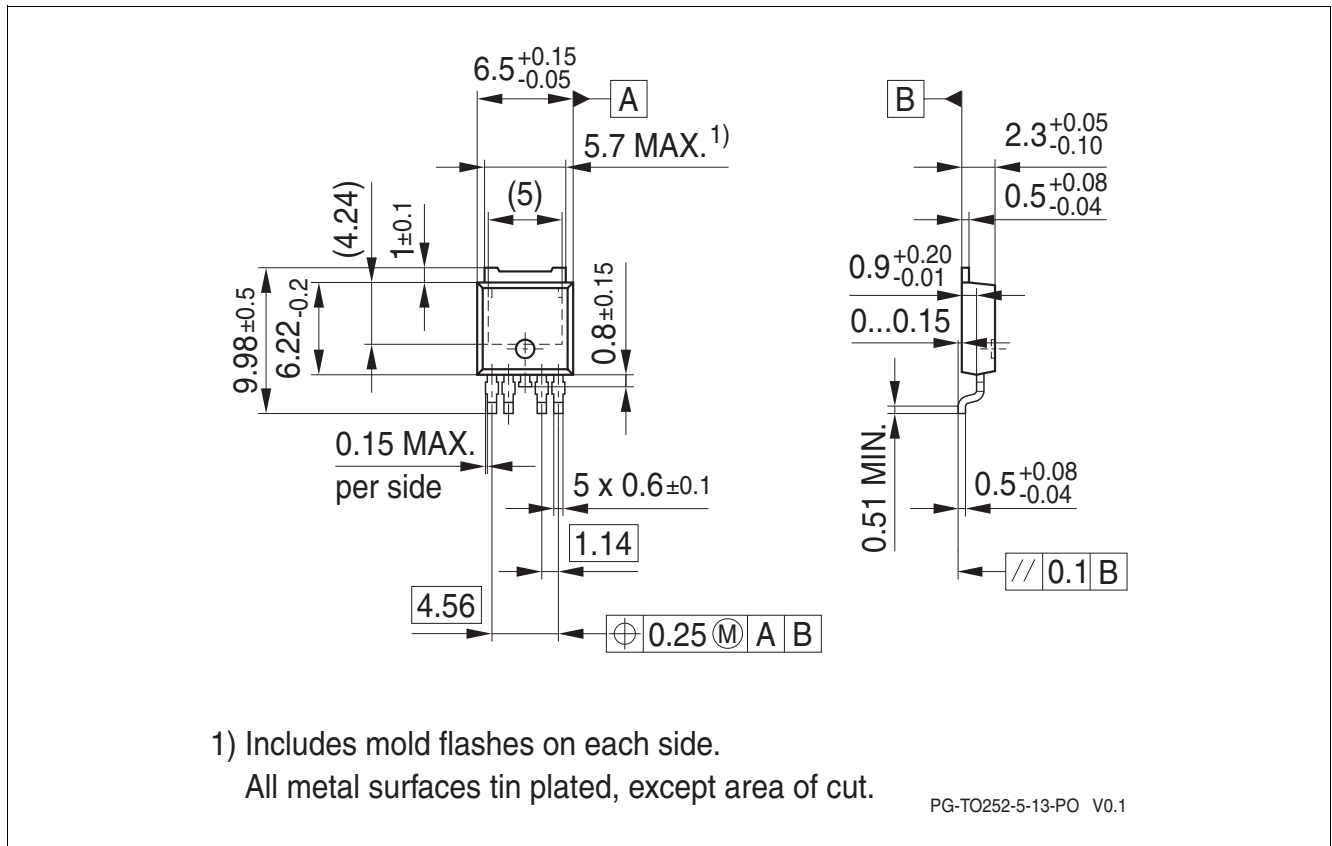
The ADJ pin of the adjustable device can be pulled above or below ground by as much as 7 V without damaging the device. If the input is left open circuit or grounded, the ADJ pin will act like an open circuit when pulled below ground and like a resistor (typically 4 k $\Omega$ ) in series with a diode when pulled above ground.

In situations where the ADJ pin is connected to a resistor divider that would pull the ADJ pin above its 7 V clamp voltage if the output is pulled high, the ADJ pin input current must be limited to less than 5 mA. For example, a resistor divider is used to provide a regulated 1.5V output from the 1.21 V reference when the output is forced to 20 V. The top resistor of the resistor divider must be chosen to limit the current into the ADJ pin to less than 5 mA when the ADJ pin is at 7 V. The 13 V difference between Q and ADJ pins divided by the 5 mA maximum current into the ADJ pin yields a minimum top resistor value of 2.6 k $\Omega$ .

## **5.6 Further application information**

For further information you may contact <https://www.infineon.com>.

## 6 Package information



**Figure 4** PG-T0252-5<sup>1)</sup>

### Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a Green Product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

<https://www.infineon.com/packages>

1) Dimensions in mm

**Revision history**

## **7 Revision history**

<b>Revision</b>	<b>Date</b>	<b>Changes</b>
Rev. 1.01	2024-11-29	Editorial changes and template update Removal of discontinued TLF1963TB (PG-TO263-5 package option)
Rev. 1.0	2012-11-08	Initial version

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