TLE986xQX Family - BF and UH steps
TLE987xQX Family - BF and UH steps

Overview

This document lists the errata of the TLE986xQX family and the TLE987xQX family.

It is strongly recommended that the device behavior and possible proposed workarounds are considered for the application.

Referenced documents:

Table 1 Reference documents

Document type	Document reference	Issue date
Datasheet	See Table 2	
User Manual	Infineon-TLE986x-UM-v01_70-EN.pdf	2022-03-11
User Manual	Infineon-TLE987x-UM-v01_70-EN.pdf	2022-03-11
BootROM User Manual	Infineon-TLE986x_TLE987x-BootROM-UM-v01_70-EN.pdf	2022-03-21

Affected products, BF and UH steps only:

Table 2 List of affected products

Device	Reference datasheet	Issue date
TLE9861QXA20	Infineon-TLE9861QXA20-DS-v02_00-EN.pdf	2022-04-14
TLE9867QXA20	Infineon-TLE9867QXA20-DS-v02_00-EN.pdf	2022-04-14
TLE9867QXA40	Infineon-TLE9867QXA40-DS-v02_00-EN.pdf	2022-04-14
TLE9867QXW20	Infineon-TLE9867QXW20-DS-v02_00-EN.pdf	2022-04-14
TLE9868QXB20	Infineon-TLE9868QXB20-DS-v02_00-EN.pdf	2022-04-14
TLE9869QXA20	Infineon-TLE9869QXA20-DS-v02_00-EN.pdf	2022-04-14
TLE9871QXA20	Infineon-TLE9871QXA20-DS-v02_00-EN.pdf	2022-04-14
TLE9873QXW40	Infineon-TLE9873QXW40-DS-v02_00-EN.pdf	2022-04-14
TLE9877QXA40	Infineon-TLE9877QXA40-DS-v02_00-EN.pdf	2022-04-14
TLE9877QXW40	Infineon-TLE9877QXW40-DS-v02_00-EN.pdf	2022-04-14
TLE9879QXA40	Infineon-TLE9879QXA40-DS-v02_00-EN.pdf	2022-04-14
TLE9879QXW40	Infineon-TLE9879QXW40-DS-v02_00-EN.pdf	2022-04-14
TLE9879-2QXA40	Infineon-TLE9879_2QXA40-DS-v02_00-EN.pdf	2022-04-14

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1 Product errata

This chapter lists the errata of the referenced products and documentation.

1.1 PORT2 CTRAP active level (0000057330-1)

Specified

In the “Port 2 Input Functions” table the P2.3 - CTRAP#_1 alternate function is specified to be a high-active input.

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.1	Input	GPI	P2_DATA.P1	
		INP1	CCPOS0_0	CCU6
		INP2	T5INB	GPT12T5
		INP3	T12HR_1	CCU6
		INP4	T5EUDB	GPT12T5
		INP5	CC61_1	CCU6
		ANALOG	AN1	ADC
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	T3IND	GPT12T3
		INP3	CTRAP#_1	CCU6
		INP4	T21EX_2	Timer 21
		INP5	CC60_1	CCU6
		INP6	EXINT0_3	SCU
		ANALOG	AN3	ADC

Figure 1 Extraction from Table 10, specified

Implemented

The P2.3 - CTRAP#_1 alternate function is implemented to be low-active.

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.1	Input	GPI	P2_DATA.P1	
		INP1	CCPOS0_0	CCU6
		INP2	T5INB	GPT12T5
		INP3	T12HR_1	CCU6
		INP4	T5EUDB	GPT12T5
		INP5	CC61_1	CCU6
		ANALOG	AN1	ADC
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	T3IND	GPT12T3
		INP3	$\overline{\text{CTRAP\#\_1}}$	CCU6
		INP4	T21EX_2	Timer 21
		INP5	CC60_1	CCU6
		INP6	EXINT0_3	SCU
		ANALOG	AN3	ADC

Figure 2 Extraction from Table 10, implemented

1.1.1 Planned fixes

Fix with next user documentation update.

1.2 RESET pin pull-up (0000057330-4)

Specified

Figure 3 shows an extraction of Table 2 of the “Pin Definitions and Functions”. The column “Reset State” defines the state of the pin in the reset condition of the device.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function
RESET	22	I/O	–	Reset input, not available during Sleep Mode

Figure 3 Extraction of Table 2, specified RESET pin conditions

Implemented

Figure 4 shows an extraction of Table 2 of the “Pin Definitions and Functions”. In the device reset condition the RESET pin is either being pulled low from external or driven low from internal, the device furthermore implements an internal pull-up which prevents the RESET pin from floating.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function
RESET	22	I/O	PU	Reset input, not available during Sleep Mode

Figure 4 Extraction of Table 2, implemented RESET pin conditions

1.2.1 Planned fixes

Fix with next user documentation update.

1.3 BootROM USER_ERASE_SECTOR, USER_ERASEPG, and USER_PROG (0000062134-25)

Scope

This erratum applies only to UH steps.

Implemented

The USER_ERASE_SECTOR, USER_ERASEPG, and USER_PROG routines make use of the RAM byte at 0x18000014. Any data being stored there is overwritten.

1.3.1 Workaround

The user code must not use the RAM location 0x18000014.

1.3.2 Planned fixes

Fix to be implemented in the next design step.

2 Latest documentation information

This chapter provides extended information on referenced documentation.

2.1 ADC1 accuracy (0000057330-8)

The accuracies stated include the ADC1 total unadjusted error (TUE_{10B}) which includes the V_{AREF} tolerance. This applies to the following specification items:

- P_8.1.39
- P_8.1.71
- P_8.1.74
- P_8.1.77[1)]
- P_8.1.78[1)]
- P_8.1.80[1)]

2.2 ADC2 accuracy (0000057330-9)

The accuracies stated include the following tolerance:

- ADC2 offset error - P_8.3.19
- ADC2 gain error - P_8.3.20
- ADC2 differential non-linearity error - P_8.3.28[1)]
- ADC2 integral non-linearity error - P_8.3.29[1)]
- V_{BG} - P_8.3.1

This applies to the following specification items:

- P_8.1.70
- P_8.1.73
- P_8.1.44
- P_8.1.47
- P_8.1.62
- P_8.1.68
- P_8.1.5
- P_8.1.48
- P_8.1.6
- P_8.2.5
- P_8.2.6
- P_8.2.7
- P_8.1.75[1)]

2.3 DC parameters of Port 0, Port 1, TMS and Reset (0000057330-11)

Table 31 in the referenced datasheet applies as well to TMS and Reset.

1) Applies to Grade 0 devices only.

3 Revision history

Revision	Date	Changes
1.0	2017-05-17	Errata obsolete
1.1	2018-05-02	Errata obsolete
		ADC1 Accuracy Addendum
		ADC2 Accuracy Addendum
1.2	2019-09-17	BootROM - USER_NVM_ECC_CHECK (0000048454-124) added
		PORT2 CTRAP active level (0000057330-1) added
		CPU->SHPR2 wrong address (0000057330-2) added
		MON wake-up/monitoring threshold voltage (0000048438-7) added
		SCU->OSC_CON Bit5 (0000057330-3) added
		RESET pin pull-up (0000057330-4) added
		Operation amplifier (0000057330-10) added
		DC parameters of Port 0, Port 1, TMS and Reset (0000057330-11) added
		ADC1 accuracy (0000057330-8) added
		ADC2 accuracy (0000057330-9) added
1.3	2022-06-03	BootROM - USER_NVM_ECC_CHECK (0000048454-124) obsolete
		CPU->SHPR2 wrong address (0000057330-2) obsolete
		MON wake-up/monitoring threshold voltage (0000048438-7) obsolete
		SCU->OSC_CON Bit5 (0000057330-3) obsolete
		BootROM USER_ERASE_SECTOR, USER_ERASEPG, and USER_PROG (0000062134-25) added
		Operational amplifier (0000057330-10) obsolete

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