TLE986xQX Family - BE-Step
TLE987xQX Family - BE-Step

Overview

This document lists the errata of the TLE986xQX family and the TLE987xQX family, for related products please refere to **Table 2**.

It is strongly recommended that the device behavior and possible proposed workarounds are considered for the application.

Affected Products, BE-Step only:

Reference User Manuals:

Table 1 Reference Documents

Document type	Document reference	Issue Date
Data Sheet	see Table 2	
User Manual	TLE986xQX-Users-Manual-14-Infineon.pdf	2019-02-26
User Manual	TLE987xQX-Users-Manual-14-Infineon.pdf	2018-08-03
BootROM User Manual	TLE986xQX-BootROM-User-Manual-13-Infineon.pdf	2015-07-10
BootROM User Manual	TLE987xQX-BootROM-User-Manual-13-Infineon.pdf	2015-07-10

Table 2 List of affected products

Device	Reference Data Sheet	Issue Date
TLE9861QXA20	TLE9861QXA20-Data-Sheet-10-Infineon.pdf	2015-04-30
TLE9867QXA20	TLE9867QXA20-Data-Sheet-10-Infineon.pdf	2015-04-30
TLE9867QXA40	TLE9867QXA40-Data-Sheet-10-Infineon.pdf	2015-04-30
TLE9869QXA20	TLE9869QXA20-Data-Sheet-10-Infineon.pdf	2015-04-30
TLE9871QXA20	TLE9871QXA20-Data-Sheet-10-Infineon.pdf	2015-04-30
TLE9877QXA20	TLE9877QXA20-Data-Sheet-10-Infineon.pdf	2015-04-30
TLE9877QXA40	TLE9877QXA40-Data-Sheet-10-Infineon.pdf	2015-04-30
TLE9879QXA20	TLE9879QXA20-Data-Sheet-10-Infineon.pdf	2015-04-30
TLE9879QXA40	TLE9879QXA40-Data-Sheet-10-Infineon.pdf	2015-04-30

Table of Contents

1 BootROM - USER_NVM_ECC_CHECK (0000048454-124)

Implemented

The function USER_NVM_ECC_CHECK uses for its operation 32 bytes on the user stack plus 1 byte in user RAM at address 0x18000011, this is not clearly specified in the BootROM User Manual.

1.1 Workaround

Adjust the project IRAM settings to exclude this address from the RAM area usable by the linker. In order to maintain memory alignment a hole of four bytes, from 0x18000010 to 0x18000013 is recommended. **Figure 1** displays an example for the TLE9871QXA20. **Table 3** lists the recommended IRAM settings for each device.

Table 3 List of recommended IRAM settings per device

Device	IRAM1 Start	IRAM1 Size	IRAM2 Start	IRAM2 Size
TLE9861QXA20	0x18000014	0xBEC	0x18000000	0x10
TLE9867QXA20	0x18000014	0x17EC	0x18000000	0x10
TLE9867QXA40	0x18000014	0x17EC	0x18000000	0x10
TLE9869QXA20	0x18000014	0x17EC	0x18000000	0x10
TLE9871QXA20	0x18000014	0xBEC	0x18000000	0x10
TLE9877QXA20	0x18000014	0x17EC	0x18000000	0x10
TLE9877QXA40	0x18000014	0x17EC	0x18000000	0x10
TLE9879QXA20	0x18000014	0x17EC	0x18000000	0x10
TLE9879QXA40	0x18000014	0x17EC	0x18000000	0x10

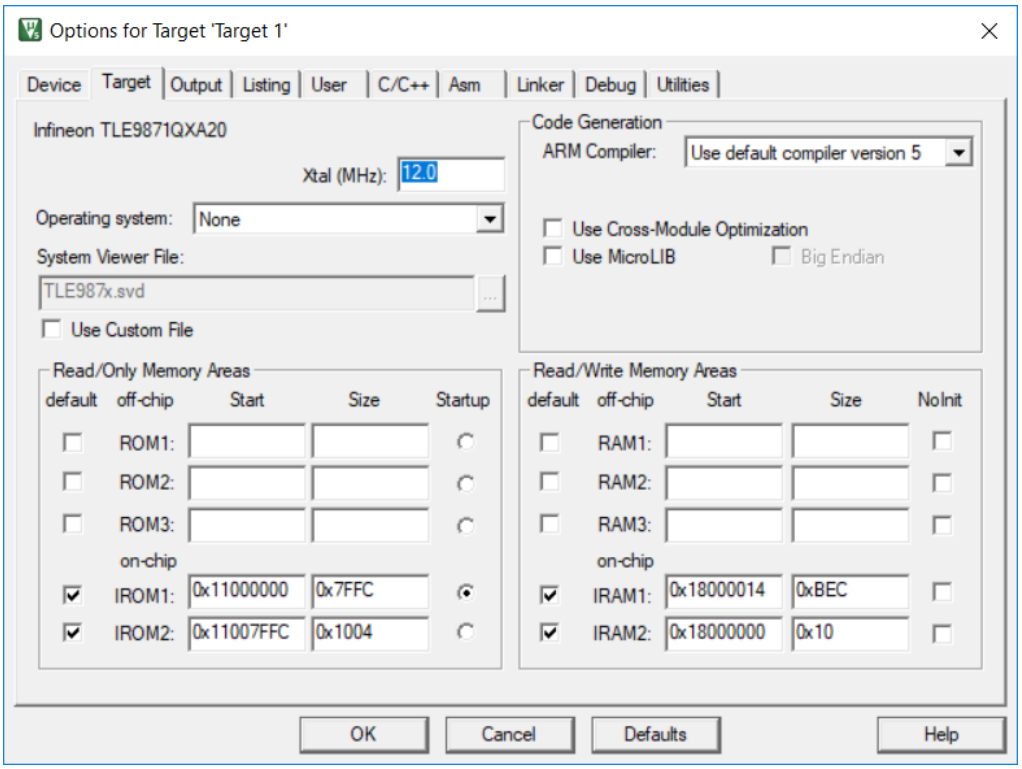


Figure 1 Example IRAM settings for the TLE9871QXA20

1.2 Planned Fixes

Fix with next user documentation update.

2 PORT2 CTRAP active level (0000057330-1)

Specified

In the Port 2 Input Function table the P2.3 - CTRAP#_1 alternate function is specified to be a high-active input.

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.1	Input	GPI	P2_DATA.P1	
		INP1	CCPOS0_0	CCU6
		INP2	T5INB	GPT12T5
		INP3	T12HR_1	CCU6
		INP4	T5EUDB	GPT12T5
		INP5	CC61_1	CCU6
		ANALOG	AN1	ADC
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	T3IND	GPT12T3
		INP3	CTRAP#_1	CCU6
		INP4	T21EX_2	Timer 21
		INP5	CC60_1	CCU6
		INP6	EXINT0_3	SCU
		ANALOG	AN3	ADC

Figure 2 Extraction from Table 10, specified

Implemented

The P2.3 - CTRAP#_1 alternate function is implemented to be low-active.

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.1	Input	GPI	P2_DATA.P1	
		INP1	CCPOS0_0	CCU6
		INP2	T5INB	GPT12T5
		INP3	T12HR_1	CCU6
		INP4	T5EUDB	GPT12T5
		INP5	CC61_1	CCU6
		ANALOG	AN1	ADC
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	T3IND	GPT12T3
		INP3	$\overline{\text{CTRAP\#\_1}}$	CCU6
		INP4	T21EX_2	Timer 21
		INP5	CC60_1	CCU6
		INP6	EXINT0_3	SCU
		ANALOG	AN3	ADC

Figure 3 Extraction from Table 10, implemented

2.1 Planned Fixes

Fix with next user documentation update.

3 CPU->SHPR2 wrong address (0000057330-2)

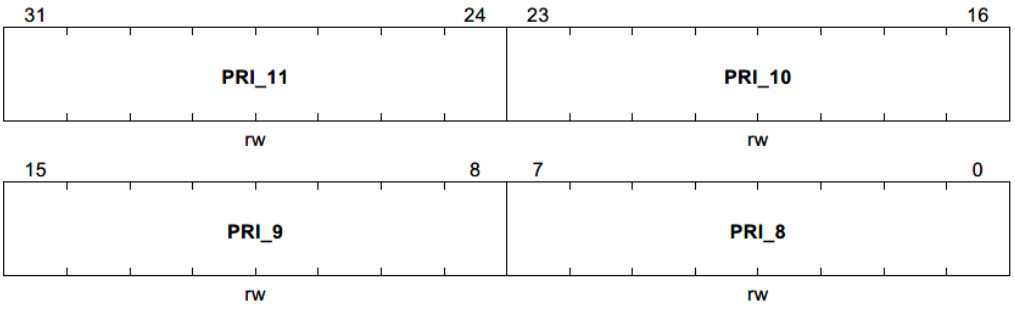
Specified

The address of the register SHPR2 is specified wrongly.

SHPR2 — **System Handler Priority Register 2**

Offset $21C_H$

Reset Value $0000\ 0000_H$



Field	Bits	Type	Description
PRI_11	31:24	rw	Priority of System Handler 11, SVCall
PRI_10	23:16	rw	Reserved for Priority of System Handler 10
PRI_9	15:8	rw	Reserved for Priority of System Handler 9
PRI_8	7:0	rw	Reserved for Priority of System Handler 8

Figure 4 Register view of specified SHPR2 register

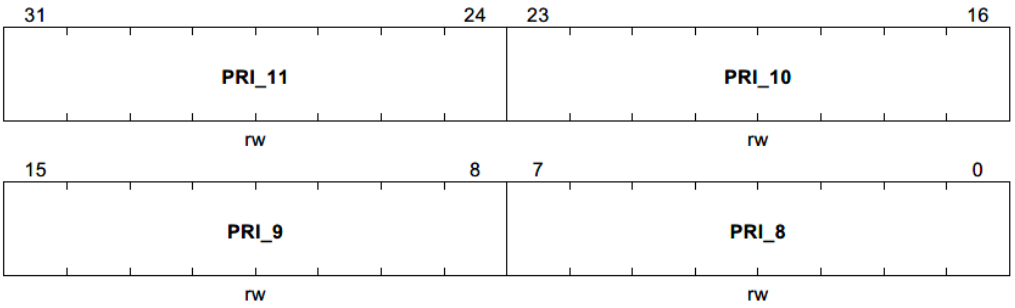
Implemented

The imlemented address for the register SHPR2 is 0xE000ED1C.

SHPR2 — **System Handler Priority Register 2**

Offset $D1C_H$

Reset Value $0000\ 0000_H$



Field	Bits	Type	Description
PRI_11	31:24	rw	Priority of System Handler 11, SVCall
PRI_10	23:16	rw	Reserved for Priority of System Handler 10
PRI_9	15:8	rw	Reserved for Priority of System Handler 9
PRI_8	7:0	rw	Reserved for Priority of System Handler 8

Figure 5 Register view of implemented SHPR2 register

3.1 Planned Fixes

Fix with next user documentation update.

4 SCU->OSC_CON Bit5 (0000057330-3)

Specified

Bit5 in the register SCU->OSC_CON is mentioned in the User Manual to be read-only with always read as '0'. Furthermore the reset value of this register upon user mode entry is declared to be 0x98.

OSC_CON
OSC Control Register **($0B0_H$)** **Reset Value: 10_H**

7	6	5	4	3	2	1	0
OSCTRIM_8	Res	Res	XPD	OSC2L	OSCWDTRST	OSCSS	
rw	r	r	rw	rh	rwh	rw	

Field	Bits	Type	Description
OSCTRIM_8	7	rw	**OSC_PLL Trim Configuration Bit [8]** This bit field enables the trimming for the OSC_PLL. User should always set this bit with any write. This bit is a protected bit. When the Protection Scheme is activated, this bit cannot be written directly. For more information on Protection Scheme, see **Section 6.12**.
Res	6	r	**Reserved** This bit field is always read as zero.
Res	5	r	**Reserved** This bit field is always read as zero.

Figure 6 Extraction of the specified OSC_CON register

Implemented

The Bit5 of the register SCU->OSC_CON is always read as '1'. In case of a write access to OSC_CON the Bit5 should remain set. The reset value upon user mode entry is 0xB8.

OSC_CON
OSC Control Register ($0B0_H$) Reset Value: 10_H

7	6	5	4	3	2	1	0
OSCTRIM_8	Res	Res	XPD	OSC2L	OSCWDTRST	OSCSS	
rw	r	rw	rw	rh	rwh	rw	

Field	Bits	Type	Description
OSCTRIM_8	7	rw	**OSC_PLL Trim Configuration Bit [8]** This bit field enables the trimming for the OSC_PLL. User should always set this bit with any write. This bit is a protected bit. When the Protection Scheme is activated, this bit cannot be written directly. For more information on Protection Scheme, see **Section 6.12**.
Res	6	r	**Reserved** This bit field is always read as zero.
Res	5	rw	**Reserved** User should always set this bit with any write. This bit is a protected bit. When the Protection Scheme is activated, this bit cannot be written directly. For more information on Protection Scheme, see **Section 6.12**.

Figure 7 Extraction of the implemented OSC_CON register

4.1 Planned Fixes

Fix with next user documentation update.

5 RESET Pin Pull-up (0000057330-4)

Specified

Figure 8 shows an extraction of Table 2 of the Pin Definitions and Functions. The column “Reset State” defines the state of the pin in the reset condition of the device.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function
RESET	22	I/O	–	Reset input, not available during Sleep Mode

Figure 8 Extraction of Table 2, specified RESET pin conditions

Implemented

Figure 9 shows an extraction of Table 2 of the Pin Definitions and Functions. In the device reset condition the RESET pin is either being pulled low from external or driven low from internal, the device furthermore implements an internal pull-up which prevents the RESET pin from floating.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function
RESET	22	I/O	PU	Reset input, not available during Sleep Mode

Figure 9 Extraction of Table 2, implemented RESET pin conditions

5.1 Planned Fixes

Fix with next user documentation update.

6 Revision History

Revision	Date	Changes
1.0	2017-05-05	Errata obsolete
1.1	2019-08-05	BootROM - USER_NVM_ECC_CHECK (0000048454-124) added
		PORT2 CTRAP active level (0000057330-1) added
		CPU->SHPR2 wrong address (0000057330-2) added
		SCU->OSC_CON Bit5 (0000057330-3) added
		RESET Pin Pull-up (0000057330-4) added

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