TLE9868QXB20 - BF-Step

Overview

This document lists the errata of the TLE9868QXB20

It is strongly recommended that the device behavior and possible proposed workarounds are considered for the application.

Referenced documents:

Table 1 Reference Documents

Document type	Document reference	Issue Date
Data Sheet	see Table 2	
User Manual	TLE9868QXB20-Users-Manual-13-Infineon.pdf	2017-07-05
BootROM User Manual	TLE986xQX-BootROM-User-Manual-14-Infineon.pdf	2016-09-22

Affected Products:

Table 2 List of affected products

Device	Reference Data Sheet	Issue Date
TLE9868QXB20	TLE9868QXB20-BF-Data-Sheet-11-Infineon.pdf	2017-06-19

Table of Contents

1 Product Errata

This chapter lists the errata of the referenced products and documentation.

1.1 Measurement Unit Overview (0000057330-5)

The **Figure 1** displays an update for the corresponding figure in the data sheet (Figure 25). The attenuator values have been replaced by the corresponding symbols described in the electrical characteristics chapter in the data sheet. The reference voltage for the ADC1 (5V) has been replaced by the symbol V_{AREF} which is specified in the electrical characteristics chapter. The reference voltage for the ADC2 (1.23V) has been replaced by the symbol V_{BG} which is specified in the electrical characteristics chapter.

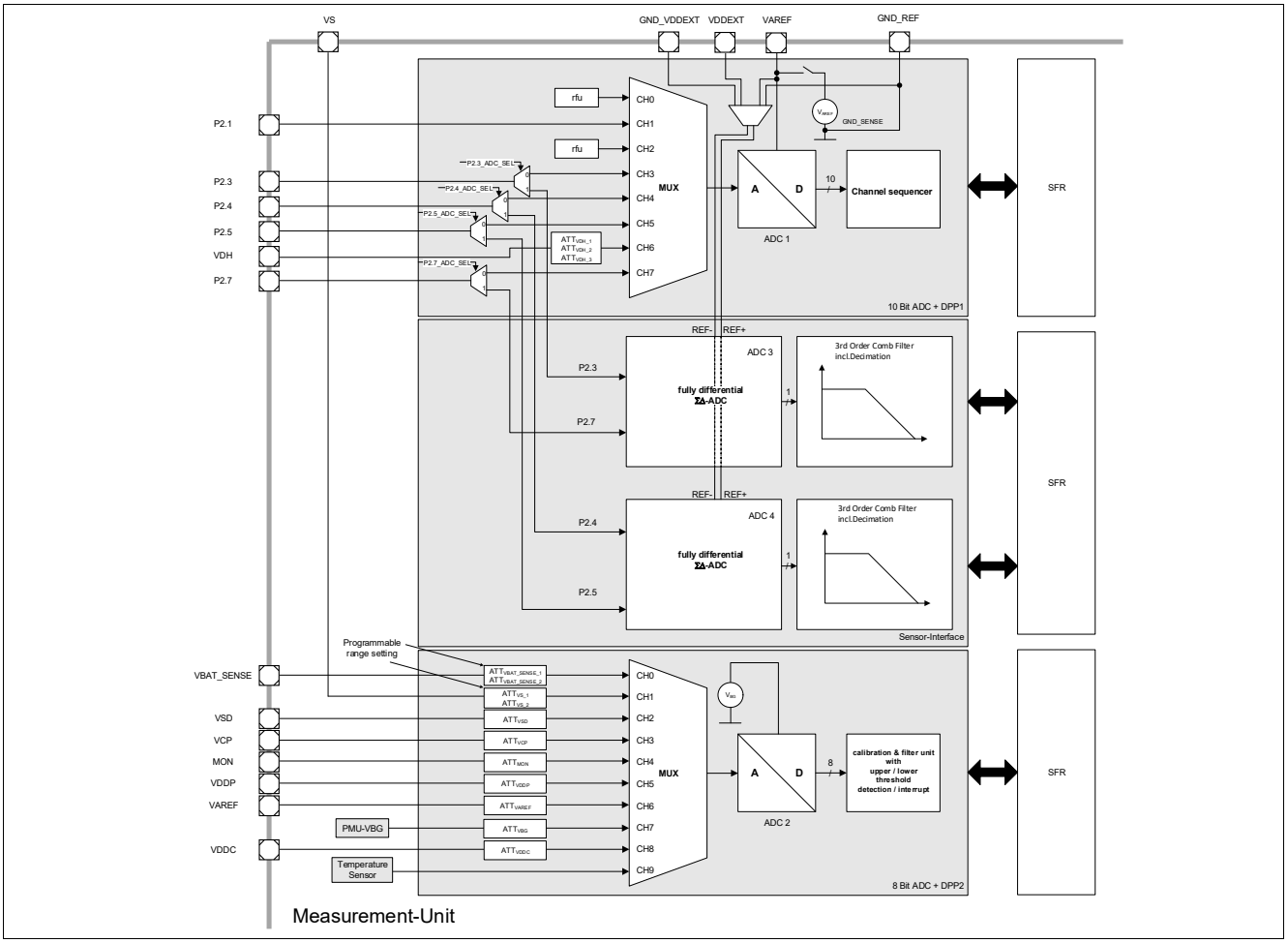

Figure 1 Measurement unit - overview for TLE9868QXB20 (DS: Figure 25)

1.1.1 Planned Fixes

Fix with next user documentation update.

1.2 External XTAL circuitry (0000057330-6)

The **Figure 2** has been updated, the frequency values, 4 - 25 MHz, for the external crystal have been replaced by the specification symbol, f_{OSC}.

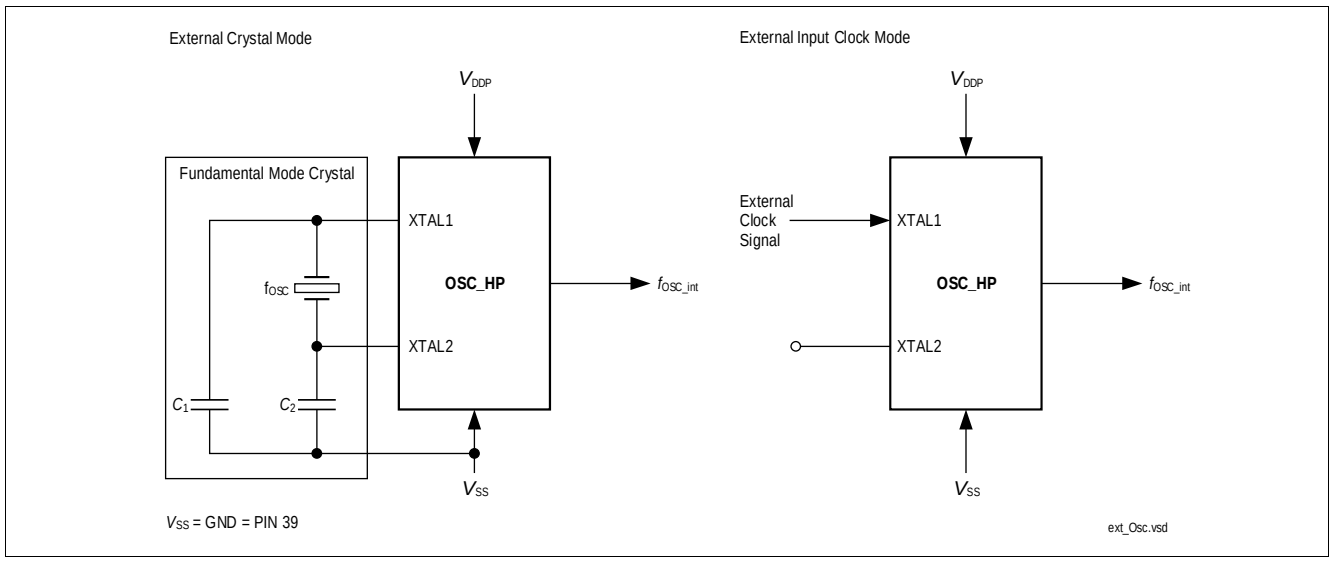

Figure 2 External XTAL circuitry (UM: Figure 21)

1.2.1 Planned Fixes

Fix with next user documentation update.

1.3 LIN internal circuitry (0000057330-7)

The **Figure 3** has been updated, the value for the device internal pullup, 30 kOhm, has been replaced by the specification symbol, R_{BUS}.

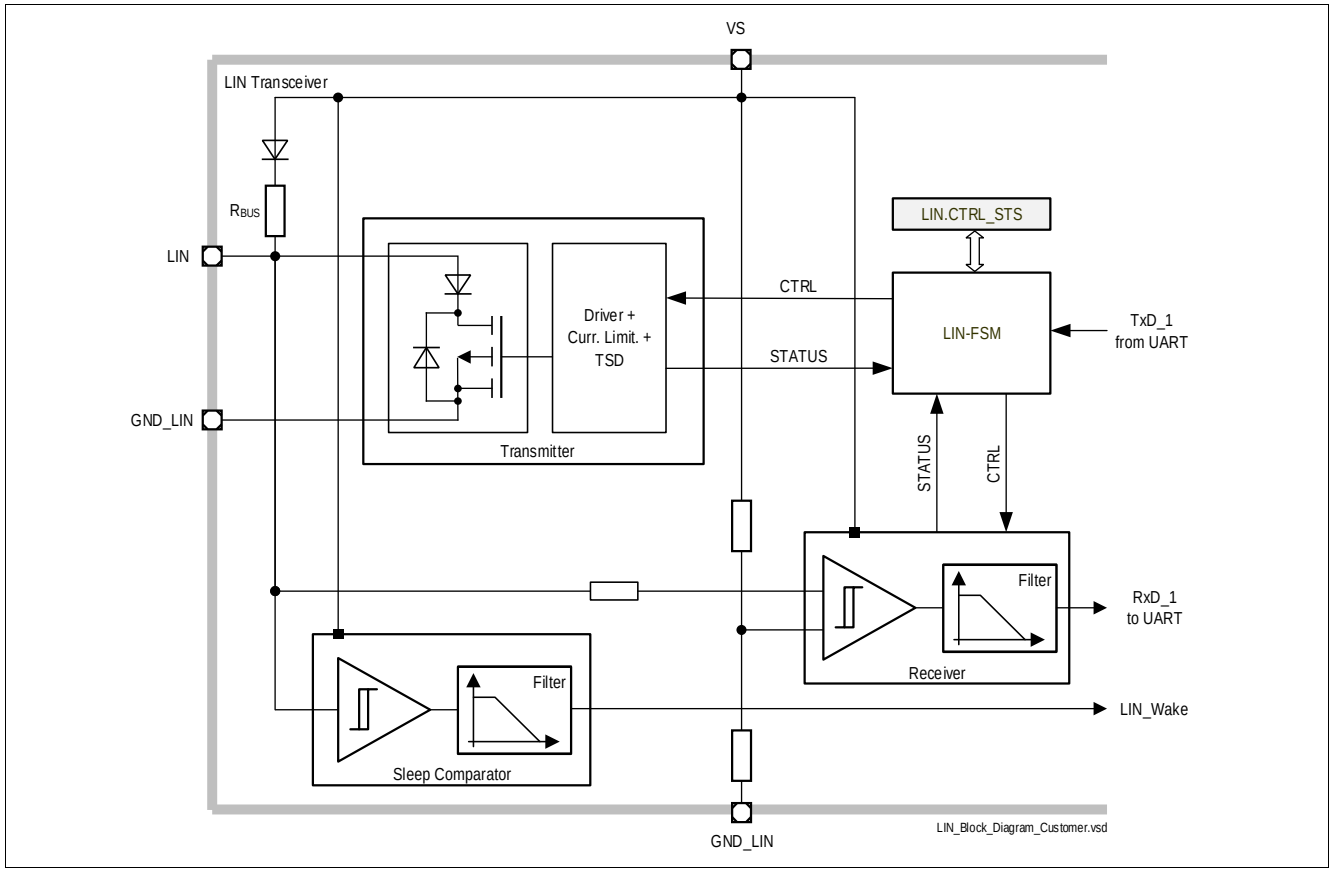

Figure 3 LIN internal circuitry (UM: Figure 174)

1.3.1 Planned Fixes

Fix with next user documentation update.

1.4 BootROM - USER_NVM_ECC_CHECK (0000048454-124)

Implemented

The function USER_NVM_ECC_CHECK uses for its operation 32 bytes on the user stack plus 1 byte in user RAM at address 0x18000015, this is not clearly specified in the BootROM User Manual.

1.4.1 Workaround

Adjust the project IRAM settings to exclude this address from the RAM area usable by the linker. In order to maintain memory alignment a hole of four bytes, from 0x18000014 to 0x18000017 is recommended. **Table 3** lists the recommended IRAM settings for each device.

Table 3 List of recommended IRAM settings per device

Device	IRAM1 Start	IRAM1 Size	IRAM2 Start	IRAM2 Size
TLE9868QXB20	0x18000018	0xFE8	0x18000000	0x14

1.4.2 Planned Fixes

Fix with next user documentation update.

1.5 PORT2 CTRAP active level (0000057330-1)

Specified

In the Port 2 Input Function table the P2.3 - CTRAP#_1 alternate function is specified to be a high-active input.

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.1	Input	GPI	P2_DATA.P1	
		INP1	CCPOS0_0	CCU6
		INP2	T5INB	GPT12T5
		INP3	T12HR_1	CCU6
		INP4	T5EUDB	GPT12T5
		INP5	CC61_1	CCU6
		ANALOG	AN1	ADC
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	T3IND	GPT12T3
		INP3	CTRAP#_1	CCU6
		INP4	T21EX_2	Timer 21
		INP5	CC60_1	CCU6
		INP6	EXINT0_3	SCU
		ANALOG	AN3	ADC

Figure 4 Extraction from Table 10, specified

Implemented

The P2.3 - CTRAP#_1 alternate function is implemented to be low-active.

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.1	Input	GPI	P2_DATA.P1	
		INP1	CCPOS0_0	CCU6
		INP2	T5INB	GPT12T5
		INP3	T12HR_1	CCU6
		INP4	T5EUDB	GPT12T5
		INP5	CC61_1	CCU6
		ANALOG	AN1	ADC
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	T3IND	GPT12T3
		INP3	$\overline{\text{CTRAP\#\_1}}$	CCU6
		INP4	T21EX_2	Timer 21
		INP5	CC60_1	CCU6
		INP6	EXINT0_3	SCU
		ANALOG	AN3	ADC

Figure 5 Extraction from Table 10, implemented

1.5.1 Planned Fixes

Fix with next user documentation update.

1.6 CPU->SHPR2 wrong address (0000057330-2)

Specified

The address of the register SHPR2 is specified wrongly.

SHPR2 — **System Handler Priority Register 2**

Offset $21C_H$

Reset Value $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI_11								PRI_10							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_9								PRI_8							
rw								rw							

Field	Bits	Type	Description
PRI_11	31:24	rw	Priority of System Handler 11, SVCall
PRI_10	23:16	rw	Reserved for Priority of System Handler 10
PRI_9	15:8	rw	Reserved for Priority of System Handler 9
PRI_8	7:0	rw	Reserved for Priority of System Handler 8

Figure 6 Register view of specified SHPR2 register

Implemented

The imlemented address for the register SHPR2 is 0xE000ED1C.

SHPR2 — **System Handler Priority Register 2**

Offset $D1C_H$

Reset Value $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRI_11								PRI_10							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRI_9								PRI_8							
rw								rw							

Field	Bits	Type	Description
PRI_11	31:24	rw	Priority of System Handler 11, SVCall
PRI_10	23:16	rw	Reserved for Priority of System Handler 10
PRI_9	15:8	rw	Reserved for Priority of System Handler 9
PRI_8	7:0	rw	Reserved for Priority of System Handler 8

Figure 7 Register view of implemented SHPR2 register

1.6.1 Planned Fixes

Fix with next user documentation update.

1.7 MON Wake-up/monitoring threshold voltage (0000048438-7)

Specified

The MON Wake-up/monitoring threshold is specified without effective temperature range.

Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_S	0.5*V_S	0.6*V_S	V	Without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s); V_S = 5.5V to 18V	P_11.1.1

Figure 8 Wake-up/Monitoring threshold voltage specified without temperature range

Implemented

The MON Wake-up/monitoring threshold is specified for a temperature range of Tj = -40°C to 85°C.

Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_S	0.5*V_S	0.6*V_S	V	Without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s); V_S = 5.5V to 18V; T_J = -40°C to 85°C	P_11.1.1

Figure 9 Wake-up/Monitoring threshold voltage specified with temperature range

1.7.1 Planned Fixes

Fix with next user documentation update.

1.8 SCU->OSC_CON Bit5 (0000057330-3)

Specified

Bit5 in the register SCU->OSC_CON is mentioned in the User Manual to be read-only with always read as ‘0’. Furthermore the reset value of this register upon user mode entry is declared to be 0x98.

OSC_CON
OSC Control Register **($0B0_H$)** **Reset Value: 10_H**

7	6	5	4	3	2	1	0
OSCTRIM_8	Res	Res	XPD	OSC2L	OSCWDTRST	OSCSS	
rw	r	r	rw	rh	rwh	rw	

Field	Bits	Type	Description
OSCTRIM_8	7	rw	**OSC_PLL Trim Configuration Bit [8]** This bit field enables the trimming for the OSC_PLL. User should always set this bit with any write. This bit is a protected bit. When the Protection Scheme is activated, this bit cannot be written directly. For more information on Protection Scheme, see **Section 6.12**.
Res	6	r	**Reserved** This bit field is always read as zero.
Res	5	r	**Reserved** This bit field is always read as zero.

Figure 10 Extraction of the specified OSC_CON register

Implemented

The Bit5 of the register SCU->OSC_CON is always read as ‘1’. In case of a write access to OSC_CON the Bit5 should remain set. The reset value upon user mode entry is 0xB8.

OSC_CON
OSC Control Register **($0B0_H$)** **Reset Value: 10_H**

7	6	5	4	3	2	1	0
OSCTRIM_8	Res	Res	XPD	OSC2L	OSCWDTRST	OSCSS	
rw	r	rw	rw	rh	rwh	rw	

Field	Bits	Type	Description
OSCTRIM_8	7	rw	**OSC_PLL Trim Configuration Bit [8]** This bit field enables the trimming for the OSC_PLL. User should always set this bit with any write. This bit is a protected bit. When the Protection Scheme is activated, this bit cannot be written directly. For more information on Protection Scheme, see **Section 6.12**.
Res	6	r	**Reserved** This bit field is always read as zero.
Res	5	rw	**Reserved** User should always set this bit with any write. This bit is a protected bit. When the Protection Scheme is activated, this bit cannot be written directly. For more information on Protection Scheme, see **Section 6.12**.

Figure 11 Extraction of the implemented OSC_CON register

1.8.1 Planned Fixes

Fix with next user documentation update.

1.9 RESET Pin Pull-up (0000057330-4)

Specified

Figure 12 shows an extraction of Table 2 of the Pin Definitions and Functions. The column “Reset State” defines the state of the pin in the reset condition of the device.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function
RESET	22	I/O	–	Reset input, not available during Sleep Mode

Figure 12 Extraction of Table 2, specified RESET pin conditions

Implemented

Figure 13 shows an extraction of Table 2 of the Pin Definitions and Functions. In the device reset condition the RESET pin is either being pulled low from external or driven low from internal, the device furthermore implements an internal pull-up which prevents the RESET pin from floating.

Table 2 Pin Definitions and Functions

Symbol	Pin Number	Type	Reset State[1)]	Function
RESET	22	I/O	PU	Reset input, not available during Sleep Mode

Figure 13 Extraction of Table 2, implemented RESET pin conditions

1.9.1 Planned Fixes

Fix with next user documentation update.

2 Latest documentation information

This chapter provides extended information on referenced documentation.

2.1 ADC1 Accuracy (0000057330-8)

The accuracies stated include the ADC1 total unadjusted error (TUE_{10B}) which includes the V_{AREF} tolerance. This applies to the following specification items:

- P_8.1.39
- P_8.1.71
- P_8.1.74

2.2 ADC2 Accuracy (0000057330-9)

The accuracies stated include the following tolerance:

- ADC2 offset error - P_8.3.19
- ADC2 gain error - P_8.3.20
- V_{BG} - P_8.3.1

This applies to the following specification items:

- P_8.1.70

- P_8.1.73
- P_8.1.44
- P_8.1.47
- P_8.1.62
- P_8.1.68
- P_8.1.5
- P_8.1.48
- P_8.1.6
- P_8.2.5
- P_8.2.6
- P_8.2.7

2.3 DC Parameters of Port 0, Port 1, TMS and Reset (0000057330-11)

Table 31 in the referenced data sheet applies as well to TMS and Reset.

3 Revision History

Revision	Date	Changes
1.0	2019-11-05	BootROM - USER_NVM_ECC_CHECK (0000048454-124) added
		PORT2 CTRAP active level (0000057330-1) added
		CPU->SHPR2 wrong address (0000057330-2) added
		SCU->OSC_CON Bit5 (0000057330-3) added
		RESET Pin Pull-up (0000057330-4) added
		DC Parameters of Port 0, Port 1, TMS and Reset (0000057330-11) added
		Measurement Unit Overview (0000057330-5) added
		External XTAL circuitry (0000057330-6) added
		LIN internal circuitry (0000057330-7) add
		ADC1 Accuracy (0000057330-8) added
		ADC2 Accuracy (0000057330-9) added

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