TLE9563/4 – Step-by-step MOSFET driver setting guide and calculator description

About this document

Scope and purpose

This application note explains:

- the parameters and calculations needed to set the MOSFET driver of the TLE9563/4.
- how to use the calculation tool for the settings of the gate drivers in PWM operation

It provides a step-by-step process to configure the MOSFET driver based on the MOSFET datasheet to control the MOSFET switching times in PWM operation:

- rise and fall times
- turn-on and turn-off delay times
- recommendations for the settings of the cross-current protection time and of the blank times

It also gives guidelines to use the TLE9563/4 gate driver settings" tool

Intended audience

This document is intended for users who develop application with the motor system IC family (TLE956x)

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1 Introduction

The Motor System IC family (TLE956x) is a multi-half-bridge MOSFET driver, which combines power, communication and supply.
All devices feature a low-dropout voltage regulator with an output current of 250mA/5V. The communication interface incorporates a CAN FD transceiver up to 5Mbit/s according to ISO 11898-2:2016 (including Partial Networking option) and/or LIN transceiver.
All devices are available in a VQFN-48 (7mm x 7mm) package.

The devices offer a wide range of diagnostic features for the bridge driver both in on-state and in off-state. This application note focuses on the off-state diagnostic features of the half-bridge.

Figure 1 Block diagram – TLE9563/4

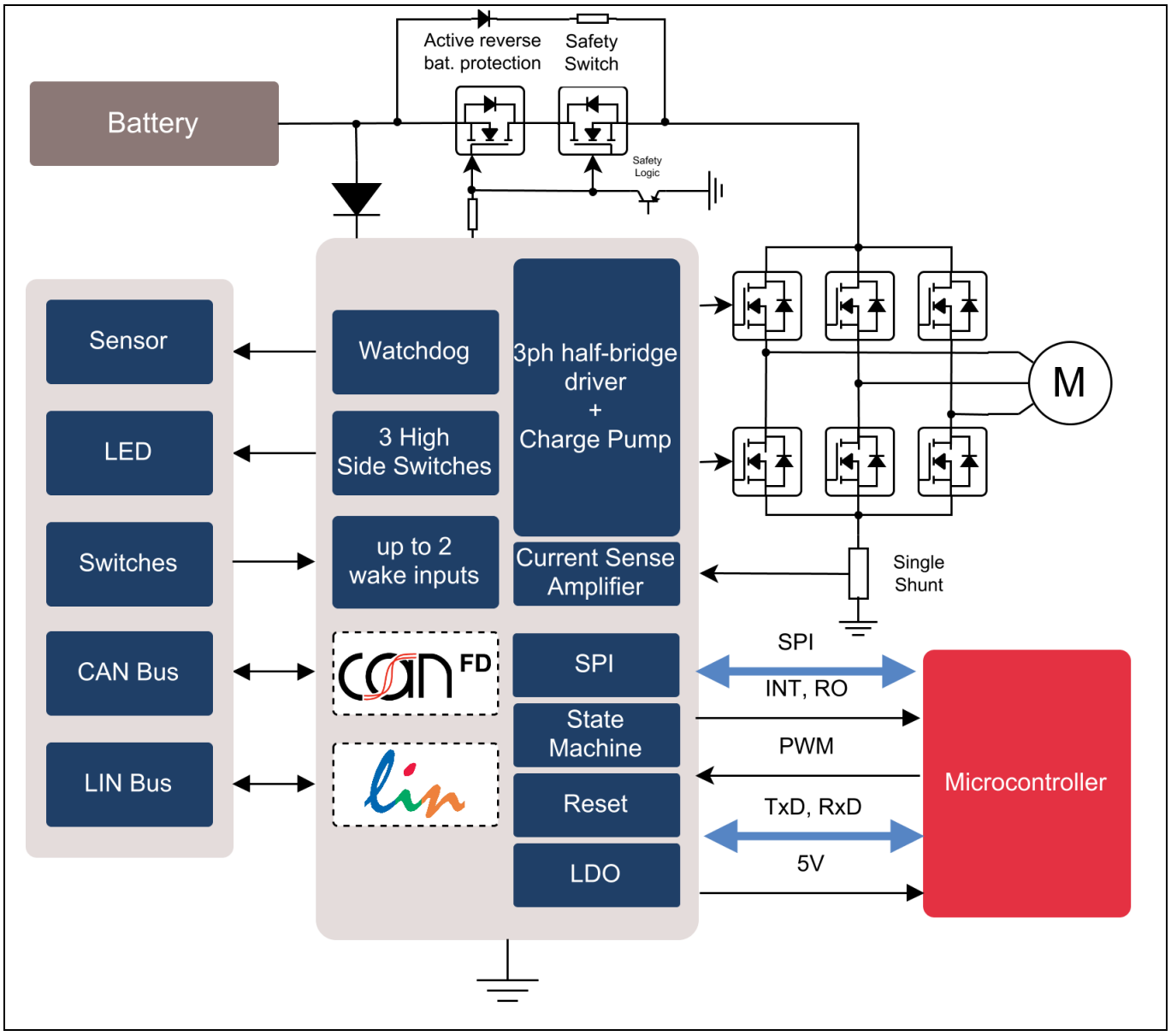
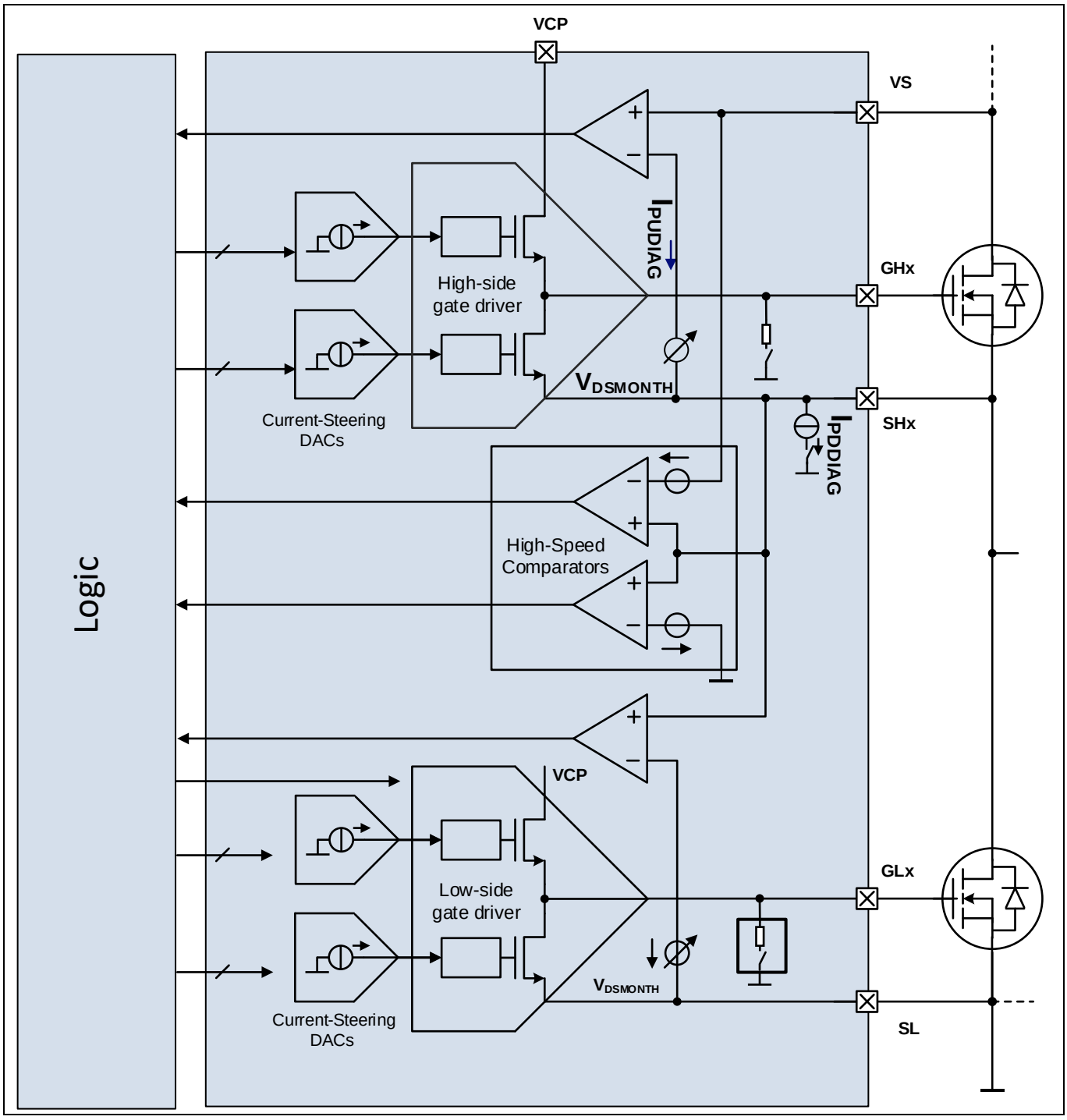


Figure 2 Block diagram of one half-bridge gate driver



2 General information

2.1 Conditions

The calculations and considerations of this document are valid for an inductive load controlled in half-bridge / full-bridge configuration with active freewheeling in PWM operation.

It is assumed that no external gate-drain / gate-source capacitance is placed at the MOSFET gate.

Note: *Electrical parameters of the TLE956x and of the MOSFETs are subject to variations such as production spread, supply voltage, temperature drift etc… The proposed calculation and settings are done with typical values for a specific MOSFET operating condition (e.g. supply voltage, load current etc…), uses small-signal MOSFET capacitances and may differ from the tested devices under different test conditions. The calculations do not have the precision of a simulation and do not replace measurements.*

2.2 Overview of the calculations steps

In this calculation tool, the user enters:

- MOSFET parameters extracted from the datasheet
- The application specific parameters and MOSFET driver's pre-charge and pre-discharge times

The calculation tool provides:

- The adapted MOSFET gate charges (Vds = Vs, Figure 5)
- The recommended settings of the MOSFET driver:
    - Gate driver currents
    - Cross-current protection times and blank times
    - Resulting switching times

Figure 3 MOSFET input parameters (example with IPZ40N04S5-3R1)

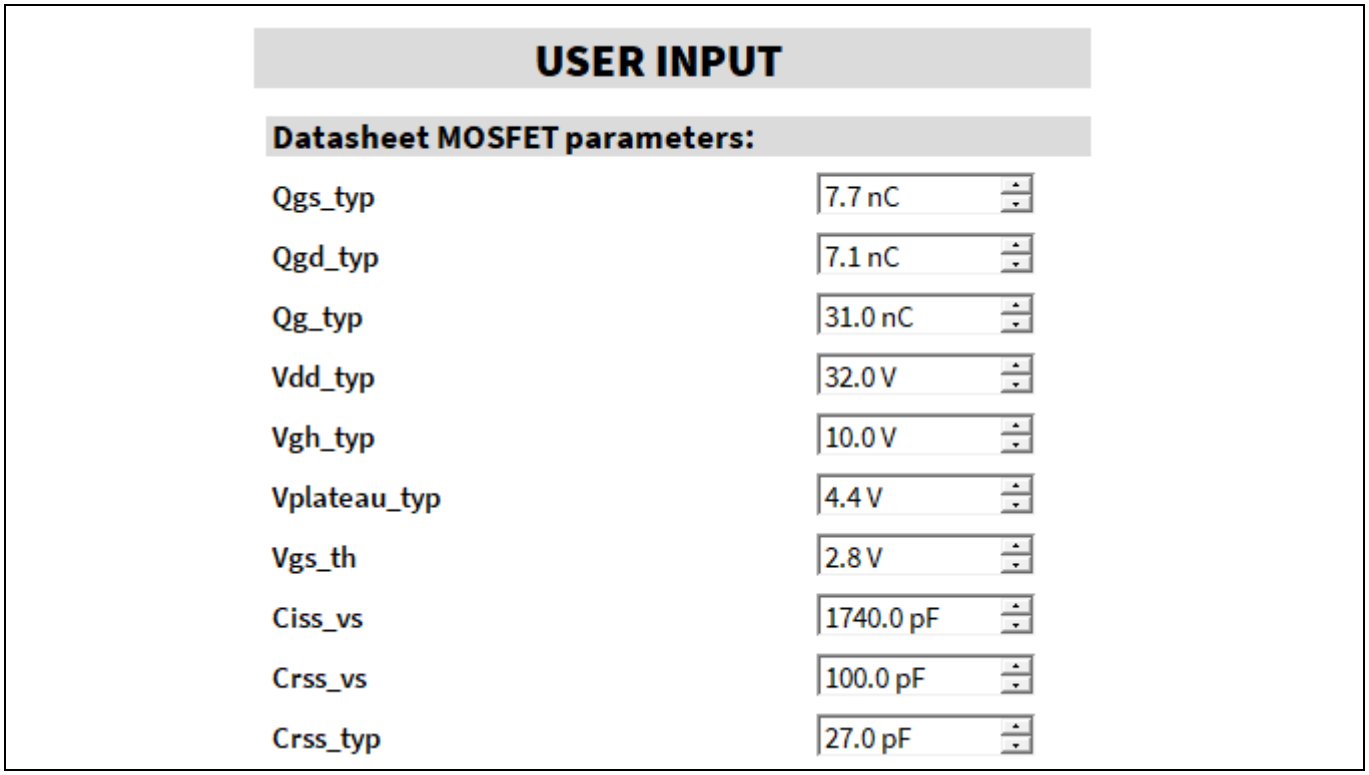


Figure 4 Application and MOSFET driver input parameters

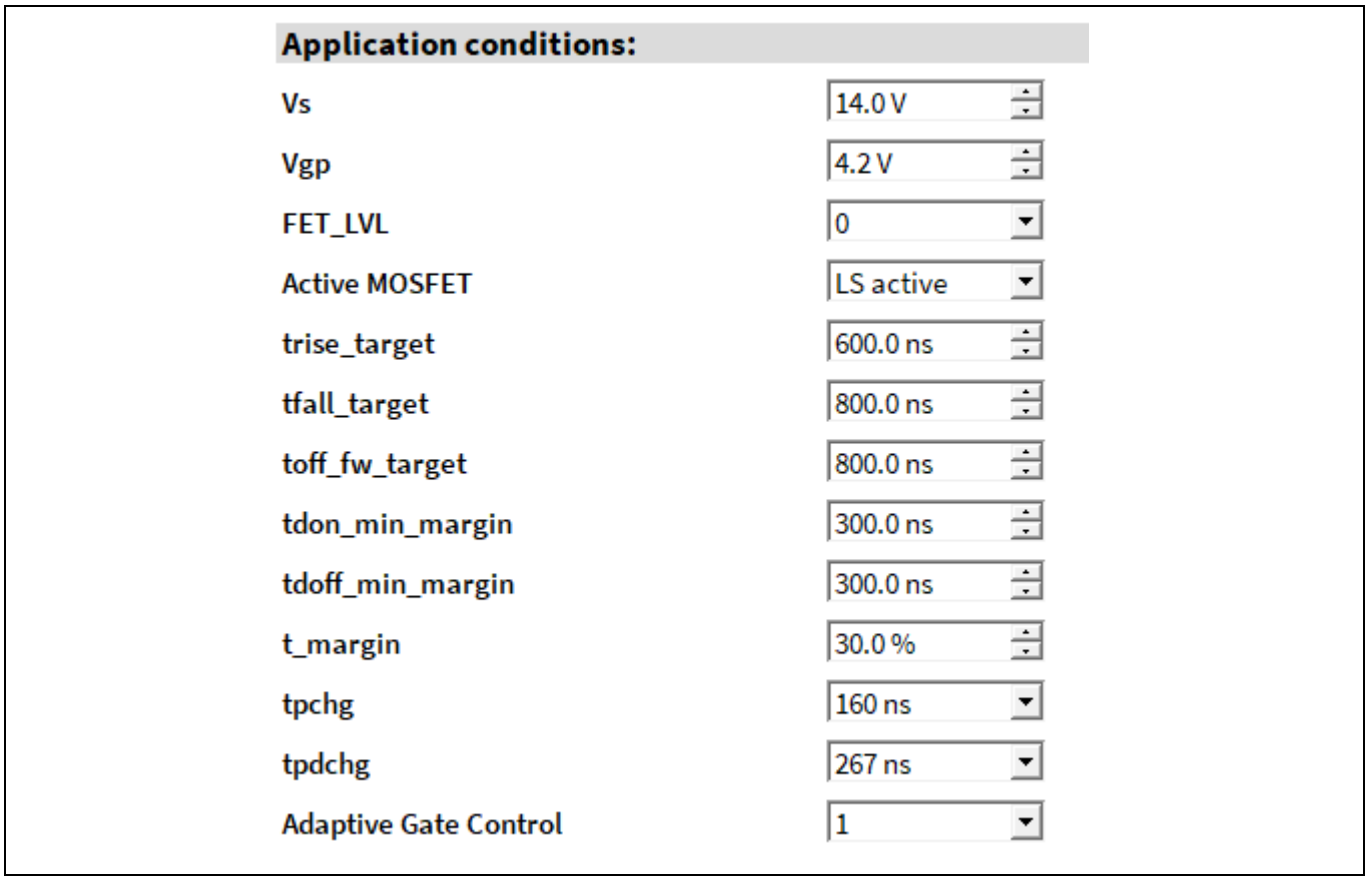
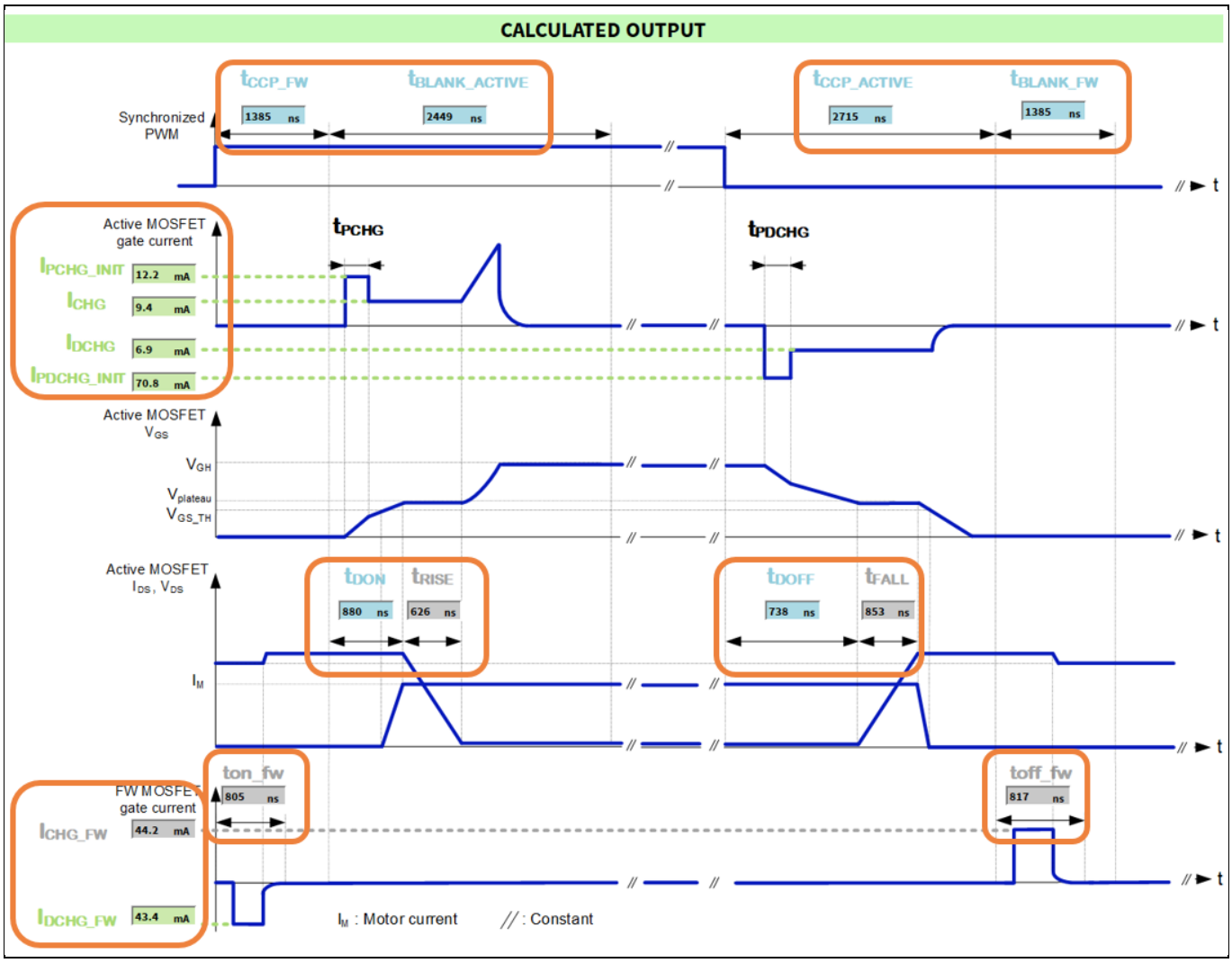


Figure 5 **Outputs: MOSFET adapted gate charges (to Vds = Vs)**

Calculated MOSFET parameters:		
Qgs	7.308	nC
Qgd	5.957	nC
Qg	34.382857	nC
Vgh_active	11.5	V
Vgh_FW	10	V
Ciss_0V	2893	pF

Figure 6 **Outputs: recommended cross-current protection time, blank time, gate driver currents and resulting switching times**



2.3 Notations

Table 1 List of notations

Abbreviation	Definition	Comment
Vds	MOSFET drain-source voltage	
Vgs	MOSFET gate-source voltage	
Ids	MOSFET drain-source current	
Vgh	MOSFET gate-source voltage when the gate is fully charged	
td_gdrv_on	TLE956x gate driver turn-on delay time	150 ns
td_gdrv_off	TLE956x gate driver turn-off delay time	150 ns
Ciss_0V	MOSFET input capacitance for drain-source voltage with Vds~ 0V and Vgs > Vplateau	Chapter 6.3

Vgh is a TLE956x parameter which depends on the high-side MOSFET, and on the setting of the FET_LVL bit (refer to Table 2 and datasheet chapter 12.7). That is the reason why FET_LVL and the position of the active MOSFET must be entered (Figure 4)

Table 2 Typical Vgh depending on FET_LVL bit and the considered high-side / low-side MOSFET

	Typ. Vgh high-side	Typ. Vgh low-side
FET_LVL = 0	10 V	11.5 V
FET_LVL = 1	11.5 V	11.5 V

2.4 Software setup

The GUI requires the installation of the Infineon Toolbox (Link). The following the steps are required:

1. Go to: **www.infineon.com/toolbox**
2. Follow the instructions provided on the toolbox installation webpage. Also see the “Download Getting Started Infineon Toolbox Guide” link for des additional user information
3. Launch the Infineon Toolbox on your PC:
4. Go to **Manage Tools** and search and install the tool: **Config Wizard for Motor System IC**
5. Start the **Config Wizard for Motor System IC**
6. Click on **TLE9563/4 GATE DRIVER SETTINGS**

Figure 7 Start of the TLE9563/4 gate driver setting tool

3 Input parameters

This chapter explains the meaning of the required input parameters.

3.1 MOSFET input parameters

This section describes the required MOSFET input parameters, and how to extract them from the MOSFET datasheet.

Table 3 List of MOSFET input parameters

Abbreviation	Definition	Unit	Comment
Qgs_typ	Typical MOSFET gate-source charge	nC	According to the datasheet conditions, Figure 9
Qgd_typ	Typical MOSFET gate-drain charge	nC	According to the datasheet conditions, Figure 9
Qg_typ	Typical MOSFET total gate charge	nC	According to the datasheet conditions (in general @Vgs = 10 V), Figure 9
Vdd_typ	Vds at which Qgd_typ is specified	V	e.g. For IPZ40N04S5-3R1: Vdd_typ = 32 V, Figure 9
Vgh_typ	Vgs at which Qg_typ is specified for full turn-on	V	e.g. For IPZ40N04S5-3R1: Vgh_typ = 10 V, Figure 9
Vplateau_typ	Vgs plateau at which Qgs_typ is specified	V	For IPZ40N04S5-3R1: Vplateau_typ=4.4 V @ Ids=40A, Figure 9
Vgs_th	Vgs threshold according to the typical application conditions (Ids, etc…)	V	According to the datasheet conditions, Figure 9
Ciss_vs	MOSFET input capacitance for drain-source voltage with Vds = Vs	pF	Figure 12, corresponding to the nominal application conditions (Vs = 14 V in this application note)
Crss_vs	MOSFET reverse transfer capacitance with Vds = Vs	pF	Figure 12
Crss_typ	MOSFET reverse transfer capacitance at Vds = Vdd_typ	pF	Figure 12

3.1.1 Gate charges Qgs_typ, Qgd_typ, Qg_typ

Qg_typ, Qgd_typ, Qg_typ are required parameters for the control of the switching times of the active MOSFET. Refer to Figure 8 for the definition.

In general the gate charges are specified for a very specific condition (32 V, 40A, Vgs from 0 to 10 V, Figure 9).

Figure 8 Gate charge definition and example (IPZ40N04S4-3R1, Infineon OptiMOS 5 MOSFET, [4])

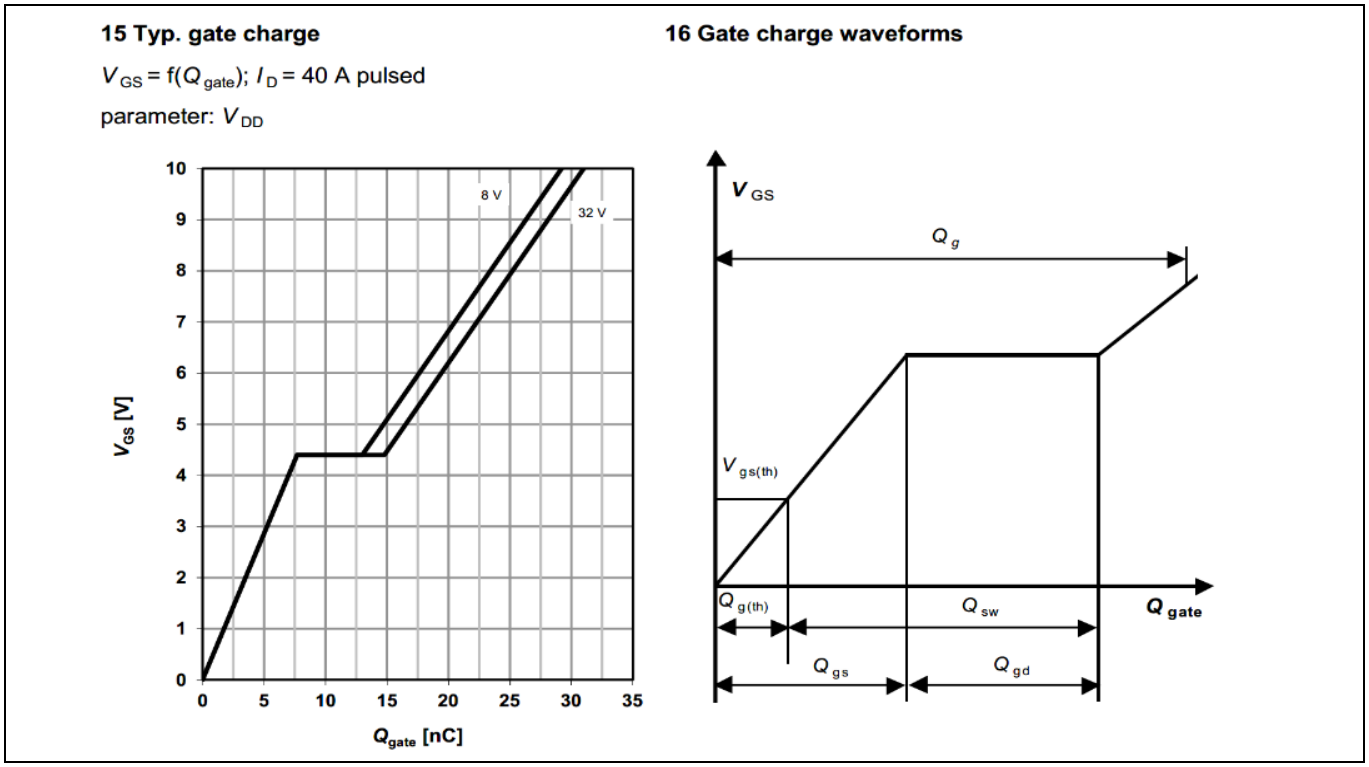


Figure 9 Example of gate charge specification (IPZ40N04S4-3R1) under specific conditions (32 V, 40A, Vgs from 0 to 10 V)

Gate Charge Characteristics[2)]

Gate to source charge	Q_{gs}	V_{DD}=32V, I_D=40A, V_{GS}=0 to 10V	-	7.7	10.2	nC
Gate to drain charge	Q_{gd}		-	7.1	10.6	
Gate charge total	Q_g		-	31	41	
Gate plateau voltage	$V_{plateau}$		-	4.4	-	V

Note: the specified gate charges in Figure 9 correspond to Qgs_typ, Qgd_typ, and Qg_typ.

These parameters depend on the working point of the active MOSFET. Indeed, these gate charges vary (among others) with:

- the applied drain-source voltage
- the MOSFET Ids current
- the applied gate-source voltage, when the MOSFET is turned on (Vgh).

Note: Qg in the MOSFET datasheets is often given for Vgs = 0V to 10V. However, the typical Vgh of the TLE956x depends on the setting of the FET_LVL bit and on the high-side/ low-side MOSFET. Therefore, Qg is re-calculated by the tool (for the applicable Vgh instead of Vgs_typ, refer to chapter 6.3).

For a more accurate control of the switching times, the gate charges must be adapted to the specific application conditions. Refer to chapter 6.

3.1.2 Gate threshold voltage Vgs_th (or Vgs(th))

Vgs_th: typical MOSFET threshold voltage (Refer to Figure 8 and Figure 10).

Figure 10 IPZ40N04S4-3R1 gate threshold voltage

Static characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D= 1mA	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=30µA	2.2	2.8	3.4	

3.1.3 MOSFET input capacitances at Vds = Vs

Ciss_vs is the input capacitance under the following conditions: Vds = Vs and Vgs = 0 V

Ciss_vs is needed to set conditions on the gate driver configurations for the pre-charge phase (AGC = 1 or 2), in order to avoid a too fast current increase of Ids (i.e. high dI_{ds} / dt) during the turn-on of the MOSFET.

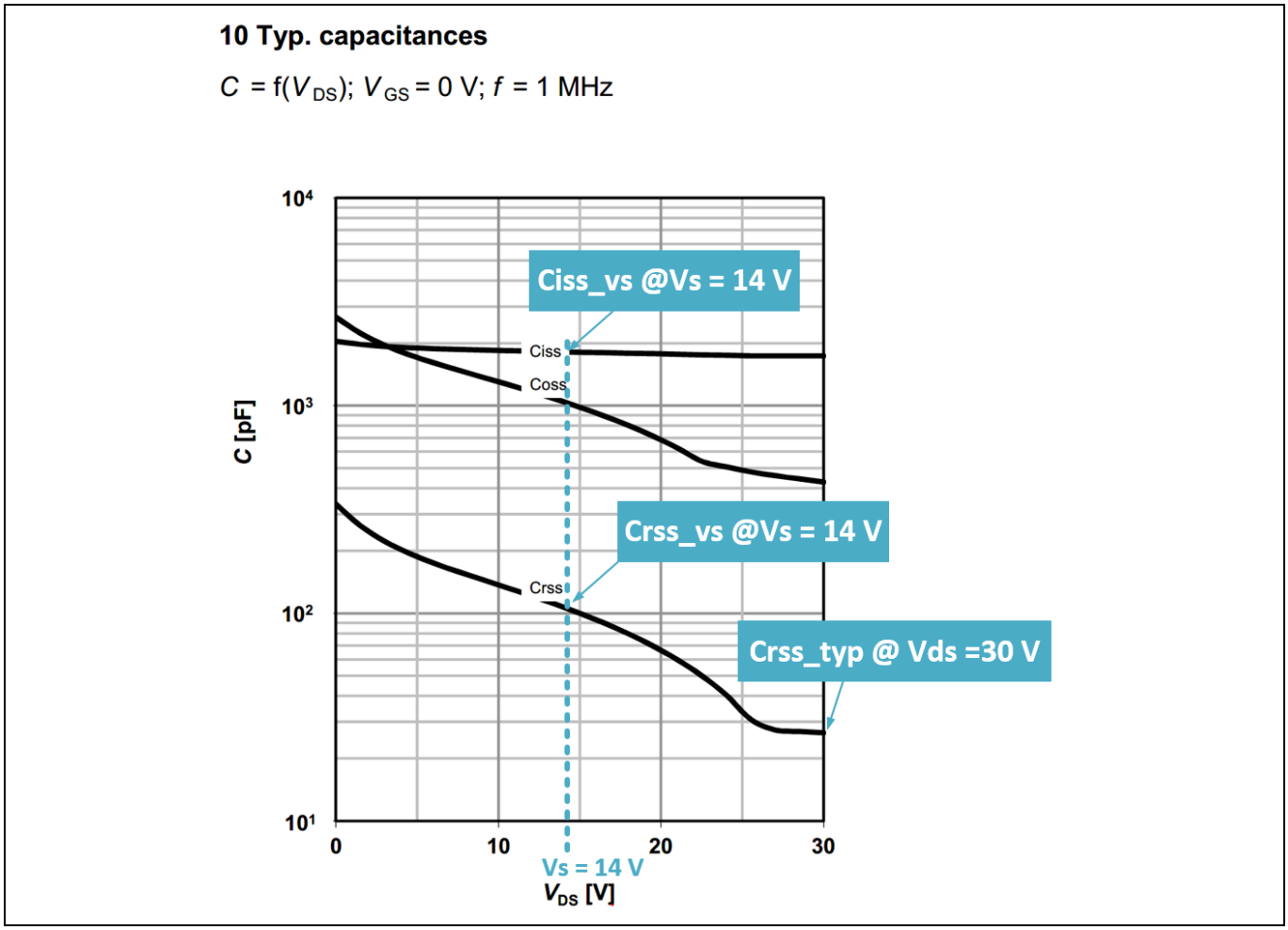
Figure 11 Specification of Ciss at Vgs = 0 V and Vds = 25 V (IPZ40N04S4-3R1)

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Dynamic characteristics[2)]						
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	1740	2310	pF
Output capacitance	C_{oss}		-	490	650	
Reverse transfer capacitance	C_{rss}		-	35	55	

The IPZ40N04S5-3R1 shows no substantial variation for the Ciss between 14 V and 25 V (Figure 12). Therefore Ciss_vs can be considered to be equal to 1740 pF for this MOSFET.

Note: The MOSFET input capacitance depends on Vds (and Vgs). This parameter is in general specified under a specific condition, which may differ from the typical application conditions.

Figure 12 Determination of Ciss_vs, Crss_vs (IPZ40N04S5-3R1, Vs = 14V)



3.1.4 MOSFET reverse transfer capacitances at Vds = Vs and Vds = Vdd_typ

Crss_vs is the reverse transfer capacitance at Vds = Vs and Vgs = 0 V.

Crss_typ is the reverse transfer capacitance at Vds = Vdd_typ and Vgs = 0 V.

Crss_vs and Crss_typ are required to estimate Qgd at Vds = Vs, using Qgd_typ (at Vds = Vdd_typ).

The value of these capacitances can be read from Figure 12 for the IPZ40N04S5-3R1. Crss @Vds = 30 V is a good estimation of Crss_typ (at Vds = Vdd_typ = 32 V), because the Crss curve is flat in this range for this MOSFET.

3.2 Application related input parameters

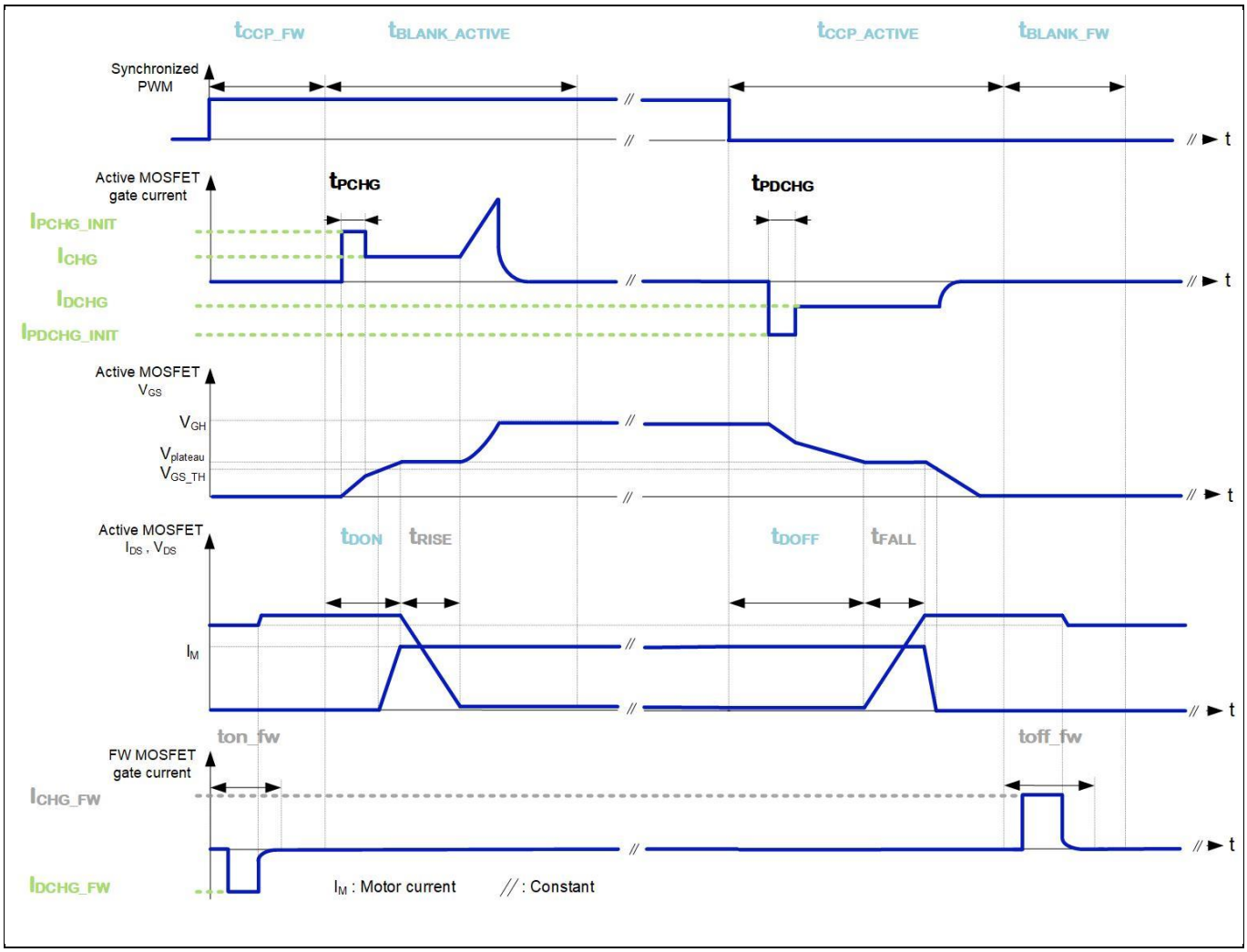
This section describes the application related input parameters, which are listed in Table 4.

Table 4 List of inputs parameters in the application conditions

Abbreviation	Definition	Unit	Comment
Vs	Nominal application supply voltage	V	Vs = 14 V in this document
Vgh	MOSFET driver gate-source voltage when the gate is fully charged [1)]	V	Refer to Table 2
Vplateau	Vgs plateau in the application conditions	V	Refer to Figure 14
trise_target	Active MOSFET target rise time	ns	
tfall_target	Active MOSFET target fall time	ns	
toff_fw_target	FW MOSFET target turn-off time	ns	
tdon_min_margin	Additional delay between the end of the pre-charge phase and the moment when Vgs reaches Vgs_th	ns	300 ns in the examples
tdoff_min_margin	Additional delay between the end of the pre-discharge phase and the moment when Vds decreases (Vgs reaches Vplateau)	ns	300 ns in the examples
t_margin	Margin in % added to the min. required cross-current protection time and blank time	%	30 % in the examples
tpchg	Gate driver pre-charge time	ns	TPRECHG register
tpdchg	Gate driver pre-discharge time	ns	TPRECHG register
AGC	Adaptive gate control bit		GENTCTRL register

Figure 13 shows the switching times, the cross-current protection time and blank time of the active and FW MOSFETs during PWM operation (the control scheme of the active MOSFET represented on Figure 13 corresponds to AGC =1 and AGC = 2).

Figure 13 Switching times and timings definition



trise_target: is the target rise time of the active MOSFET. This parameter is defined as the duration of the Vds slope at the turn-on of the active MOSFET (Refer to Figure 13).

tfall_target: is the target fall time of the active MOSFET. This parameter is defined as the duration of the Vds slope at the turn-off of the active MOSFET (Refer to Figure 13).

toff_fw_target is the target switch-off time of the FW MOSFET.

tccp_active is the cross-current protection time of the active MOSFET. The gate driver must be configured so that active MOSFET is off before the end of the tCCP_ACTIVE

tccp_fw is the cross-current protection time of the FW MOSFET. The gate driver must be configured so that the FW MOSFET is off before the end of the tCCP_FW.

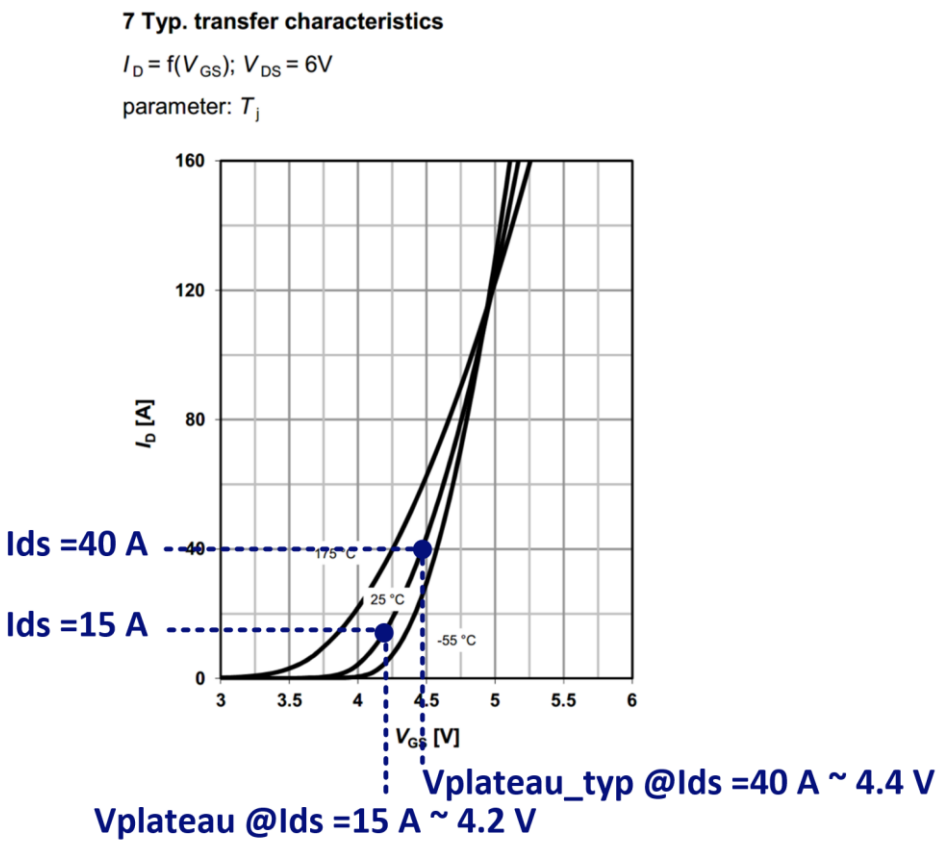
t_margin: is the margin (in percent) added to the minimum required cross-current protection times and the blank times for the active MOSFET and for the FW MOSFET.

tdon_min_margin is relevant for AGC = 1 and 2 (refer to datasheet for information about the AGC bit).

It is a minimum delay between the end of the pre-charge phase and the moment when Vgs reaches Vgs_th. Refer to chapter 4.

tdoff_min_margin: is relevant for AGC = 1 or 2. It is the minimum delay between the end of the pre-discharge phase and the beginning of tfall. Refer to chapter Refer to chapter 4.

Figure 14 Determination of Vplateau in the application conditions – IPZ40N04S5-3R1, Ids = 15 V



3.3 Output parameters

The calculation tool provides the recommended charge and discharge currents for the active and FW MOSFETs and the expected switching times. The user will also find the recommendations for the blank time and cross-current protection times.

The MOSFET gate charges Qg, Qgs and Qgd are adapted by the calculation tool according to the description in chapter 6.

Note that the maximum allowed pre-charge current pre-discharge currents (for AGC = 1 or 2) is supposed to be set to 100 mA typ.

Table 5 List of output parameters

Abbreviation	Definition	Unit	Control register
ICHG	Active MOSFET charge current	mA	HB_ICHG
IDCHG	Active MOSFET discharge current	mA	
ICHG_FW	FW MOSFET charge current	mA	
IDCHG_FW	FW MOSFET discharge current	mA	
IPCHG_INIT	Active MOSFET initial pre-charge current	mA	HB_PCHG_INIT
IPDCHG_INIT	Active MOSFET initial pre-discharge current	mA	
tdon	Active MOSFET turn-on delay time	ns	
tdoff	Active MOSFET turn-off delay time	ns	
trise	Active MOSFET effective rise time	ns	
tfall	Active MOSFET achievable fall time	ns	
ton_fw	FW MOSFET turn-on time	ns	
toff_fw	FW MOSFET turn-off time	ns	
tblank_active	Active MOSFET selected blank time	ns	CCP_BLK
tccp_active	Active MOSFET current-cross protection time	ns	
tblank_fw	FW MOSFET blank time	ns	
tccp_fw	FW MOSFET current-cross protection time	ns	

Notes:

1. trise, tfall, ton_fw, toff_fw may differ from trise_target, tfall_target, ton_fw_target and toff_fw_target. This difference is due to the fact that the calculation of trise, tfall, ton_fw, toff_fw considers the nearest available gate driver's charge and discharge currents
2. tdon, tdoff, ton_fw and toff_fw include the gate driver delay times td_gdrv_on and td_gdrv_off
3. tblank_active is selected so that its **minimum** value fulfills [0.12], [1.12]. The calculation tool displays the corresponding **typical** value.f
4. tccp_active is selected so that its **minimum** value fulfills [0.13], [1.13]. The calculation tool displays the corresponding **typical** value.

5. tccp_fw is selected so that its **minimum** value fulfills [0.14], [1.14]. The calculation tool displays the corresponding **typical** value.
6. tblank_fw is selected so that its **minimum** value fulfills [0.15], [1.15]. The calculation tool displays the corresponding **typical** value.

4 Recommendations

4.1 Conditions on trise_target and tfall_target

trise_target and tfall_target are input parameters determined by the application requirements.These parameters are determined by the **trade-off between the electromagnetic emissions (EME) and the switching losses**, and must be defined for each application according to their specific requirements.

4.2 Conditions on the pre-charge phase (AGC = 1 and AGC = 2)

If the pre-charge phase is activated, **the pre-charge phase should be over before the Ids increases in the active MOSFET (i.e. before Vgs = Vgs_th).** If this condition is not fulfilled, then the possible high pre-charge current causes a fast increase of Ids, resulting in a high EME.

This criteria is taken into account in 5.2.1 Step 3 and gives a condition on IPCHG_INIT.

tdon_min_margin (e.g. 300 ns) further reduces the maximum allowed pre-charge current, in order to avoid a fast increase of Ids.

Note: tdon_min_margin is an additional delay, which is directly reflected on the turn-on delay time, explaining the name of the parameter.

4.3 Recommendation for tpchg (AGC = 1 and AGC = 2)

tpchg must fulfill two conditions:

1. It should be as short as possible in order to avoid an unnecessary increase of tdon
2. It should be long enough, so that the charges delivered during the pre-charge phase (tpchg x IPCHG) and during the charge phase allow to reach the target tdon.

For the common MOSFETs used in combination with the TLE9563/4, **tpchg = 160 ns is often a good starting point**.

4.4 Conditions on the pre-discharge phase (AGC = 1 and AGC = 2)

When the pre-discharge phase is activated (AGC = 1 or 2), **the pre-discharge phase should over before the decrease of Vds.** If this condition is not fulfilled, then the possible high pre-discharge current causes a fast decrease of Vds, resulting in a high EME.

This criteria is taken into account in 5.2.1 Step 4 (AGC = 1 or 2) and gives a condition on IPDCHG_INIT.

tdoff_min_margin (e.g. 300 ns) further reduces the maximum allowed pre-discharge current, in order to avoid that the pre-discharge phase is still active during the increase of Vds.

Note: in the calculations of this application note, a symmetrical tdon and tdoff requires tdoff_min_margin > tdon_min_margin

4.5 Recommendation for tpdchg (AGC = 1 or 2)

tpdchg must fulfill two conditions:

1. It should be as short as possible in order to avoid an unnecessary increase of tdoff
2. It should be long enough, so that the charges removed from the MOSFET's gate during the pre-discharge phase (tpdchg x IPDCHG) and during the discharge phase allow to reach the target tdoff.

For the common MOSFETs used in combination with the TLE9563/4 such as the IPZ40N04S5-3R1, tpdchg = 267 ns is often suitable.

4.6 Recommendations for toff_fw_target

The turn-off (and the turn-on) of the FW MOSFET has a much lower impact on the EME than for the active MOSFET. Therefore it is possible to turn-off the FW MOSFET faster than the active MOSFET: e.g. between 600 ns and 1 µs as a starting point. toff_fw_target determines the suitable FW discharge current.

Note: IDCHG_FW is determined by toff_fw_target and by the MOSFET characteristics. The setting FW MOSFET charge and discharge currents are set by common control bits, therefore the turn-on time of the FW MOSFET is also determined.

5 Calculation of the gate driver currents and timings

This chapter shows the calculations that apply for for AGC = 0, AGC =1 or AGC = 2.

5.1 Calculation with Adaptive Gate Control disabled (AGC = 0)

This section shows the formulas used to calculate the required gate driver settings based on the input parameters when AGC = 0.

In this mode, the pre-charge and pre-discharge phases are disabled. The gate of the active MOSFET is charged, repectively discharged with the constant currents ICHG and IDCHG.

5.1.1 Calculation of gate driver currents with AGC = 0

This section calculates the required ICHG, IDCHG, IDCHG_FW.

Table 6 Calculation of gate driver currents with AGC = 0

Step	Parameters [mA]	Formula	
1	**Active MOSFET Charge current**	$ICHG = \frac{Qgd}{trise\_target}$	[0.1]
2	**Active MOSFET Discharge current**	$IDCHG = \frac{Qgd}{tfall\_target}$	[0.2]
3	**Active MOSFET initial pre-charge current** [1]	$IPCHG\_INIT = ICHG$	[0.3]
4	**Active MOSFET initial pre-discharge current** [1]	$IPDCHG\_INIT = IDCHG$	[0.4]
5	**FW MOSFET discharge current**[3]	$IDCHG\_FW = \frac{Ciss\_0v \times Vgh}{toff\_fw\_target - td\_gdrv\_off}$	[0.5]

1) These parameters are not relevant if AGC = 0: Therefore the IPCHG_INIT and IPDCHG_INIT must not be programmed when AGC = 0.

2) Once the required current is calculated, the nearest available MOSFET driver current of the TLE9563/4 is selected by the calculation tool. Refer to the datasheet rev. 1.0, Table 13 and Table 14, [1].

3) The FW MOSFET charge current is automatically determined when the FW MOSFET discharge current is selected (the FW MOSFET charge and discharge currents are set by the same control bits, [1]).

5.1.2 Timing calculation with AGC = 0

This section calculates the effective trise, tfall, tdon, tdoff, ton_fw, toff_fw, tblank_active, tccp_active, tccp_fw, and tblank_fw.

Attention: ***The nearest available ICHG, IDCHG, ICHG_FW and IDCHG_FW must be used in this calculation step.***

Table 7 Timing calculation with AGC = 0

Step	Parameters	Formula	
6	**Effective rise time**	$\text{trise} = \frac{\text{Qgd}}{\text{ICHG}}$	[0.6]
7	**Effective fall time**	$\text{tfall} = \frac{\text{Qgd}}{\text{IDCHG}}$	[0.7]
8	**Turn-on delay time**	$\text{tdon} = \frac{\text{Qgs}}{\text{ICHG}} + \text{td\_gdrv\_on}$	[0.8]
9	**Turn-off delay time**	$\text{tdoff} = \frac{\text{Qg}-\text{Qgs}-\text{Qgd}}{\text{IDCHG}} + \text{td\_gdrv\_off}$	[0.9]
10	**FW turn-on time**	$\text{ton\_fw} = \frac{\text{Ciss\_0v x Vgh}}{\text{ICHG\_FW}} + \text{td\_gdrv\_on}$	[0.10]
11	**FW turn-off time**	$\text{toff\_fw} = \frac{\text{Ciss\_0v x Vgh}}{\text{IDCHG\_FW}} + \text{td\_gdrv\_off}$	[0.11]
12	**Active MOSFET blank time**[1)]	$\text{tblank\_active} = (\text{tdon} + \text{trise}) \text{ x } (1 + \text{t\_margin})$	[0.12]
13	**Active MOSFET CCP**[2)] **time**	$\text{tccp\_active} = (\text{tdoff} + \text{tfall} + \frac{\text{Qgs}}{\text{IDCHG}}) \text{ x } (1 + \text{t\_margin})$	[0.13]
14	**FW CCP**[2)] **time**	$\text{tccp\_fw} = \text{toff\_fw x } (1 + \text{t\_margin})$	[0.14]
15	**FW blank time**	$\text{tblank\_fw} = \text{ton\_fw x } (1 + \text{t\_margin})$	[0.15]

1) CCP : Cross current protection

12 If the MOSFET must have the full Rdson at the end of tblank_active (i.e. Vgs = Vgh) and the postcharge phase is disabled, then [0.12] must be changed to:

$$\text{tblank\_active} = (\text{tdon} + \text{trise} + \frac{\text{Qg}-\text{Qgs}-\text{Qgd}}{\text{ICHG}}) \text{ x } (1 + \text{t\_margin}).$$

5.2 Calculation with precharge and predischarge enabled (AGC = 1 or 2)

This section shows the formulas used to calculate the required gate driver settings based on the input parameters when AGC = 1 and AGC = 2.

For AGC = 1:

- the pre-charge phase is enabled. The MOSFET is charged with the current IPCHG_INIT during this phase
- the pre-discharge phase is enabled. The MOSFET is discharged with the current IPDCHG_INIT during this phase
- tdon and tdoff are not regulated by the TLE9563/4

For AGC = 2:

- tdon and tdoff are regulated by the TLE9563/4
- the pre-charge is enabled. The MOSFET is initially charged with the current IPCHG_INIT during this phase for the first PWM period. Then the device adapts IPCHG cycle-by-cycle.
- the pre-discharge phase is enabled. The MOSFET is initially discharged with the current IPDCHG_INIT during this phase for the first PWM period. Then the device adapts IPDCHG cycle-by-cycle.

5.2.1 Calculation of gate driver currents with AGC = 1 or 2

Table 8 Calculation of gate driver currents with AGC = 1 or 2

Step	Parameters [mA]	Formula	
1	**Active MOSFET charge current**	$ICHG = \frac{Qgd}{trise\_target}$	[1.1]
2	**Active MOSFET discharge current**	$IDCHG = \frac{Qgd}{tfall\_target}$	[1.2]
3	**Active MOSFET initial pre-charge current**	$IPCHG\_INIT = \frac{Qg-(tdon\_min-td\_gdrv\_on-tpchg)\ x\ ICHG}{tpchg}$	[1.3]
4	**Active MOSFET initial pre-discharge current**	$IPDCHG\_INIT = \frac{Qg-Qgs-Qgd-(tdoff\_min-td\_gdrv\_off-tpdchg)\ x\ IDCHG}{tpdchg}$	[1.4]
5	**FW discharge current** [2)]	$IDCHG\_FW = \frac{Ciss\_0V\ x\ Vgh}{toff\_fw\_target - td\_gdrv\_off}$	[1.5]

1) The nearest available current must be selected. Refer to the datasheet rev. 1.0, Table 13 and Table 14, [1] and the corresponding datasheet.

2) The FW MOSFET charge current is automatically determined when the FW MOSFET discharge current is selected (the FW MOSFET charge and discharge currents are set by the same control bits, [1] and the corresponding datasheet.).

3 Condition on IPCHG_max to ensure that the pre-charge phase is over before Vgs = Vgs_th:

$$IPCHG\_INIT \leq \mathbf{IPCHG\_max} = \frac{Vgs\_th\ x\ Ciss\_vs}{tpchg}$$

The minimum allowed tdon (noted tdon_min), considering a margin (tdon_min_margin) is given by:

$$tdon\_min = \frac{Qg - tpchg\ x\ \mathbf{IPCHG\_max}}{ICHG} + td\_gdrv\_on + tpchg + tdon\_min\_margin$$

4 Condition on IPDCHG_max to ensure that the pre-discharge phase is over before Vgs reaches Vplateau at the turn-off of the active MOSFET:

$$IPDCHG\_INIT \leq IPDCHG\_max = \frac{Qg-Qgs-Qgd}{tpdchg}$$

The minimum allowed tdoff (noted tdoff_min), considering a margin (tdoff_min_margin) is given by:

$$tdoff\_min = \frac{Qg - Qgs - Qgd - tpdchg \times \mathbf{IPDCHG\_max}}{IDCHG} + td\_gdrv\_off + tpdchg + tdoff\_min\_margin$$

5.2.2 Timing calculation with AGC = 2

Table 9 Timing calculations with AGC = 2

Step	Parameters [ns]	Formula	
7	**Effective rise time**	$trise = \frac{Qgd}{ICHG}$	[1.7]
8	**Effective fall time**	$tfall = \frac{Qgd}{IDCHG}$	[1.8]
9	**Turn-on delay time**	$tdon = \frac{Qgs - tpchg \times IPCHG\_INIT}{ICHG} + td\_gdrv\_on + tpchg$	[1.9]
10	**Turn-off delay time**	$tdoff = \frac{Qg - Qgs - Qgd - tpdchg \times IPDCHG\_INIT}{IDCHG} + td\_gdrv\_off + tpdchg$	[1.10]
11	**FW turn-on time**	$ton\_fw = \frac{Ciss\_0v \times Vgh}{ICHG\_FW} + td\_gdrv\_on$	[1.11]
12	**FW turn-off time**	$toff\_fw = \frac{Ciss\_0v \times Vgh}{IDCHG\_FW} + td\_gdrv\_off$	[1.12]
13	**Active MOSFET blank time**	$tblank\_active = (tdon + trise) \times (1 + t\_margin)$	[1.13]
14	**Active MOSFET CCP[2] time**	$tccp\_active = (tdoff + tfall) \times (1 + t\_margin)$	[1.14]
15	**FW CCP time**	$tccp\_fw = toff\_fw \times (1 + t\_margin)$	[1.15]
16	**FW blank time**	$tblank\_fw = ton\_fw \times (1 + t\_margin)$	[1.16]

6 Adaption of the gate charges to the application conditions

The MOSFET Qgs, Qgd and Qg are specified for specific conditions. Refer to Figure 9: IPZ40N04S5-3R1:

Vs = 32 V, Vgs from 0 to 10 V and Ids = 40 A.

However, the value of the gate charge depends on the supply voltage, the load current ([2] [3]), and Vgh. for the TLE9563/4.

6.1 Adaption of Qgs (at Vds = Vs)

During the turn-on of the active MOSFET until Vgs = Vplateau, the current delivered by the gate driver charges Ciss. Therefore the charge injected in the MOSFET gate until Vgs reaches Vplateau is equal to Ciss_vs x Vplateau

Qgs (at Vds = Vs) = Ciss_vs x Vplateau

Example: Vs = 14 V, Vplateau = 4.2 V

Ciss_vs ~ 1740 pF

Qgs = 1740 x 10^{-12} x 4.2 ~ 7.3 nC

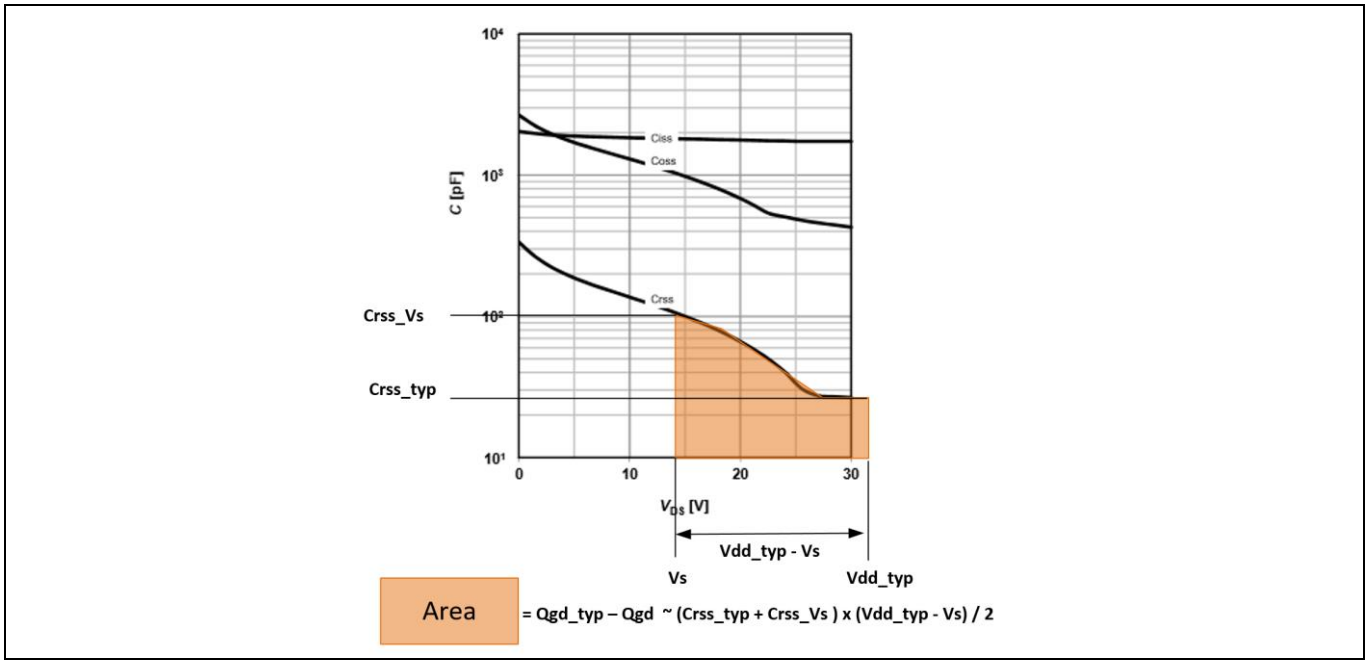
6.2 Adaption of Qgd (at Vds = Vs)

An estimation of Qgd consist in using Qgd_typ and substracting the gate charge related to Crss between Vdd_typ and Vds = Vs ([2] [3]). The gate charge difference is represented by the highlighted area in Figure 15.

Approximating this area to a trapezoid, gives Qgd_typ – Qgd ~ x (Crss_vs + Crss_typ) x (Vdd_typ - Vs) / 2.

Qgd = Qgd_typ - (Crss_vs + Crss_typ) x (Vdd_typ - Vs)/ 2.

Figure 15 Estimation of the difference between Qgd_typ and Qds



Example: MOSFET IPZ40N04S5-3R1, Vs = 14 V, Vdd_typ = 32V

Crss_vs = 100 pF, Crss_typ ~ 27 pF, Qgd_typ = 7.1 nC

Qgd = 7.1 x 10^{-9} – (100 + 27) x 10^{-12} x (32 - 14) / 2 ~ 6.0 nC

6.3 Adaption of Qg at (Vds = Vs) for the active MOSFET

During the turn-on phase of the active MOSFET, the remaining charge delivered by the MOSFET driver between the end of the Miller plateau and Vgs = Vgh represents the charge required to charge Ciss_0v from Vplateau to Vgh.

Qg – Qgd – Qgs = Ciss_0v x (Vgh – Vplateau)

Qg = Ciss_0v x (Vgh – Vplateau)

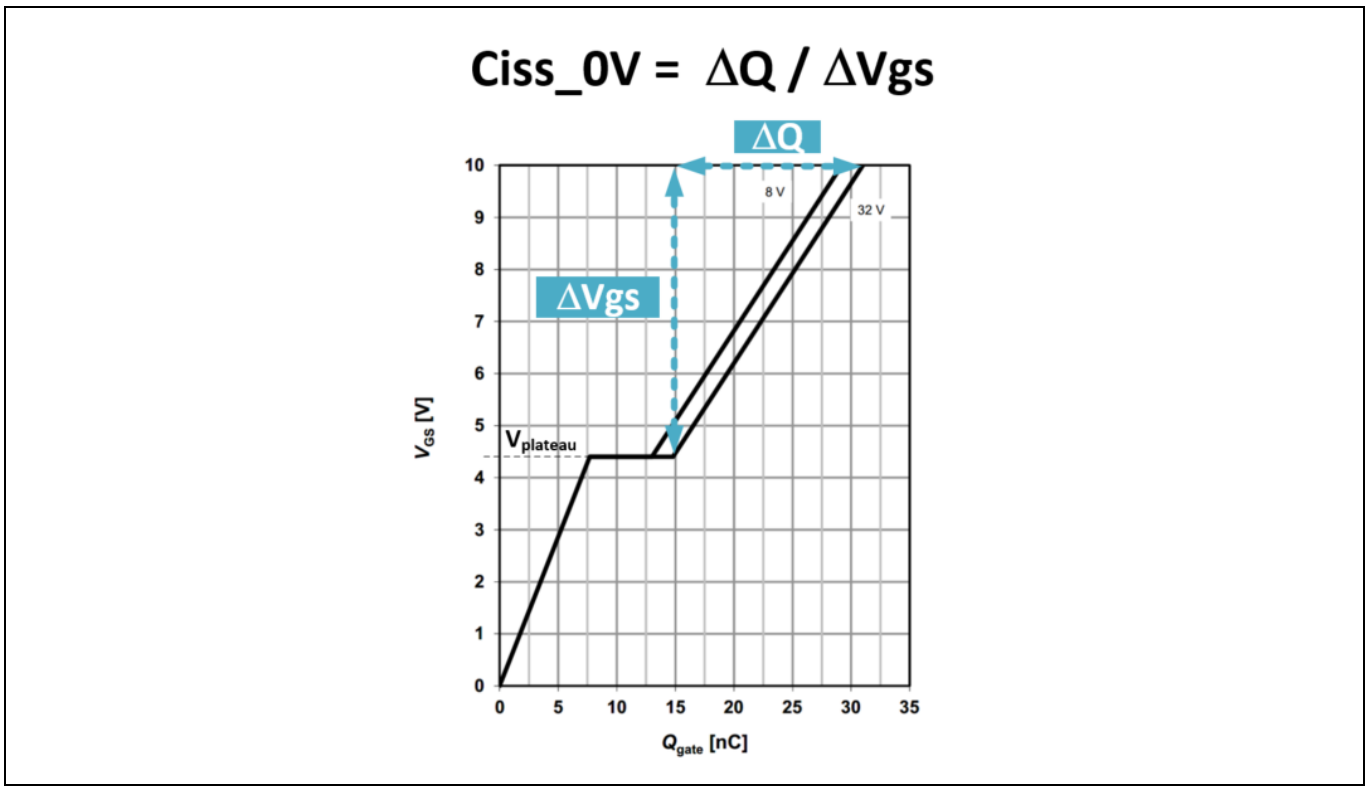
Where Ciss_0v is the MOSFET input capacitance with Vds close to 0 V

This parameter is not directly provided in the MOSFET datasheets. It is the inverse slope of the graph Vgs versus gate charge (Figure 16).

Ciss_0v = (Qg_typ – Qgs_typ – Qgd_typ) / (Vgh_typ – Vplateau_typ)

Qg = Qgd + Qgs + Ciss_0v x (Vgh – Vplateau)

Figure 16 Determination of Ciss_0v (IPZ40N04S5-3R1)



Example:

MOSFET IPZ40N04S5-3R1, Vs = 14 V,

Vgh_typ = 10V, Vgh = 11.5 V (low-side PWM or high-side PWM with FET_LVL = 0)

Qgs_typ = 7.7 nC, Qgd_typ = 7.1 nC, Qg_typ = 31 nC

Vplateau_typ = 4.4 V, Vplateau = 4.2 V

In 6.1 and 6.2, we have seen that Qgs = 7.3 nC, Qgd = 6.0 nC

Ciss_0V = $\frac{(31-7.1-7.7)\times 10^{-9}}{(10-4.4)}$ ~ 2.89 nF

Qg = 7.3 x 10^{-9}+ 6.0 x 10^{-9}+ 2.89 x 10^{-9} x (11.5 – 4.2) ~ 34.4 nC

7 Conclusions

This application note provides recommendations for the setting of the gate driver of the TLE9563/4 in PWM operation. It also gives step-by-step calculation details used by the gate driver setting tool for the determination of the MOSFET driver currents and timings and the resulting MOSFET switching times, for an open loop control.

However, the MOSFET switching times are dependent from the application conditions (e.g. current, voltage timings) and is subject to the production spread of the MOSFET and the Muti MOSFET driver itself.

To overcome the limitations of an open loop control, the TLE9563/4 also integrates features which allows a closed loop regulation of the switching times:

- a self-regulation of tdon and tdoff can be done by the TLE9563/4
- a closed loop regulation of trise and tfall can be done by the microcontroller thanks to measured in-application switching times provided by the TLE9563/4. The principle is described in the application note [2].

8 References

[1]. Datasheet TLE956x , Link

[2]. Rise and fall time regulation with current source MOSFET drivers Link

[3]. AND9083. MOSFET gate charge origin and its applications. Link

[4]. Datasheet IPZ40N04S5-3R1. Link

Revision history

Document version	Date of release	Description of changes
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