Multiple half-bridge drivers

SPI Protocol of the TLE941xy family

Application Note

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Automotive Power

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1 Abstract

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This application note is gives information for the handling of the Serial Peripheral Interface (SPI) between a device of the TLE941xy family and a microcontroller. After a general description of SPI interfaces, this document presents the SPI protocol of the TLE941xy and gives examples of SPI communications in different configurations. The last section of this document deals with failure detections on the SPI bus.

2 Introduction

The TLE941xy family consists of multiple half-bridge drivers designed especially for automotive motion control application such as Heating, Ventilation, and Air Conditioning (HVAC) and exterior side mirror. The product family offers devices from three to twelve half-bridges. **Figure 1** shows the block diagram of the 12-fold half-bridge driver: TLE94112EL.

The devices integrate a SPI interface to configure and control the outputs and for diagnostic purpose.

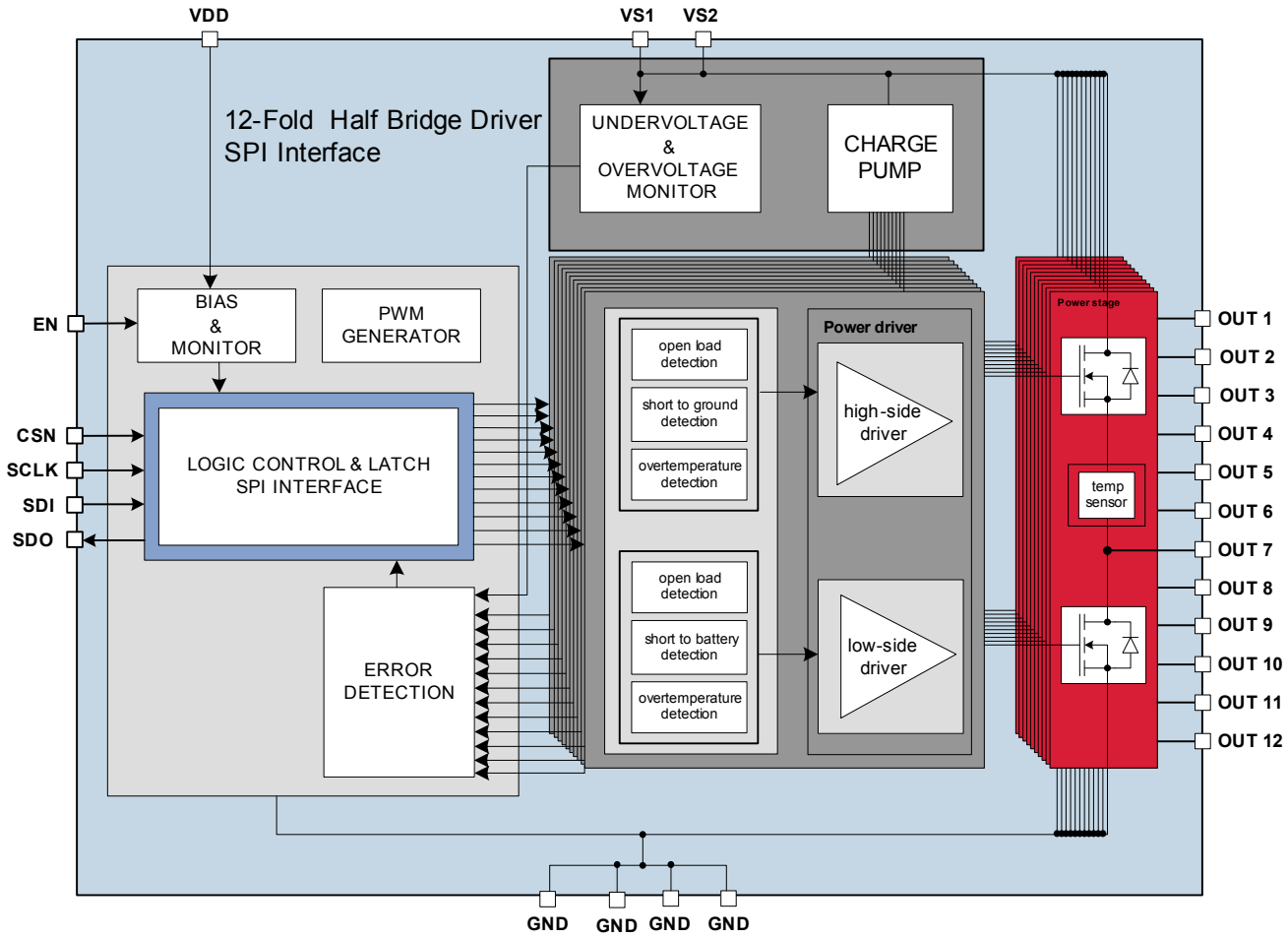


Figure 1 Block Diagram of TLE94112EL

3 List of acronyms

Table 1 List of acronyms

Acronyms	Meaning
CPHA	Clock Phase
CPOL	Clock Polarity
CSN	Chip Select Not
GEF	Global Error Flag of TLE941xy
GSR	Global Status Register of TLE941xy
LABT	Last Address Byte Token of TLE941xy
LE	Load Error bit of the TLE941xy devices
LSB	Least Significant Bit
MCSN	Master CSN output
MISO	Master Input Slave Output
MOSI	Master Output Slave Input
MSB	Most Significant Bit
NPOR	Negated Power-On Reset bit of the Global Status Register of the TLE941xy
OP	Operation bit of the TLE941xy (Bit7 of the address byte)
POR	Power-On Reset
SCLK	Serial Clock
SDI	Serial Data Input
SDO	Serial Data Output
SPI	Serial Parallel Interface
SPI_ERR	SPI Error bit of the TLE941xy
TPW	Temperature Pre-Warning bit of the TLE941xy
TSD	Temperature Shutdown bit of the TLE941xy
VS_OV	VS Overvoltage bit of the TLE941xy
VS_UV	VS Undervoltage bit of the TLE941xy

4 General description of SPI interfaces

A system with an SPI interface consists of one master (microcontroller) and one or several slave devices. The SPI interface supports a synchronous data transfer. The microcontroller provides the clock signal and initiates every communication.

This interface is often used when few I/O lines are available, but the communication between two or more devices must be fast and easy to implement.

The SPI bus consists of four unidirectional signal lines:

- **CSN: Chip Select Not**. The CSN is always an input for the slave device, and is controlled by the master. A slave is selected when its CSN pin is pulled Low by the microcontroller, and the communication starts. When the CSN pin of a device is High, this device is not selected and its SDO pin is in high impedance.
- **SCLK: Serial Clock.** This pin receives the clock signal from the microcontroller, which is used for the timing of the serial interface.
- **SDI: Serial Data Input**. This pin receives the data from the microcontroller output, often called Master Output / Slave Input or MOSI
- **SDO: Serial Data Output**. This pin drives the data signal of the microcontroller input, often called Master Input / Slave Output or MISO

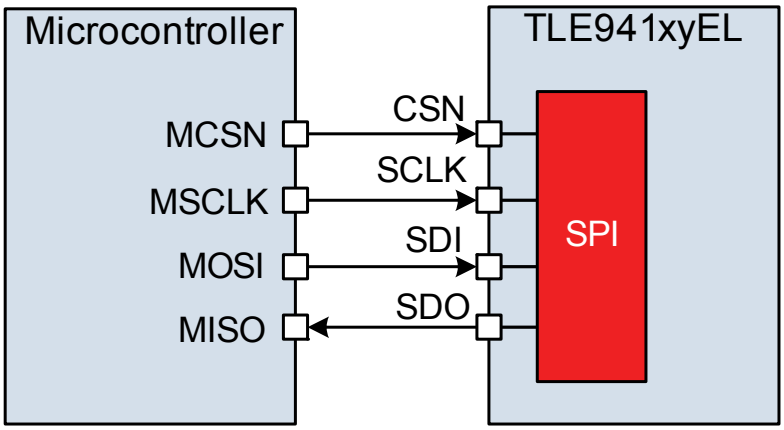


Figure 2 Definition of SPI signals

5 SPI protocol of the TLE941xy

This section summarizes the communication protocol implemented by the TLE941xy family. For further information, refer to the datasheets of the corresponding devices.

5.1 Structure of an SPI Frame

The microcontroller sends to the TLE941xy an address byte followed by a data byte, with the Least Significant Bit (LSB) transmitted first. The LSB of the address byte must be 1 (**Figure 5**, A0 = 1).

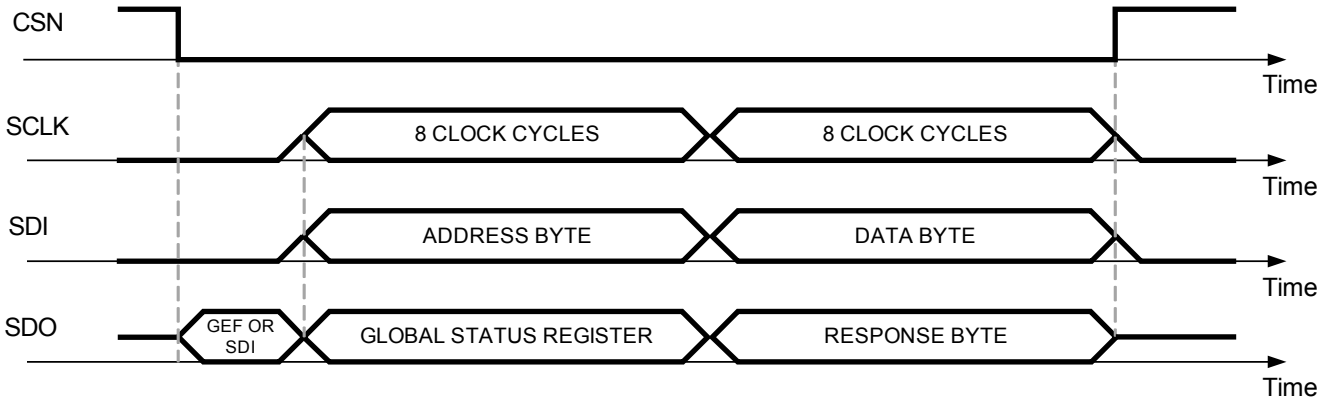


Figure 3 TLE941xy - Structure of a SPI Frame

5.2 Transmission mode

A communication starts when the master selects the addressed slave by pulling Low its CSN pin. This allows to have one master and several slaves, sharing the same SCLK, SDI and SDO signals.

During each communication **a full-duplex** data transfer is supported: the master and the addressed slave receive and transfer data at the same time.

Transmission mode depends on:

- the SCLK level when the transmission is initiated (often called Clock Polarity or CPOL) when the SPI communication starts (CSN is pulled Low)
- the sampling edge of the data (often called Clock Phase or CPHA)

The TLE941xy family is compatible with the following setting: CPOL = 0 and CPHA = 1 (**Figure 4**):

- The SCLK must be Low during the CSN falling edge (CPOL = 0)
- The TLE941xy accepts data at the SDI pin on the SCLK falling edges and shifts out new data at SDO on the SCLK rising edges (CPHA = 1)

The first bit received by the TLE941xy SDI (during the first SCLK falling edge) is interpreted as the Least Significant Bit (LSB, Bit0). The first transmitted bit by SDO must be interpreted by the microcontroller as LSB as well. Refer to **Figure 4** and **Figure 5**.

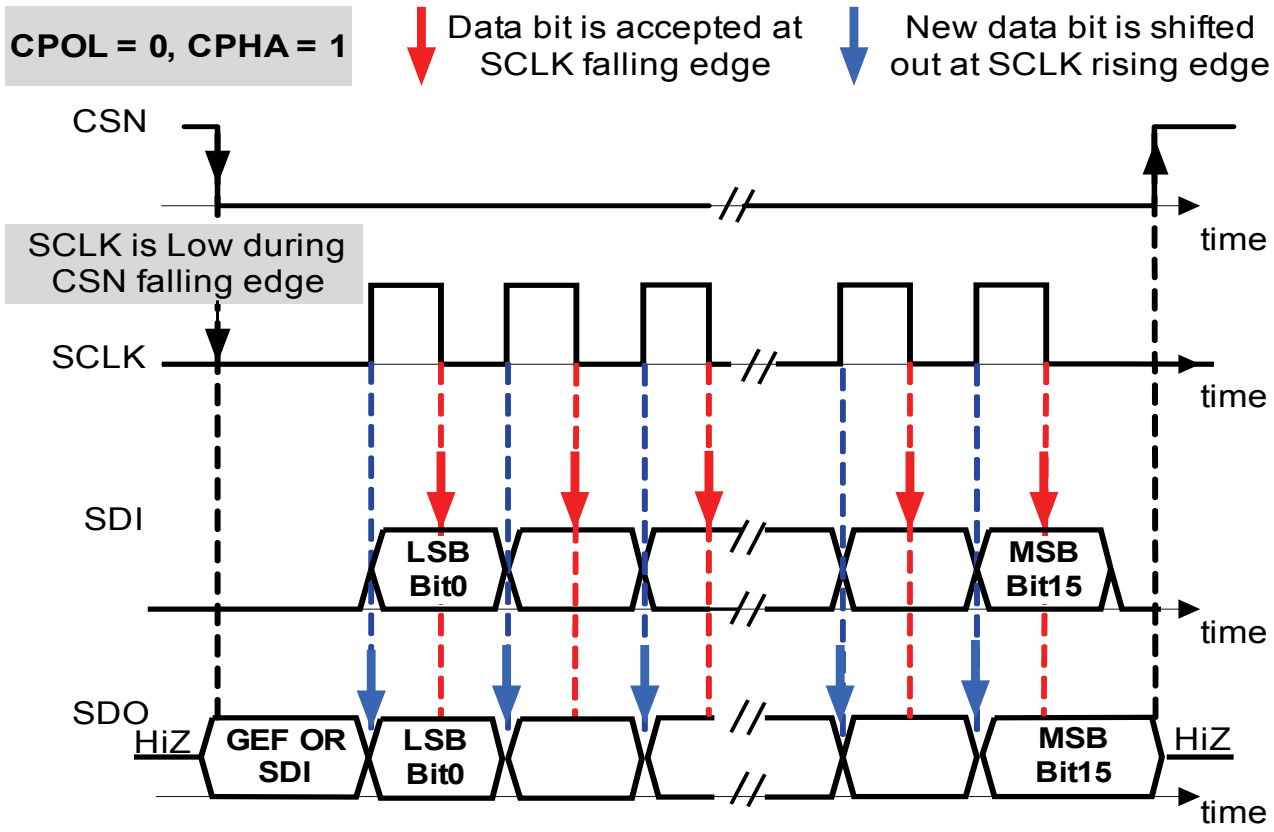


Figure 4 Transmission Mode for the TLE941xy: CPOL = 0, CPHA = 1, LSB sent first

	LSB	Address Byte							Data Byte							MSB
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SDI	A0 =1	A1 (LABT)	A2	A3	A4	A5	A6	A7 (OP)	D0	D1	D2	D3	D4	D5	D6	D7

	LSB	Global Status Register							Response Byte							MSB
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
SDO	0	TPW	TSD	NPOR	VS_OV	VS_UV	LE	SPI_ ERR	D0	D1	D2	D3	D4	D5	D6	D7

Time

Figure 5 TLE941xy - Content of the address byte and Global Status Register

Read, write and clear access

A read access, respectively a write access, to **a control register** is done when the OP bit (Bit 7 of the address byte) is equal to 0, respectively equal to 1 (see **Figure 5**).

A read access, respectively a clear access, to **status register** is done when the OP bit (Bit 7 of the address byte) is equal to 0, respectively equal to 1 (see **Figure 5**).

Figure 6 shows an example of SPI frame with one TLE941xy:

SDI received frame: 0b 0000 0000 0000 0011

- Address byte = 0b 0000 0011: Read control register HB_ACT_1_CTRL
- Data byte = 0b 0

SDO transmitted frame: 0b 0000 1001 0000 1000

- GEF = 0
- Global Status Register = 0b 0000 1000: NPOR bit = 1, the device does not come from a power-on reset.
- Response Byte (content of the HB_ACT_1_CTRL): 0b 0000 1001 (Low Side 1 and High Side 2 are ON)

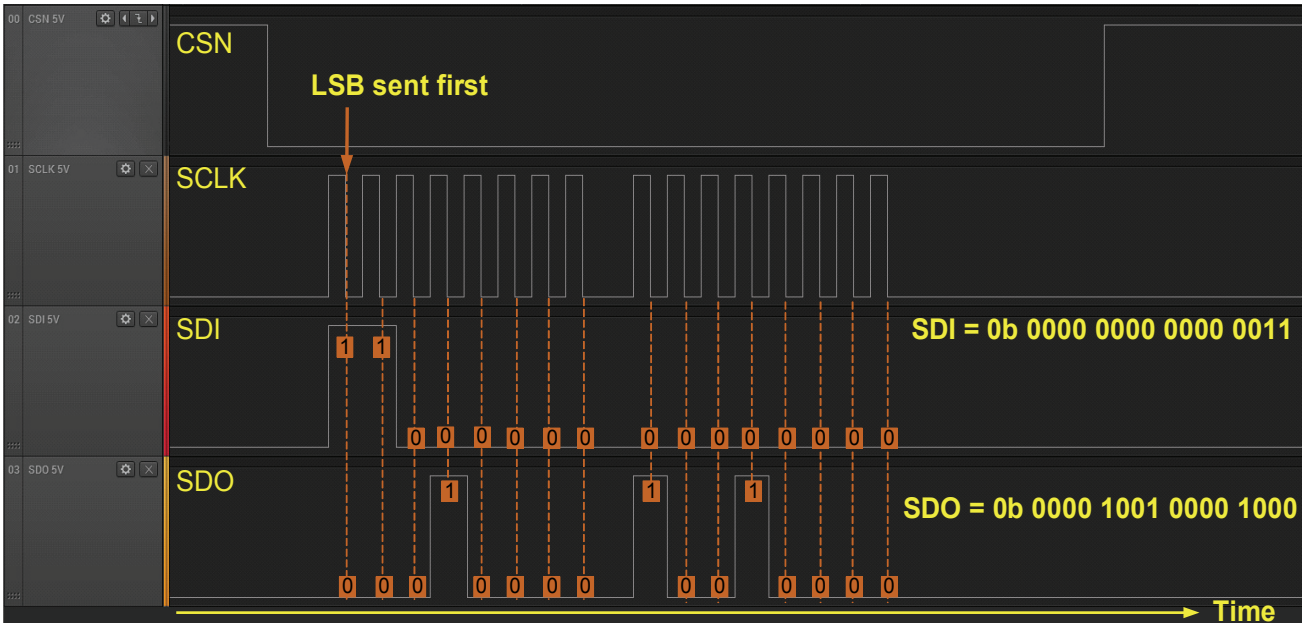


Figure 6 Example of SPI frame between the microcontroller and one TLE941xy

5.3 Communication Protocol

During each communication, the microcontroller sends an address byte followed by a SDI data byte. Simultaneously, the TLE941xy sends to the microcontroller the following response: (Figure 4)

- before the first SCLK rising edge: Alogic OR between the Global Error Flag (GEF) and the signal present at SDI (see Figure 7)[1)]
- followed by the Global Status Register (GSR) during the first eight SCLK cycles
- followed by the response byte during the next eight SCLK cycles

The GSR provides to the microcontroller an overview of the device status. All failures detectable by the TLE941xy are reported in this byte (Table 3):

- SPI Protocol Error (SPI_ERR)
- Load Error (LE): Logical OR combination between open load and overcurrent for one of the outputs
- VS Undervoltage (VS_UV)
- VS Overvoltage (VS_OV)
- Negated Power-On Reset (NPOR)
- Temperature Shutdown (TSD)

1) SDI should be 0 between the CSN falling edge and the first rising edge to enable the microcontroller to read the GEF.

- Temperature Pre-Warning (TPW)

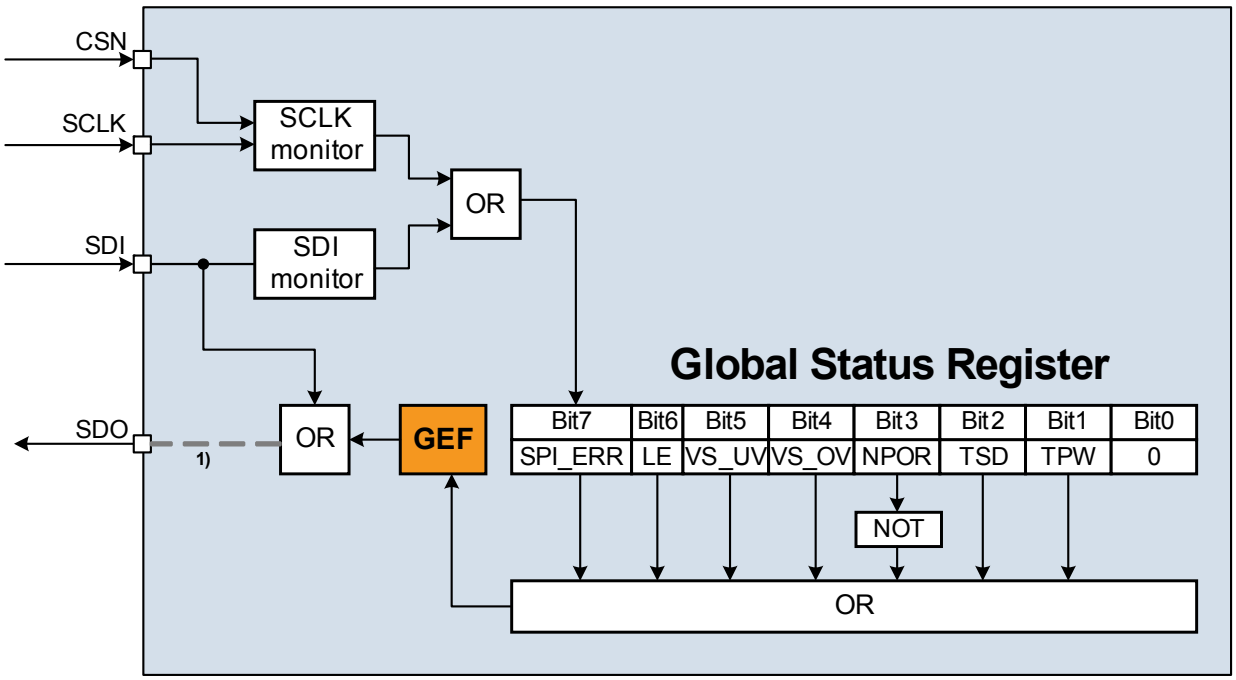
Note: The protocol requires the LSB of the GSR to be 0.

Table 2 Description of the Global Error Register

Bit	Type of Failure	Status bit	Polarity	Comment
Bit 7	SPI Protocol Error	SPI_ERR	Active High	-
Bit 6	Open Load or Overcurrent	LE	Active High	-
Bit 5	VS Undervoltage	VS_UV	Active High	-
Bit 4	VS Overvoltage	VS_OV	Active High	-
Bit 3	Power-On Reset	**NPOR**	**Active Low**	NPOR = 0 in POR condition NPOR = 1 if no POR is detected
Bit 2	Thermal Shutdown	TSD	Active High	-
Bit 1	Thermal Pre-Warning	TPW	Active High	-
Bit 0	Not Applicable	-	-	The LSB of the GSR is always 0

All the status bits of the GSR are active High, with the exception of the NPOR. As we will see in **Chapter 8.2**, this enables the microcontroller to detect and distinguish the following failures: SDO is shorted to “0”, SDO is shorted to 1, the device comes from a power-on reset.

The Global Error Flag is an logic OR combination of the status bits of the GSR, with the exception of the NPOR (**Figure 7**): GEF = (SPI_ERR) OR (LE) OR (VS_UV) OR (VS_OV) OR Negated (NPOR) OR (TSD) OR (TPW).



[1] CSN = Low, SCLK = Low
Before SCLK first rising edge

Figure 7 Global Error Flag

Table 3 Failure reporting in the Global Status Register and by the Global Error Flag

Condition	Status bit in GSR	Global Error Flag
SPI Protocol Error	SPI_ERR = 1	GEF = 1
Open Load or Overcurrent	LE = 1	GEF = 1
VS Undervoltage	VS_UV = 1	GEF = 1
VS Overvoltage	VS_OV = 1	GEF = 1
Power-On Reset	**NPOR = 0** (Figure 8)	GEF = 1
Thermal Shutdown	TSD = 1	GEF = 1
Thermal Pre-Warning	TPW = 1	GEF = 1
No Failure	SPI_ERR = 0 LE = 0 VS_UV = 0 VS_OV = 0 **NPOR = 1** TSD = 0 TPW = 0 See Figure 9	GEF = 0

Figure 8 shows the Global Error Flag and the Global Status Register when the TLE941xy comes from a power-on reset, and no other failure is detected: The GEF is set and NPOR bit = 0.

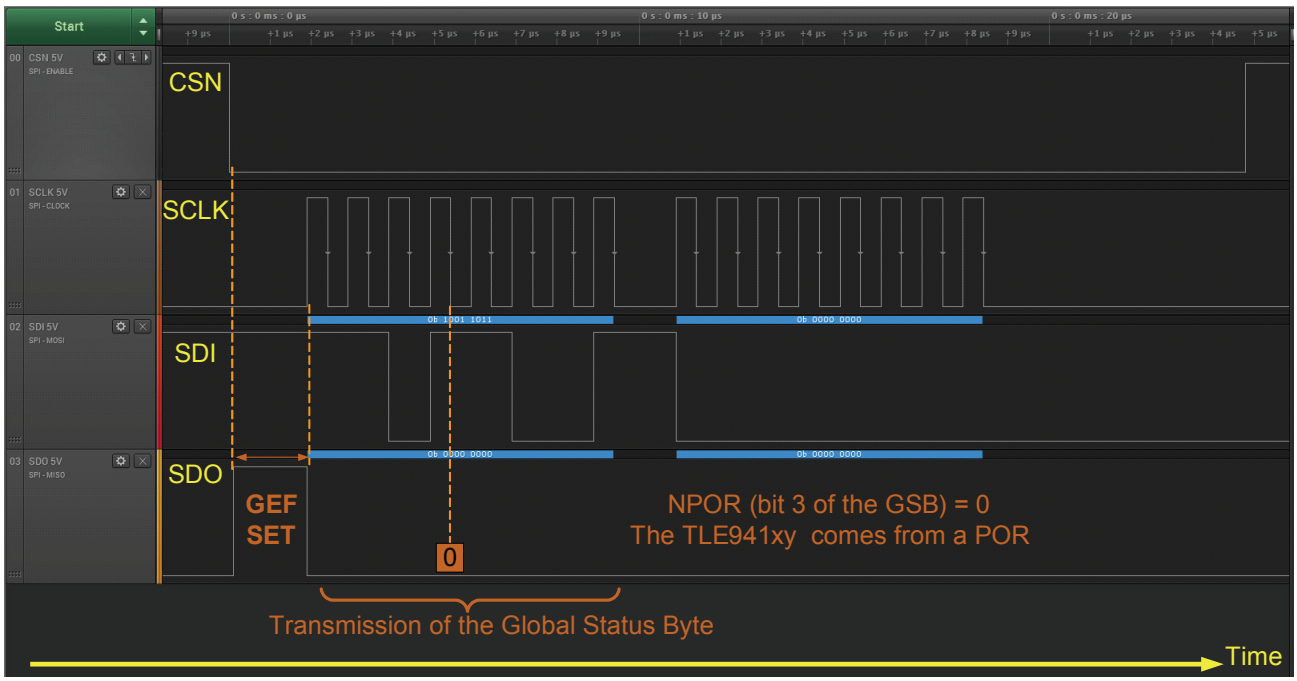


Figure 8 Example of NPOR bit and GEF when the device come from a power-on reset

Figure 9 shows the Global Error Flag and the Global Status Register when the TLE941xy does not detect any failure: GEF = 0, and NPOR =1, the other bits of the status register are reset.

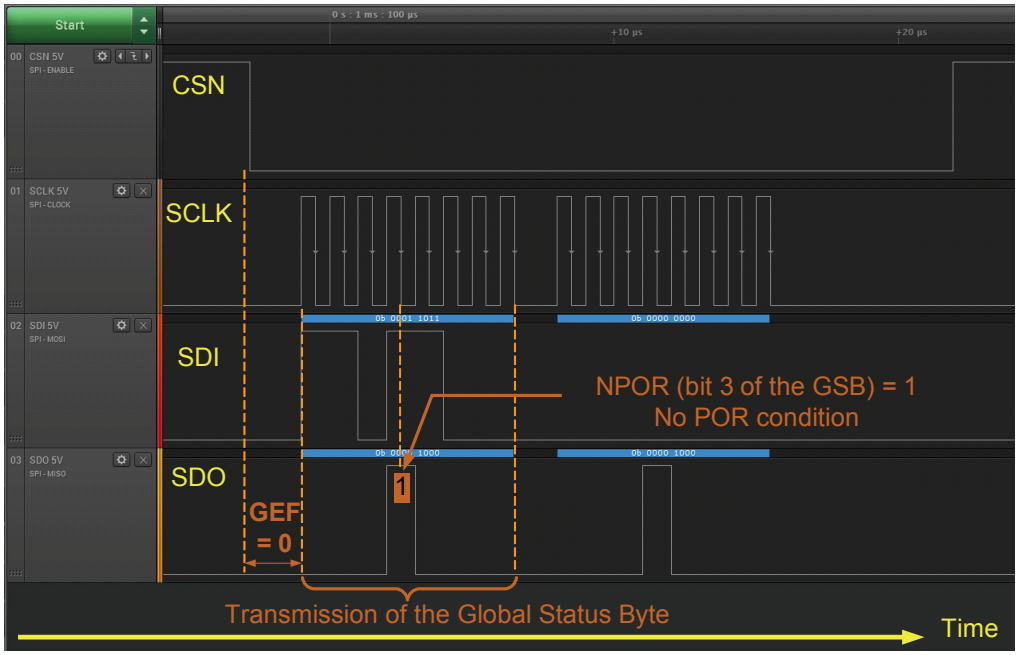


Figure 9 Example of GEF and Global Status Register when no failure is detected

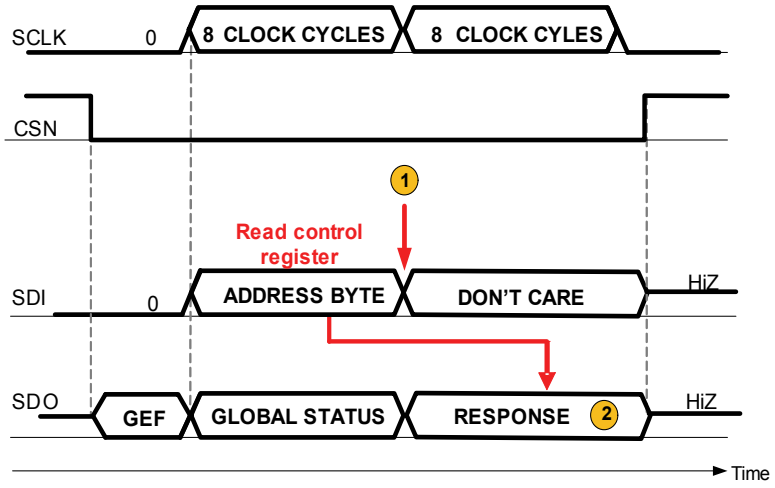
5.4 In-Frame Response

The protocol of the TLE941xy family supports an **in-frame response**: A request and the corresponding response are sent during the same SPI frame.

The TLE941xy receives during the first eight SCLK cycles the address byte (request). The address byte is decoded by the device when the first byte is received. Then it sends the corresponding response data during the following eight SCLK cycles.

Figure 10, Figure 11, Figure 12 and Figure 13 show the in-frame response of the TLE941xy devices during:

- a read access to a control register
- a write access to a control register
- a read access to a status register
- a clear access to a status register

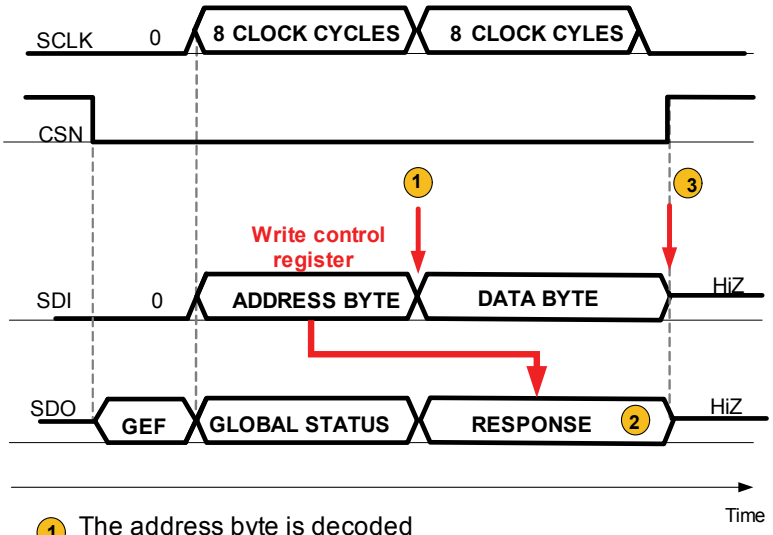


1 The address byte is decoded (e.g. read control register HB_ACT1_CTRL)

2 The content of the addressed control register (e.g. register HB_ACT1_CTRL) is sent by SDO within the same frame

Figure 10 Reading a control register

For a write access to a control register, the new data byte is written into the corresponding register at the rising edge of CSN signal (see **Figure 11**).

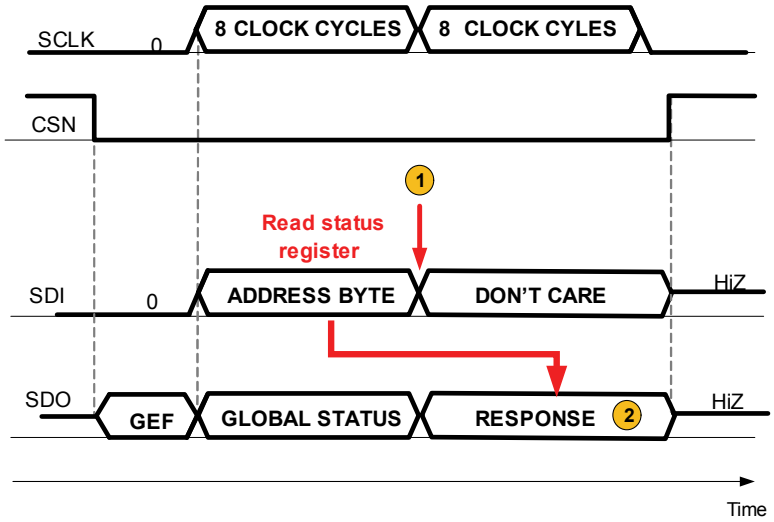


1 The address byte is decoded (e.g. write control register e.g. HB_ACT1_CTRL)

2 The previous content of the addressed control register is sent by SDO within the same frame

3 The new data byte is written in the addressed control register

Figure 11 Writing new data in a control register

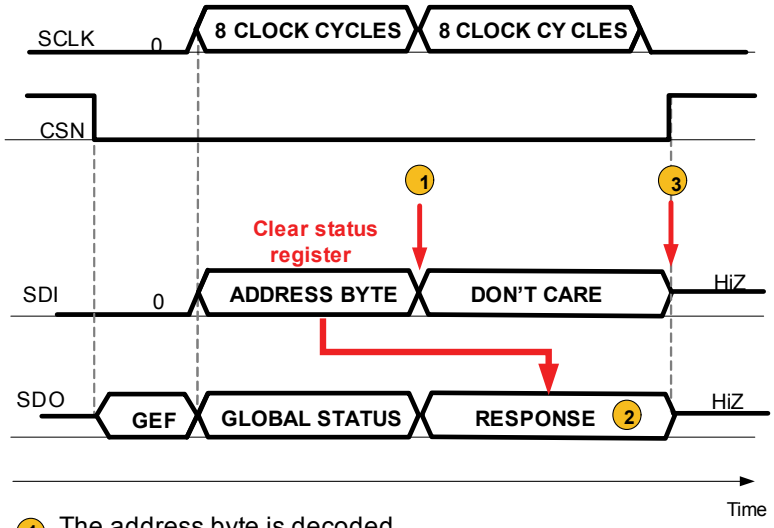


1 The address byte is decoded (e.g. Read status register SYS_DIAG_2)

2 The content of the addressed status register is sent by SDO within the same frame

Figure 12 Reading a status register

A status register is cleared at the rising edge of the CSN signal (see **Figure 13**).



1 The address byte is decoded (e.g. Clear status register SYS_DIAG_2)

2 The content of the addressed status register is sent by SDO within the same frame

3 The addressed status register is cleared

Figure 13 Clearing a status register

5.5 Comparison with the TLE841xy Family

The TLE84110EL and TLE84106EL are the predecessors of the TLE94110EL and TLE94106EL. This section gives an overview of the differences between the SPI protocols of the TLE941xy and the TLE841xyEL families.

Table 4 SPI protocol - Comparison between TLE941xy and TLE841xyEL

TLE941xy	TLE84110/06EL
The least significant bit is sent first	The most significant bit is sent first
In-frame response is supported	In-frame response is not supported
Reading the content of the control registers is possible	Reading the content of the control registers is not possible
Additional control and status registers to support new features and a more detailed diagnostic: e.g. internal PWM generator, frequency modulation of the oscillator, individual diagnostic of overcurrent and open load failure for each high side and low sides	

6 SPI bus with multiple slaves

Two configurations are possible when the SPI bus consists of several slave devices: the individual slave configuration and the daisy chain configuration. The TLE941xy devices are compatible with both options.

6.1 Individual Slave Configuration

In the individual slave configuration, the microcontroller controls the CSN pin of each slave separately to select one single slave at the beginning of each transmission. See example with three SPI slaves in **Figure 14**.

Because the slaves share the same clock signal and data lines, only the slave, whose CSN is pulled Low accepts the SPI communication and responds to the incoming request.

In this configuration, SPI frames are shorter compared to a daisy chain, but at the cost of additional microcontroller outputs for each slave CSN pin.

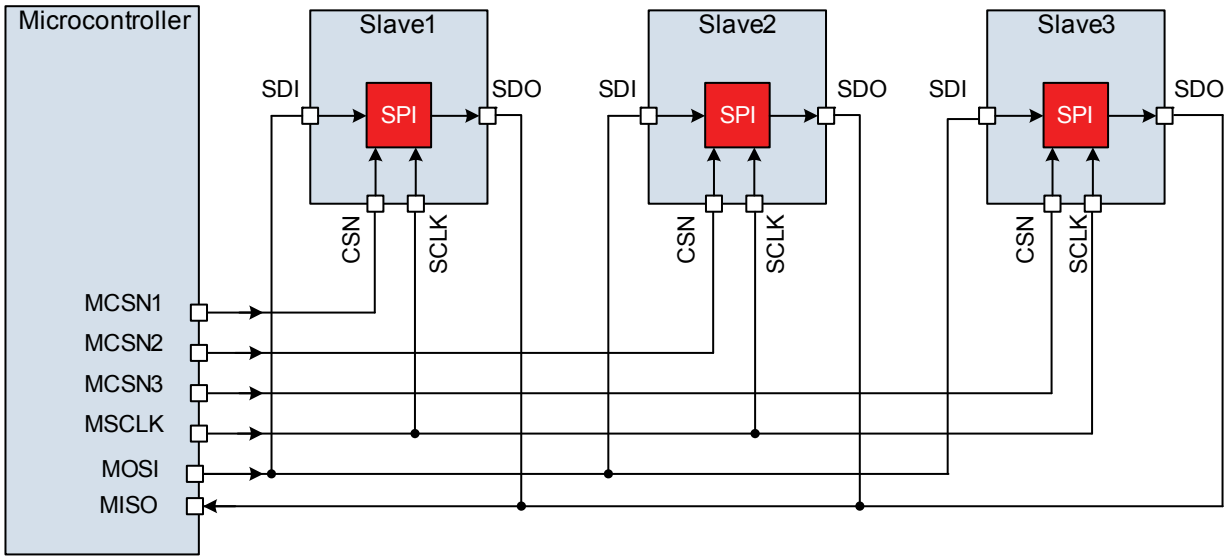


Figure 14 SPI Bus in independent slave configuration

The LABT bit must be 1 in this configuration. Otherwise the TLE941xy interprets the incoming frame as a SPI protocol error.

6.2 Daisy Chain

In the daisy chain topology, one master is connected to several slaves as shown in **Figure 15**. The main benefit of this configuration is the lower number of required microcontroller outputs: One single output controls the CSN pins of all slaves.

The SPI frame for the last device in the daisy chain must first go through the previous slaves. Therefore, the SPI frames in this configuration are longer: the number of SCLK pulses for one SPI frame in daisy chain is the sum of the SCLK pulses of each device present in the chain.

With standard SPI protocols supporting daisy chain configurations, the requests are interpreted at the end of the SPI frames, after the CSN rising edge. The requests and the corresponding responses cannot be transmitted during the same frame. Therefore two consecutive SPI frames are required in order to read a status register. The first one for the request, the second one for the response corresponding to the request. Such SPI protocols do not support an in-frame response.

In contrast to standard SPI protocols, the patent-pending protocol of the TLE941xy supports in-frame responses in daisy chain configuration. One single SPI frame is necessary to send the request to read a register of the TLE941xy and to receive the corresponding response, reducing the SPI bus load.

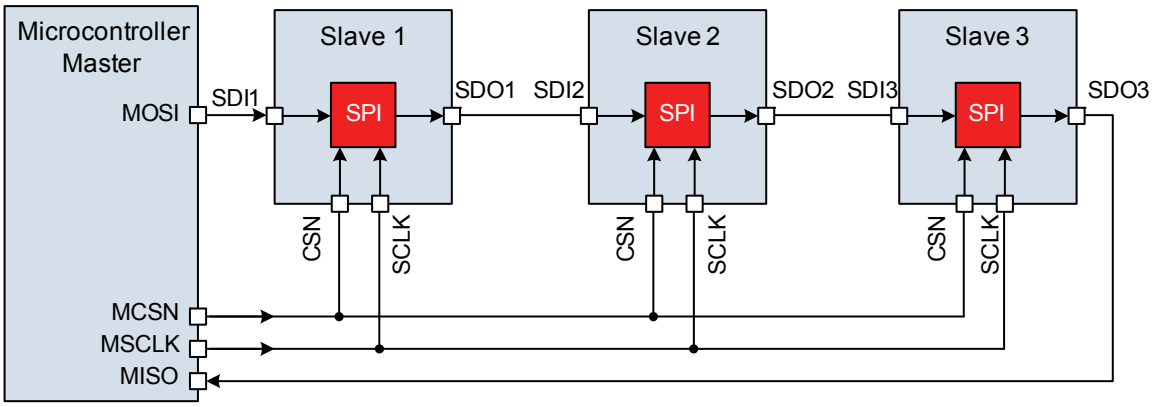


Figure 15 SPI Bus in daisy chain configuration

By convention, the first slave device (Slave 1) is the device whose SDI is connected to the MOSI. The SDO of the last device (Slave3 in **Figure 15**) is connected to the MISO.

6.2.1 Daisy chain only with TLE941xy devices

This section deals with daisy chains consisting only of devices belonging to the TLE941xy family.

In this configuration, the microcontroller must send the address and data bytes in the following order:

1. All address bytes are sent first:
   a) the address byte of TLE941xy_1 is sent first, followed by the address byte of the TLE941xy_2 etc,...
   b) the LSB of each address byte must be equal to 1[1)].
   c) the LABT[2)] of the last address byte must be equal to 1, while the LABT of the other address byte must be equal to 0.

1) An address byte with LSB = 0 is reported by the TLE941xy as a communication failure. Consequently the SPI_ERR bit is set.

2) See **Figure 5**

2. Then, the data bytes are sent altogether once the address bytes have been transmitted
   a) the data of the TLE941xy_1 is sent first followed by, the data of the TLE941xy_2 etc,...

During the same SPI frame, the microcontroller receives:

1. an OR combination of the GEF of each TLE941xy, between the CSN falling edge and the first SCLK rising edge[1)]
2. the Global Status Registers of the different devices in the reverse order.
3. the response bytes of the TLE941xy in reverse order.

Figure 17 and **Figure 18** respectively **Figure 20** and **Figure 21**, show the structure of the SPI frames for two, respectively three TLE941xy in daisy chain.

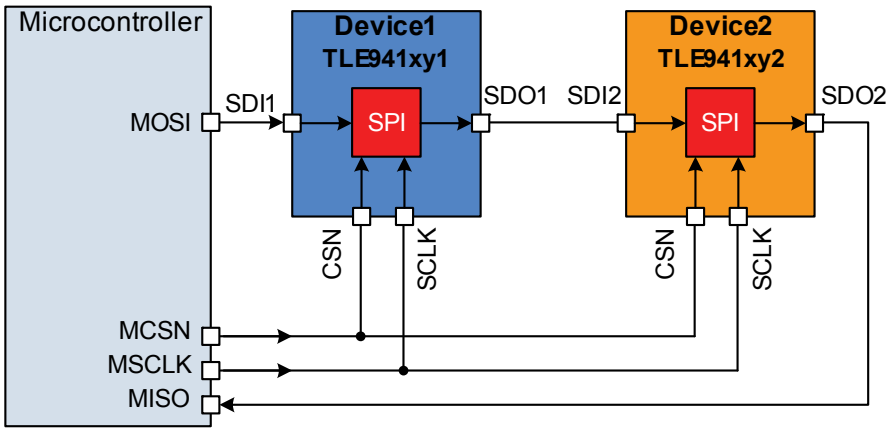


Figure 16 Daisy chain with two TLE941xy

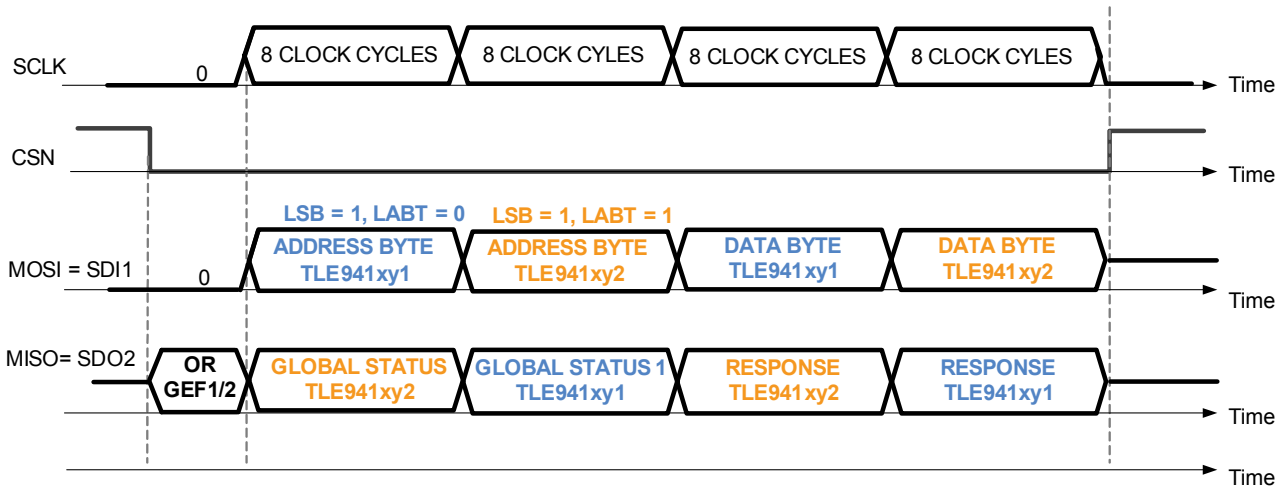


Figure 17 SPI Frame with two TLE941xy in daisy chain

1) MOSI must be 0 between the CSN falling edge and the first SCLK rising edge

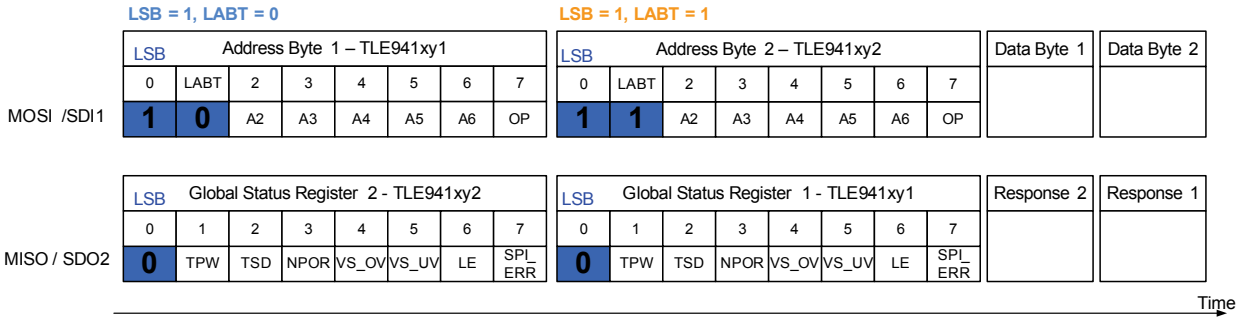


Figure 18 Detailed SPI Frame with two TLE941xy in daisy chain

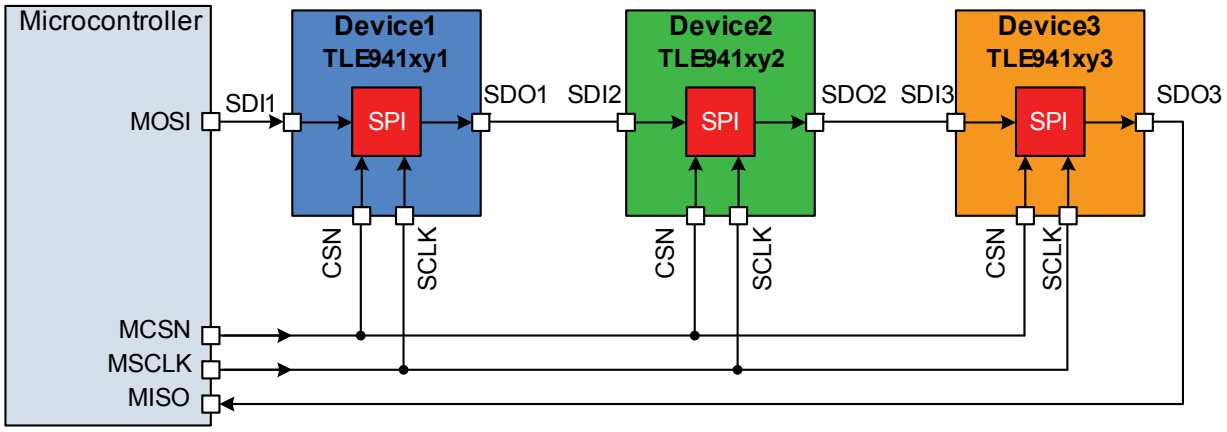


Figure 19 Daisy chain with three TLE941xy

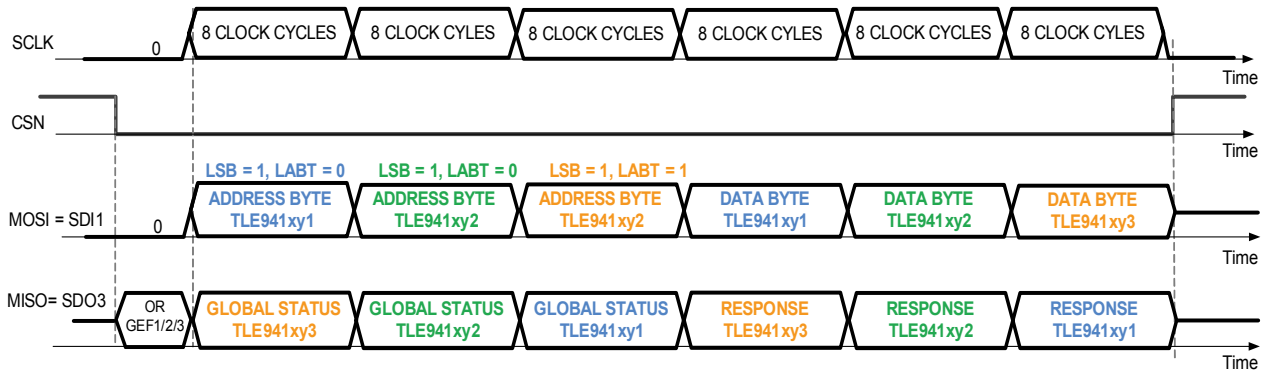


Figure 20 SPI Frame with three TLE941xy in daisy chain

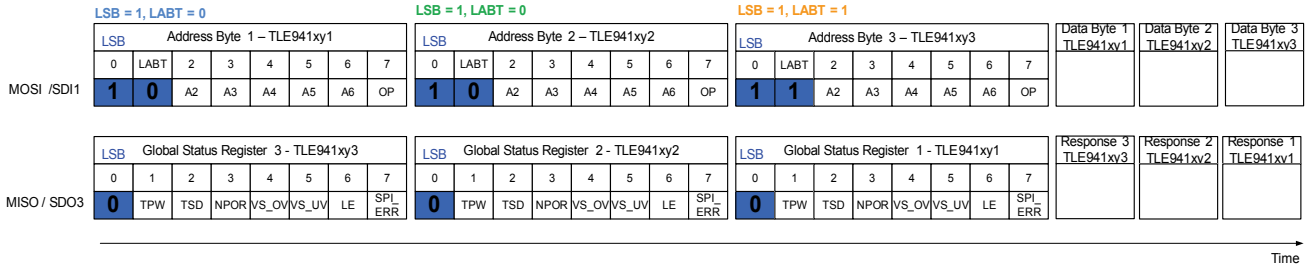


Figure 21 Detailed SPI Frame with three TLE941xy in daisy chain

6.2.2 Daisy chain with devices not belonging to the TLE941xy family

The TLE941xy can also be connected in daisy chain with devices not belonging to the TLE941xy family, provided that these devices fulfill the following requirements:

- they support the same Clock Polarity and Clock Phase: CPOL = 0, CPHA = 1
- the number of SCLK cycles during one SPI frame is a multiple of 8
- the required SPI timings are compatible with those of the TLE941xy family
- they are connected at the end of the daisy chain, whereas the TLE941xy are connected at the beginning of the daisy chain (refer to examples **Figure 22**, **Figure 24**, and **Figure 26**).

In this configuration, the microcontroller must send the information in the following order:

1. All address bytes of the TLE941xy are sent first:
   a) the address byte of TLE941xy_1 is sent first, followed by the address byte of the TLE941xy_2 etc,...
   b) the LSB of all address bytes must be equal to 1
   c) the LABT of the last address byte must be equal to 1, while the LABT of the other address bytes must be equal to 0
2. The data bytes are sent altogether once the address bytes have been transmitted
   a) the data of the TLE941xy_1 is sent first followed by, the data of the TLE941xy_2 etc,...
3. Then the requests of the devices not belonging to the TLE941xy family must be sent in the reverse order

The microcontroller receives:

1. an OR combination of the GEF of each TLE941xy, between the CSN falling edge and the first SCLK rising edge, provided that the other devices copy the signal present on their SDI to their SDO[1)]
2. the response bytes of the devices not belonging to the TLE941xy family in reverse order
3. the Global Status Registers of the TLE941xy devices in the reverse order
4. the response of the TLE941xy devices in reverse order

1) MOSI must be 0 between the CSN falling edge and the first SCLK rising edge

Example of daisy chain with one TLE941xy and one TLE84110EL

Between the CSN falling edge and the SCLK first rising edge, the TLE84110EL copies the signal present to its SDI (= GEF) to its SDO, which allows the microcontroller to read the GEF during this phase (**Figure 23**).

Note: the TLE84110EL does not support an in-frame response. Instead, the response sent during a SPI frame corresponds to the request from the previous SPI frame.

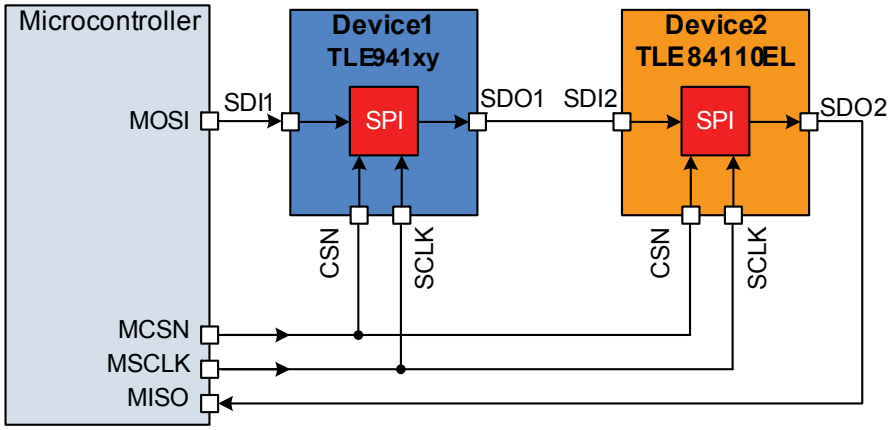


Figure 22 Daisy chain with one TLE941xy and one TLE84110EL

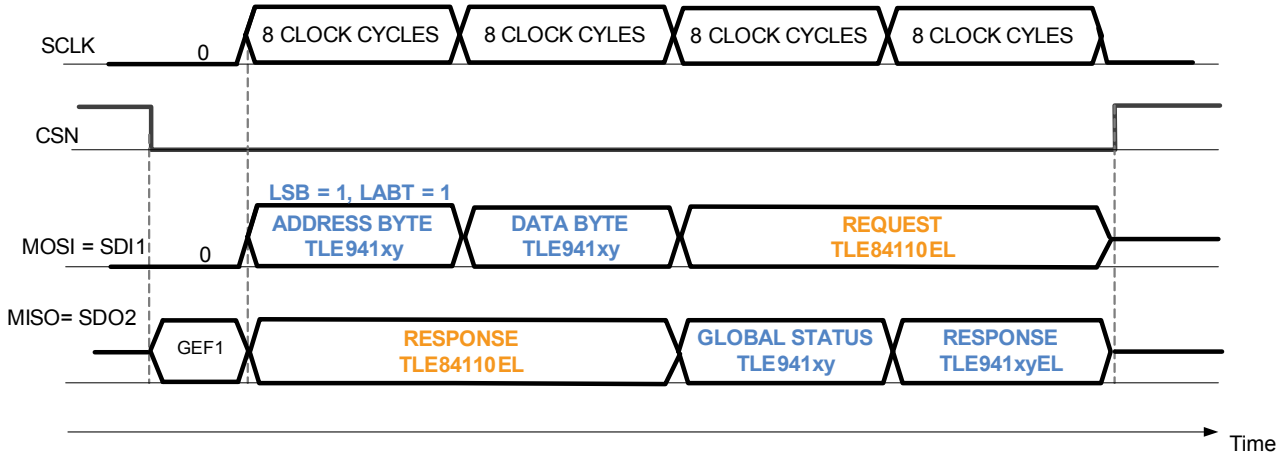


Figure 23 SPI frame with one TLE941xy and one TLE84110EL in daisy chain

Example of daisy chain with two TLE941xy and one TLE84110EL

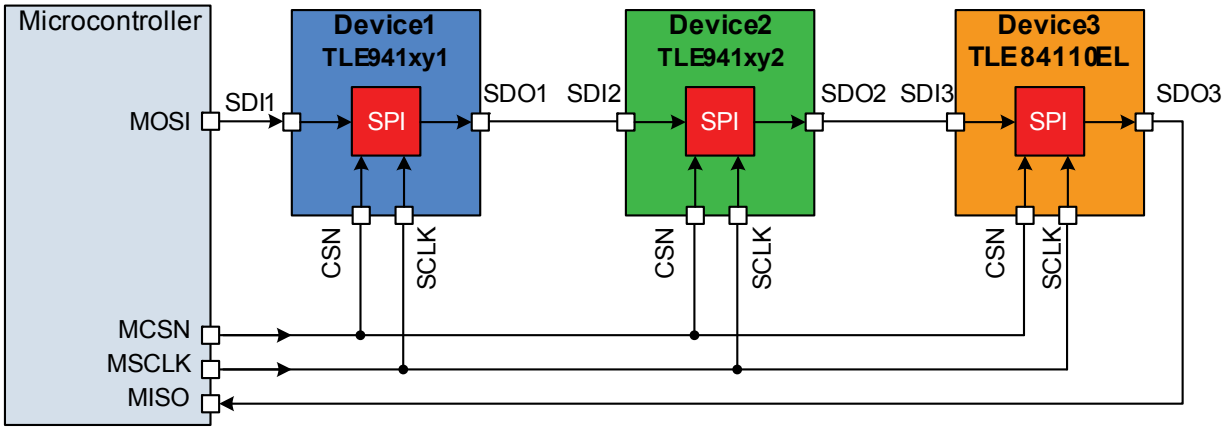


Figure 24 Daisy chain with two TLE941xy and one TLE84110EL

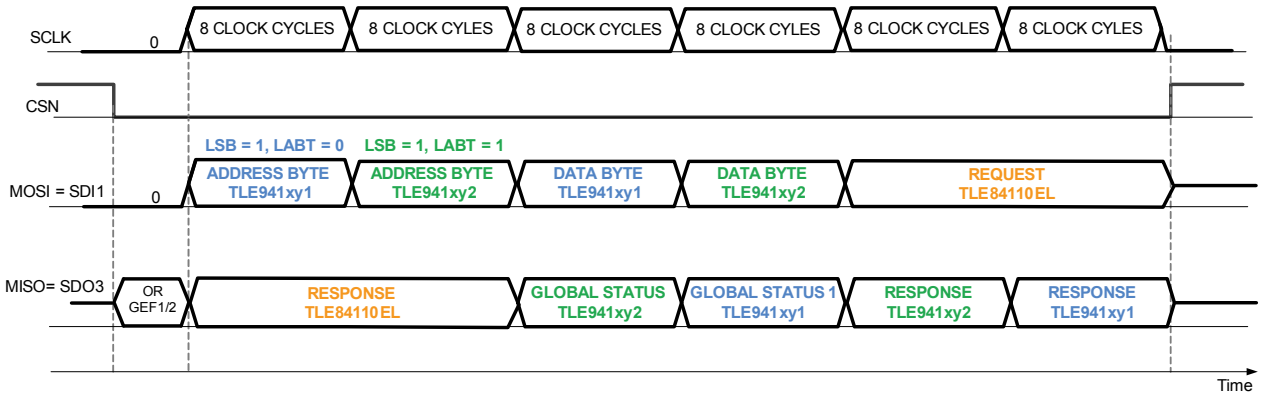


Figure 25 SPI frame with two TLE941xy and one TLE84110EL in daisy chain

Example of daisy chain with one TLE941xy and two TLE84110EL

Figure 26 shows the SPI daisy chain with one TLE941xy and two TLE84110EL.

The microcontroller sends first the address byte of the TLE941xy followed by the request for the TLE84110EL_2, followed by the request for the TLE84110EL_1 (refer to Figure 27).

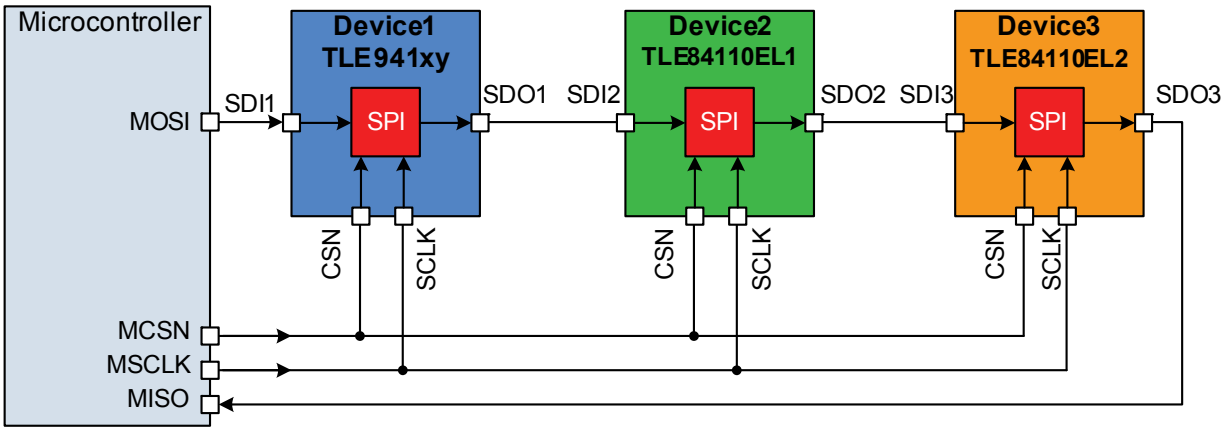


Figure 26 Daisy chain with one TLE941xy and twoTLE84110EL

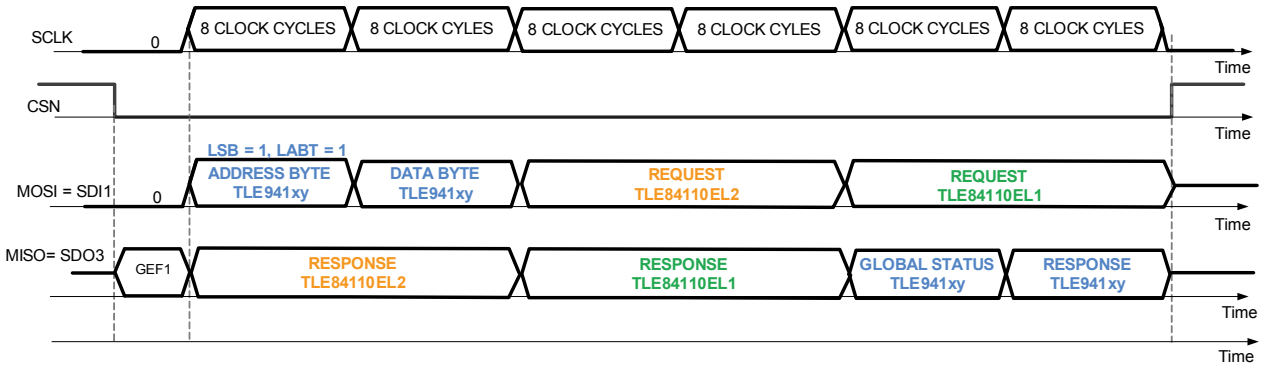


Figure 27 SPI frame with one TLE941xy and twoTLE84110EL in daisy chain

7 Fast diagnostic

The TLE941xy family offers the possibility to verify if one or several devices have detected a fault condition without sending a complete SPI frame. Instead, it is sufficient to pull down the CSN pin of the corresponding device, without any clock cycle, to read the Global Error Flag. In this case, the SDO pin acts as an fault pin.

The duration of CSN Low phase must be at least 75ns, in order to have a valid Global Error Flag at the SDO pin (t_{ENSDO} is the relevant datasheet parameter).

Attention: SDI must be Low when CSN is pulled down.

If SDI = 0, when CSN = 0, SDO reports the Global Error Flag (see **Figure 28**).

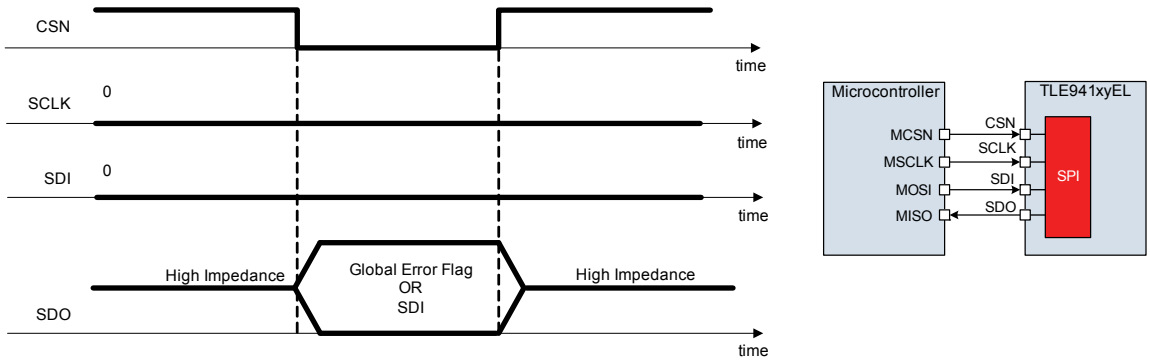


Figure 28 Example of fast diagnostic with one TLE941xy device

The advantages of this fast diagnostic is even bigger in daisy chain configuration, because a long SPI frame is saved. If SDI1 = 0 when CSN =0 (see **Figure 28**), then the microcontroller reads directly and OR combination of the Global Error Flags of each TLE941xy present in the daisy chain.

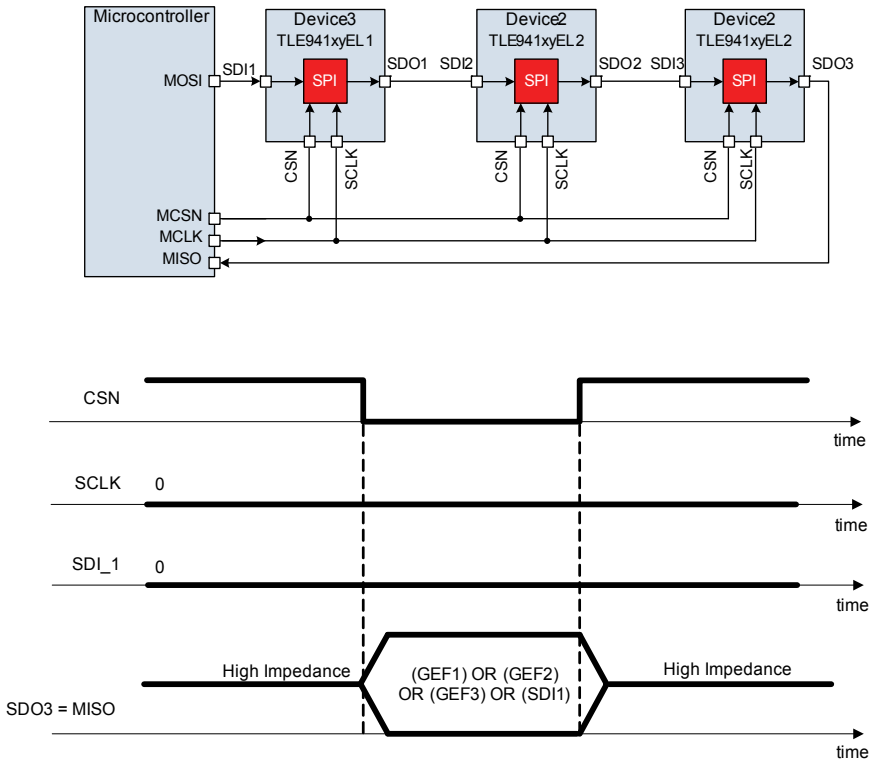


Figure 29 Example of fast diagnostic with three TLE941xy devices in daisy chain

8 SPI Failure Mode and Effect Analysis

This chapter deals with the detection of failures of one of the SPI line and give a Failure Mode Effect Analysis (FMEA) of the SPI interface. The common failures are considered: One of the SPI signal is either shorted to 0, shorted to 1, or left open.

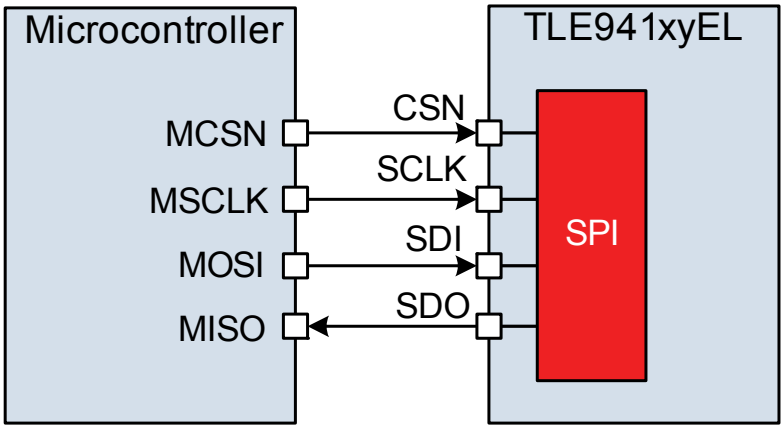


Figure 30 Definition of SPI signals

8.1 Detection of failures on SDI

The TLE941xy reports a SPI error by setting the SPI_ERR bit if the SDI line is shorted to 0 or to 1:

SDI line is shorted to “0”

The communication protocol of the TLE941xy requires the LSB (Less Significant Bit or Bit0) of an address byte to be 1. If the SDI line is shorted to 0, no address byte is detected during the SPI frame. Consequently the TLE941xy reports a SPI error (SPI_ERR = 1) during the next SPI frame and the GEF is set to 1.

SDI line is left open

The TLE941xy integrates a pull-down resistor at the SDI input. If the microcontroller initiates a communication, while the SDI line is open, the device will react as if SDI was shorted to 0. Consequently, the SPI_ERR bit and the GEF are set.

SDI line is shorted to 1

If the SDI line is shorted to 1, in particular the TLE941xy receives the address byte 0xFF. That is interpreted by the TLE941xy as an access to an invalid address. The TLE941xy reports a SPI error and the GEF is set to 1.

8.2 Failure on SDO line

This section shows that the SPI protocol of the TLE941xy enables the microcontroller to distinguish the following conditions:

- SDO shorted to 0
- SDO shorted to 1
- The device comes from a power-on reset
- SDO is not shorted and does not come from a power-on reset

Table 5 shows the content of the Global Error Flag and of the Global Status Register (GSR) in the different conditions.

Table 5 GEF and Global Status Register in different conditions[1)]

		Global Status Register							
	-	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Condition	**GEF**	**SPI_ERR**	**LE**	**VUV**	**VSOV**	**NPOR**	**TSD**	**TPW**	**LSB**
SDO line Shorted to “0”	0	0	0	0	0	0	0	0	0
SDO line Shorted to “1”	1	1	1	1	1	1	1	1	1
Power-On Reset (and no shorted SDO line)	1	x	x	x	x	0	x	x	0
No Power-On Reset (and no shorted SDO line)	x	x	x	x	x	1	x	x	0

1) x = don’t care

Condition 1: SDO line is shorted to 0

The microcontroller reads GEF = 0 and all bits of the GSR are 0

Condition 2: SDO line is shorted is to 1

The microcontroller reads GEF = 1 and all bits of the GSR are 1

Condition 3: Power-On Reset (and no shorted SDO line)

The microcontroller reads GEF = 1 and NPOR = 0 (refer to example in Figure 8). This combination is distinct from Condition 1 and Condition 2.

Condition 4: No Power-On Reset (and no shorted SDO line)

The microcontroller reads: NPOR = 1 and LSB of the GSR = 0 (refer to example in Figure 9). This combination is distinct from Condition 1, Condition 2 and Condition 3.

The microcontroller can differentiate these four conditions based on the information provided by the GEF and the GSR. It can also detect the first three conditions as a failure of the SPI bus.

SDO line open

The microcontroller detects that SDO shorted either to 0 or to 1, depending on the stray resistance which determines the level on SDO

8.3 Failure on SCLK line

SCLK line is shorted to 0

If SCLK is shorted to 0 during the SPI communication, then no clock cycle is detected by the TLE941xy and SDO is equal to (GEF) AND (SDI) when CSN is Low.

Two cases are possible: Either GEF = 0 or GEF = 1 before the SCLK failure.

Case 1: If GEF = 0 before the failure, then SDO = (GEF) OR (SDI) = SDI (see **Figure 31**). The microcontroller expects the first byte to be the Global Status Register, whose LSB must be 0 (refer to **Table 2**). However, since SDO = SDI, the microcontroller receives the address byte, whose LSB = 1 (See **Chapter 5.1**).

According to the SPI protocol of the TLE941xy, the LSB received by SDO should be 0. This inconsistency can be used by the microcontroller to detect the failure.

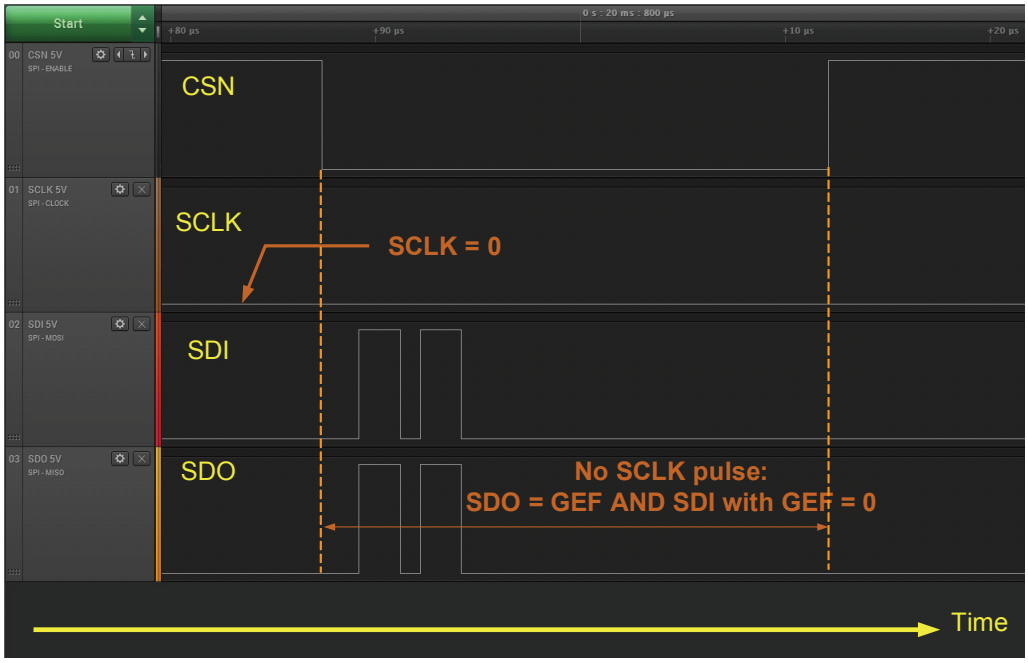


Figure 31 Example of SPI frame with SCLK signal shorted to 0 and GEF = 0

Case 2: If GEF = 1 before the failure, then SDO = (GEF) OR (SDI) = 1 during the complete SPI frame. The microcontroller interprets the incoming frame as a shorted SDO line. See **Figure 32**.

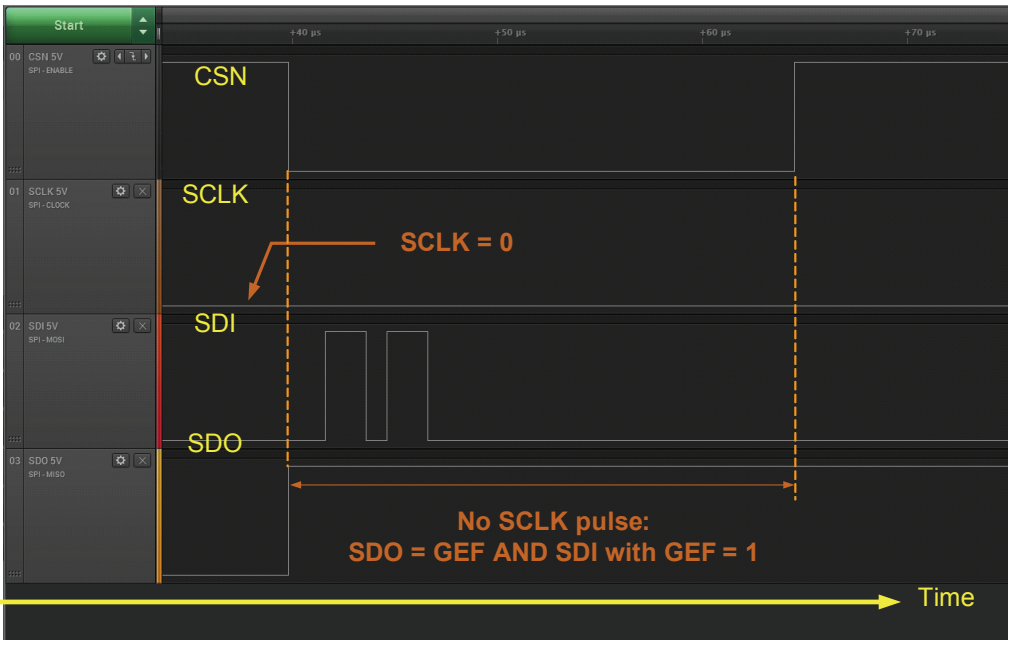


Figure 32 Example of SPI frame with SCLK signal shorted to 0 and GEF = 1

In both cases, the microcontroller reads SDO frames which are not allowed in normal conditions.

SCLK line is open

SCLK has an internal pull-down resistor. This case is equivalent to SCLK shorted to 0.

SCLK line is shorted to 1

The TLE941xy family requires the SCLK signal to be 0 at least 125 ns before the CSN falling edge (refer to the datasheet, parameter t_{BEF}). This condition is not met, therefore the TLE941xy sets SPI_ERR and GEF bits. In the following SPI frames, the GEF (=1) is reported during the complete SPI frame. The microcontroller interprets the incoming frame as a shorted SDO to 1. Refer to **Figure 33**.

According to the SPI protocol of the TLE941xy, the LSB received by SDO should be 0. This inconsistency can be used by the microcontroller to detect the failure.

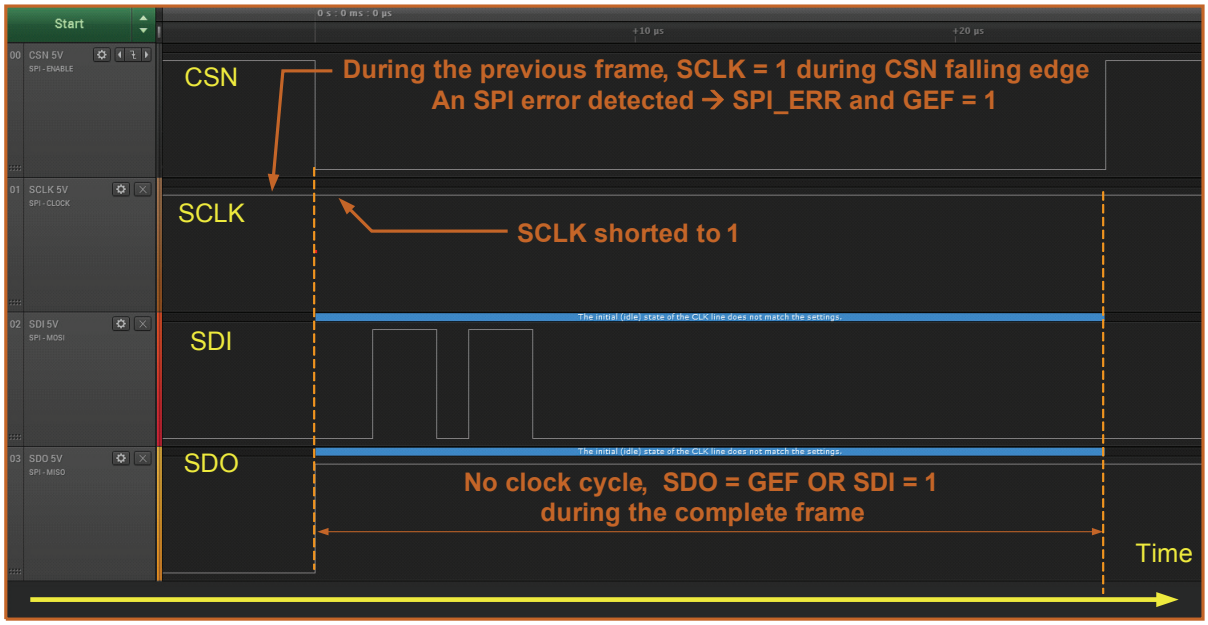


Figure 33 Example of SPI frame with SCLK signal shorted to 1

8.4 Failure on CSN line

CSN line is shorted to 0

If CSN is shorted to 0, then during the second SPI frame (while CSN is kept to 0) the TLE941xy copies the signal present on SDI to SDO (see **Figure 34**). This failure is similar to SCLK shorted to 0 with GEF = 0:

The microcontroller expects the first byte to be the Global Status Register, whose LSB must be 0 (refer to **Table 2**). However, since SDO = SDI, the microcontroller receives the address byte, whose LSB = 1 (See **Chapter 5.1**).

According to the SPI protocol of the TLE941xy, the LSB received by SDO should be 0. This inconsistency can be used by the microcontroller to detect the failure.

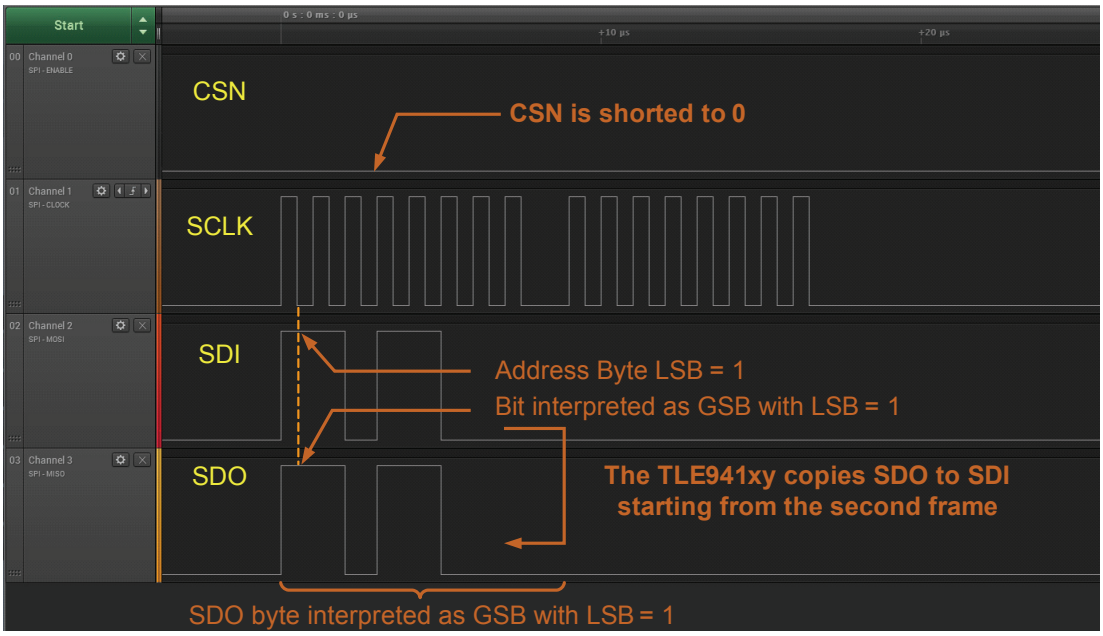


Figure 34 SPI frame with CSN shorted to 0

CSN line is shorted to 1

If the CSN is shorted to 1, SDO of the TLE941xy is in high impedance. The microcontroller detects that SDO shorted either to 0 or to 1, depending on the stray resistance which determines the level on SDO.

8.5 Failure Mode and Effect Analysis of the SPI bus

This section provides a FMEA of the SPI bus, considering the following failures:

- an SPI signal shorted to 0
- an SPI signal shorted to 1
- an SPI signal left open

Table 6 SPI Failure Mode and Effect Analysis

Failure Mode	Potential Effect	Detection	Comments
SDI shorted to 0	SPI commands are not transmitted to the TLE941xy[1)]	Yes	SPI_ERR bit set, see **Chapter 8.1**
SDI shorted to 1	SPI commands are not transmitted to the TLE941xy[1)]	Yes	SPI_ERR bit set, see **Chapter 8.1**
SDI disconnected	SPI commands are not transmitted to the TLE941xy	Yes	SPI_ERR bit set, see **Chapter 8.1**
SDO shorted to 0	µC does not receive correct data from TLE941xy	Yes	See **Chapter 8.2**
SDO shorted to 1	µC does not receive correct data from TLE941xy	Yes	See **Chapter 8.2**
SDO disconnected	µC does not receive correct data from TLE941xy	Yes	See **Chapter 8.2**
SCLK shorted to 0	No SPI communication[1)]	Yes	See **Chapter 8.3**

Table 6 SPI Failure Mode and Effect Analysis

Failure Mode	Potential Effect	Detection	Comments
SCLK shorted to 1	No SPI communication[1)]	Yes	See **Chapter 8.3**
SCLK disconnected	No SPI communication	Yes	See **Chapter 8.3**
CSN shorted to 0	Write and clear commands are not executed	Yes	See **Chapter 8.4**
CSN shorted to 1	No SPI communication[1)]	Yes	See **Chapter 8.4**
CSN disconnected	No SPI communication[1)]	Yes	See CSN shorted to 1

1) The short circuit can cause the microcontroller output to deliver a high current. If the current exceeds the maximum rating of the microcontroller I/O, it is recommended to place a serial resistor.

9 Conclusion

The patent-pending SPI protocol of the TLE941xy family presents two main advantages: It supports an in-frame response in daisy chain and with independent slave selection. This feature reduces the number of SPI frames required to read a status register and lowers the SPI bus load. It also enables the detection of a failure on the SPI bus. This document has also given hints to handle the communication with multiple slaves in daisy chain configuration, provided that the devices not belonging to the TLE941xy fulfill the pre-requisites.

10 Additional Information

- References: Datasheet of
  - TLE94112EL
  - TLE94110EL
  - TLE94108EL
  - TLE94106EL
  - TLE94104EP
  - TLE94103EP
- For further information you may contact **http://www.infineon.com/**

11 Revision History

Revision	Date	Changes
1.0	2016-04-25	First release

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