CAN FD signal improvement transceiver

Features

- Compliant to ISO 11898-2:2024, SAE J2284-4/-5
- Loop delay symmetry for *controller area network (CAN)* FD data frames up to 8 Mbit/s
- Certified according to latest Toyota conformance test performed by VeLIO (Vehicle LAN Interoperability and Optimization)
- Standby mode with minimized quiescent current
- Wake-up indication on the RxD output
- Very low *electromagnetic emission (EME)* allows the use without additional common mode choke
- Excellent *electrostatic discharge (ESD)* robustness ±8 kV *human body model (HBM)* and IEC 61000-4-2
- CAN short circuit proof to ground, battery and VCC
- TxD timeout function
- Very low CAN bus leakage current in power-down state
- Overtemperature protection
- Protected against automotive transients according to ISO 7637 and SAE J2962-2
- Green Product (RoHS compliant)

RoHS
Green
AEC Qualified
CAN FD
CAN FD SIC

Potential applications

- Gateway module
- Body control module (BCM)
- Engine control unit (ECU)
- ADAS
- Radar

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE9371SJ is a first generation CAN FD signal improvement transceiver, used in HS *CAN* for automotive applications and also for industrial applications. It is designed to fulfill the requirements of ISO 11898-2:2024 physical layer specification as well as SAE J1939 and SAE J2284.

The TLE9371SJ is available in a halogen free and *Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS)* compliant PG-DSO-8 package.

As an interface between the physical bus layer and the HS CAN, the TLE9371SJ protects the microcontroller against interference generated in the network. A very high *ESD* robustness and the optimized *residual fault (RF)* immunity allows the use in automotive applications without additional protection devices, such as suppressor diodes or common mode chokes.

While the TLE9371SJ is not supplied the transmitter is switched off and behaves passive with the lowest possible load to all other nodes of the HS CAN.

Based on the high symmetry of the CANH and CANL output signals, the TLE9371SJ provides very low *EME* within a wide frequency range. The TLE9371SJ fulfills stringent *electromagnetic compatibility (EMC)* test limits without additional external circuitry, such as a common mode choke.

Due to the excellent symmetry combined with the optimized delay symmetry of the receiver the TLE9371SJ supports CAN FD data frames. Depending on the size of the network and its parasitic effects the device supports a transmission rate up to 8 Mbit/s.

Dedicated low-power modes, like standby mode require very low quiescent current while the device is powered up. In standby mode the typical quiescent current on V_{CC} is below 10 µA while the device can still wake up from a bus signal on the HS CAN bus.

Fail-safe features such as overtemperature protection, output current limitation and the TxD timeout feature protect the TLE9371SJ and the external circuitry from damage.

Type	Package	Marking
TLE9371SJ	PG-DSO-8	9371

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1 Block diagram

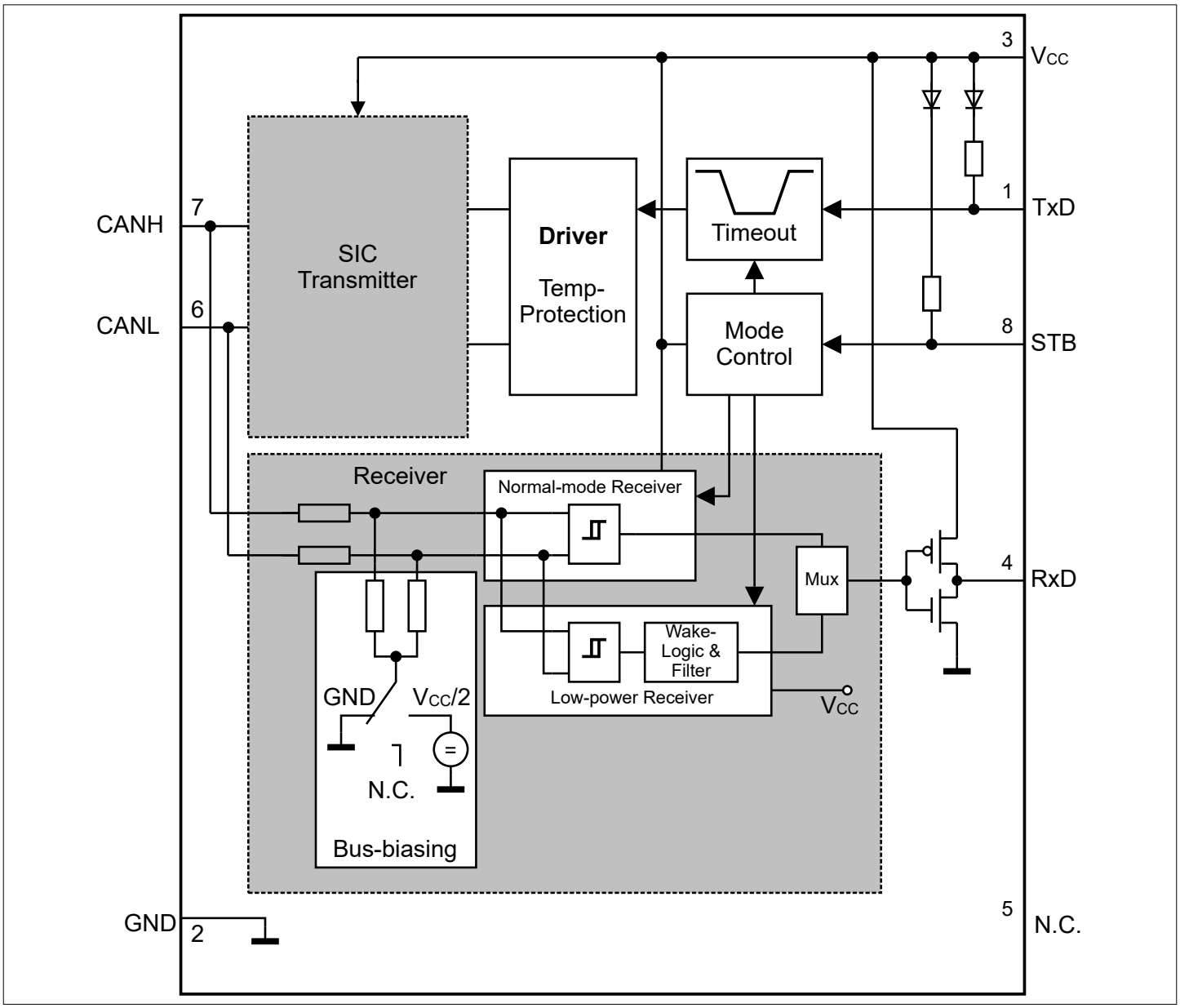

Figure 1 Block diagram

2 Pin configuration

2.1 Pin assignment

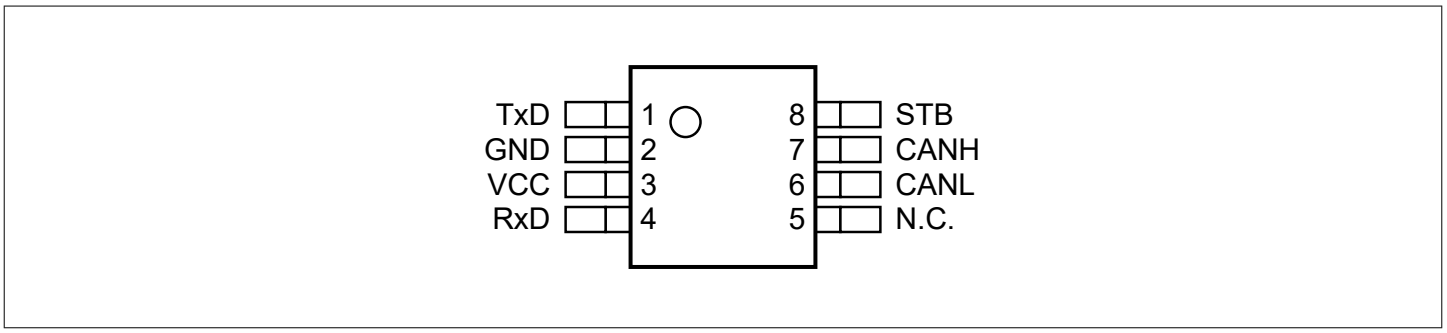

Figure 2 Pin configuration

2.2 Pin definitions and functions

Table 1 Pin definitions and functions

Pin No.	Symbol	Function
1	TxD	**Transmit data input;** Internal pull-up to V_{CC}, “low” for dominant state.
2	GND	**Ground**
3	VCC	**Transmitter supply voltage;** 1 uF decoupling capacitor to *ground (GND)* required.
4	RxD	**Receive data output;** “Low” in dominant state.
5	N.C.	**Not connected;** Pin has no function and is not connected internally.
6	CANL	**CAN bus low level I/O;** “Low” in dominant state.
7	CANH	**CAN bus high level I/O;** “High” in dominant state.
8	STB	**Standby input;** Internal pull-up to V_{CC}, “low” for normal-operating mode.

3 High-speed CAN functional description

HS *CAN* is a serial bus system that connects microcontrollers, sensors and actuators for real-time control applications. The use of the CAN within road vehicles is described by the international standard ISO 11898. According to the 7-layer OSI reference model the physical layer of a HS CAN bus system specifies the data transmission from one CAN node to all other available CAN nodes within the network. The physical layer specification of a CAN bus system includes all electrical specifications of a CAN. The CAN transceiver is part of the physical layer. The TLE9371SJ is a high-speed CAN transceiver with a dedicated bus wake-up function as defined in the latest ISO 11898-2 HS CAN standard.

3.1 High-speed CAN physical layer

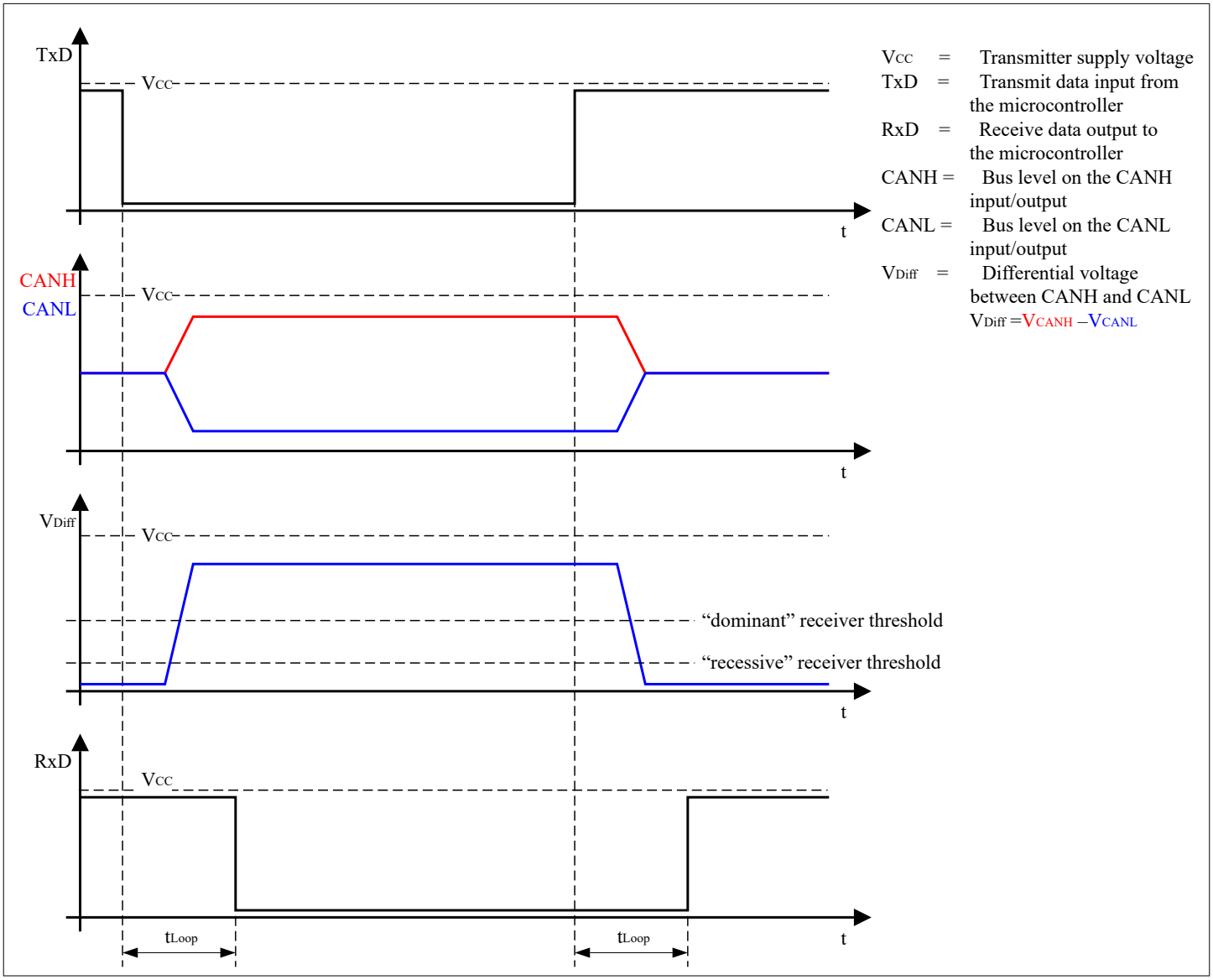

Figure 3 High-speed CAN bus signals and logic signals

The TLE9371SJ is a high-speed *CAN* transceiver, operating as an interface between the CAN controller and the physical bus medium. A HS CAN is a two wire, differential network, which allows data transmission rates up to 5 Mbit/s. The characteristic for a HS CAN is that the logical high level and logical low level (microcontroller interface) are converted into a differential signal (CAN bus interface) with the states dominant and recessive, see Figure 3.

The CANH and CANL pins are the interface to the CAN bus and both pins operate as an input and output. The RxD and TxD pins are the interface to the microcontroller. The pin TxD is the serial data input from the CAN controller, the RxD pin is the serial data output to the CAN controller. The device includes a receiver and a transmitter unit, allowing the transceiver to send data to the bus medium and monitor the data from the bus medium at the same time, see Figure 1. The device converts the serial data stream from the transmit data input TxD, into a differential output signal on the CAN bus, provided by the CANH and CANL pins. The receiver stage of the device monitors the data on the CAN bus and converts them to a serial, single-ended signal on the RxD output pin. A “low” signal on the TxD pin creates a dominant signal on the CAN bus. The receiver converts this dominant signal to a “low” signal on the RxD pin, see Figure 3. The feature of broadcasting data to the CAN bus and listening to the data traffic on the CAN bus simultaneously is essential to support the bit-to-bit arbitration within the network.

The voltage levels for HS CAN transceivers are defined in ISO 11898-2. Whether a data bit is dominant or recessive depends on the voltage difference between the CANH and CANL pins:

$V_{Diff} = V_{CANH} - V_{CANL}$.

For a dominant signal on the CAN bus the high-speed transceiver creates a differential signal of $V_{Diff} \geq 1.5$ V. To receive a recessive signal from the CAN bus the amplitude of the differential $V_{Diff} \leq 0.5$ V.

In a partially supplied high-speed CAN, the CAN bus nodes have different power supply conditions. Some nodes are connected to the common power supply while other nodes are disconnected from the power supply and in power-down state. Regardless of whether the CAN bus node is supplied or not, each node connected to the common bus media must not interfere with the communication. The device supports partially-supplied networks. In power-down state, the receiver input resistors are switched off and the transceiver input has a high resistance.

For permanently supplied ECUs, the HS CAN transceiver, the device provides a stand-by mode. In stand-by mode, the power consumption of the device is optimized to a minimum, while the device is still able to recognize wake-up patterns on the CAN bus and signal the wake-up event to the external microcontroller.

The voltage level on the digital input TxD and on the digital output RxD is determined by the power supply level at the V_{CC} pin. Depending on the voltage level at the V_{CC} pin, the signal levels on the logic pins (STB, TxD and RxD) are compatible with microcontrollers having a 5 V *input/output (I/O)* supply.

4 Modes of operation

The device supports the following modes of operation, see Figure 4:

- Normal-operating mode
- Standby mode

The mode selection input pin STB triggers mode changes. If a wake-up event occurs on the HS *CAN* bus, then the device indicates that on the RxD output pin in stand-by mode, but it does not trigger a mode change. An power-down event on the supply VCC powers down the device.

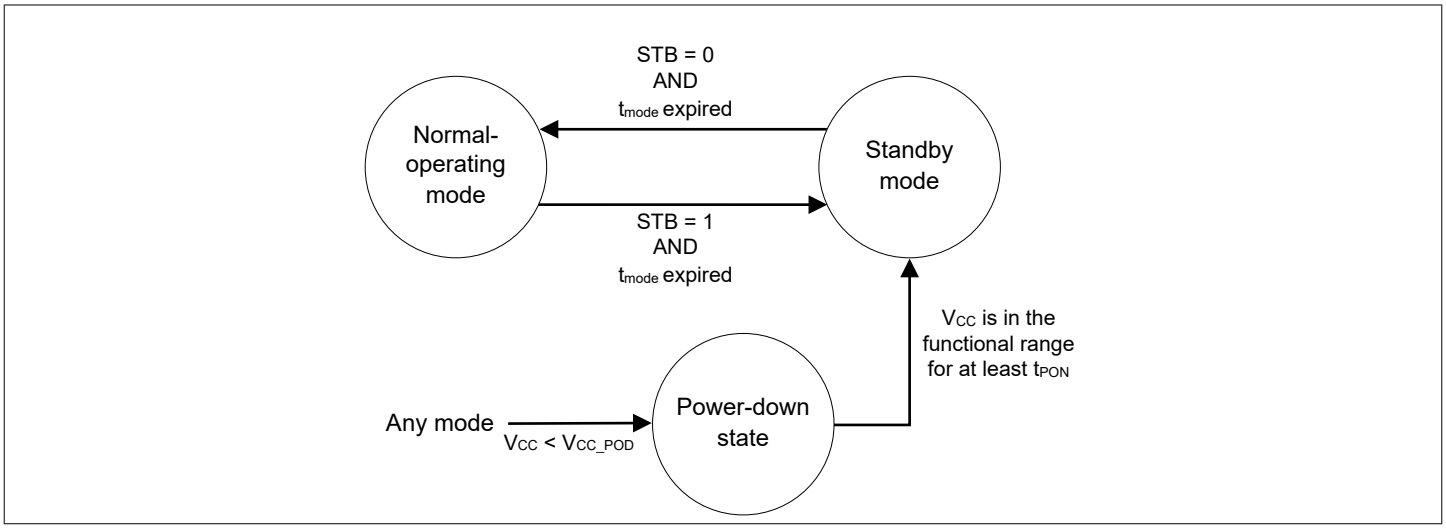

Figure 4 Mode state diagram

4.1 Normal-operating mode

In normal-operating mode all functions of the device are available and the device is fully functional. Data can be received from the HS *CAN* bus as well as be transmitted to the HS CAN bus.

- The transmitter is enabled and drives data stream on the TxD input pin to the bus pins CANH and CANL
- The receiver is enabled and converts the signals from the bus to a serial data stream on the RxD output pin
- The bus biasing is connected to $V_{CC}/2$ if $V_{CC} > V_{CC\_UV}$
- The TxD timeout function is enabled, see Chapter 5.4
- The overtemperature protection is enabled, see Chapter 5.6
- The undervoltage detection on V_{CC} is enabled, see Chapter 5.3

Conditions for entering normal-operating mode of the device:

- If $V_{CC} > V_{CC\_POD}$ and the STB pin is “low”, then the device enters normal-operating mode after t_{Mode} from standby mode, see Figure 4

If a “low” signal is applied on TxD input pin during a mode change to normal-operating mode, device disables the transmitter as long as “low” signal is applied on the TxD input pin. If a “high” signal is applied on the TxD input pin for at least t_{TxD_rel}, then the device enables the transmitter, see Figure 5.

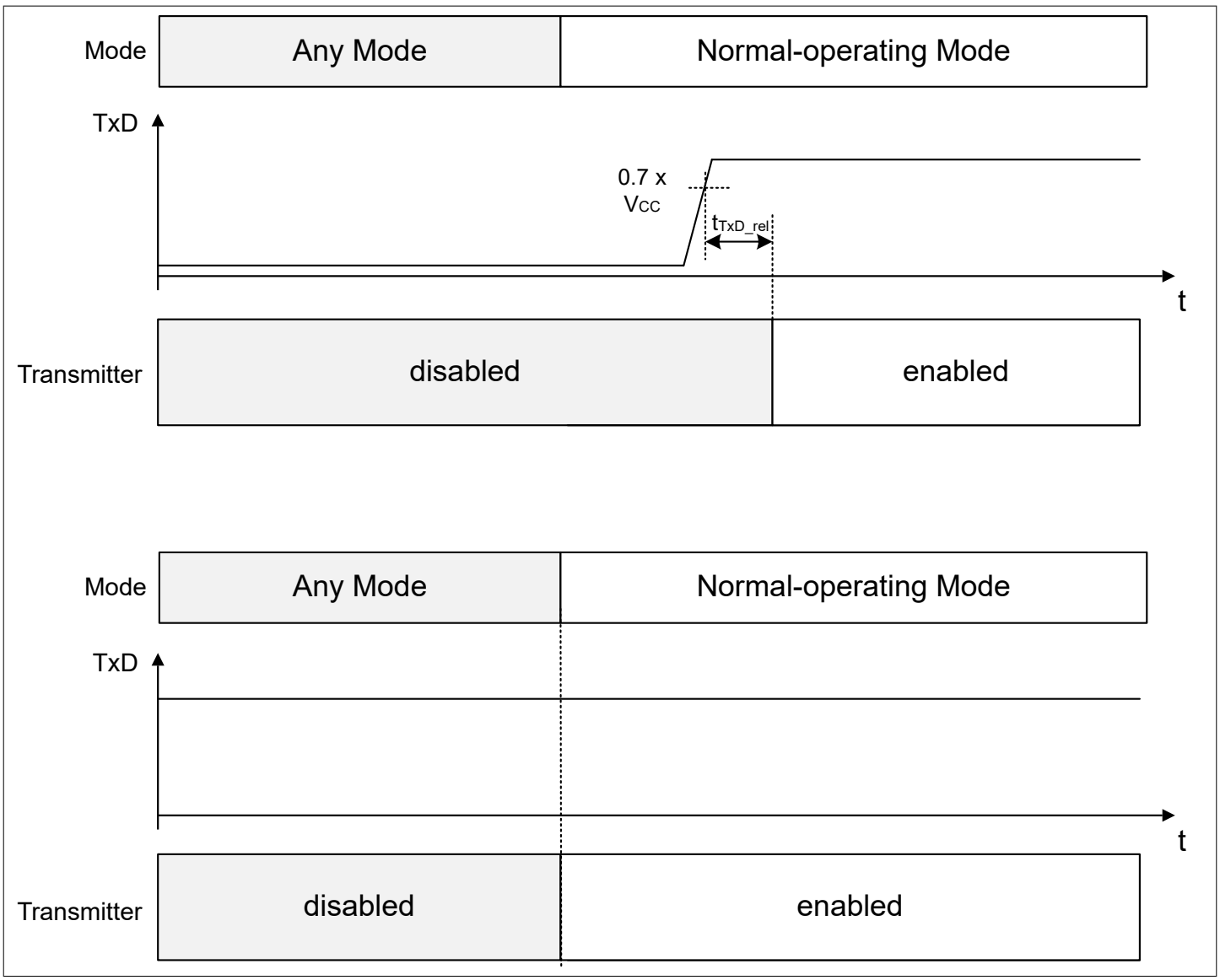

Figure 5 Mode change to normal-operating mode with dominant signal on TxD

4.2 Standby mode

The standby mode is the low-power mode of the device. In standby mode the following functions are defined:

- The transmitter is disabled and does not drive the data stream on the TxD input pin to the bus pins CANH and CANL
- The low-power receiver is enabled and monitors the HS *CAN* bus for a valid wake-up pattern (WUP). The RxD output pin indicates the detection of a valid wake-up pattern (Chapter 4.4.2). As long as no wake-up event is detected, the default of the RxD output is "high". After detecting a wake-up, the RxD follows the bus with a certain delay (see Figure 8)
- The device monitors the CAN bus for a valid wake-up pattern, Chapter 4.4
- Bus biasing is connected to *GND*
- TxD dominant timeout function is disabled
- The overtemperature protection is disabled
- The undervoltage detection on V_{CC} is disabled, see Chapter 5.3

Conditions for entering standby mode of the device:

- If $V_{CC} > V_{CC\_POD}$ and the STB pin is “high”, then the device enters standby mode after t_{Mode} from normal-operation mode
- If V_{CC} is in the functional rage for at least t_{PON}, then the device enters standby mode from power-down state

4.3 Power-down state

In power-down state the device is not functional and has the following behavior:

- The transmitter and receiver are disabled
- The bus biasing is set to high impedance
- The TxD timeout function is disabled
- The overtemperature protection is disabled
- The undervoltage detection on V_{CC} is disabled
- RxD follows the V_{CC} voltage

Conditions for entering power-down state of the device:

- V_{CC} is below the V_{CC_POD} threshold

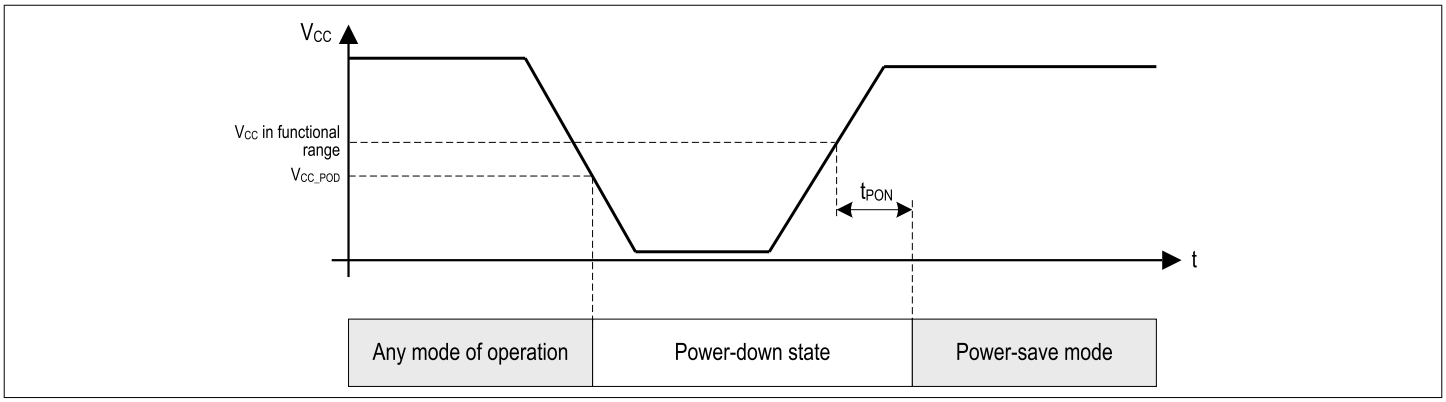

Figure 6 Power-down and power-up behavior

4.4 Bus wake-up pattern (WUP) detection

The device has implemented the bus wake-up mechanism according to ISO 11898-2:2024. In standby mode the low power receiver monitors the activity on the *CAN* bus and in case it detects a wake-up pattern, it indicates the wake-up signal on the RxD output pin. A wake-up event does not trigger a mode change. The device remains in standby mode until the microcontroller has requested a mode change to the normal-operating mode.

4.4.1 Bus wake-up pattern (WUP)

The wake-up pattern contains a dominant signal with the pulse width t_{Filter}, followed by a recessive signal with the pulse width t_{Filter} and another dominant signal with the pulse width t_{Filter}. t_{Wake} starts at the first valid dominant pulse (pulse width > t_{Filter}). The subsequent recessive and dominant pulse must occur within t_{Wake} to fulfill a wake-up pattern, see Figure 7. As long as the device does not detect a wake-up event, the RxD output remains “high”.

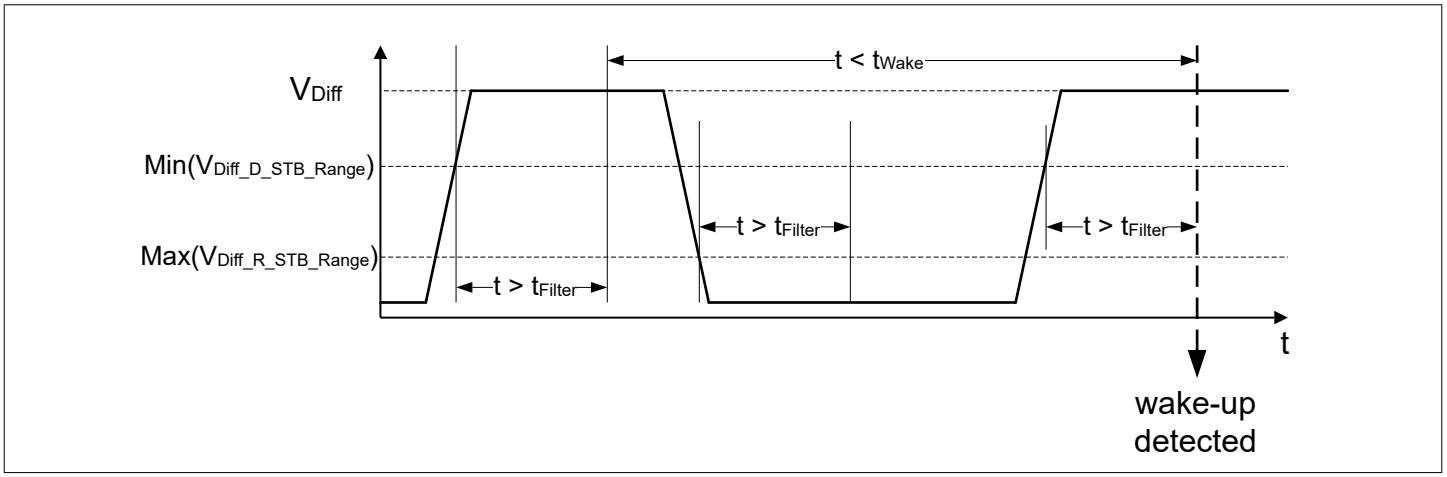

Figure 7 Remote wake-up signal

4.4.2 RxD pin wake-up behavior

If the device detects a wake-up event, then it sets the RxD output pin to “low” and then the RxD output follows the *CAN* bus signal with the delay of t_{WU} as long as the pulse width exceeds the filter time t_{Filter}, see Figure 8.

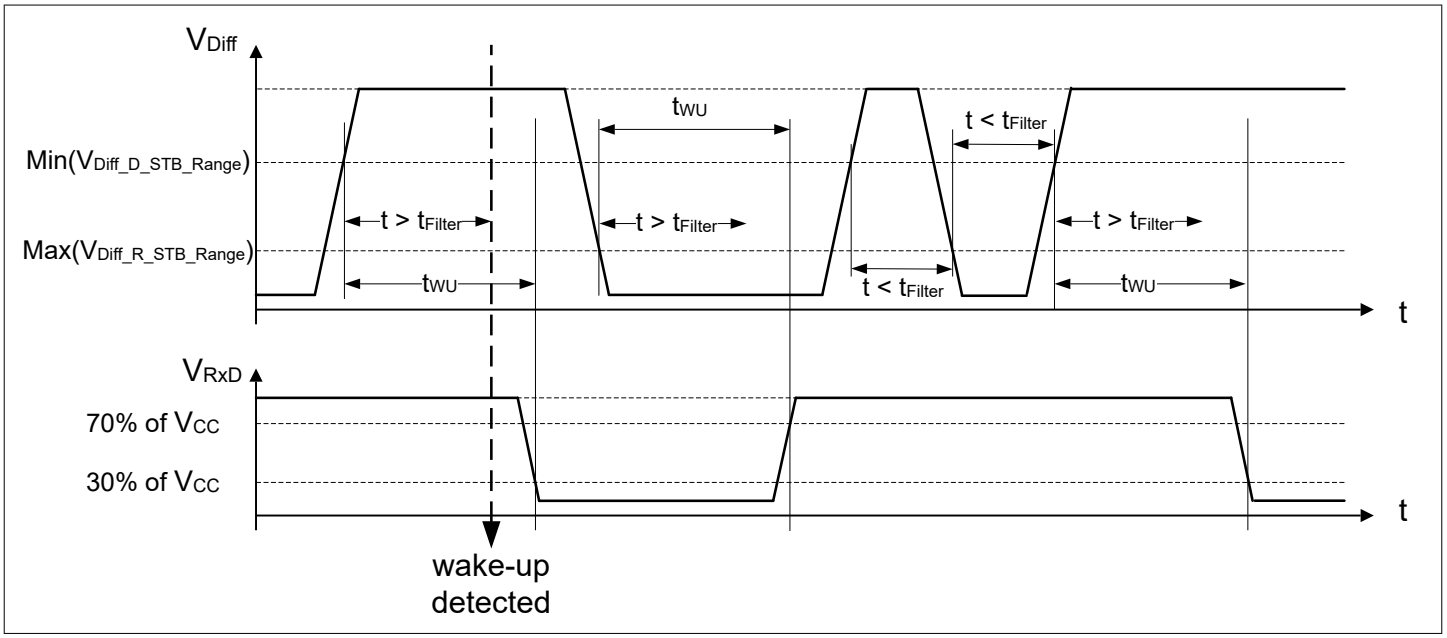

Figure 8 RxD signal follows the CAN bus signal

If at least one of the following conditions is fulfilled, then the device disables the RxD pin wake up behavior:

- A mode change to normal-operating mode is performed during a wake-up pattern
- The voltage supply $V_{CC} < V_{CC\_POD}$

5 Fail safe functions

5.1 Short circuit protection

The CANH and CANL bus pins are proven to cope with a short circuit fault against *GND* and against the supply voltages. A current limiting circuit protects the transceiver against damages. If the device heats up due to a continuous short on the CANH or CANL pin, the internal overtemperature protection switches off the bus transmitter.

5.2 Unconnected logic input pins

If the input pins are not connected and floating, then the integrated pull-up resistors at the digital input pins force the device into fail safe behavior, see .

Table 2 Unconnected logical input pins

Input signal	Default state	Comment
TxD	“High”	Pull-up resistor to V_{CC}
STB	“High”	Pull-up resistor to V_{CC}

5.3 V_{CC} undervoltage

If $V_{CC} < V_{CC\_UV}$, then the V_{CC} supply of the transceiver is in undervoltage condition with the following functions independent of the transceiver mode, see Figure 9:

- Transmitter is deactivated
- The bus biasing is set to *GND*

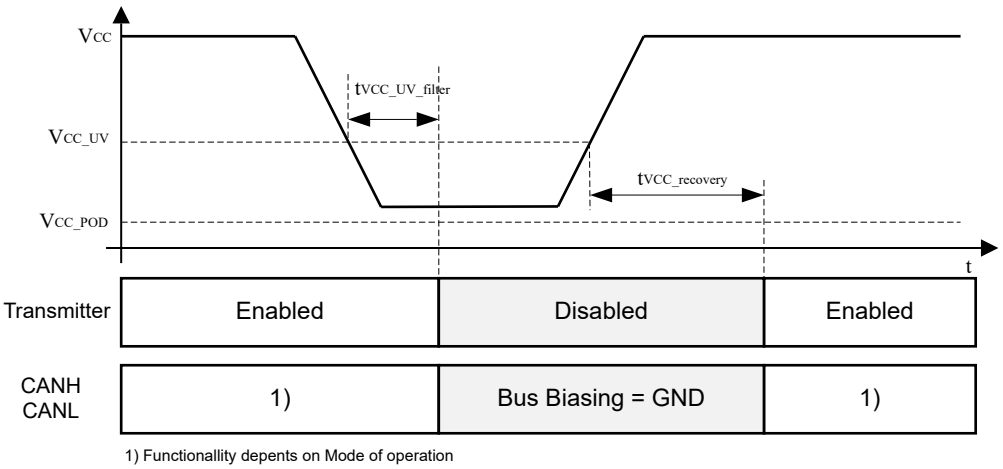

Figure 9 Undervoltage on the transmitter supply V_{CC}

5.4 TxD timeout function

If the logical signal on the TxD pin is permanently “low”, then the TxD timeout feature protects the *CAN* bus from blocked communication due to this errant logic signal. A permanent “low” signal on the TxD pin can occur due to a locked-up microcontroller or in a short circuit on the printed circuit board, for example. In normal-operating mode, a “low” signal on the TxD pin for the time $t > t_{TXD\_TO}$ enables the TxD timeout feature and the device disables the transmitter, see Figure 10. The receiver is still active and the RxD output pin continues monitoring data on the bus.

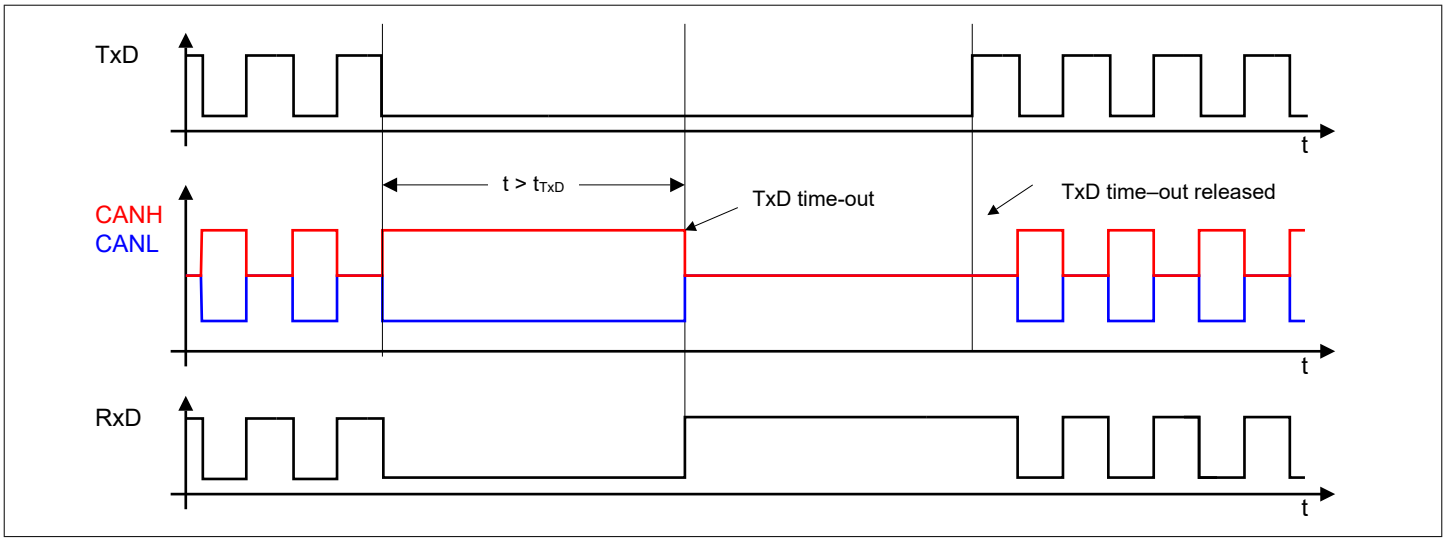

Figure 10 TxD timeout function

5.5 Delay time for mode change

The HS *CAN* transceiver device changes the mode of operation within the time window t_{Mode}. During the mode change from standby power-save mode to a non-low power mode the device sets the RxD output to “high” and RxD does not reflect the status on the CANH and CANL input pins.

5.6 Overtemperature protection

The device has an integrated overtemperature detection to protect the device against thermal overstress of the transmitter. The overtemperature protection is only active in normal-operating mode. If an overtemperature condition ($T_{Junction} \geq T_{JSD}$) occurs, then the temperature sensor disables the transmitter while the transceiver remains in normal-operating mode. After the device cools down ($T_{Junction} < T_{JSD}$) the device activates the transmitter again, see Figure 11. A hysteresis is implemented within the temperature sensor.

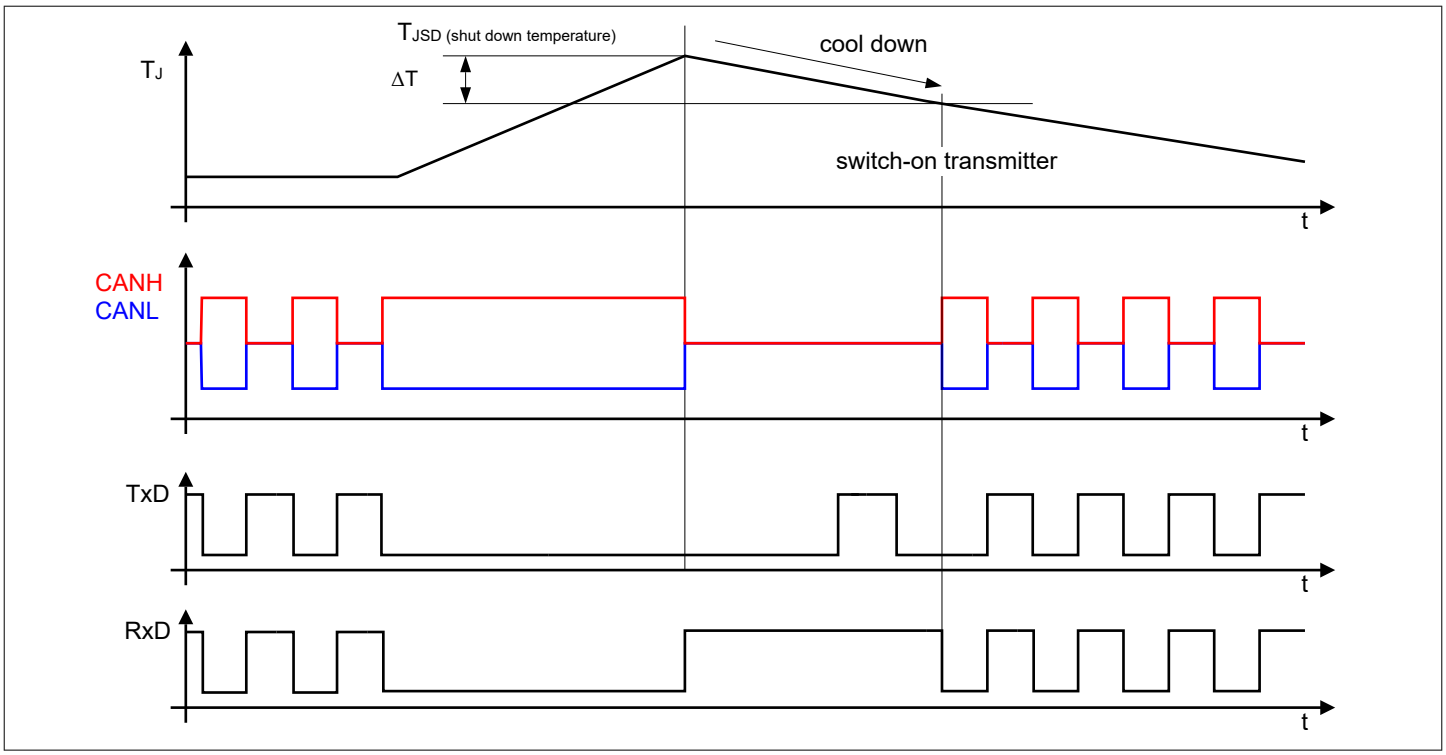

Figure 11 Overtemperature protection

6 General product characteristics

6.1 Absolute maximum ratings

Table 3 Absolute maximum ratings voltages, currents and temperatures[1)]

All voltages with respect to ground; positive current flowing into pin;
(unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Transmitter supply voltage	V_{CC}	-0.3	–	6.0	V	–	P_7.1.1
CANH and CANL *direct current (DC)* voltage versus *GND*	V_{CANH}	-40	–	40	V	–	P_7.1.3
Differential voltage between CANH and CANL	V_{CAN_Diff}	-40	–	40	V	–	P_7.1.4
Voltages at the digital *I/O* pins: STB, TxD	V_{MAX_IO}	-0.3	–	6.0	V	–	P_7.1.8
Voltages at the digital I/O pins: RxD	V_{MAX_RxD}	-0.3	–	V_{CC}+0.3	V	–	P_7.1.10
Currents							
RxD output current	I_{RxD}	-5	–	5	mA	–	P_7.1.11
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_7.1.12
Storage temperature	T_S	-55	–	150	°C	–	P_7.1.13
ESD robustness							
ESD robustness at CANH, CANL versus GND	$V_{ESD\_HBM\_CAN}$	-8	–	8	kV	2) HBM; 100 pF via 1.5 kΩ	P_7.1.14
ESD robustness at all other pins	$V_{ESD\_HBM\_ALL}$	-2	–	2	kV	2) HBM; 100 pF via 1.5 kΩ	P_7.1.15
ESD robustness at corner pins	$V_{ESD\_CDM\_CP}$	-750	–	750	V	3) CDM	P_7.1.16
ESD robustness at any other pins	V_{ESD_CDM}	-500	–	500	V	3) CDM	P_7.1.17

1) Not subject to production test, specified by design.
2) Human body model (HBM) robustness according to AE - Q100-002.
3) Charge device model (CDM) robustness according to AEC - Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard.

***Note**: Latchup robustness: class II according to AEC - Q100-04.*

***Note**: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Integrated protection functions are designed to prevent integrated circuit (IC) destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal-operating range. Protection functions are not designed for continuous repetitive operation.*

6.2 Functional range

Table 4 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltages							
Transmitter supply voltage	V_{CC}	4.75	–	5.25	V	–	P_7.2.1
Thermal parameters							
Junction temperature	T_j	-40	–	150	°C	1)	P_7.2.3

1) Not subject to production test, specified by design.

***Note**: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

6.3 Thermal resistance

***Note**: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, please visit www.jedec.org.*

Table 5 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Thermal resistances							
Junction to ambient PG-DSO-8	R_{thJA_DSO8}	–	120	–	K/W	2)	P_7.3.2
Thermal shutdown (junction temperature)							
Thermal shutdown temperature, rising	T_{JSD}	170	180	190	°C	Temperature falling: minimum 150°C	P_7.3.3
Thermal shutdown hysteresis	ΔT	5	10	20	K	–	P_7.3.4

1) Not subject to production test, specified by design.
2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board. The product (chip and package) was simulated on a 76.2 mm × 114.3 mm × 1.5 mm board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu).

7 Electrical characteristics

7.1 Power supply interface

7.1.1 Current consumption

Table 6 Current consumption

4.75 V < V_{CC} < 5.25 V;R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption at V_{CC} normal-operating mode, recessive state	I_{CC_R}	–	2.8	4	mA	V_{TxD} = V_{CC}; V_{STB} = 0 V; V_{CANH} = V_{CANL} = V_{CC}/2	P_8.1.4
Current consumption at V_{CC} normal-operating mode, dominant state	I_{CC_D}	–	38	48	mA	V_{TxD} = V_{STB} = 0 V; $t < t_{TxD}$	P_8.1.9
Current consumption at V_{CC} standby mode	$I_{CC(STB)}$	–	–	20	µA	V_{TxD} = V_{STB} = V_{CC}	P_8.1.15

7.1.2 Undervoltage detection

Table 7 Undervoltage detection

4.75 V < V_{CC} < 5.25 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
V_{CC} undervoltage threshold	V_{CC_UV}	4.25	4.35	4.5	V	–	P_8.1.25
V_{CC} undervoltage filter time	$t_{VCC\_UV\_filter}$	1	–	10	µs	1)	P_8.1.27
V_{CC} undervoltage recovery time	$t_{VCC\_recovery}$	–	–	70	µs	1)	P_8.1.28
V_{CC} power-down threshold	V_{CC_POD}	2.0	2.5	3.0	V	–	P_8.1.31
Power-up delay time	t_{PON}	–	–	280	µs	1) Figure 6	P_8.1.33

1) Not subject to production test, specified by design.

7.2 CAN controller interface

Table 8 CAN controller interface

4.75 V < V_{CC} < 5.25 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Receiver output RxD							
"High" level output current	I_{RxD_H}	–	-2	-1	mA	V_{RxD} = V_{CC} - 0.4 V; V_{Diff} < 0.5 V	P_8.2.2
"Low" level output current	I_{RxD_L}	1	2	–	mA	V_{RxD} = 0.4 V; V_{Diff} > 0.9 V	P_8.2.3
Transmitter input TxD							
"High" level input voltage	V_{TxD_H}	0.7 × V_{CC}	–	6.0	V	Recessive state	P_8.2.5
"Low" level input voltage	V_{TxD_L}	-0.3	–	0.3 × V_{CC}	V	Dominant state	P_8.2.7
Internal pull-up resistor TxD	R_{TxD}	35	50	70	kΩ	–	P_8.2.9
Input capacitance	C_{TxD}	–	–	10	pF	1)	P_8.2.10
TxD dominant timeout	t_{TxD}	1	–	4	ms	Normal-operating mode	P_8.2.11
Standby input STB							
"High" level input voltage	V_{Mode_H}	0.7 × V_{CC}	–	6.0	V	–	P_8.2.15
"Low" level input voltage	V_{Mode_L}	-0.3	–	0.3 × V_{CC}	V	Normal-operating mode	P_8.2.17
Internal pull-up resistor	R_{Mode}	35	50	70	kΩ	–	P_8.2.19
Input capacitance	C_{Mode}	–	–	10	pF	1)	P_8.2.20

1) Not subject to production test, specified by design.

7.3 Receiver

Table 9 Receiver characteristics

4.75 V < V_{CC} < 5.25 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Common mode range	V_{CMR}	-12	–	12	V	–	P_8.3.1
Differential range dominant state, normal-operating mode	$V_{Diff\_D\_Range}$	0.9	–	8.0	V	1) V_{CMR}	P_8.3.4
Differential range recessive state, normal-operating mode	$V_{Diff\_R\_Range}$	-3.0	–	0.5	V	1) V_{CMR}	P_8.3.6
Differential range dominant state, standby mode	$V_{Diff\_D\_STB\_Range}$	1.15	–	8.0	V	1) V_{CMR}	P_8.3.8
Differential range recessive state, standby mode	$V_{Diff\_R\_STB\_Range}$	-3.0	–	0.4	V	1) V_{CMR}	P_8.3.10
Single ended internal resistance	R_{CAN_H}, R_{CAN_L}	30	–	50	kΩ	1) recessive state; -2 V ≤ V_{CANH} ≤ 7 V; -2 V ≤ V_{CANL} ≤ 7 V	P_8.3.12
Differential internal resistance	R_{Diff}	60	–	100	kΩ	1) recessive state; -2 V ≤ V_{CANH} ≤ 7 V; -2 V ≤ V_{CANL} ≤ 7 V	P_8.3.13
Input resistance deviation between CANH and CANL	ΔR_i	-1	–	1	%	1) recessive state; V_{CANH} = V_{CANL} = 5 V	P_8.3.14
Input capacitance CANH, CANL versus *GND*	C_{In}	–	20	40	pF	1) 2)	P_8.3.15
Differential input capacitance	C_{InDiff}	–	10	20	pF	1) 2)	P_8.3.16

1) Not subject to production test, specified by design.
2) S2P-method; f = 10 MHz.

7.4 Transmitter

Table 10 Transmitter characteristics

4.75 V < V_{CC} < 5.25 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANL, CANH recessive state output voltage	$V_{CANL,H}$	2.0	2.5	3.0	V	Normal-operating mode; $V_{TxD} = V_{CC}$; no load	P_8.4.2
CANH, CANL recessive state differential output voltage $V_{Diff\_R\_NM} = V_{CANH} - V_{CANL}$	$V_{Diff\_R\_NM}$	-50	–	50	mV	Normal-operating mode; $V_{TxD} = V_{CC}$; no load	P_8.4.4
CANL dominant state output voltage, normal-operating mode	V_{CANL}	0.5	–	2.25	V	V_{TxD} = 0 V; 45 Ω < R_L < 65 Ω	P_8.4.5
CANH dominant state output voltage, normal-operating mode	V_{CANH}	2.75	–	4.5	V	V_{TxD} = 0 V; 45 Ω < R_L < 65 Ω	P_8.4.6
Differential voltage dominant state, normal-operating mode	$V_{Diff\_D\_NM}$	1.5	2.0	3.0	V	$V_{Diff} = V_{CANH} - V_{CANL}$; V_{TxD} = 0 V; 50 Ω < R_L < 65 Ω	P_8.4.7
Differential voltage extended bus load	$V_{Diff\_EXT\_BL}$	1.4	2.0	3.3	V	Dominant state; normal-operating mode; V_{TxD} = 0 V; 45 Ω < R_L < 70 Ω	P_8.4.8
Differential voltage dominant state high extended bus load normal-operating mode	$V_{Diff\_HEXT\_BL}$	1.5	–	5.0	V	1) V_{TxD} = 0 V; R_L = 2240 Ω	P_8.4.9
CANH, CANL recessive output voltage difference standby mode	V_{Diff_STB}	-0.2	–	0.2	V	No load	P_8.4.10
CANL, CANH recessive output voltage standby mode	V_{CANL,H_STB}	-0.1	–	0.1	V	No load	P_8.4.11
Driver symmetry $V_{SYM} = V_{CANH} + V_{CANL}$	V_{SYM}	0.95 × V_{CC}	1.0 × V_{CC}	1.05 × V_{CC}	V	1) 2) C_1 = 4.7 nF	P_8.4.12

(table continues...)

Table 10 (continued) Transmitter characteristics

4.75 V < V_{CC} < 5.25 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
CANL short circuit current	I_{CANLsc}	-115	–	115	mA	-3 V < $V_{CANLshort}$ < 18 V; $t < t_{TxD}$; V_{TxD} = 0 V	P_8.4.13
CANH short circuit current	I_{CANHsc}	-115	–	115	mA	-3 V < $V_{CANHshort}$ < 18 V; $t < t_{TxD}$; V_{TxD} = 0 V	P_8.4.14
CANH leakage current	$I_{CANH,lk}$	-5	–	5	µA	V_{CC} = 0 V; 0 V < V_{CANH} ≤ 5 V; V_{CANH} = V_{CANL}	P_8.4.16
CANL leakage current	$I_{CANL,lk}$	-5	–	5	µA	V_{CC} = 0 V; 0 V < V_{CANL} ≤ 5 V; V_{CANH} = V_{CANL}	P_8.4.18
Differential internal resistance	$R_{DIFF\_act\_rec}$	75	–	125	Ω	–	P_8.4.21
Optional internal single-ended impedance	$R_{SE\_SIC\_act\_rec}$	37.5	–	66.5	Ω	–	P_8.4.22
Start time of active signal improvement phase	$t_{act\_rec\_start}$	–	–	120	ns	–	P_8.4.23
End time of active signal improvement phase	$t_{act\_rec\_end}$	355	–	–	ns	– –	P_8.4.24
Start time of passive recessive phase	$t_{pas\_rec\_start}$	450	–	530	ns	–	P_8.4.25

1) Not subject to production test, specified by design.
2) V_{SYM} observed during dominant and recessive state and also during the transition from dominant to recessive and vice versa, while TxD is stimulated by a square wave signal. This parameter must be valid for all the possible transmission rates.

7.5 Dynamic transceiver parameters

Table 11 Electrical characteristics dynamic transceiver parameters

4.75 V < V_{CC} < 5.25 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Loop delay from TxD to RxD	t_{Loop}	80	–	190	ns	C_1 = 0 pF; C_2 = 100 pF; C_{RxD} = 25 pF; C_{VCC} = 100 nF; R_L = 60 Ω; V_{TxD} = rise (10% to 90%) and fall (90% to 10%) time < 10 ns; 125 kbit/s < 1/t_{Bit} < 8 Mbit/s; see Figure 12, Figure 13	P_8.5.1
Transmitter propagation delay TxD to bus (“high” until recessive; “low” until dominant)	t_{prop_T}	30	–	80	ns	C_1 = 0 pF; C_2 = 100 pF; C_{VCC} = 100 nF; R_L = 60 Ω; V_{TxD} = rise (10% to 90%) and fall (90% to 10%) time < 10 ns; see Figure 12, Figure 13	P_8.5.3
Propagation delay bus to RxD (dominant until “low”; recessive until “high”)	t_{prop_R}	30	–	110	ns	C_1 = 0 pF; C_2 = 100 pF; C_{RxD} = 25 pF; C_{VCC} = 100 nF; R_L = 60 Ω; V_{TxD} = rise (10% -> 90%) and fall (90% -> 10%) time < 10 ns; see Figure 12, Figure 13	P_8.5.4
Delay times							
Delay time for mode change	t_{Mode}	–	–	20	µs	–	P_8.5.5
Transmitter release time after entering normal-operating mode in dominant state	t_{TxD_rel}	–	–	5	µs	–	P_8.5.6
CAN activity filter time	t_{Filter}	0.5	–	1.8	µs	–	P_8.5.7
Bus wake-up timeout	t_{Wake}	0.8	–	10	ms	1)	P_8.5.8

(table continues...)

Table 11 (continued) Electrical characteristics dynamic transceiver parameters

4.75 V < V_{CC} < 5.25 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Bus wake-up delay time	t_{WU}	–	–	5	µs	–	P_8.5.9
CAN FD characteristics							
Received recessive bit width variation	$\Delta t_{Bit(RxD)}$	-30	–	20	ns	$\Delta t_{Bit(RxD)} = t_{Bit(RxD)} - t_{Bit(TxD)}$; C_1 = 0 pF; C_2 = 100 pF; C_{RxD} = 25 pF; C_{VCC} = 100 nF; R_L = 60 Ω; V_{TxD} = rise (10% to 90%) and fall (90% to 10%) time < 10 ns; 125 kbit/s < 1/t_{Bit} < 8 Mbit/s; see Figure 12, Figure 13	P_8.5.10
Receiver timing symmetry variation	Δt_{Rec}	-20	–	15	ns	$\Delta t_{Rec} = t_{Bit(RxD)} - t_{Bit(Bus)}$; C_1 = 0 pF; C_2 = 100 pF; C_{RxD} = 25 pF; C_{VCC} = 100 nF; R_L = 60 Ω; V_{TxD} = rise (10% to 90%) and fall (90% to 10%) time < 10 ns; 125 kbit/s < 1/t_{Bit} < 8 Mbit/s; see Figure 12, and Figure 14	P_8.5.11

(table continues...)

Table 11 (continued) Electrical characteristics dynamic transceiver parameters

4.75 V < V_{CC} < 5.25 V; R_L = 60 Ω; -40°C < T_j < 150°C; all voltages with respect to ground; positive current flowing into pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Transmitted recessive bit width variation	$\Delta t_{Bit(Bus)}$	-10	–	10	ns	$\Delta t_{Bit(Bus)} = t_{Bit(Bus)} - t_{Bit(TxD)}$; C_1 = 0 pF; C_2 = 100 pF; C_{RxD} = 25 pF; C_{VCC} = 100 nF; R_L = 60 Ω; V_{TxD} = rise (10% to 90%) and fall (90% to 10%) time < 10 ns; 125 kbit/s < $1/t_{Bit}$ < 8 Mbit/s; see Figure 12 and Figure 14	P_8.5.12

1) Not subject to production test, specified by design.

7.6 Diagrams

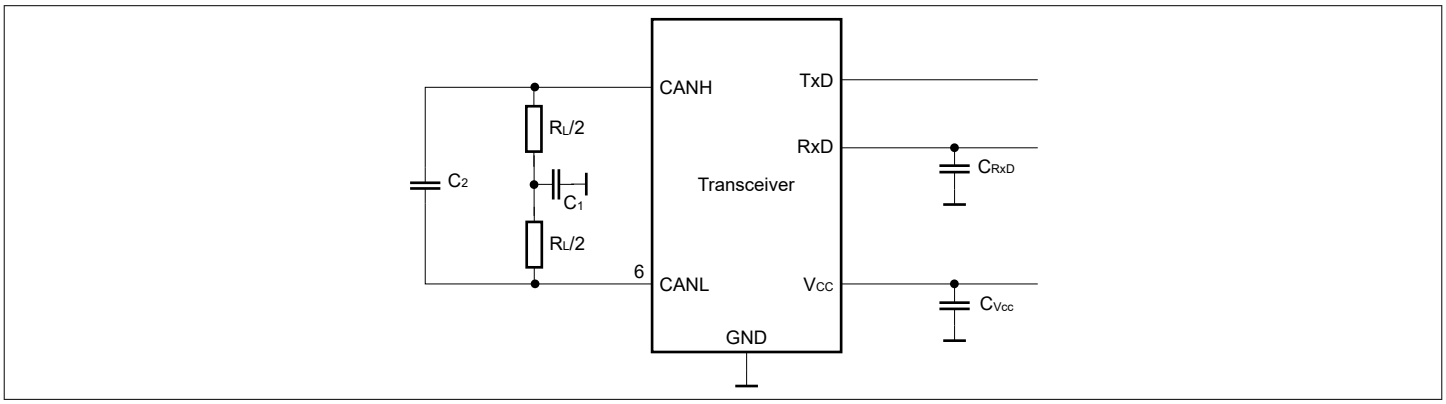

Figure 12 Test circuit

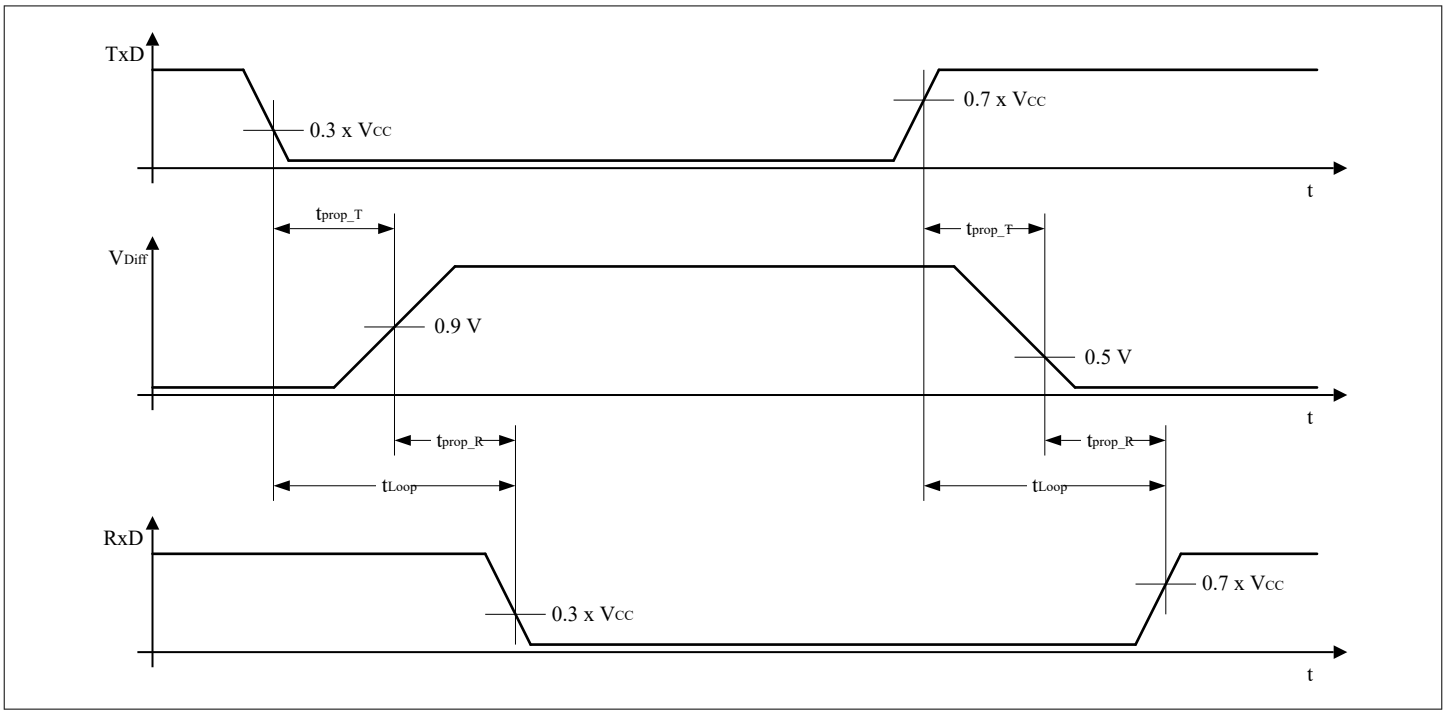

Figure 13 Timing diagram for dynamic characteristics

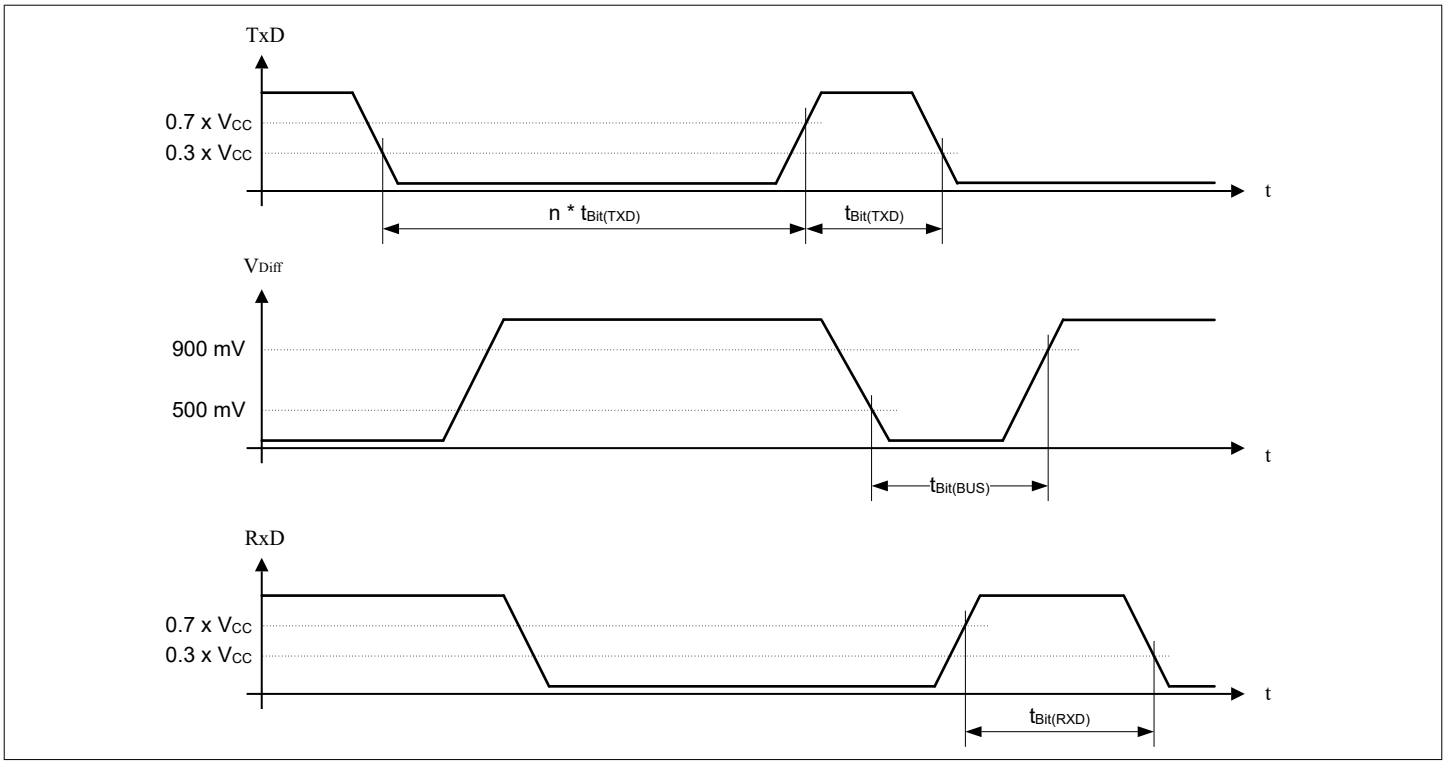

Figure 14 CAN FD electrical parameters

8 Application information

8.1 ESD robustness according to IEC 61000-4-2

Tests for *ESD* robustness according to IEC 61000-4-2 Gun test (150 pF, 330 Ω) have been performed. The results and test conditions are available in a separate test report.

Table 12 ESD robustness according to IEC 61000-4-2

Performed Test	Result	Unit	Remarks
Electrostatic discharge voltage at pin CANH and CANL versus *GND*	≥ +8	kV	1) Positive pulse
Electrostatic discharge voltage at pin CANH and CANL versus GND	≤ -8	kV	1) Negative pulse

1) Not subject to production test. ESD robustness ESD GUN according to GIFT / ICT paper: "*EMC* Evaluation of *CAN* Transceivers, version IEC TS62228", section 4.3. (DIN EN 61000-4-2).
Tested by external test facility IBEE Zwickau – EMC test report available on request.

8.2 Application example

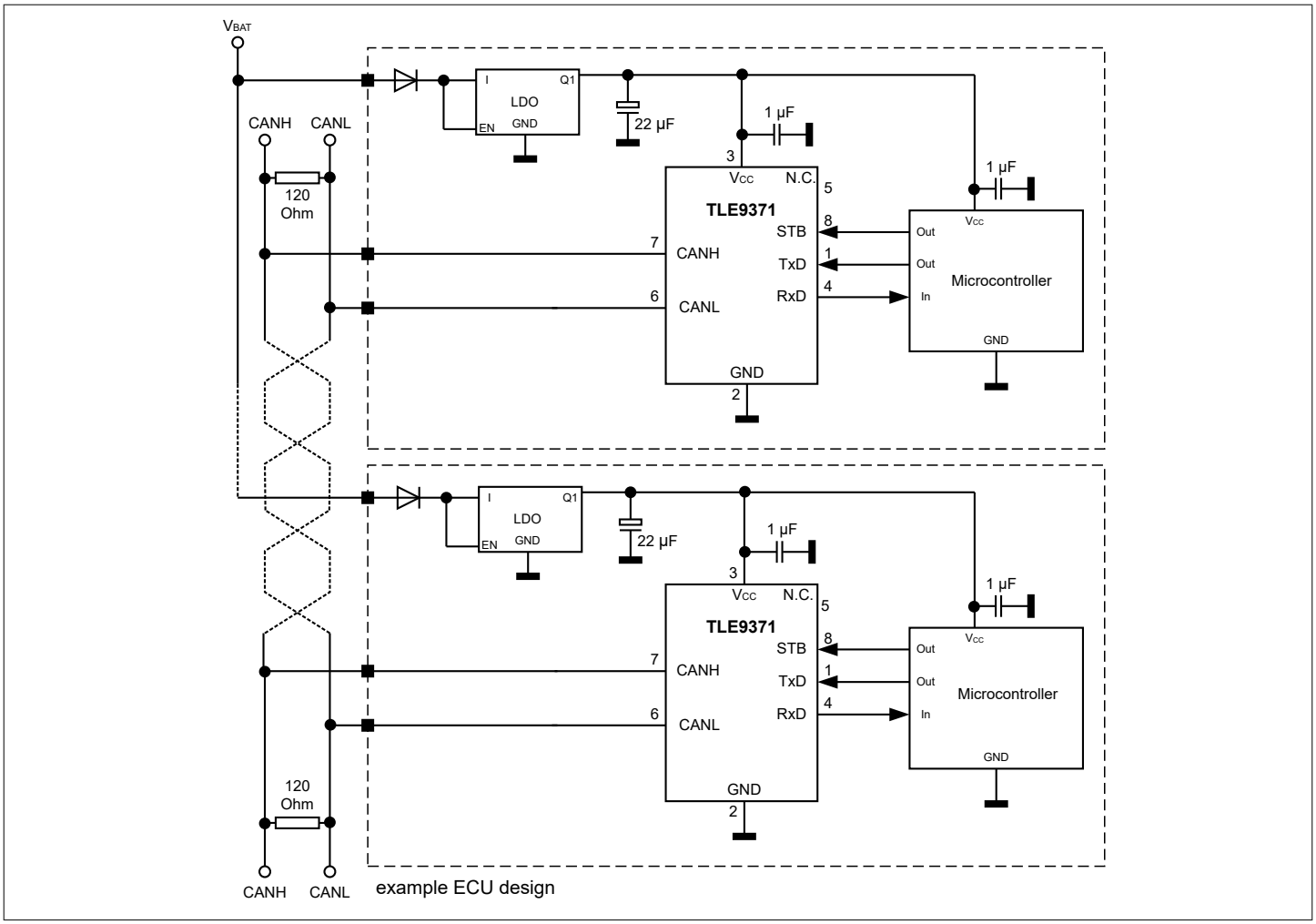

Figure 15 Application diagram

8.3 Further application information

- For further information you may visit: http://www.infineon.com/

9 Package information

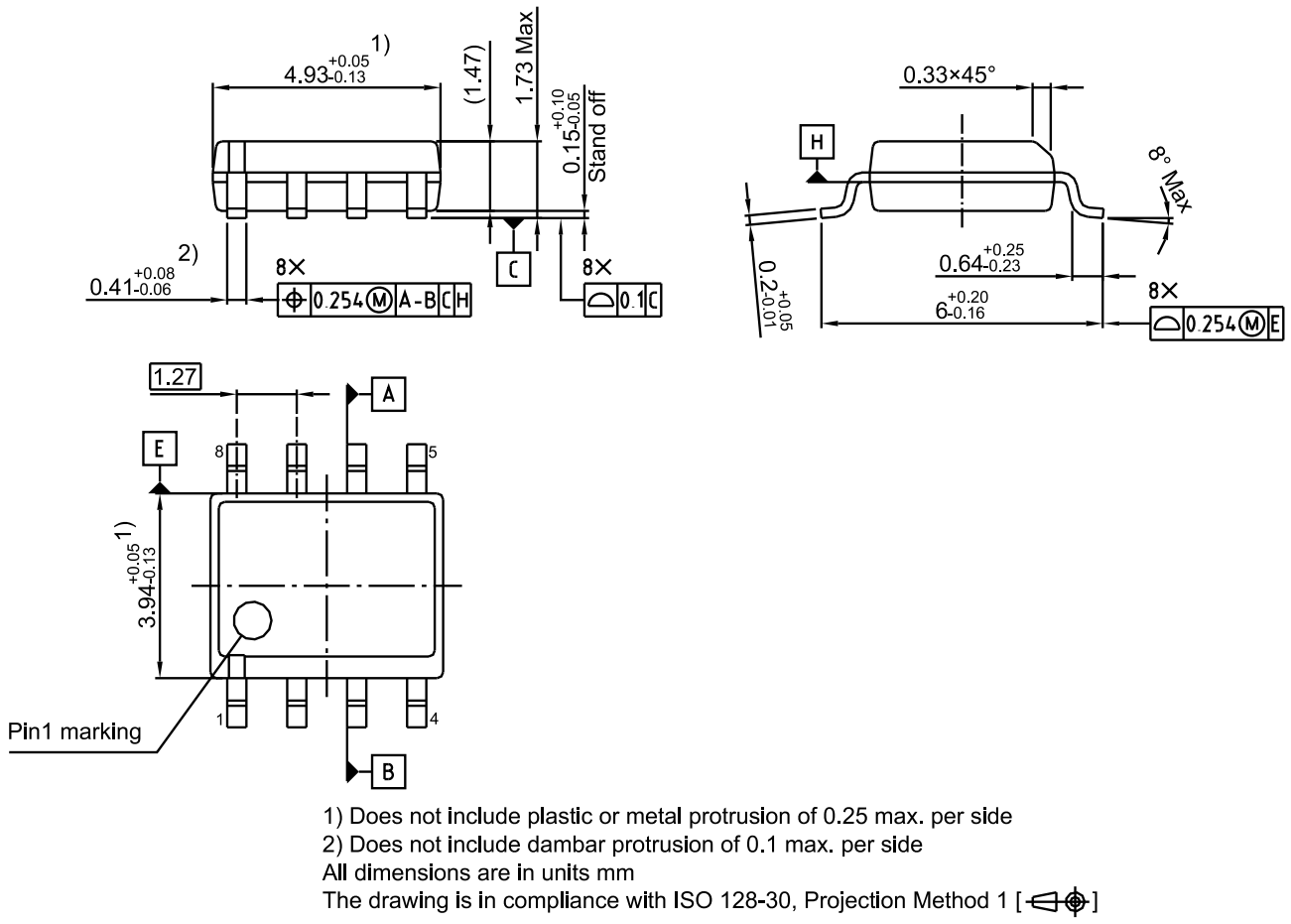

Figure 16 PG-DSO-8

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations, the device is available as a Green Product. Green Products are *RoHS* compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

Information on packages

For more information on packages, such as recommendations on assembly, refer to www.infineon.com/packages.

Glossary

CAN

controller area network (CAN)

DC

direct current (DC)

One-directional flow of electric charge. An electrochemical cell is a prime example of DC power. Direct current may flow through a conductor such as a wire, but can also flow through semiconductors, insulators, or even through a vacuum as in electron or ion beams. The electric current flows in a constant direction, distinguishing it from alternating current (AC).

EMC

electromagnetic compatibility (EMC)

The ability of electrical equipment and systems to function acceptably in their electromagnetic environment, by limiting the unintentional generation, propagation and reception of electromagnetic energy which may cause unwanted effects such as electromagnetic interference (EMI) or even physical damage in operational equipment.

EME

electromagnetic emission (EME)

An emission within the electromagnetic spectrum.

ESD

electrostatic discharge (ESD)

A sudden and momentary flow of electric current between two electrically charged objects caused by contact, an electrical short or dielectric breakdown.

GND

ground (GND)

HBM

human body model (HBM)

A model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD) based on a human body.

I/O

input/output (I/O)

The communication between an information processing system and another information processing system.

IC

integrated circuit (IC)

A miniature electronic circuit built on the surface of a thin substrate of a semiconductor material.

RF

residual fault (RF)

Portion of a random hardware fault that by itself leads to the violation of a safety goal, occurring in a hardware element, where that portion of the random hardware fault is not controlled by a safety mechanism.

RoHS

Restriction of Hazardous Substances in Electrical and Electronic Equipment (RoHS)

European Union (EU) rules restricting the use of hazardous substances in electrical and electronic equipment to protect the environment and public health.

Revision history

Revision	Date	Changes
1.10	2025-06-17	Datasheet updated according to ISO 11898-2:2024
1.0	2023-02-28	Datasheet created

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