TLE9241QU

User manual

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1 About this document

Scope and purpose

This document provides guidance on how to use the TLE9241QU in an application. It is provided in addition to the datasheet of the device.

Intended audience

Engineers designing in the TLE9241QU into a transmission system or into any other system.

Preconditions

All parameters, definitions and calculations are based on TLE9241QU datasheet, revision 1.0.

2 Block diagram

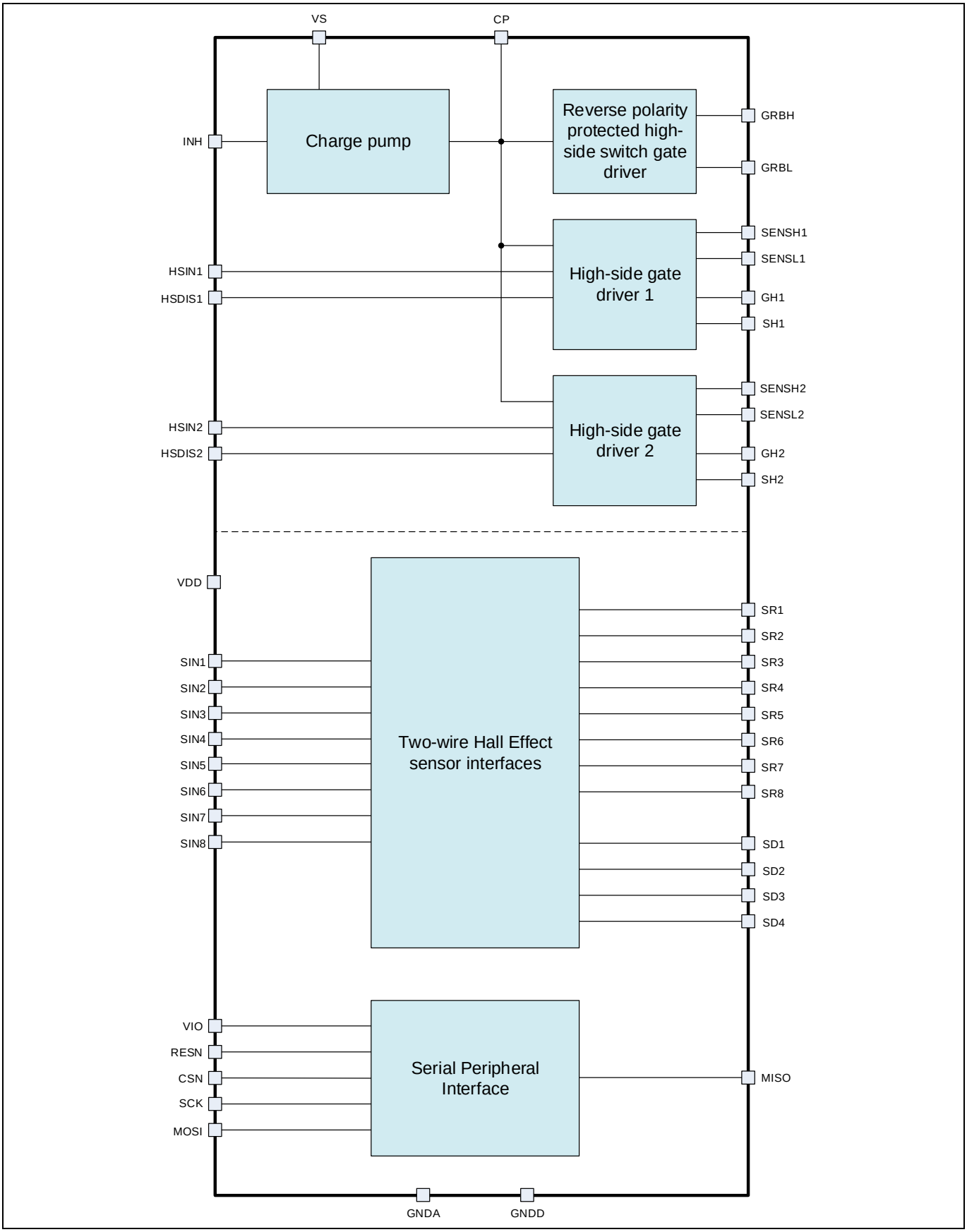

Figure 1 Block Diagram TLE9241QU

3 General product characteristics

3.1 Application note for reset input

RESN = LOW shall apply for at least T_{RESN_MIN} in order to reset the registers to their default values. During RESN = LOW, the high side drivers will be off independently of the status at pins HSINx and HSDISx.

Table 1 Application note for RESN pulse

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Minimum RESN pulse-width	T_{RESN_MIN}	20			µs	Application information only

3.2 System overtemperature behaviour

The device has four temperature sensors, one per pair of Hall Effect sensor interface channels (see chapter 6). In case all of these temperature sensors detect overtemperature ($T > T_{SD}$, see parameter P_3.2.13) but none of the sensor interfaces is in an overcurrent condition, the bit SYS_OT in register GSR (see section 7.4.1) will be set.

The SYS_OT bit being set does not affect the functionality of the device. The microcontroller shall monitor the bit and prevent operation outside the junction temperature range specified in the absoute maximum ratings (datasheet parameter P_3.1.14).

3.3 Startup time estimation and CP capacitor dimensioning

The charge pump capacitor C_{CP} is connected between the CP pin and the VS pin. It is used to store the charge required to turn on the MOSFETs connected to GRBL and the high side switches connected to GH1 and GH2. In this section, the startup time after power-on reset will be calculated depending on the size of the charge pump capacitor.

3.3.1 General considerations

The dominant factor for the startup time is the charge pump voltage becoming stable. In order to have as much stability as possible, the capacitor shall be chosen as large as possible.

Input parameters

- Charge pump current (dependent on input voltage on pin VS and on the charge pump voltage),
- Charge pump undervoltage threshold vs. pin VS: V_{CPUV},
- Size of charge pump capacitor: C_{CP}.

Assumptions

For further calculation, the following assumptions are made:

1. Supply voltage at pin VS: $V_{S,min}$ = 5.5 V (P_3.2.1),
2. Linear dependency of the charge pump between V_{CP} = 0 and V_{CP} = 9 V,
3. Minimum charge pump output current assumed (according to assumption 1),
4. Charge pump out of undervoltage at max. limit $V_{CPUV\_rise,max}$ = 9.0 V (P_3.2.9),
5. Maximum tolerance of output capacitor.

These assumptions (except 2.) are worst case assumptions; in reality the startup time will be below the simulated example.

3.3.2 Simulation

To model the behaviour, a simple Spice simulation is used.

- The current source is assumed linear with I_{CP} = 300 µA (P_3.2.12b/c),
- C_{CP} = 150…290 nF assumed (~220 nF nominal),

The result of the simulation (charging of capacitor) is shown in Figure 2.

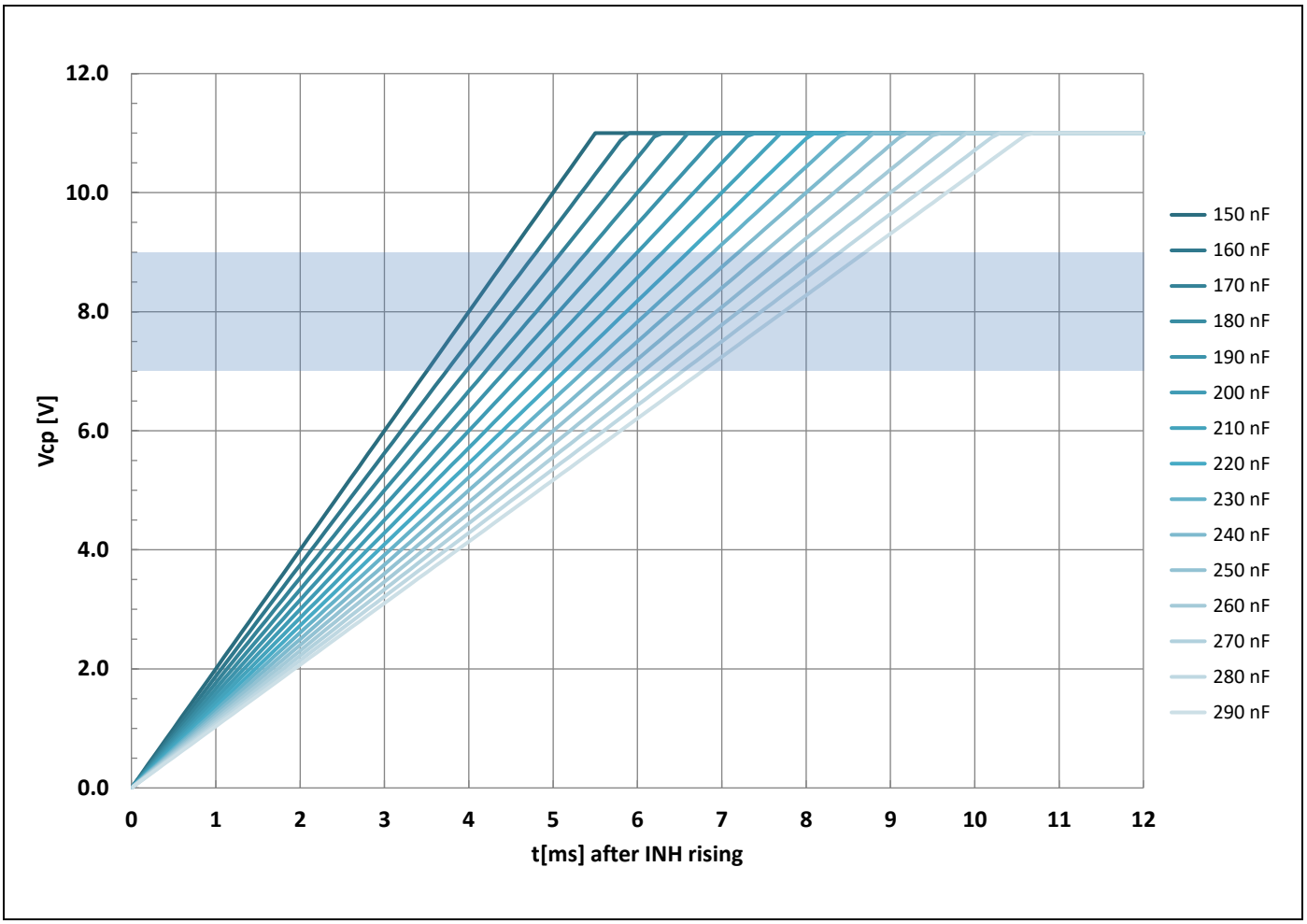

Figure 2 Simulation result for charge pump startup for different charge pump capacitors (150 – 290 nF), assuming typical clamping at 11 V.

This shows that the charge pump will be out of undervoltage (voltage crossing 7 V - 9 V) latest after 8.7 ms. In order to account for the non-linearity of the charge pump current, a factor of 1.5 is considered, i.e. results in 13 ms max. startup time.

3.3.3 Summary

To be below 15 ms (datasheet parameter P_4.1.5), capacitors up to nominal 220 nF can be chosen. The startup time will be met even assuming worst case performance of charge pump according to the datasheet.

3.3.4 Stability check

An undervoltage condition of the charge pump by normal switching should be prevented. This means that the voltage drop by switching the MOSFETs needs to be smaller than the hysteresis of the charge pump undervoltage detection.

Two cases need to be considered:

- Turning on the power switch connected to pin GRBL, and
- Turning on all high side switches connected to pins GH1 and GH2.

For each of these cases, the maximum gate charge required to turn on the MOSFETs may not cause a charge pump voltage drop higher than the hysteresis. To be on the safe side and increase stability as well as EMC performance, a safety factor of two shall be added.

Input parameters

Chip parameter:

- Minimum charge pump undervoltage hysteresis: $V_{CPUV\_hyst,min}$ = 1 V (P_3.2.16).

Note: To improve EMC performance and stability, only V_{max_drop} = 0.5 V drop should be accepted.

MOSFET parameters:

- Number n of MOSFETs connected,
- Maximum gate charge Q_{g_max}.

Calculation formula

$C_{CP} = dQ / dV = n * Q_{g\_max} / V_{max\_drop}$,

i.e. $V_{max\_drop} = (n * Q_{g\_max}) / C_{CP}$.

Example calculation

As an example, 2 MOSFETs IPD50N04S4-08 are used as high side switches (connected to GH1 and GH2):

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Gate Charge Characteristics[2)]						
Gate to source charge	Q_{gs}	V_{DD}=32V, I_D=50A, V_{GS}=0 to 10V	-	8.0	10.4	nC
Gate to drain charge	Q_{gd}		-	2.4	5.5	
Gate charge total	Q_g		-	17.2	22.4	
Gate plateau voltage	$V_{plateau}$		-	6.7	-	V

[2)] Defined by design. Not subject to production test.

Figure 3 IPD50N04S4-08 Rev. 1.0 of 2010-04-06 datasheet extract

From the datasheet, Q_{g_max} = 22.4 nC is used for calculation. n = 2 is used to turn on both HS switches simultaneously:

V_{max_drop} = 0.45 V for C_{CP} = 100 nF,

V_{max_drop} = 0.20 V for C_{CP} = 220 nF.

3.3.5 Summary

A charge pump capacitance of 220 nF is recommended to achieve good stability and maintain a reasonable startup time. The capacitance can be lowered to min. 100 nF if the startup time needs to be improved.

3.4 Thermal characteristics

Under normal circumstances, the TLE9241QU will not dissipate much power and therefore will not generate a high amount of self-heating. However, if one or more of the Hall Effect sensor interface channels is/ are in current limitation (e.g. due to a short to Battery), this may change.

This section will consider the following two cases:

- “typical case”: operation without short on the sensor interfaces, and
- “one sensor interface in current limitation”: operation with a short to Battery on one of the sensor interfaces.

Simulation results for thermal resistances junction to case and junction to ambient are listed in Table 2.

Table 2 Thermal resistance

Parameter	Symbol	Values			Unit	Note or test condition
		Min.	Typ.	Max.		
Thermal resistance junction to case, typical case	$R_{th,jc(typ)}$		4		K/W	
Thermal resistance junction to ambient, JEDEC 2s2p board, typical case	$R_{th,ja(2s2p,typ)}$		30		K/W	
Thermal resistance junction to case, one sensor interface in current limitation	$R_{th,jc(lim)}$		12		K/W	
Thermal resistance junction to case, JEDEC 2s2p board, one sensor interface in current limitation	$R_{th,ja(2s2p,lim)}$		40		K/W	see also Figure 4.

The transient behaviour in case of a sensor interface in current limitation (i.e. shorted to Battery) on a JEDEC 2s2p board is shown in Figure 4.

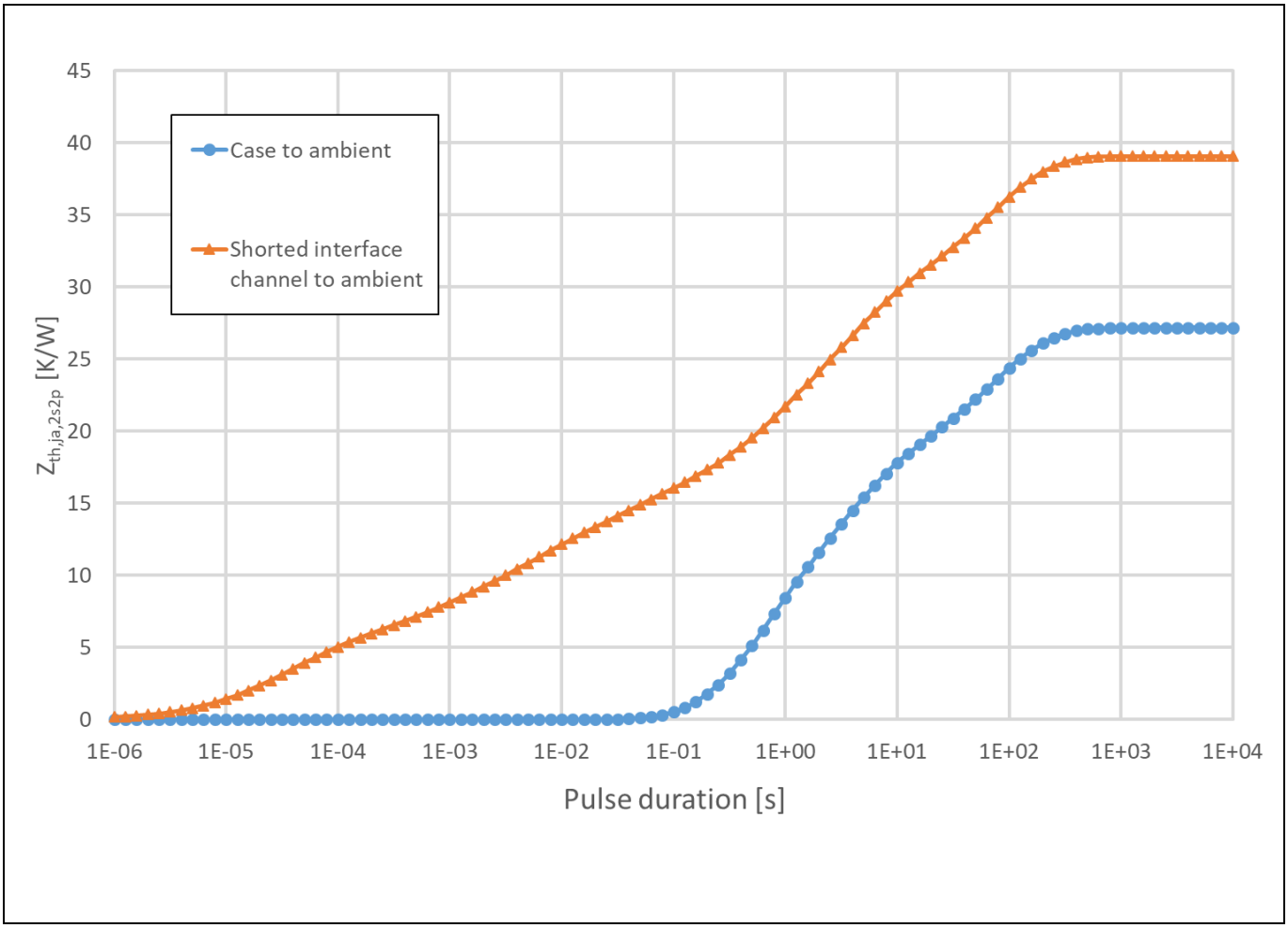

Figure 4 Transient thermal behaviour for shorted Hall Effect sensor channel on JEDEC 2s2p board

4 Reverse polarity protected high-side switch gate driver

4.1 Block diagram

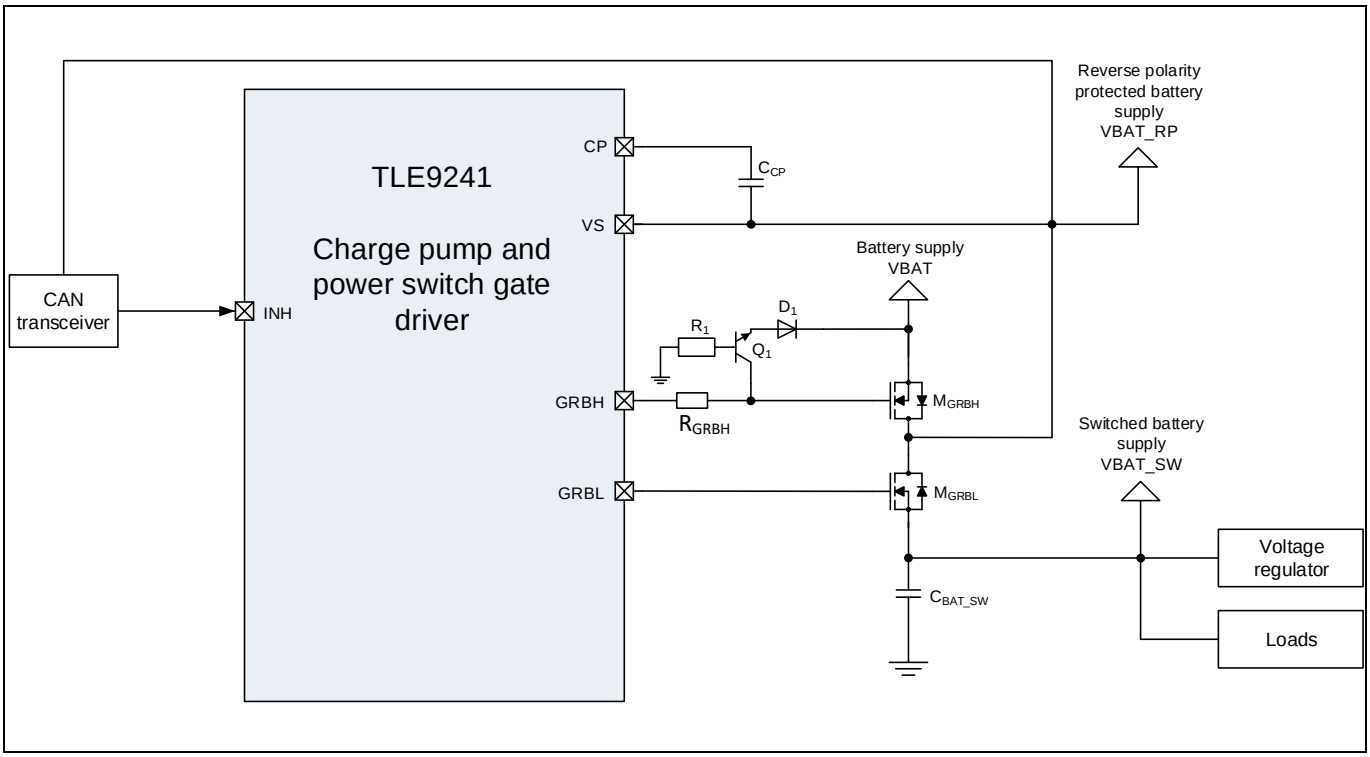

Figure 5 Reverse polarity power switch gate driver

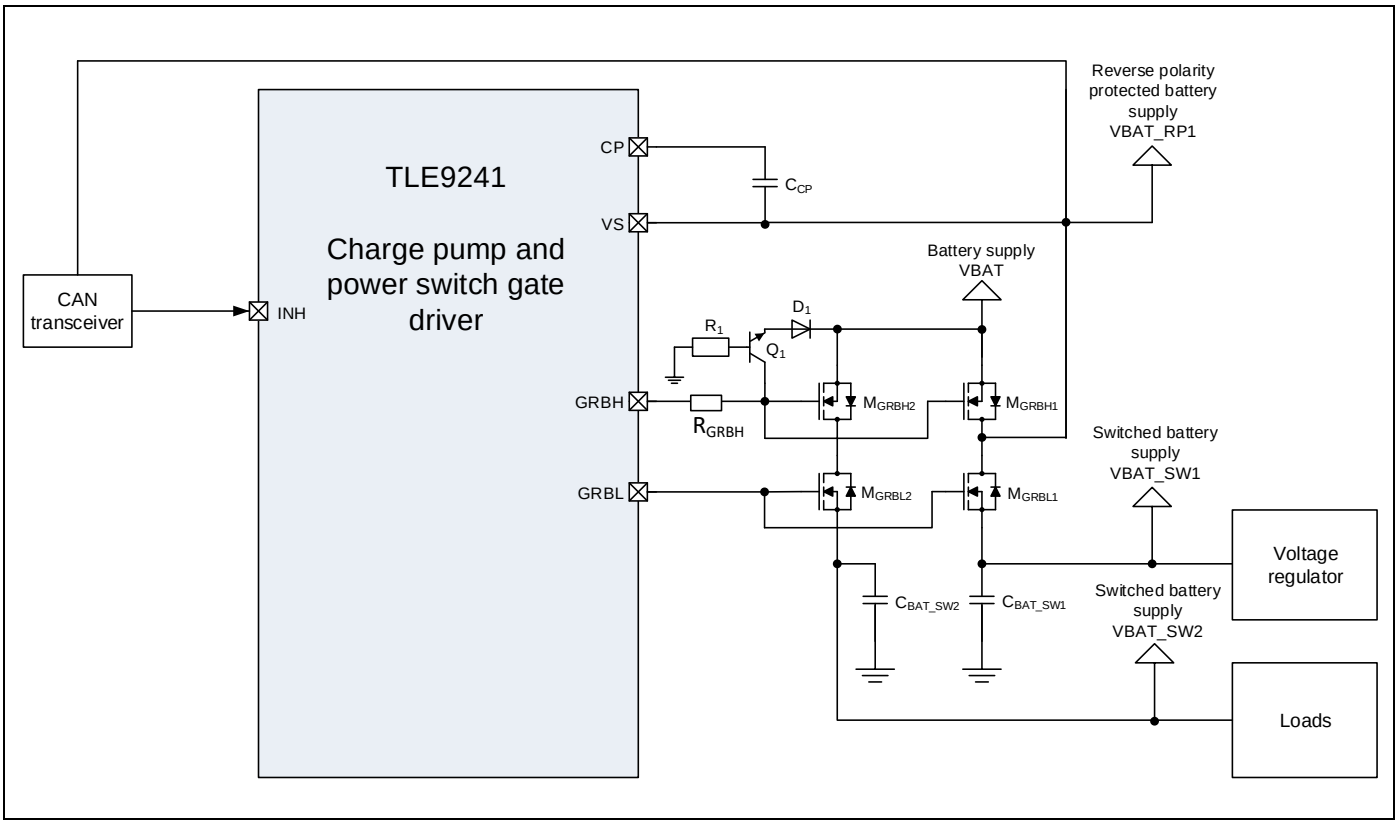

Figure 6 Reverse polarity power switch gate driver (configuration with 2 MOSFETs each)

4.2 Description

The power switch is typically used to reduce the quiescent current of the control module when the control module is in standby mode. The power switch comprises two external normal level n-channel MOSFETs in an anti-serial configuration with a common drain connection to serve as reverse polarity protection as well.

A minimum VS pin voltage of 5.0 V is required to start the charge pump and a minimum of 5.5 V is required for the charge pump to achieve the full output performance.

Pin INH is typically connected to the Inhibit output pin of a CAN transceiver. The pin has an integrated passive pull down device to prevent a floating input pin in case of an open circuit.

The external MOSFET controlled by the GRBH pin is used as an active reverse-polarity protection. It requires an external transistor circuitry (consisting of R_1, Q_1, D_1) to pull the gate voltage of the external MOSFET below ground when the VBAT node is below ground. In case large negative voltage is applied to the VBAT node, the current into the GRBH pin needs to be limited by a gate resistor R_{GRBH}.

The external MOSFET controlled by the GRBL pin will actively clamp an inductive flyback transient if the power switch is turned off while current is flowing into an external inductive load and hence prevent any destruction of the external MOSFET transistors.

The power switch pre-driver function does not require application of the VDD and VIO supplies. Also, there are no SPI registers associated with the power switch pre-driver feature.

5 High-side gate drive channels

5.1 Block diagram

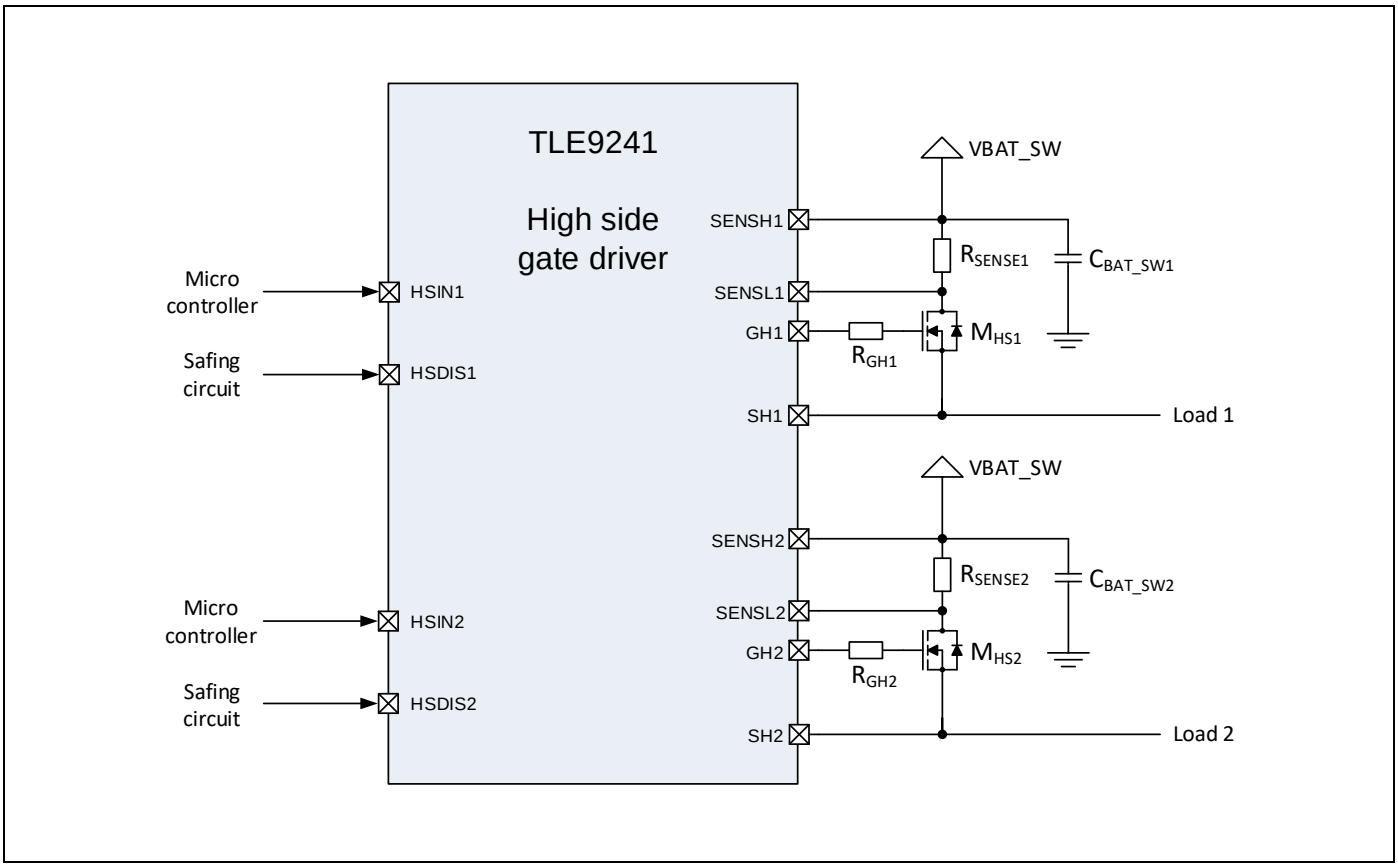

Figure 7 High-side gate drive channels

Note: For use of the high-side drivers to control a two channel MOSFET with common drain connection, it is possible to move M_{HSx} to the other side of the sense resistor R_{SENSEx}, i.e. M_{HSx} will be connected between node VBAT_SW (drain connection) and pin SENSHx (source connection). Pin SHx shall be connected to the SENSHx node in that case. See Figure 8.

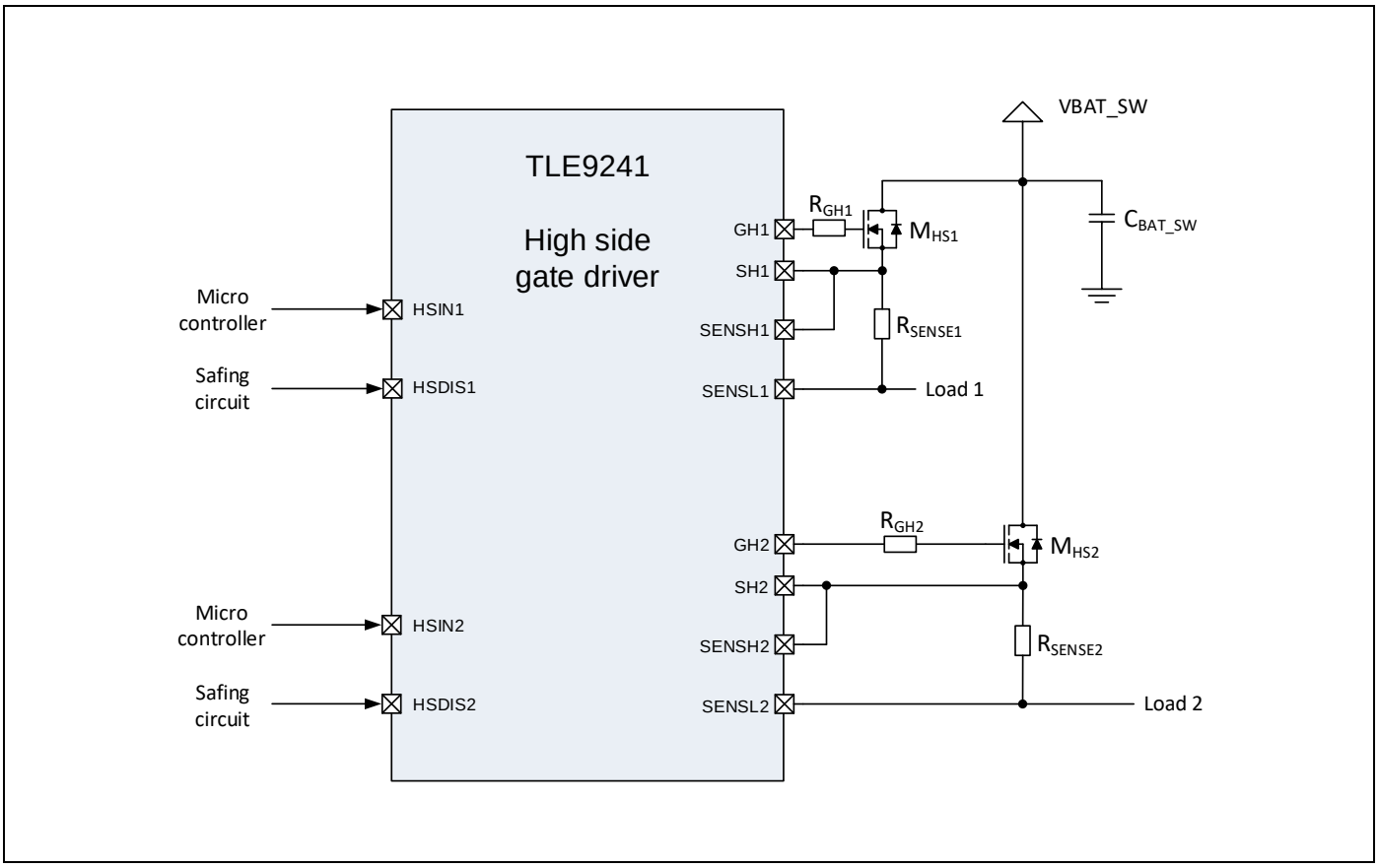

Figure 8 High-side gate drive channels (alternative configuration for dual MOSFETs with common drain connection)

5.2 Description

The high-side drivers are typically used as safety switches for disconnecting power from external loads such as transmission solenoids when a system fault is detected. The two channels are identical and independent with the exception of a common overcurrent detection threshold.

5.2.1 Control

To control a high-side driver, one of the input pins, HSINx, is typically connected to a digital output of the main microcontroller. The other input pin, HSDISx, is typically connected to a digital output of a redundant path (safing circuit). Each input is compatible with 5.0 V and 3.3 V CMOS output logic levels. Each HSINx input has an integrated pull down current and each HSDISx input pin has an integrated pull up current. This is to prevent a floating input pin in case of an open pin fault so that the affected high-side switch becomes disabled. The pre-driver output is in the ON state only if HSINx is HIGH and HSDISx is LOW.

The state information of the high-side driver output can be used by the diagnostic software to detect a short to battery when the switch is off and to detect an external MOSFET failure (shorted or open). The high-side driver output state register bits OUT1_STAT and OUT2_STAT in the HSDRVx registers (see sections 7.4.2, 7.4.3) are not latched.

If direct control via the input pins HSINx is not desired, the high-side driver can be configured for SPI control by setting bit SPI_CTRL_INx in the HSDRVx registers (see sections 7.4.2 and 7.4.3) to 1_B. Then, the status bits of the input pins INx_STAT can be used to control the high-side drivers. The pre-driver output is in the ON state only if HSDISx is LOW and the INx_STAT bit is set to 1_B.

5.2.2 Diagnosis and protection

The diagnosis system of the TLE9241QU works together with the control chip for the low-side MOSFETs. Low-side driver chips use a diagnostic system to check for open-load and short-to-ground faults on the ground related end of the load.

If the load is disconnected from the high-side switch or the high-side switch is unable to turn ON, the low-side driver diagnosis will detect the fault. Only in case of a short circuit to battery of the high-side switch, an additional mechanism is required to detect this fault. Therefore the high side gate driver of the TLE9241QU has an integrated current sink which can be controlled by SPI bits I_DIAG1_EN and I_DIAG2_EN (see registers HSDRV1 and HSDRV2, sections 7.4.2, 7.4.3) that tries to pull down the SHx nodes to ground level when the high-side switch is turned OFF. The current sink is protected against reverse voltage which can occur during discharge of an inductive load. See Figure 9.

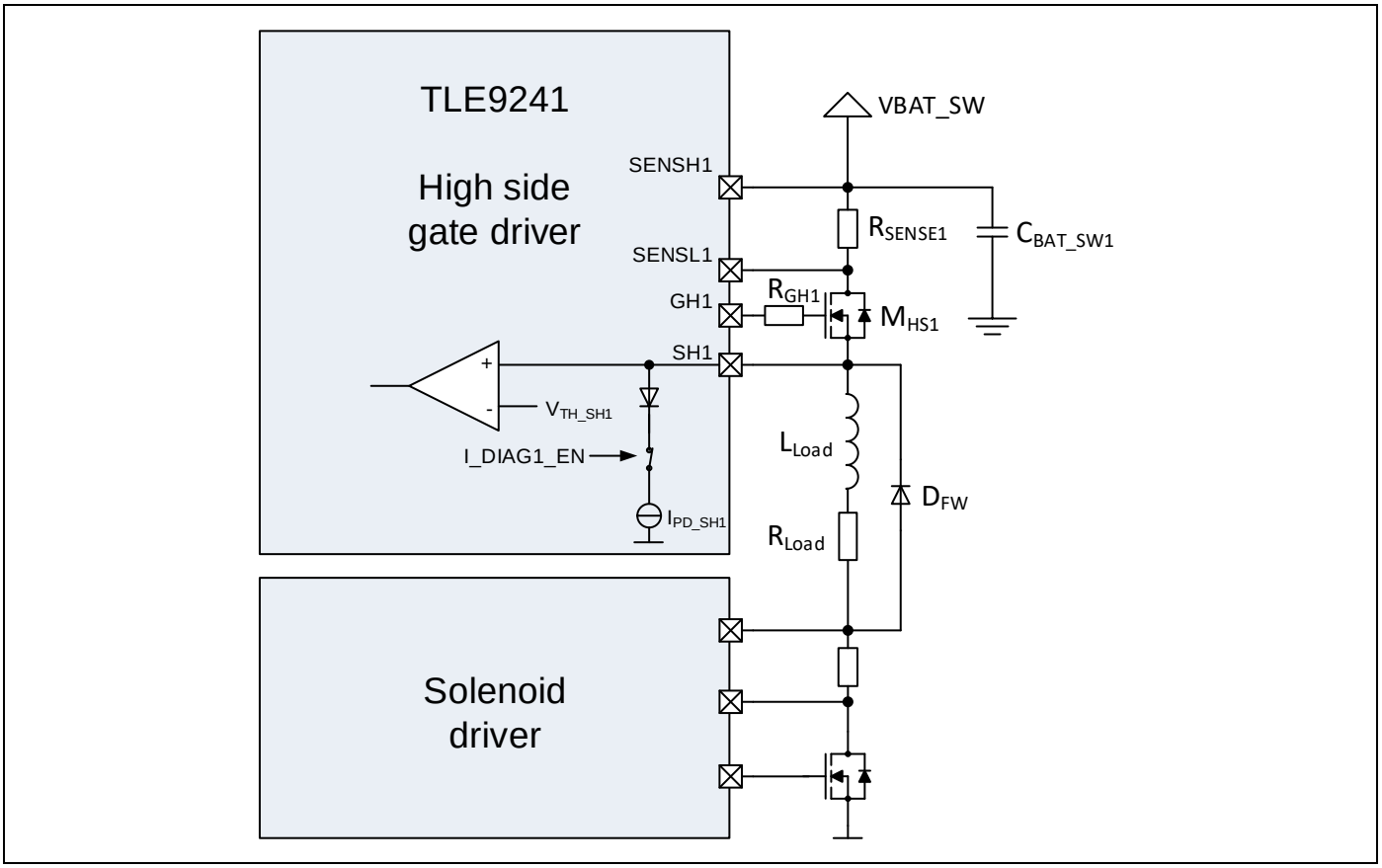

Figure 9 High side driver diagnosis current (channel 1)

In case the high-side driver is switching off and there is no freewheeling diode (D_{FW}) available across the load, the high side switch M_{HSX} (X = 1..2) will clamp the energy stored in the inductor (L_{Load}). For this scenario, the switch must be capable of clamping that amout of energy. In addition, oscillations can be prevented by adding resistors R_{GHX} (X = 1..2).

5.2.3 Overcurrent behaviour

Overcurrent diagnostic is performed after switch on when the high side blanking time T_{BL_HS} (P_5.1.6) has expired. Overcurrent is detected if the programmed threshold (I_{OCX}; X = 0..7) is exceeded for longer than the overcurrent filter time T_{FLT_OC}. The overcurrent filter is a digital filter derived from the system clock and therefore very accurate. When an overcurrent fault is detected, the channel is turned off and a high-side overcurrent fault flag

(OC1_FAIL or OC2_FAIL, see sections 7.4.2, 7.4.3) will be set. Configuration of the overcurrent threshold (bits HS_OC_TH in the Global status register, see section 7.4.1) does not affect the high side blanking time T_{BL_HS}.

The fault flags OC1_FAIL and OC2_FAIL can be accessed by an SPI read command (see sections 7.4.2, 7.4.3). The overcurrent fault is latched and can be cleared by writing a 0_B to the high-side overcurrent fault bit by an SPI write command. To re-enable the channel, first the overcurrent fault must be cleared, and then the channel state must transition from disabled to enabled by toggling the HSINx input pin from LOW to HIGH if controlled by pin (SPI_CTRL_INx = 0_B, see registers HSDRVx, sections 7.4.2, 7.4.3) or the HSIN control bit INx_STAT must be (re)set to 1_B if controlled by SPI (SPI_CTRL_INx = 1_B; no need to set the bit to 0_B first). The following list decribes these options:

1. (HSINx control, case 1):

- Clear OCx_FAIL (see registers HSDRVx, sections 7.4.2, 7.4.3) via SPI,
- Set HSINx to LOW,
- Wait for at least the high side blanking time T_{BL_HS} (P_5.1.6; time starts at HSINx falling edge),
- Set HSINx to HIGH.

2. (HSINx control, case 2):

- Set HSINx to LOW,
- Clear OCx_FAIL (see registers HSDRVx, sections 7.4.2, 7.4.3) via SPI,
- Wait for at least the high side blanking time T_{BL_HS} (P_5.1.6; time starts at CSN rising edge),
- Set HSINx to HIGH.

3. (SPI control):

- Clear OCx_FAIL (see registers HSDRVx, sections 7.4.2, 7.4.3) via SPI,
- Set INx_STAT to 1_B (needs separate HSDRVx command) via SPI.

When the RESN pin is LOW or the VDD supply voltage is below the undervoltage threshold (V_{DDUV}, P_3.2.8), both high-side channels are in the off state and the overcurrent faults flags OCx_FAIL (see registers HSDRVx, sections 7.4.2, 7.4.3) are cleared.

6 Two-wire Hall Effect sensor interfaces

6.1 Block diagram

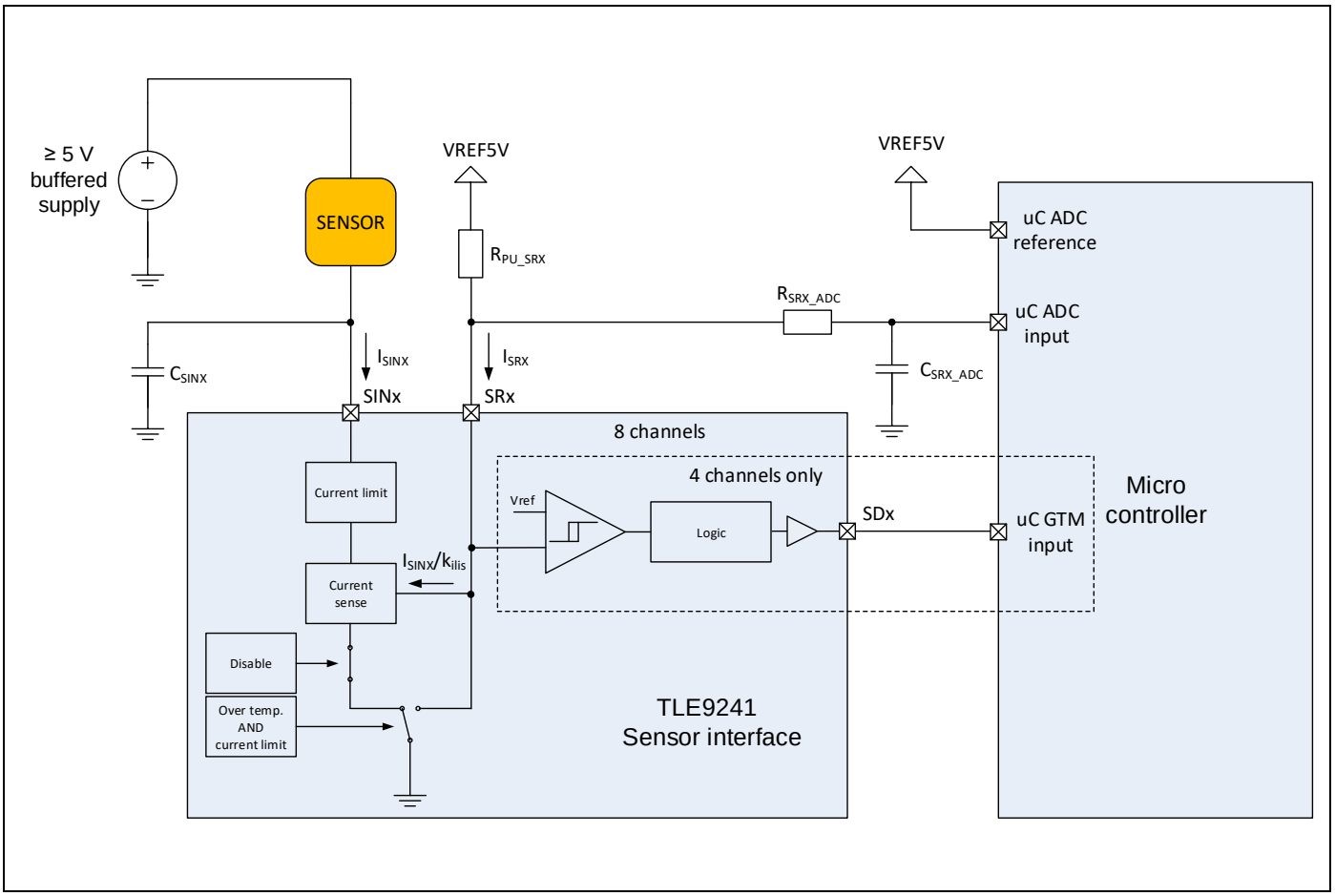

Figure 10 Sensor interface (switch position shows normal operation, i.e. channel enabled, not in overtemperature)

6.2 Description

The Hall sensor is connected between a supply (min. 5 V) and the SINx input pins. The sunk sensor current is mirrored with a ratio of typ. 20:1 (parameter k_{ilis}) to the analogue output pins SRx. The SRx pins require an external pull up resistor (R_{PU_SRX}) to generate an analogue voltage signal which is typically filtered and connected to an ADC input of the main microcontroller. The pull up resistor R_{PU_SRX} should be connected to the the reference supply VREF5V of the microcontroller ADC in order to cancel out all inaccuracies coming from that supply voltage.

The voltage on the SRx pin is inversely proportional to the sensor current I_{SINX} (see Figure 11). The state and fault status of the sensor can be detected in software by comparing the respective ADC output with pre-chosen threshold values: The minimum voltage of the SRx output pin (corresponding to the maximum measurable sensor current) is limited to the specified saturation voltage value V_{SAT_SRX} (P_6.1.10). Any value below V_{SAT_SRX} will indicate the channel is in overtemperature shutdown.

An internal register (HALLST) contains the detected state of each sensor channel. This register can be accessed by an SPI read command, see section 7.4.5. The state of the sensor is determined by comparing the SRx output pin voltage to a fixed threshold. The comparator circuit includes hysteresis for noise rejection. Since the sensor state comparision threholds are fixed, the sensor characteristics can be adjusted be selecting an appropriate value for

R_{PU_SRX}. This threshold is common to all channels (see parameters I_{TH_H}, P_6.1.6, and I_{TH_L}, P_6.1.7, assuming R_{PU_SRX} = 3.5 kΩ).

Four interface channels can be assigned to digital output pins SDx and thus can be used especially for speed sensor applications. The four digital outputs, SD1-4, can be connected to the main microcontroller to measure the period and pulse-width of the speed sensor signals (SDx output characteristic see also Figure 11). These output pins have 5 V CMOS output logic levels. The state of the output pin is the same as the value of the respective bit in the sensor state register HALLST. The digital output pins can be mapped to one of two sensor channels by configuration via the SDOMUX register (see section 7.4.7).

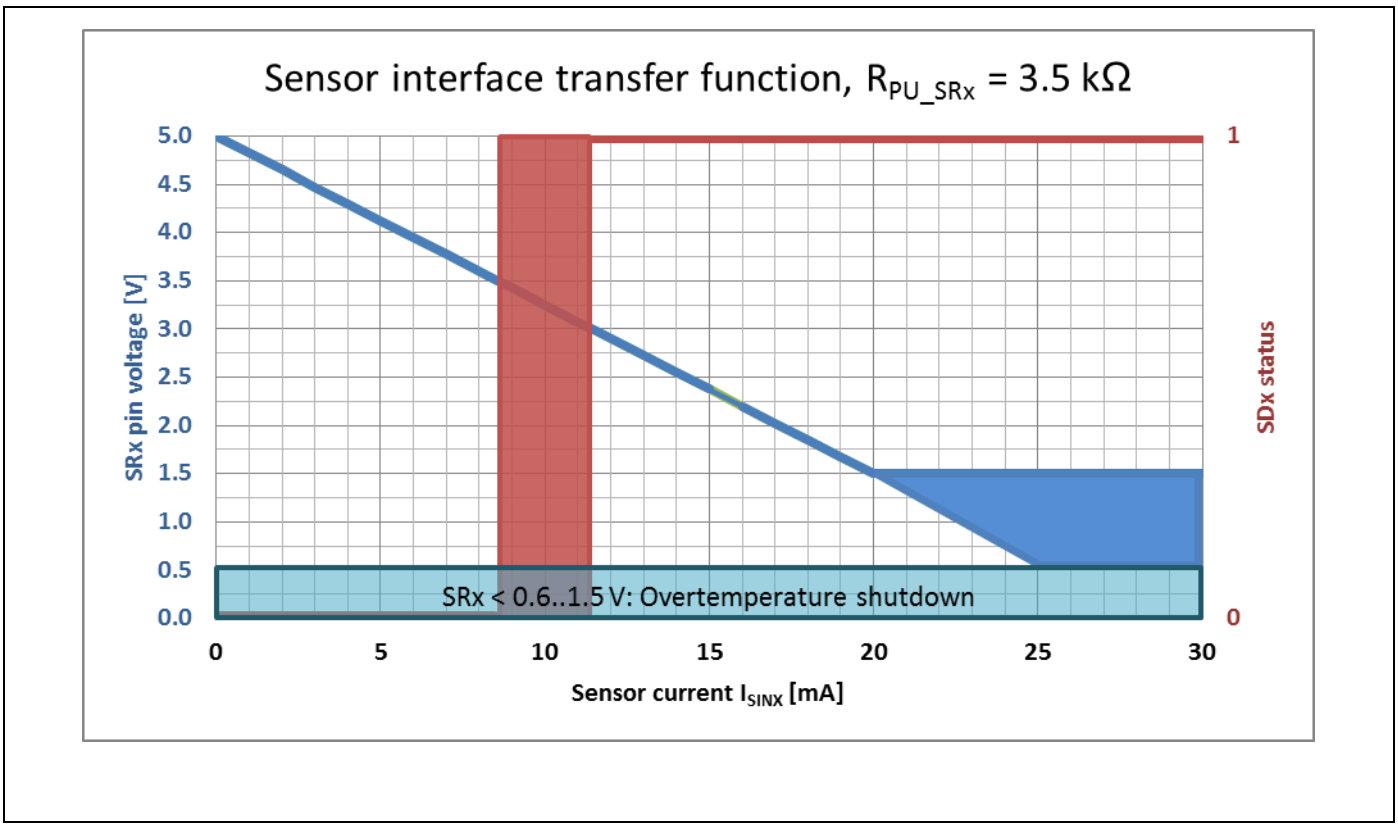

Figure 11 Sensor interface transfer function

When the temperature of the internal circuit exceeds the overtemperature threshold and the channel is in current limitation, an overtemperature fault bit is set in the HALLOT register (see section 7.4.6) which can be accessed by an SPI read. This fault is latched and can be cleared by writing a 0_B to the corresponding overtemperature fault bit. The write command will be ignored if the over temperature condition is still present.

The respective enable bit in the HALLEN register (see section 7.4.4) is automatically cleared when an overtemperature fault is detected. Also, the SRx pin is driven to a voltage close to ground potential, and the SDx pin is driven HIGH.

After clearing the overtemperature fault bit, the respective enable bit(s) for the disabled channel(s) must be set to 1 to re-enable the channel(s).

All sensor interface channels are enabled when the RESN pin transitions from LOW to HIGH and the VDD supply voltage is above the undervoltage threshold (V_{DDUV}, P_3.2.8). Each channel can be individually disabled by clearing the enable bit in the HALLEN register (see section 7.4.4) by an SPI write command.

6.3 Hall Effect sensor re-activation after overtemperature shutdown

This section will provide details about measures to be taken in case the Hall Effect sensors have been switched off due to overtemperature detection while in current limitation mode.

6.3.1 Purpose

The purpose is to protect the device from continuous operation at very high temperatures.

Note: Overtemperature events are considered exceptions. Nevertheless, measures shall be taken to protect the device.

6.3.2 Recommendation

Operation with a junction temperature above 150°C should be prevented. To achieve this, the following should be done:

- Wait some time (> 1 s, cooldown time depending on application) until re-activating the channel, and
- Avoid repeated re-tries.

7 SPI interface

7.1 Block diagram

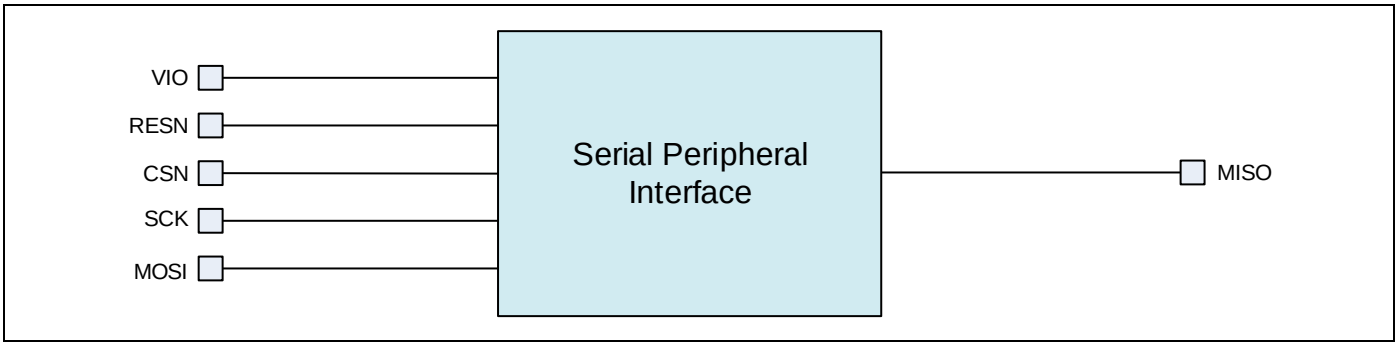

Figure 12 SPI interface

Note: For information about the RESN input pin, see section 3.1.

7.2 SPI frame

MOSI SPI frame

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RN/W	PARITY	0	0	0	ADDR[2]	ADDR[1]	ADDR[0]	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

MISO SPI frame

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RN/W	PARITY	FAULT comm.	FAULT global	0	ADDR[2]	ADDR[1]	ADDR[0]	DATA[7]	DATA[6]	DATA[5]	DATA[4]	DATA[3]	DATA[2]	DATA[1]	DATA[0]

Note: The parity bit (odd) is calculated over the entire frame (bit 15 + bits 13 - 0)

The SPI frame transmitted by the TLE9241QU (from the MISO pin) includes a “global” fault bit (MISO frame, bit 12) which indicates if an error of the type “GEN_FAULT” or “SYS_OT” (see Global Status Register, section 7.4.1) is present.

Also, the SPI frame includes a “communication” fault bit (MISO frame, bit 13) which indicates if an error of the type “COM_ERR” or “PAR_ERR” (see Global Status Register, section 7.4.1) is present.

7.3 Description

The diagnosis and control communication interface is based on the serial peripheral interface (SPI). The SPI is a full duplex synchronous serial slave interface which uses four signal lines: MISO, MOSI, SCK and CSN.

Data is transferred by the lines MOSI and MISO at the data rate given by SCK. The falling edge of CSN indicates the beginning of a data access. Data is sampled on the MOSI line at the falling edge of SCK and shifted out on line MISO at the rising edge of SCK. Each access must be terminated by a rising edge of CSN. A counter ensures that data is taken only when 16 bits have been transferred. If in one transfer cycle the number of bits transferred is not 16, the data frame is ignored and the communication error flag is set.

The interface includes a supply pin, VIO, which can be supplied with either 3.3 V or 5.0 V according to the I/O voltage requirement of the SPI master (e.g. the main microcontroller).

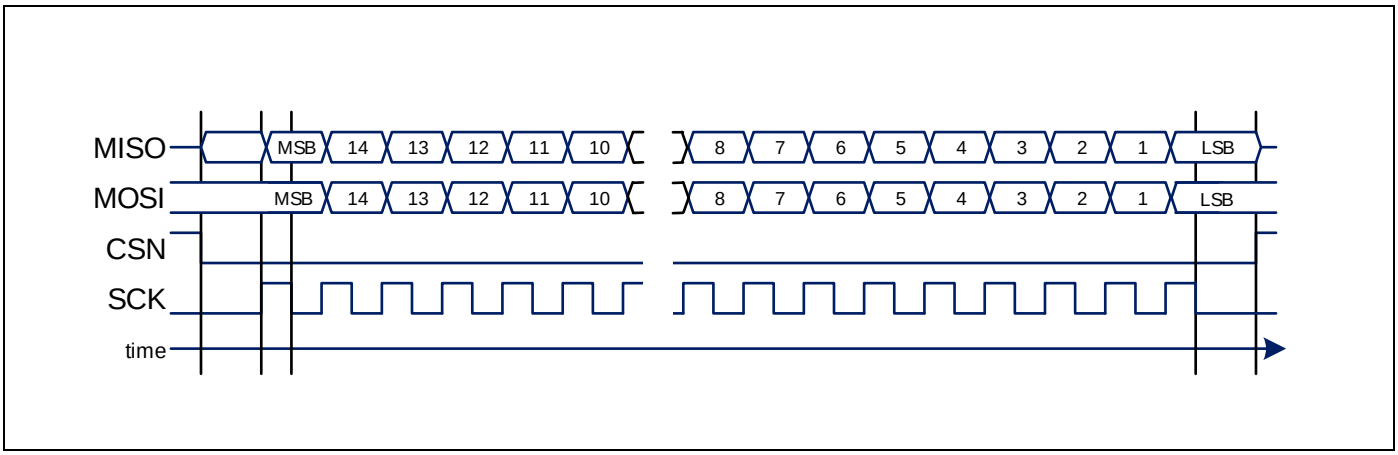

Figure 13 SPI interface signal overview

7.4 SPI registers

For each command received at the MOSI pin of the SPI interface, a serial data stream is returned at the same time on the MISO pin. The content of the MISO data frame is dependent on the command which was received on the MOSI pin during the previous frame. A READ command (RN/W = 0_B) returns the contents of the addressed register one SPI frame later. The data bits in the READ command are ignored. A WRITE command (RN/W = 1_B) will write the data bits in the SPI word to the addressed register. The actual contents of that register will be returned to the SPI master (microcontroller) during the next SPI frame. The response is not an echo of the data received from the SI pin, it is the content of the register addressed in the previous SPI Frame.

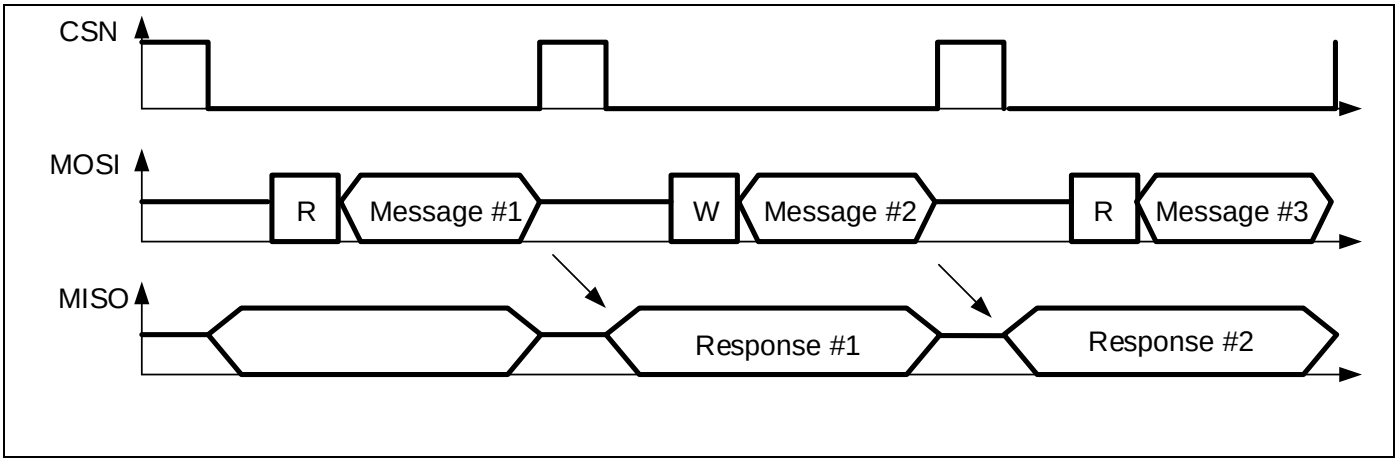

Figure 14 SPI protocol

Each SPI message for the TLE9241QU has a length of 16 bits. The message from the microcontroller must be sent MSB first. The data from the MISO pin is sent MSB first.

The response to an invalid SPI message is the IC version ID register (ICVID, see section 7.4.8).

The MISO data in the very first frame after a reset condition is fixed but subject to change and therefore shall be ignored in the application.

7.4.1 Global status register (GSR)

GSR
Global Status Register ($0x0_H$) **Reset value:** **$0x41_H$**

Field	Bits	Type	Description
HS_OC_TH	7:5	rw	**High-side overcurrent detection threshold voltage** $0x7_H$ **200 mV**, $0x6_H$ **175 mV**, $0x5_H$ **150 mV**, $0x4_H$ **125 mV**, $0x3_H$ **100 mV**, $0x2_H$ **75 mV** (default), $0x1_H$ **50 mV**, $0x0_H$ **25 mV**,
SYS_OT	4:4	r	**System/ambient overtemperature** $0x1_H$ **EN**, System/ambient temperature is too hot $0x0_H$ **DIS**, No system overtemperature failure has been detected (default)
GEN_FAULT	3:3	r	**General fault flag** $0x1_H$ **EN**, At least one fault was detected $0x0_H$ **DIS**, No fault was detected (default)
COM_ERR	2:2	wc	**Communication error flag** $0x1_H$ **EN**, At least one communication failure was detected $0x0_H$ **DIS**, No communication failure was detected (default)
PAR_ERR	1:1	wc	**Parity error flag** $0x1_H$ **EN**, At least one parity error was detected $0x0_H$ **DIS**, No parity error was detected (default)
RES_POR	0:0	wc	**Reset/Power-on reset** $0x1_H$ **EN**, A reset or POR has occurred since this bit was cleared (default) $0x0_H$ **DIS**, No reset or POR has occurred since this bit was cleared

The Global Status Register GSR includes a RES_POR (Reset – power on reset) bit which is set when the RESN pin transitions from LOW to HIGH and the VDD supply voltage is higher than the undervoltage threshold. The RES_POR bit is cleared by writing a 0_B to the RES_POR bit by an SPI write command.

There is parity checking of both incoming and outgoing SPI messages. A PAR_ERR fault bit is set whenever a parity error is detected. This fault bit is latched and can be reset by writing a 0_B to the PAR_ERR bit by an SPI write command.

In addition, there is a communication error fault bit (COM_ERR) which is set whenever a communication error is detected. Errors include wrong number of clock pulses and an invalid SPI command. The fault is latched and can be reset by writing a 0_B to the COM_ERR bit by an SPI write command.

Also, there is a general fault bit (GEN_FAULT) which indicates if a fault was detected. It includes overcurrent of a high-side pre driver and overtemperature of a Hall Effect sensor.

7.4.2 High-side driver 1 (HSDRV1)

HSDRV1
High-Side DRiVer 1 (0x1$_H$) **Reset value: 0x08$_H$**

Field	Bits	Type	Description
OC1_FAIL	7:7	wc	**High-side 1 overcurrent failure detection** 0x1$_H$ **EN**, Overcurrent failure detected (high-side driver switched OFF) 0x0$_H$ **DIS**, No overcurrent failure was detected (default)
N.A.	6:5	r	**Unused** 0x0$_H$
SPI_CTRL_IN1	4:4	rw	**High-side driver 1 input control mode** 0x1$_H$ **SPI**, High-side pre-driver input is controlled via SPI bit IN1_STAT 0x0$_H$ **PIN**, High-side pre-driver input is controlled via HSIN1 pin (default)
I_DIAG1_EN	3:3	rw	**High-side output 1 diagnosis current enable** 0x1$_H$ **ON**, Diagnosis current ENABLED (default) 0x0$_H$ **OFF**, Diagnosis current DISABLED
OUT1_STAT	2:2	r	**High-side output 1 status diagnosis** 0x1$_H$ **EN**, Output voltage is above the threshold voltage V_{TH_SHX} 0x0$_H$ **DIS**, Output voltage is below the threshold voltage V_{TH_SHX} (default)
IN1_STAT	1:1	r/rw [1)]	**High-side 1 IN pin status/control** 0x1$_H$ **EN**, High-side driver is commanded ON 0x0$_H$ **DIS**, High-side driver is commanded OFF (default)
DIS1_STAT	0:0	r	**High-side 1 DIS pin status** 0x1$_H$ **EN**, High-side driver is enabled 0x0$_H$ **DIS**, High-side driver is disabled (default)

[1)] r for SPI_CTRL_IN1 = 0$_B$; rw for SPI_CTRL_IN1 = 1$_B$

7.4.3 High-side driver 2 (HSDRV2)

HSDRV2
High-Side DRiVer 2 (0x2$_H$) **Reset value: 0x08$_H$**

Field	Bits	Type	Description
OC2_FAIL	7:7	wc	**High-side 2 overcurrent failure detection** 0x1$_H$ **EN**, Overcurrent failure detected (high-side driver switched OFF) 0x0$_H$ **DIS**, No overcurrent failure was detected (default)
N.A.	6:5	r	**Unused** 0x0$_H$
SPI_CTRL_IN2	4:4	rw	**High-side driver 2 input control mode** 0x1$_H$ **SPI**, High-side pre-driver input is controlled via SPI bit IN2_STAT 0x0$_H$ **PIN**, High-side pre-driver input is controlled via HSIN2 pin (default)
I_DIAG2_EN	3:3	rw	**High-side output 2 diagnosis current enable** 0x1$_H$ **ON**, Diagnosis current ENABLED (default) 0x0$_H$ **OFF**, Diagnosis current DISABLED
OUT2_STAT	2:2	r	**High-side output 2 status diagnosis** 0x1$_H$ **EN**, Output voltage is above the threshold voltage V_{TH_SHX} 0x0$_H$ **DIS**, Output voltage is below the threshold voltage V_{TH_SHX} (default)
IN2_STAT	1:1	r/rw [1)]	**High-side 2 IN pin status/control** 0x1$_H$ **EN**, High-side driver is commanded ON 0x0$_H$ **DIS**, High-side driver is commanded OFF (default)
DIS2_STAT	0:0	r	**High-side 2 DIS pin status** 0x1$_H$ **EN**, High-side driver is enabled 0x0$_H$ **DIS**, High-side driver is disabled (default)

[1)] r for SPI_CTRL_IN2 = 0$_B$; rw for SPI_CTRL_IN2 = 1$_B$

7.4.4 Hall interface enable (HALLEN)

HALLEN

HALL interface ENable ($0x3_H$) **Reset value:** **$0xFF_H$**

Field	Bits	Type	Description
SENS_EN8	7:7	rw	**Sensor interface 8 enable** $0x1_H$ **EN**, Sensor interface is enabled (default) $0x0_H$ **DIS**, Sensor interface is disabled
SENS_EN7	6:6	rw	**Sensor interface 7 enable** $0x1_H$ **EN**, Sensor interface is enabled (default) $0x0_H$ **DIS**, Sensor interface is disabled
SENS_EN6	5:5	rw	**Sensor interface 6 enable** $0x1_H$ **EN**, Sensor interface is enabled (default) $0x0_H$ **DIS**, Sensor interface is disabled
SENS_EN5	4:4	rw	**Sensor interface 5 enable** $0x1_H$ **EN**, Sensor interface is enabled (default) $0x0_H$ **DIS**, Sensor interface is disabled
SENS_EN4	3:3	rw	**Sensor interface 4 enable** $0x1_H$ **EN**, Sensor interface is enabled (default) $0x0_H$ **DIS**, Sensor interface is disabled
SENS_EN3	2:2	rw	**Sensor interface 3 enable** $0x1_H$ **EN**, Sensor interface is enabled (default) $0x0_H$ **DIS**, Sensor interface is disabled
SENS_EN2	1:1	rw	**Sensor interface 2 enable** $0x1_H$ **EN**, Sensor interface is enabled (default) $0x0_H$ **DIS**, Sensor interface is disabled
SENS_EN1	0:0	rw	**Sensor interface 1 enable** $0x1_H$ **EN**, Sensor interface is enabled (default) $0x0_H$ **DIS**, Sensor interface is disabled

7.4.5 Hall sensor status (HALLST)

HALLST

HALL sensor STatus ($0x4_H$) **Reset value:** **$0x00_H$**

Field	Bits	Type	Description
SENS8_STATE	7:7	r	**Sensor interface 8 sensor state** $0x1_H$ **HIGH**, Sensor is in HIGH state $0x0_H$ **LOW**, Sensor is in LOW state (default)
SENS7_STATE	6:6	r	**Sensor interface 7 sensor state** $0x1_H$ **HIGH**, Sensor is in HIGH state $0x0_H$ **LOW**, Sensor is in LOW state (default)
SENS6_STATE	5:5	r	**Sensor interface 6 sensor state** $0x1_H$ **HIGH**, Sensor is in HIGH state $0x0_H$ **LOW**, Sensor is in LOW state (default)
SENS5_STATE	4:4	r	**Sensor interface 5 sensor state** $0x1_H$ **HIGH**, Sensor is in HIGH state $0x0_H$ **LOW**, Sensor is in LOW state (default)
SENS4_STATE	3:3	r	**Sensor interface 4 sensor state** $0x1_H$ **HIGH**, Sensor is in HIGH state $0x0_H$ **LOW**, Sensor is in LOW state (default)
SENS3_STATE	2:2	r	**Sensor interface 3 sensor state** $0x1_H$ **HIGH**, Sensor is in HIGH state $0x0_H$ **LOW**, Sensor is in LOW state (default)
SENS2_STATE	1:1	r	**Sensor interface 2 sensor state** $0x1_H$ **HIGH**, Sensor is in HIGH state $0x0_H$ **LOW**, Sensor is in LOW state (default)
SENS1_STATE	0:0	r	**Sensor interface 1 sensor state** $0x1_H$ **HIGH**, Sensor is in HIGH state $0x0_H$ **LOW**, Sensor is in LOW state (default)

7.4.6 Hall sensor overtemperature (HALLOT)

HALLOT

HALL sensor OverTemperature ($0x5_H$) **Reset value:** **$0x00_H$**

Field	Bits	Type	Description
SENS8_OT	7:7	wc	**Sensor interface 8 overtemperature** $0x1_H$ **EN**, Overtemperature failure was detected $0x0_H$ **DIS**, No overtemperature failure was detected (default)
SENS7_OT	6:6	wc	**Sensor interface 7 overtemperature** $0x1_H$ **EN**, Overtemperature failure was detected $0x0_H$ **DIS**, No overtemperature failure was detected (default)
SENS6_OT	5:5	wc	**Sensor interface 6 overtemperature** $0x1_H$ **EN**, Overtemperature failure was detected $0x0_H$ **DIS**, No overtemperature failure was detected (default)
SENS5_OT	4:4	wc	**Sensor interface 5 overtemperature** $0x1_H$ **EN**, Overtemperature failure was detected $0x0_H$ **DIS**, No overtemperature failure was detected (default)
SENS4_OT	3:3	wc	**Sensor interface 4 overtemperature** $0x1_H$ **EN**, Overtemperature failure was detected $0x0_H$ **DIS**, No overtemperature failure was detected (default)
SENS3_OT	2:2	wc	**Sensor interface 3 overtemperature** $0x1_H$ **EN**, Overtemperature failure was detected $0x0_H$ **DIS**, No overtemperature failure was detected (default)
SENS2_OT	1:1	wc	**Sensor interface 2 overtemperature** $0x1_H$ **EN**, Overtemperature failure was detected $0x0_H$ **DIS**, No overtemperature failure was detected (default)
SENS1_OT	0:0	wc	**Sensor interface 1 overtemperature** $0x1_H$ **EN**, Overtemperature failure was detected $0x0_H$ **DIS**, No overtemperature failure was detected (default)

7.4.7 Sensor digital output MUX (SDOMUX)

SDOMUX
Sensor Digital Output MUX ($0x6_H$) **Reset value: $0x00_H$**

Field	Bits	Type	Description
N.A.	7:4	r	**Unused** $0x0_H$
SD4_8	3:3	rw	**Digital Hall sensor interface assignment 4/8** $0x1_H$ **SENS8**, Hall sensor interface 8 is connected to SD4 $0x0_H$ **SENS4**, Hall sensor interface 4 is connected to SD4 (default)
SD3_7	2:2	rw	**Digital Hall sensor interface assignment 3/7** $0x1_H$ **SENS7**, Hall sensor interface 7 is connected to SD3 $0x0_H$ **SENS3**, Hall sensor interface 3 is connected to SD3 (default)
SD2_6	1:1	rw	**Digital Hall sensor interface assignment 2/6** $0x1_H$ **SENS6**, Hall sensor interface 6 is connected to SD2 $0x0_H$ **SENS2**, Hall sensor interface 2 is connected to SD2 (default)
SD1_5	0:0	rw	**Digital Hall sensor interface assignment 1/5** $0x1_H$ **SENS5**, Hall sensor interface 5 is connected to SD1 $0x0_H$ **SENS1**, Hall sensor interface 1 is connected to SD1 (default)

7.4.8 IC version ID (ICVID)

ICVID
IC Version ID ($0x7_H$) **Reset value: 0xA2**

Field	Bits	Type	Description
ICVID	7:0	r	**IC Version ID** 0xA2, Chip release version

8 Application information

This chapter describes how the device is used in its environment.

8.1 Application diagram

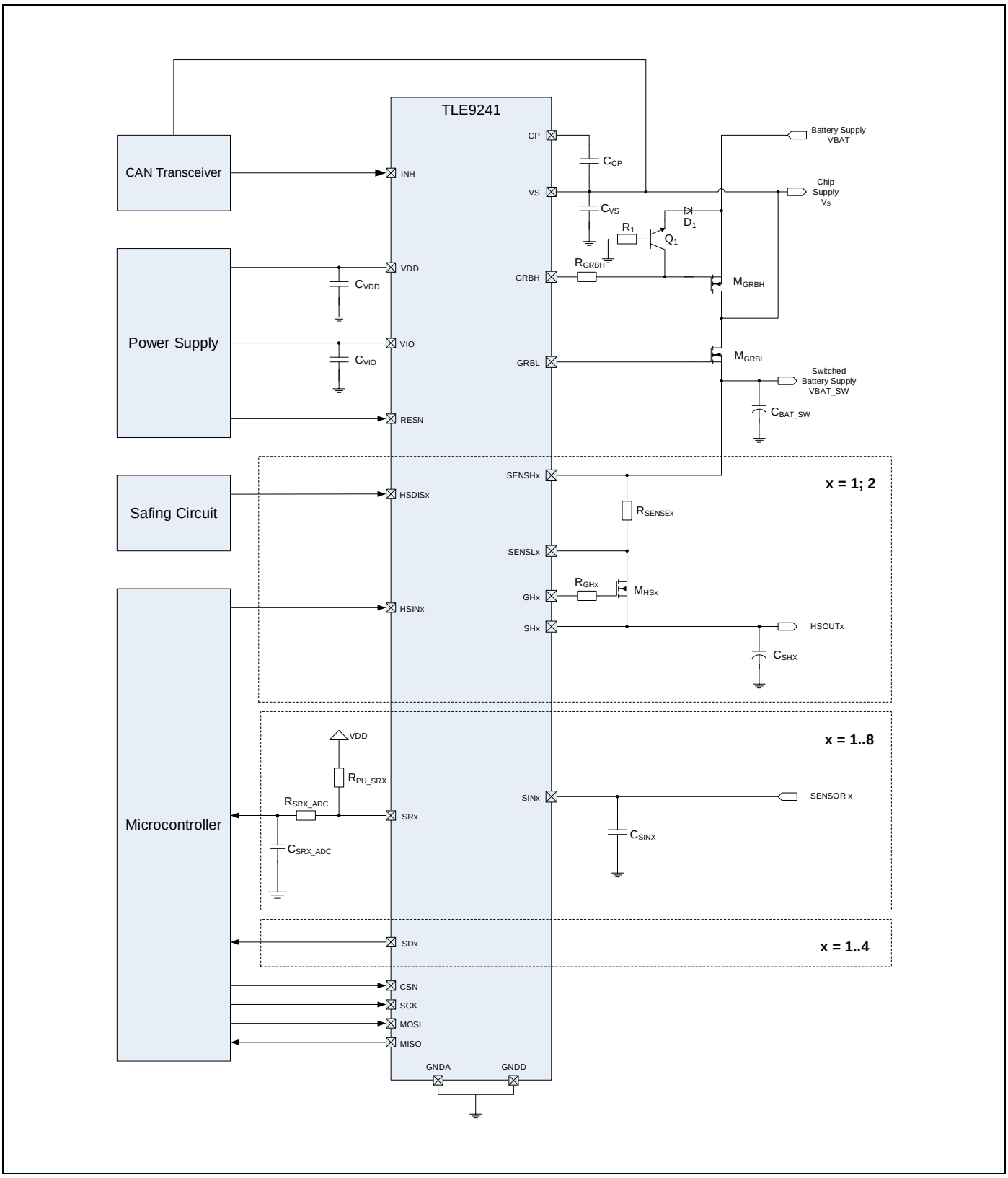

Figure 15 Application circuit

Notes:

1. *The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*
2. *If compliance to ISO Test pulse 2 is required also in sleep mode, specific measures such as moving the capacitor shown on the VBAT_SW(switched node, C_{BAT_SW}) to the VS node, should be considered. Please be aware that the capacitor can be exposed to positive and negative voltages in such a configuration.*

8.2 External components

The following table gives recommendations for the external components shown in Figure 15.

8.2.1 Active components

This section lists components to be considered as example (may need to be adapted based on the individual application requirements):

- D_1: BAL99_323,
- Q_1: BC846B,
- M_{GRBH}: IPC50N04S5-5R8,
- M_{GRBL}: IPC50N04S5-5R8,
- M_{HSX}: IPZ40N04S5-8R4 (see also note in section 5.1).

8.2.2 Passive components

Table 3 Passive components (nominal values, tolerance not considered)

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Supply input capacitor	C_{VS}, C_{VDD}, C_{VIO}		100		nF	place close to IC pin
Charge pump capacitor	C_{CP}	100		220	nF	see section 3.3 on dimensioning C_{CP}, place close to IC pin
SRx pullup resistor	R_{PU_SRX}		3.5		kΩ	
SRx ADC filter resistor	R_{SRX_ADC}		47		kΩ	
SRx ADC filter capacitor	C_{SRX_ADC}		22		nF	
SINx sensor input capacitance	C_{SINX}		100		nF	
Sense resistor	R_{SENSEX}		7		mΩ	
High side GHx gate resistor	R_{GHX}		100		Ω	optional, to minimize oscillations in case of inductive discharge
GRBH gate resistor	R_{GRBH}		47		kΩ	optional
Bias resistor	R_1		10		kΩ	
Bulk capacitor	C_{BAT_SW}		10		µF	see note 2 in section 8.1

Revision history

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