Switching behavior analysis for TLE92108/4

About this document

Scope and purpose

This application note provides information about the analysis of typical bridge switching defects due to wrong configurations of TLE92108/4 from the MOTIX™ family. This document should be used with the corresponding datasheet, which contains full technical details on the device specification and operation.

Intended audience

Developers working with the TLE92108/4.

Table of contents

1 Introduction

The TLE92108/4 is a Multiple-MOSFET driver IC dedicated to control up to sixteen n-channel MOSFETs. Eight half-bridge drivers are integrated in TLE92108, respectively four half-bridge drivers in TLE92104 for DC motor control applications such as automotive power seats, power lift gates, cargo cover, sunroof, door lock, window lifts, etc.

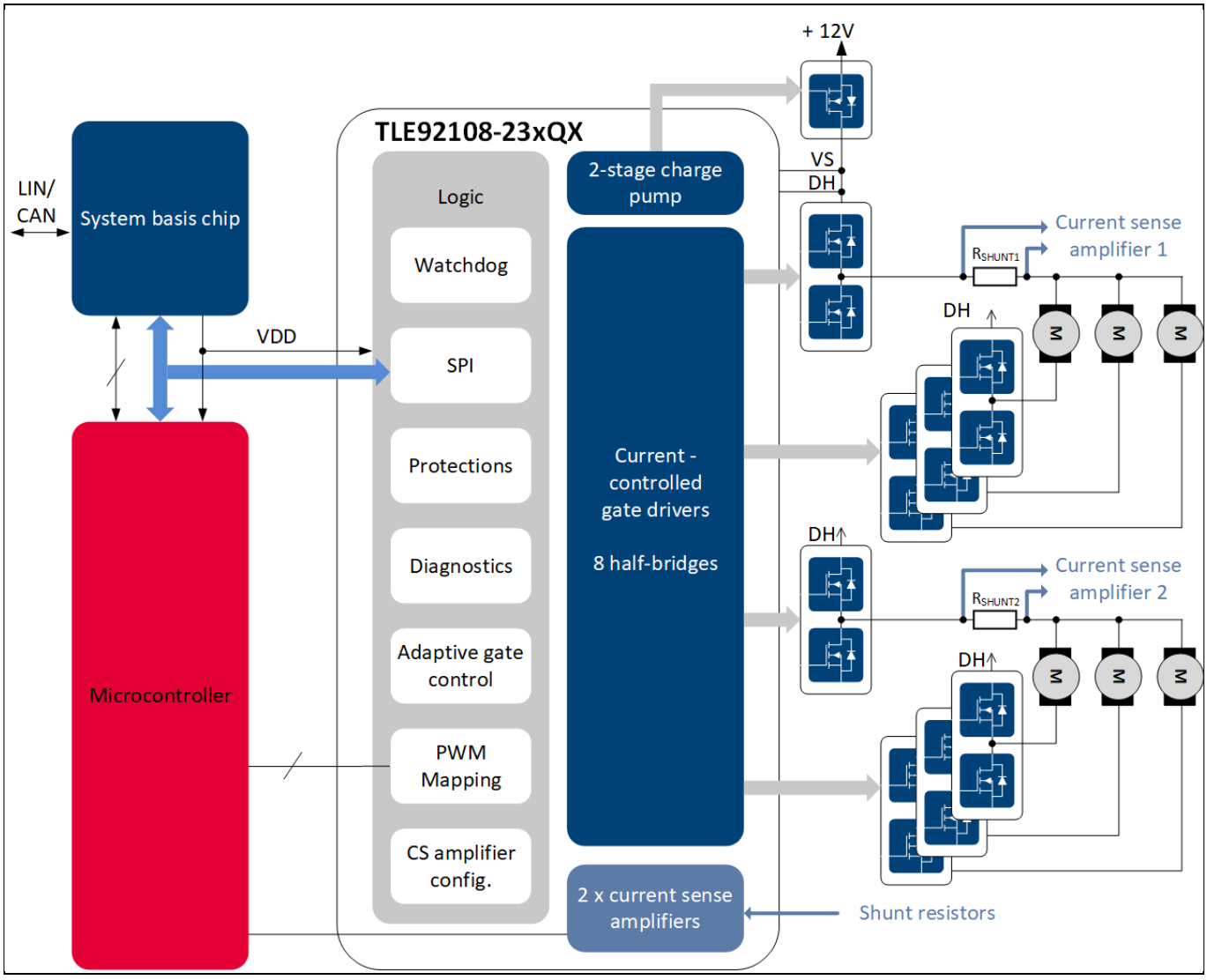

Figure 1 TLE92108 simplified block diagram in one of the possible half-bridge configurations

2 Example of a working configuration

2.1 Test setup

2.1.1 Device under test

Infineon's TLE92108 APPKIT is the device to be tested. It provides users with an easy method to measure and evaluate the TLE92108 Multi MOSFET Driver ICs. The main board is loaded with Infineon's Multi MOSFET Driver IC TLE92108/4, including eight half-bridge MOSFETs and an active reverse polarity protection MOSFET. On the board, there is a connector for uIO stick, with which it is possible to configure TLE92108/4 using Config Wizard in the Infineon Toolbox, as is shown in **belowFigure 2**.

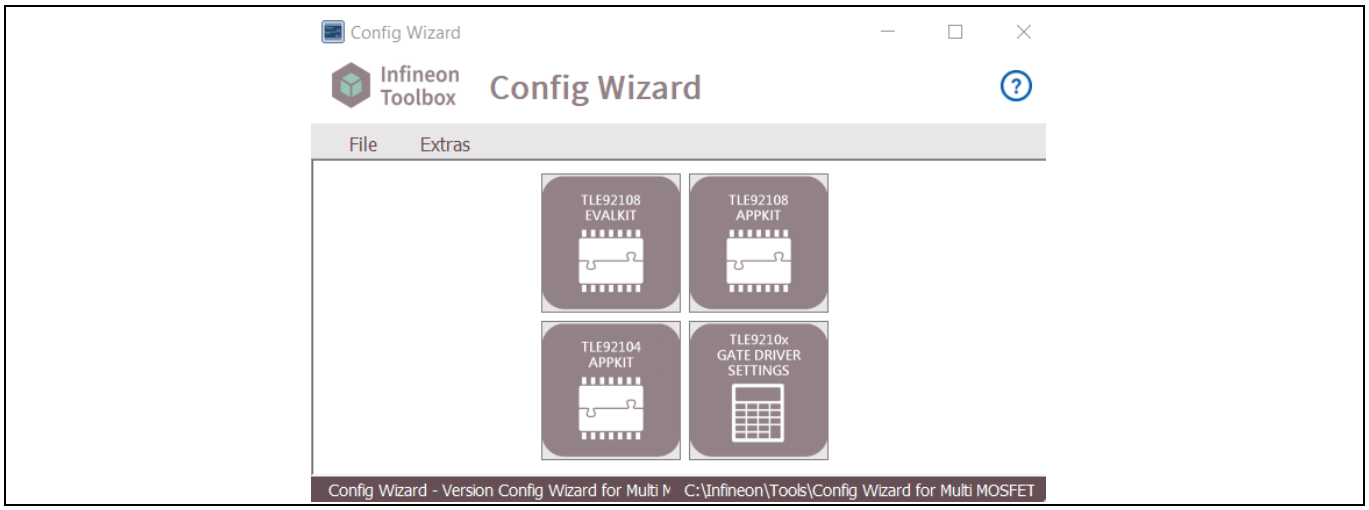

Figure 2 Config Wizard for multi MOSFET

2.1.2 Motor

The motor implemented in all tests shown in this application note is a 12V brush DC motor with 2 pole pairs. This motor features high rotation speed and large moment of force, which is 1 Kgf.cm. The motor is powered with a 12 V DC voltage source. At this voltage level, the rated speed of the motor is 3500 RPM, and the rated power is 30 W.

2.1.3 Config Wizard

The graphical interface Config Wizard supports developers in configuring the parameters of TLE92108/4. There are three categories of configuration, 'Motor Control', 'Detailed Settings' and 'PWM Diagnostics respectively'. In this example, a correct configuration is presented which should be taken as a reference.

As is shown in **Figure 3**, half bridge 1 and half bridge 2 are enabled, where LS1 is the active MOSFET controlled by PWM1 with a defined duty cycle. In this case, HS1 is the freewheeling MOSFET. All other configurations are from default settings defined in Config Wizard provided as reference. Note that the Config Wizard pre-configures the control registers of TLE92108/4 and optimizes the settings for the IPZ40N04S5-3R1 MOSFET.

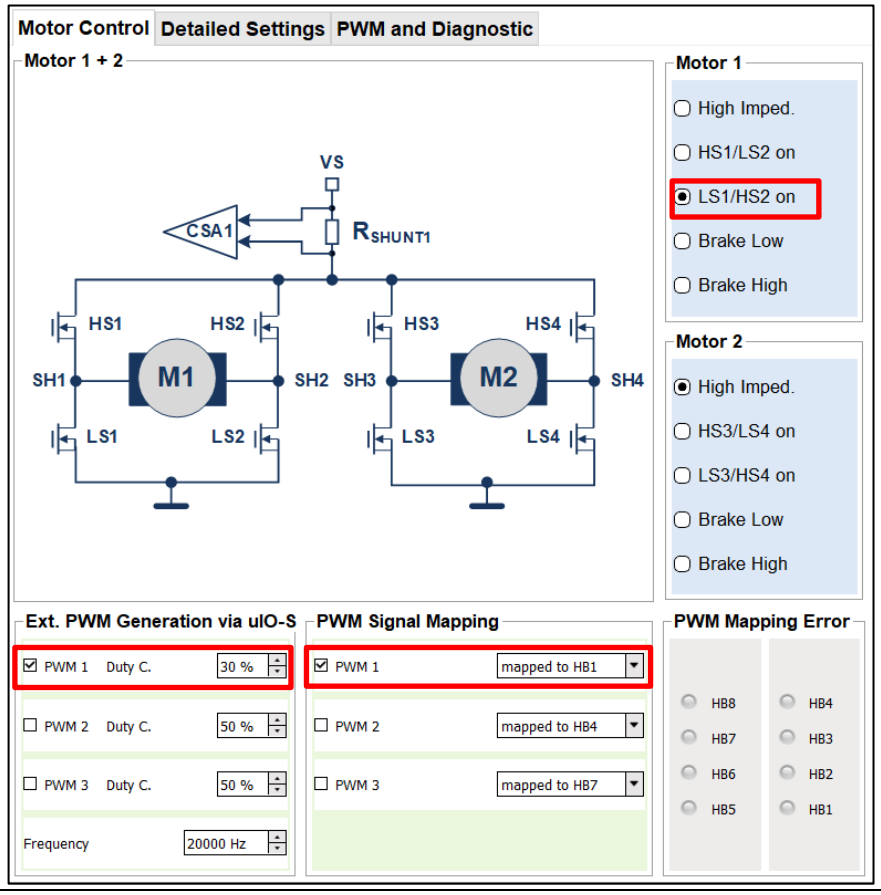

Figure 3 Configuration with LS1/HS2 on and PWM1 mapped to HB1

2.2 Overview of parameters

To achieve different switching behavior the settings in the Config Wizard can be modified, as shown in **Table 1**.

Table 1 Default parameter settings in Config Wizard

Parameter	Description	Default value
$t_{blank\_active1}$	Blank time of active MOSFET on half bridge 1	2 µs
t_{FVDS}	Drain source monitoring filter time	1 µs
I_{HOLD}	Hold charge/discharge current	12.5 mA / 14.2 mA
I_{CHG}	Charge current	8 mA
I_{DCHG}	Discharge current	9.4 mA
$t_{CCP\_active1}$	Cross current conduction time of active MOSFET on half bridge 1	3 µs
V_{DSTH}	Drain-source overvoltage threshold	0.2 V
Postcharge	-	enabled
Adaptive gate control	-	pre-discharge activated

The following abbreviations and symbols are used in this document:

Table 2 Symbol definition

Symbol	Description
HS	High side
LS	Low side
HB	Half bridge
FW	Free-wheeling
V_{GLS}	Low side gate voltage
V_{SH}	Voltage of junction point between high side and low side
I_G	Gate current
t_{CCP}	Cross current protection time
V_{DS}	Voltage drop across drain and source of MOSFET
V_{FD}	Forward voltage of the MOSFET’s body diode
VDSOV	Drain-source overvoltage
t_{blank}	Blank time
EM	Electromagnetic

2.3 Analysis of reference measurement

To better understand the switching behavior of the device, the following pins are measured:

- PWM1: PWM signal applied to PWM 1
- V_{GLS1}: voltage of low side 1 gate
- V_{SH1}: voltage of the junction point between high side 1 and low side 1
- I_G: gate current of low side 1

As shown in **Figure 4**, the gate driver switches on and off controlled by the PWM signal. This figure shows the desired switching behavior of a MOSFET, which is taken as the reference for switching error diagnosis. Detailed analysis of the switching behavior is shown in two parts: switch-on and switch-off respectively.

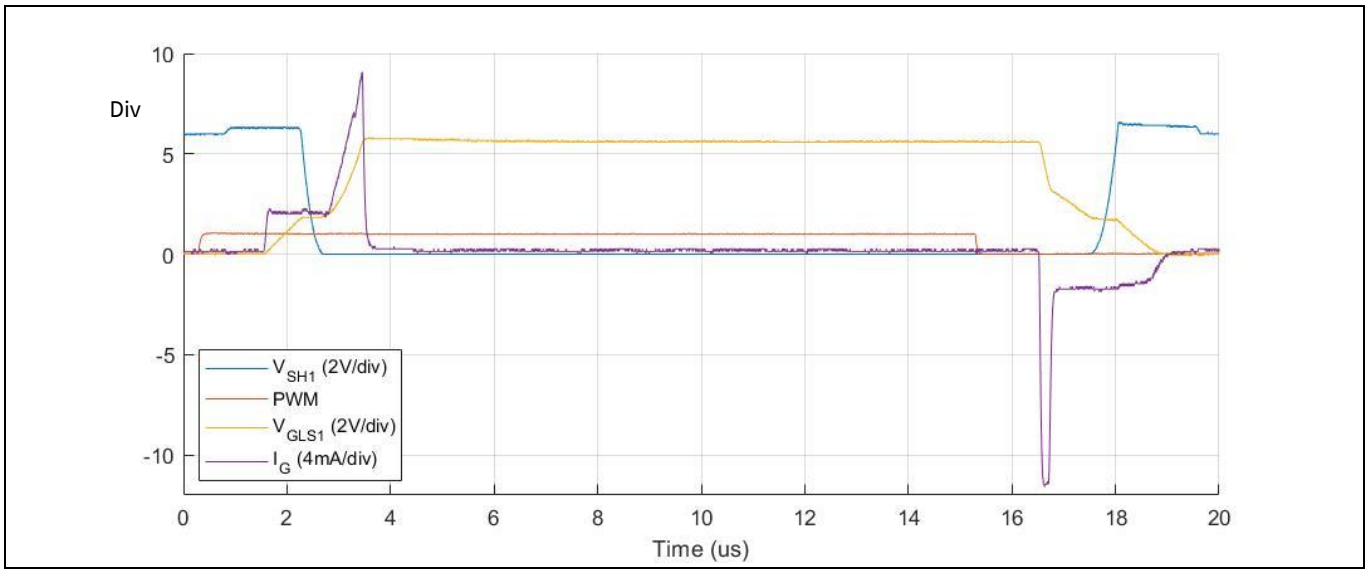

Figure 4 Overview of measurement result with default configuration

2.3.1 Switch-on analysis

When the active MOSFET switches on, the following phases can be seen, as shown in **Figure 5**:

1. At the PWM1 rising edge, the FW MOSFET is first turned off during t_{CCP} FW to avoid cross-current conduction. V_{SH1} increases slightly when the FW MOSFET is completely turned off.
2. After t_{CCP} FW, if the FW discharge current is configured correctly, the FW MOSFET is already switched off, and the active MOSFET will be switched on:
    a. Initially I_G = 8 mA, and V_{GLS1} ramps up steadily.
    b. During Miller Plateau, V_{GLS1} and I_G are both constant, and V_{SH1} drops down from $V_S + V_{FD}$ to $R_{dson} \times I_{load}$.
    c. After Miller Plateau, the MOSFET conducts, and is further charged with the postcharge current. V_{GLS1} rises up.
    d. When V_{GLS1} is about 11 V, the MOSFET is completely switched on.

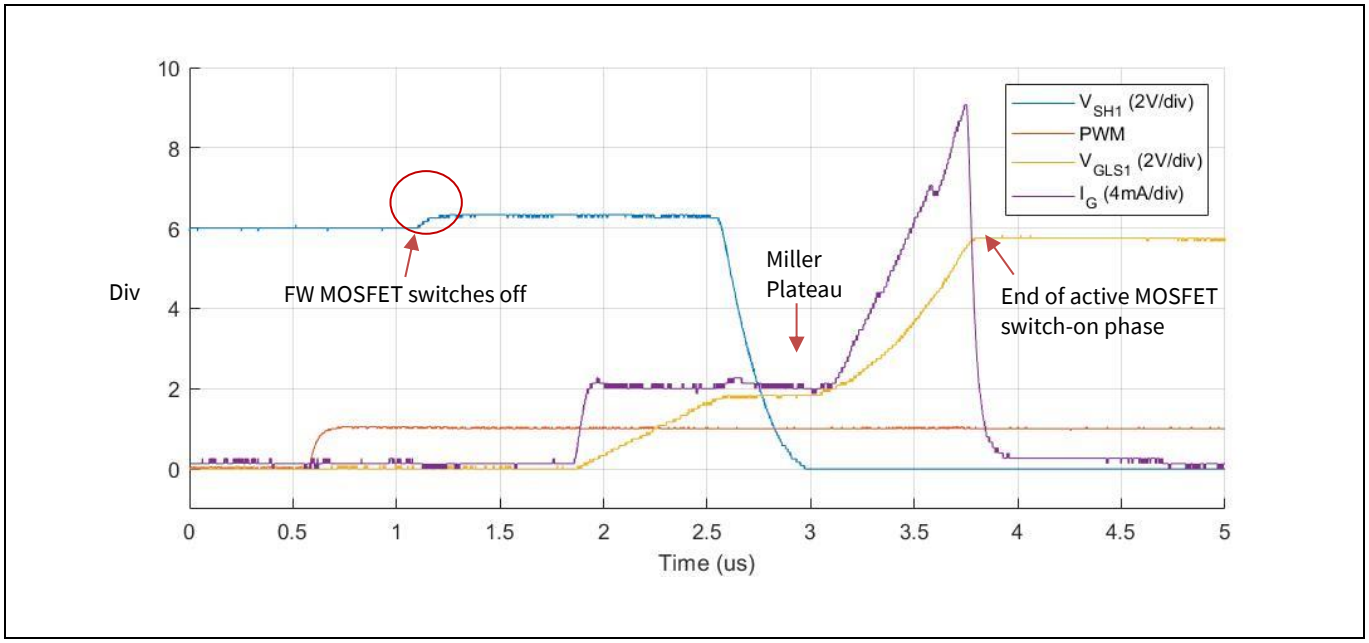

Figure 5 Active MOSFET switch-on behavior

2.3.2 Switch-off analysis

When the active MOSFET switches off, the following phases can be observed, as shown in **Figure 6**:

1. At the PWM1 falling edge, after t_{CCP} FW, the active MOSFET will be turned off:
   a. The Config Wizard presets a 58.6 mA pre-discharge current for 250 ns.
   b. After the pre-discharge phase, I_G = -9.4 mA, the active MOSFET is slowly discharged until it reaches Miller Plateau.
   c. After Miller Plateau, the MOSFET is further discharged with the constant discharge current until it is completely off.
2. At the end of t_{CCP} active, the gate of the FW MOSFET starts to be charged. When the FW MOSFET is fully turned on, V_{SH1} decreases by V_{FD}.

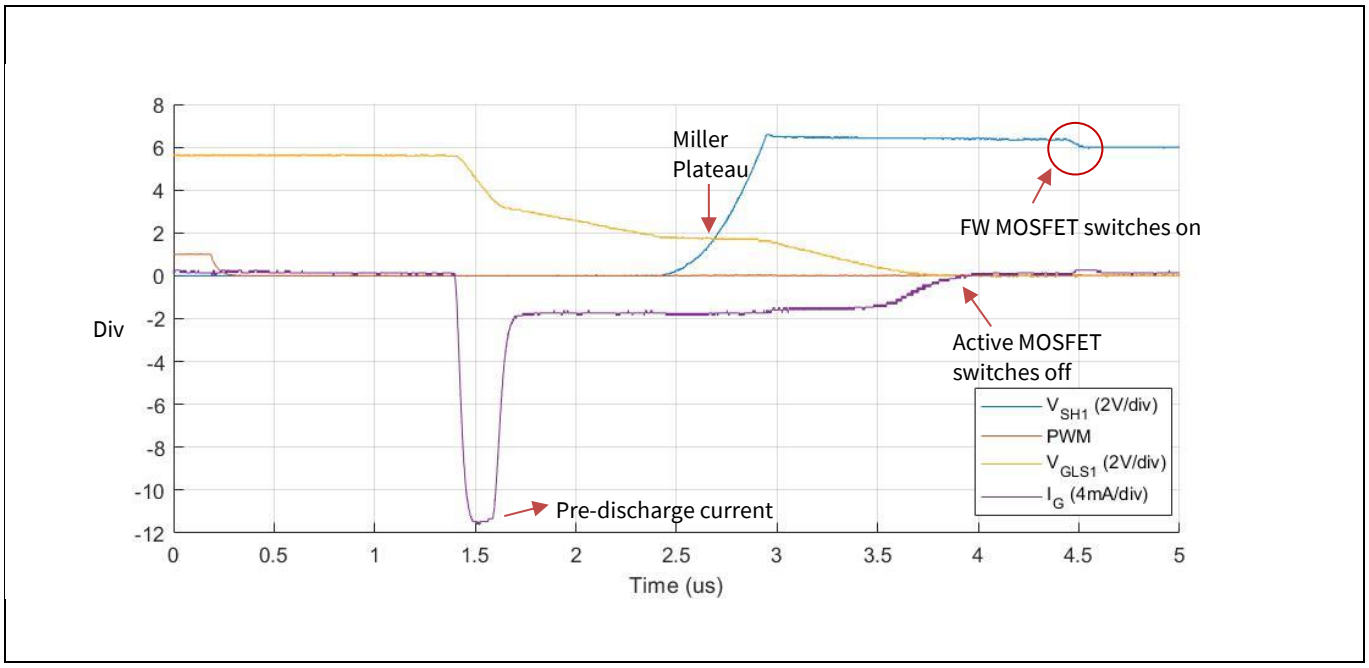

Figure 6 Active MOSFET switch-off behavior

3 Drain-source overvoltage error triggered due to short blank time and VDS filter time

Drain-source monitoring is a protection method implemented in TLE92108/4-232QX device to detect the short circuit. When the voltage drop across the drain and source of a MOSFET is bigger than the pre-defined threshold, the device reports a VSDOV error and switches off the impacted half bridges. If the drain-source monitoring threshold and the filter time are not properly defined, this error can be triggered even in normal operation.

To show the effect of this error, the settings of the gate driver are adapted, as shown in **Figure 7**. The $t_{blank\_active1}$ is the smallest value at 625 ns. t_{FVDS} = 0.5 us, which is the shortest filter time. All other settings are exactly the same as during the first test. Refer to **Table 3**.

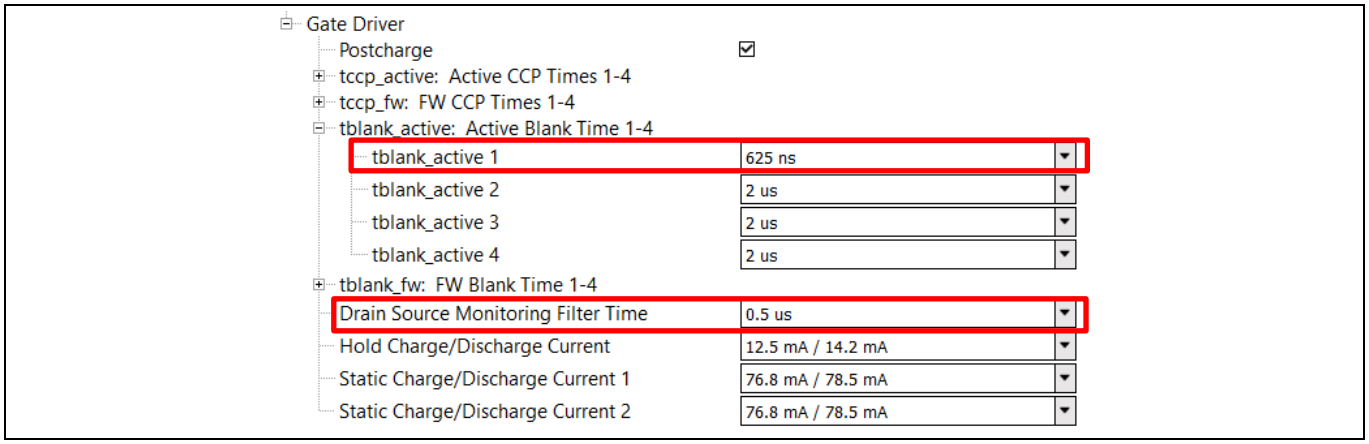

Figure 7 Blank time and filter time settings

Table 3 Configuration for drain-source overvoltage error test

Parameter	Default value	New value
$t_{blank\_active1}$	2 µs	625 ns
t_{FVDS}	1 µs	0.5 µs
I_{HOLD}	12.5 mA / 14.2 mA	-
I_{CHG}	8 mA	-
I_{DCHG}	9.4 mA	-
$t_{CCP\_active1}$	3 µs	-
V_{DSTH}	0.2 V	-
Postcharge	enabled	-
Adaptive gate control	pre-discharge activated	-

As shown in **Figure 8**:

1. After t_{CCP} FW, the active MOSFET is charged.
2. During $t_{blank\_active1}$ and t_{FVDS}, the gate of active MOSFET is charged with different currents: pre-charge current, constant charge current I_{CHG}, and a post charge current.
3. When $t_{blank\_active1}$ and t_{FVDS} expire, drain-source monitoring is active. At this specific time, the active MOSFET is still in Miller Plateau, and V_{DS} is still dropping down, which can be bigger than V_{DSTH}. In this example, due to big V_{DS}, the VDSOV error is triggered.

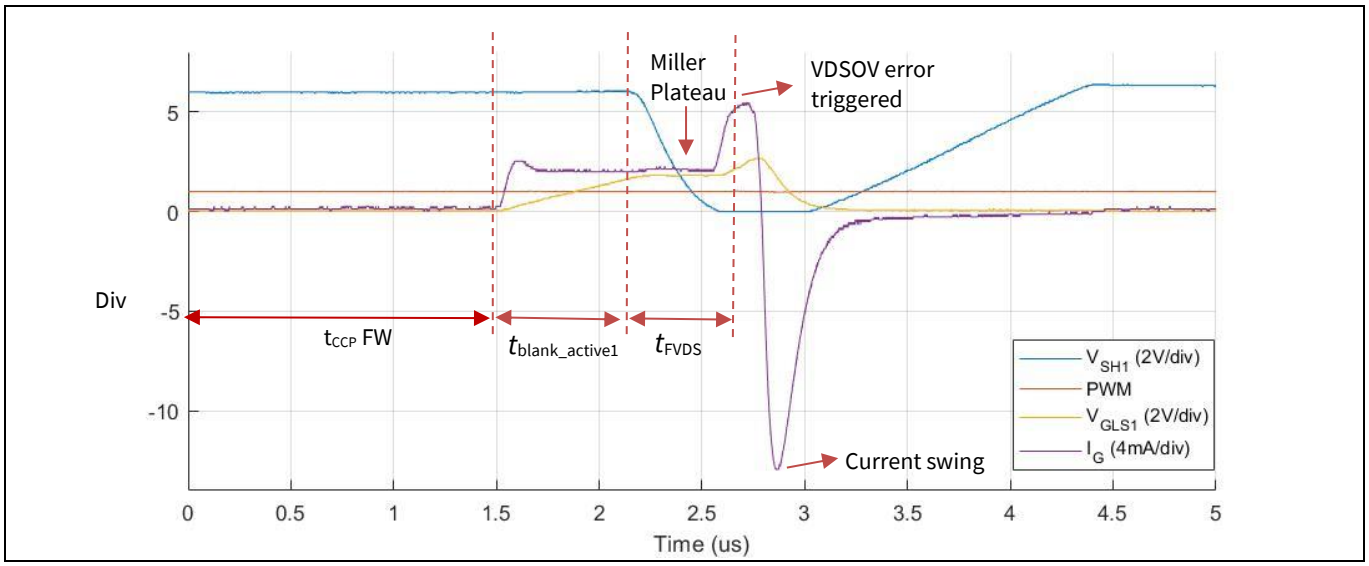

Figure 8 VDSOV error triggered when initially switching on the active MOSFET

When the VDSOV error is triggered, the device switches off the active MOSFET to protect the device, as shown in **Figure 8**. The effect of these wrong settings can be seen during the first PWM, and afterwards all MOSFETs are off. In this case, the motor will not run.

To avoid triggering the VDSOV error during the MOSFET turn-on phase, the blank time must be longer than the MOSFET turn-on time.

4 VDSOV error due to slow charging

4.1 Disable pre-charge and postcharge

VDSOV error can be triggered when the MOSFET is charged too slowly. To see the effect of slow charging, postcharge is deactivated, as shown in **Figure 9**. All other settings are exactly the same as during the first test. Refer to **Table 4**.

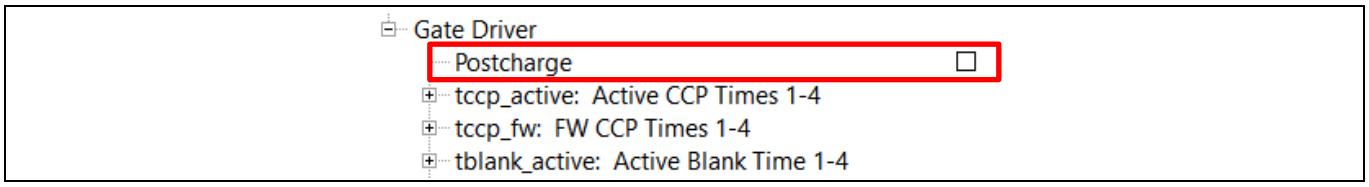

Figure 9 Disable postcharge

Table 4 Configuration for VDSOV error test with postcharge disabled

Parameter	Default value	New value
$t_{blank\_active1}$	2 µs	-
t_{FVDS}	1 µs	-
I_{HOLD}	12.5 mA / 14.2 mA	-
I_{CHG}	8 mA	-
I_{DCHG}	9.4 mA	-
$t_{CCP\_active1}$	3 µs	-
V_{DSTH}	0.2 V	-
Postcharge	enabled	disabled
Adaptive gate control	pre-discharge activated	-

As shown in **Figure 10**:

1. With the postcharge phase disabled, the gate of the active MOSFET is charged with I_{CHG} = 8 mA for $t_{blank\_active1}$ + t_{FVDS} = 3 µs in total.
2. Afterwards, I_{HOLD} = 12.5 mA continues to charge the MOSFET until it is fully charged.

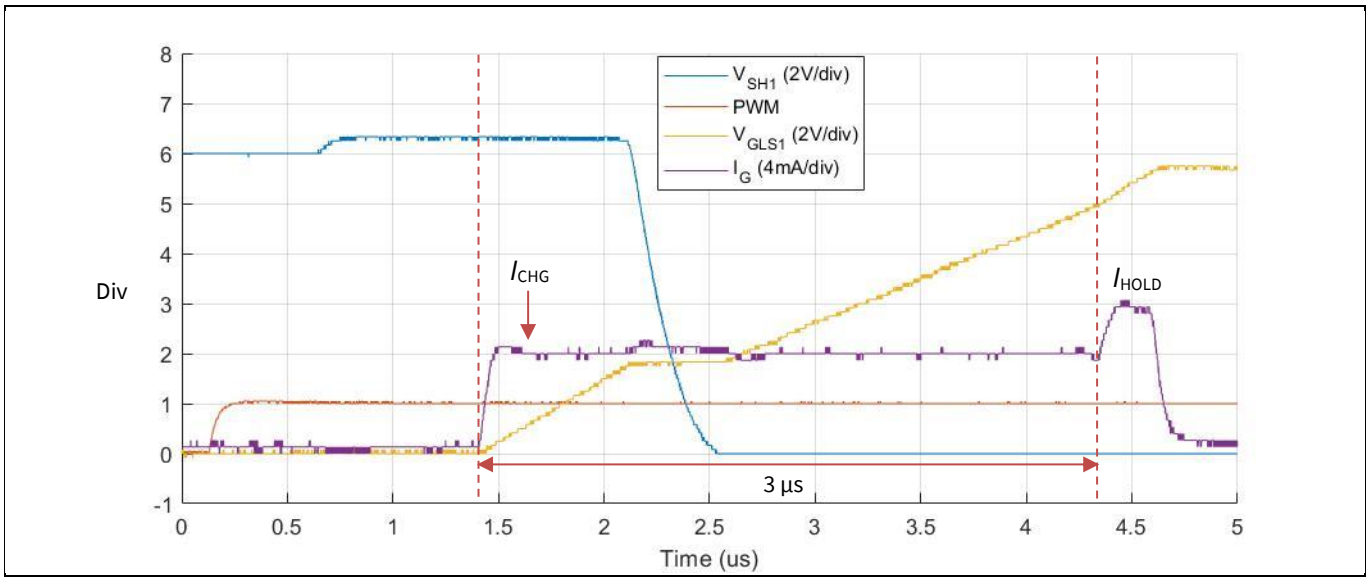

Figure 10 Active MOSFET switches on without pre-charge and postcharge current

In this example, no VDSOV is detected, because $V_{SH1} < V_{DSTH}$ when t_{FVDS} expires. It is recommended that I_{HOLD} should not be seen in the MOSFET turn-on phase, which is a sign that the MOSFET switches too slowly.

To avoid VDSOV, it is recommended to define a proper constant charge current that is big enough to turn on the MOSFET within $t_{blank\_active1} + t_{FVDS}$, or enable pre-charge and postcharge.

4.2 VDSOV error triggered with smaller gate charge current

The settings in **Figure 11** show that a VDSOV is detected if the charge current is further decreased. All other settings are exactly the same as in chapter **4.1**.Refer to **Table 5**.

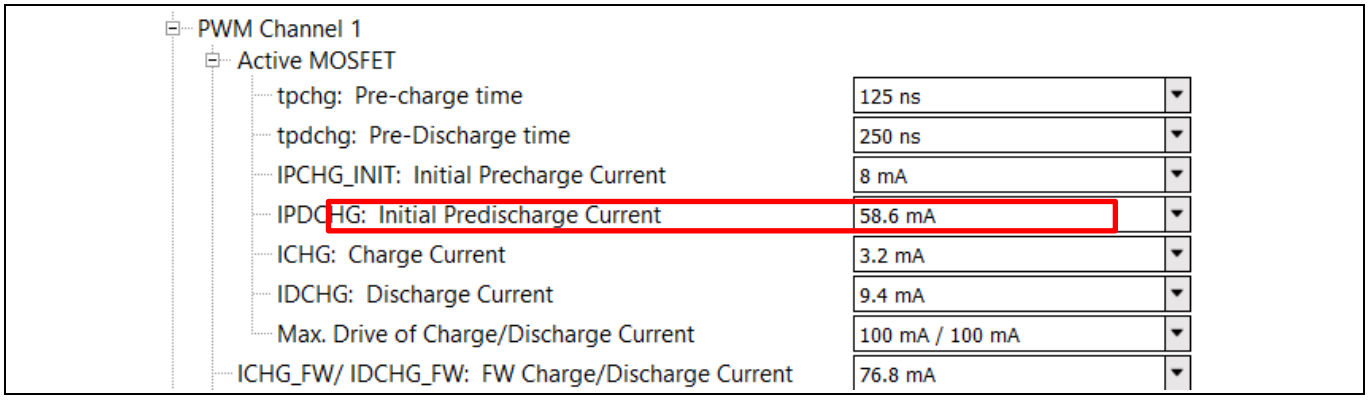

Figure 11 Decrease gate charge current ICHG

Table 5 Configuration for VDSOV error test with smaller charge current

Parameter	Default value	New value
$t_{blank\_active1}$	2 µs	-
t_{FVDS}	1 µs	-
I_{HOLD}	12.5 mA / 14.2 mA	-
I_{CHG}	8 mA	3.2 mA
I_{DCHG}	9.4 mA	-
$t_{CCP\_active1}$	3 µs	-
V_{DSTH}	0.2 V	-
Postcharge	enabled	disabled
Adaptive gate control	pre-discharge activated	-

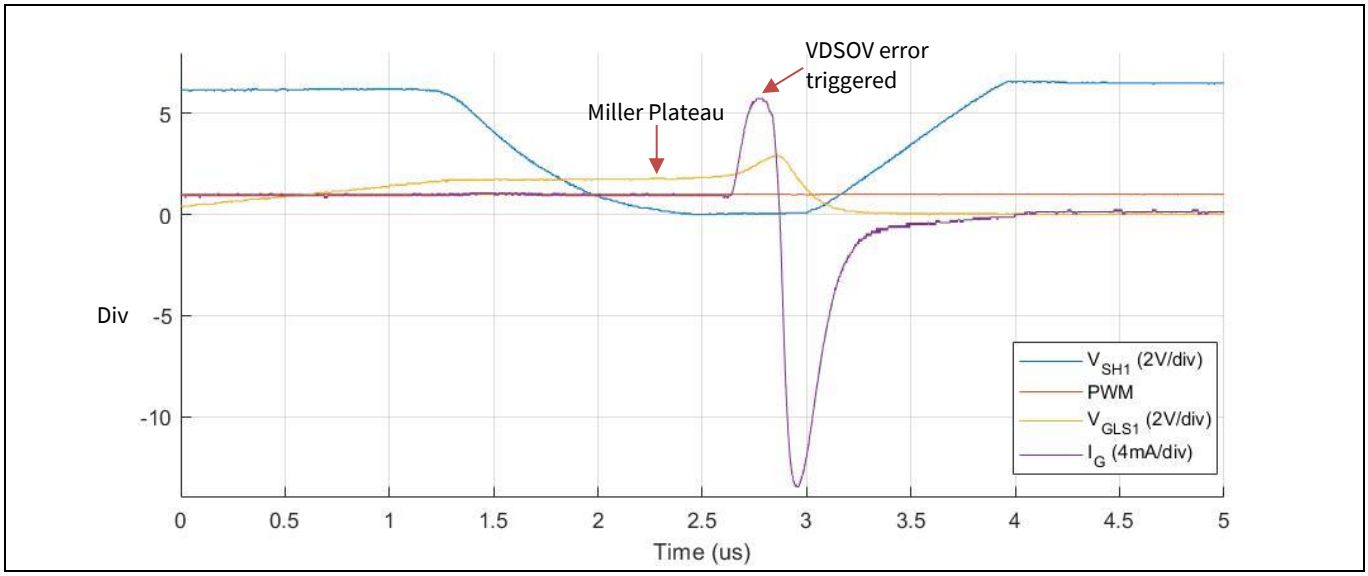

Figure 12 VDSOV due to slow turn-on

As shown in **Figure 12**, after $t_{blank\_active1} + t_{FVDS} = 3\ \mu s$, $V_{SH1} > V_{DSTH}$, which triggers the VDSOV error.

To avoid triggering the VDSOV error in normal load conditions the active MOSFET must be completely turned on within $t_{blank} + t_{FVDS}$. Enabling pre-charge and postcharge can help as well.

4.3 Adaptive gate control

The pre-charge/discharge is enabled in this test to charge the gate faster, as shown in **Figure 13**. All other settings are exactly the same as in chapter **4.2**. Refer to **Table 6**.

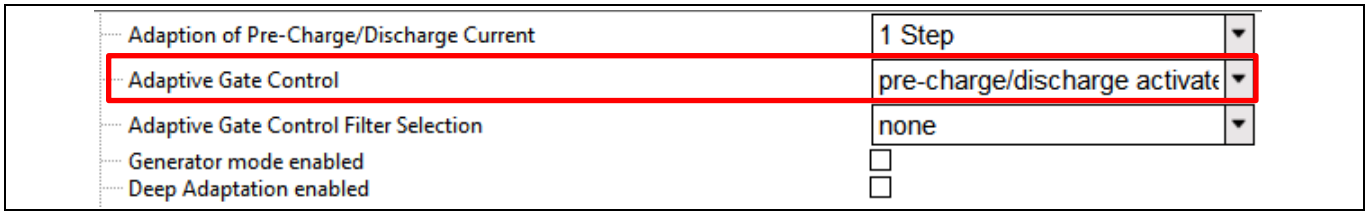

Figure 13 Enable pre-charge in Config Wizard

Table 6 Configuration for adaptive gate control test with small charge current

Parameter	Default value	New value
$t_{blank\_active1}$	2 µs	-
t_{FVDS}	1 µs	-
I_{HOLD}	12.5 mA / 14.2 mA	-
I_{CHG}	8 mA	3.2 mA
I_{DCHG}	9.4 mA	-
$t_{CCP\_active1}$	3 µs	-
V_{DSTH}	0.2 V	-
Postcharge	enabled	disabled
Adaptive gate control	pre-discharge activated	pre-charge/discharge activated

As shown in **Figure 14**, the VDSOV error is gone, but I_{HOLD} can still be seen due to small I_{CHG}. So, by activating pre-charge, the active MOSFET is turned on before the drain-source monitoring starts.

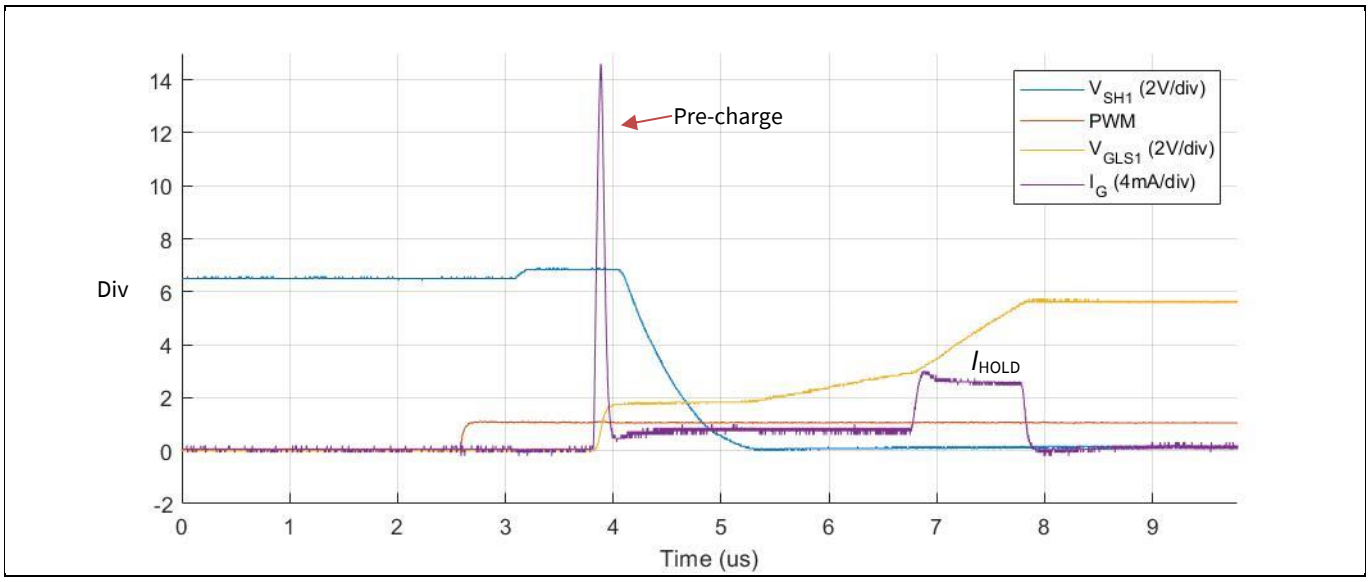

Figure 14 Enable pre-charge

When I_{CHG} = 10.3 mA, as shown in **Table 7**, there is no I_{HOLD} as shown in **Figure 15**. This is the desired MOSFET control.

Table 7 Configuration for adaptive gate control test with bigger charge current

Parameter	Default value	New value
$t_{blank\_active1}$	2 µs	-
t_{FVDS}	1 µs	-
I_{HOLD}	12.5 mA / 14.2 mA	-
I_{CHG}	8 mA	10.3 mA
I_{DCHG}	9.4 mA	-
$t_{CCP\_active1}$	3 µs	-
V_{DSTH}	0.2 V	-
Postcharge	enabled	disabled
Adaptive gate control	pre-discharge activated	pre-charge/discharge activated

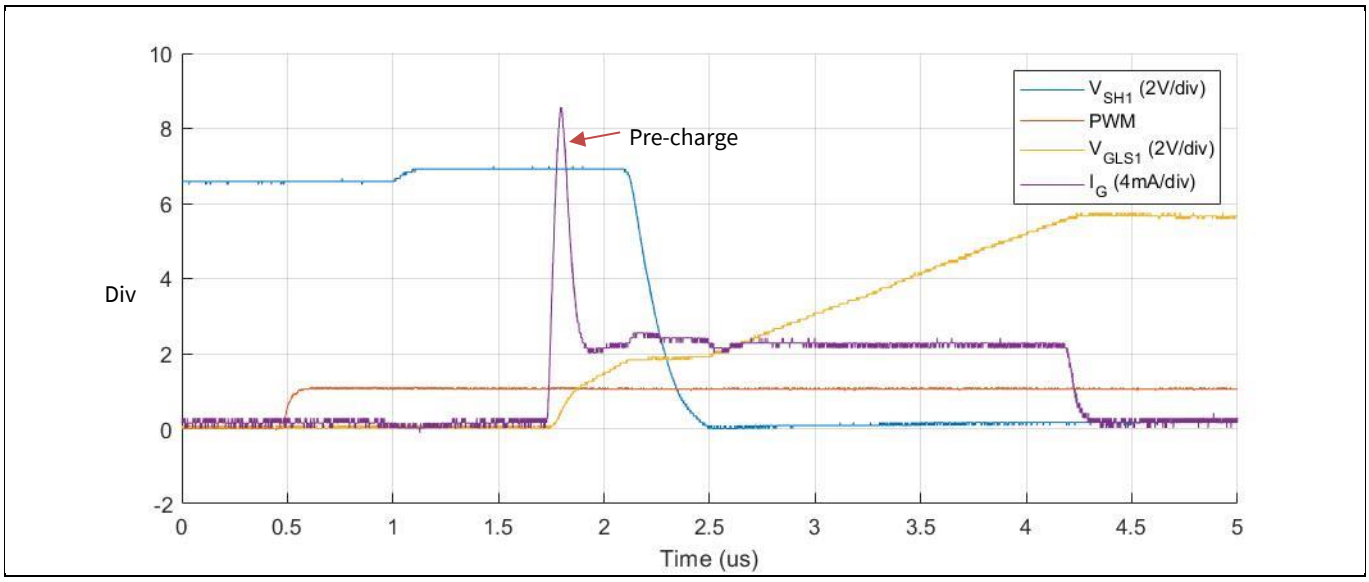

Figure 15 Enable pre-charge and increase I_{CHG}

In conclusion, enabling pre-charge, postcharge and increase I_{CHG} can help turn on the MOSFET much faster and avoid a VDSOV error.

5 Effect of hard off

The gate of the MOSFET, which has to be turned off, has to be fully discharged within t_{CCP} if the MOSFET driver is correctly configured. This section analyses the switching behavior when this condition is not fulfilled.

At the end of the $t_{CCP\_active1}$, if the MOSFET is not off, it will be discharged with the maximum discharge current (100 mA) to switch off the MOSFET as fast as possible and reduce the risk of parasitic cross-conduction, caused by a rapid change of VSHx associated with the coupling through the gate-drain capacitance of the MOSFETs. This phase is called hard off phase.

During the hard off phase, the slew rate of V_{SH} is not controlled by the constant I_{DCHG}, but by the hard off, causing a high EM emission. So, hard off should be avoided. In this example, the pre-discharge is disabled to slow down the switch-off of active MOSFET. $t_{CCP\_active1}$ = 2 µs. All other parameters are by default. Refer to **Table 8**:

Table 8 Configuration for hard off effect test with small t_{CCP}

Parameter	Default value	New value
$t_{blank\_active1}$	2 µs	-
t_{FVDS}	1 µs	-
I_{HOLD}	12.5 mA / 14.2 mA	-
I_{CHG}	8 mA	-
I_{DCHG}	9.4 mA	-
$t_{CCP\_active1}$	3 µs	2 µs
V_{DSTH}	0.2 V	-
Postcharge	enabled	-
Adaptive gate control	pre-discharge activated	disabled

As shown in **Figure 16**, the active MOSFET is not turned off within $t_{CCP\_active1}$. Then, the MOSFET enters the hard off phase. The gate is discharged as fast as possible to avoid cross conduction, which leads to a big swing in I_{DCHG}. The peak of I_{DCHG} is about -55 mA.

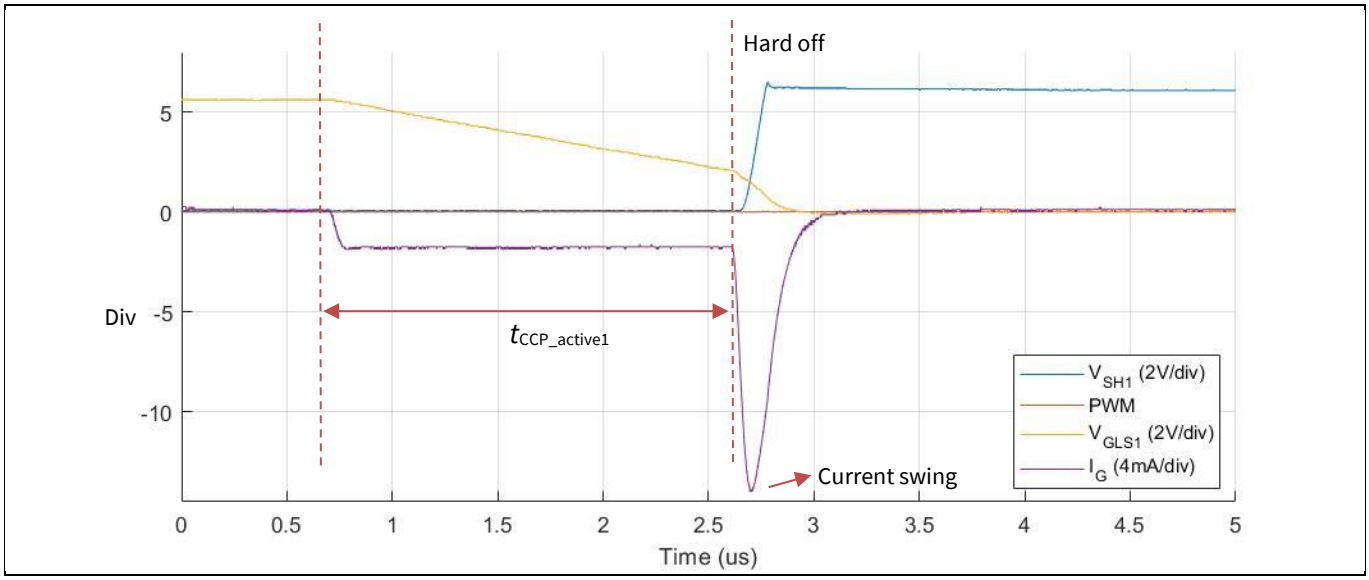

Figure 16 Hard off controlling the MOSFET slew rate

To further slow down the discharge phase, I_{DCHG} is lowered down to 4.3 mA, as is shown in **Figure 17**. All other parameters are the same as during the previous test. Refer to **Table 9**.

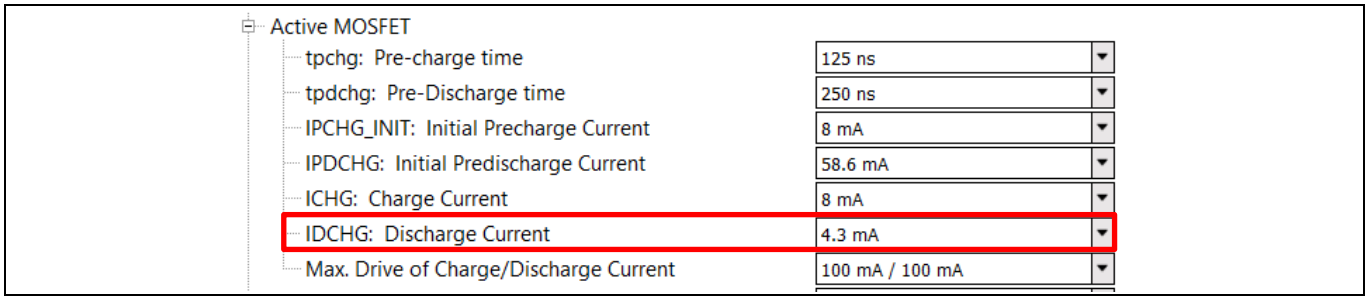

Figure 17 Configuration of IDCHG of active MOSFET

Table 9 Configuration for hard off effect test with small t_{CCP} and discharge current

Parameter	Default value	New value
$t_{blank\_active1}$	2 µs	-
t_{FVDS}	1 µs	-
I_{HOLD}	12.5 mA / 14.2 mA	-
I_{CHG}	8 mA	-
I_{DCHG}	9.4 mA	4.3 mA
$t_{CCP\_active1}$	3 µs	2 µs
V_{DSTH}	0.2 V	-
Postcharge	enabled	-
Adaptive gate control	pre-discharge activated	disabled

As is shown in **Figure 18**, at the end of $t_{CCP\_active1}$, V_{GLS1} = 8 V. Compared with previous tests, during the hard off phase, more gate charges are sunk in a very short time. So, there is a big swing in V_{SH1}. The voltage and current swing as well as a steep voltage slope will introduce even more EM emission.

To avoid the effect of the big slew rate and emission during the hard off phase, it is recommended to enable pre-discharge and configure the MOSFET driver so that the MOSFETs are turned offwithin t_{CCP}.

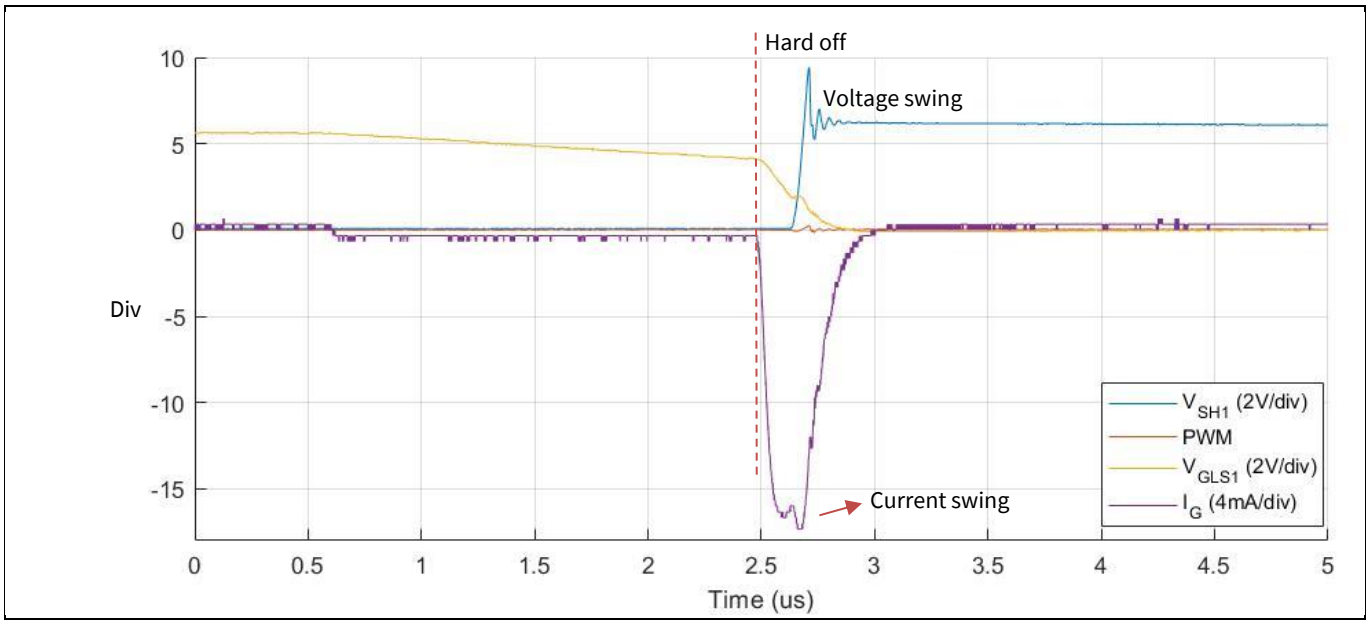

Figure 18 Hard-off at high VDS

6 Conclusion

This application note shows the typical configuration of TLE92108/04, which might lead to switching errors. For the TLE92108/04 to work correctly and efficiently, define the parameters mentioned in the examples properly.

Revision history

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