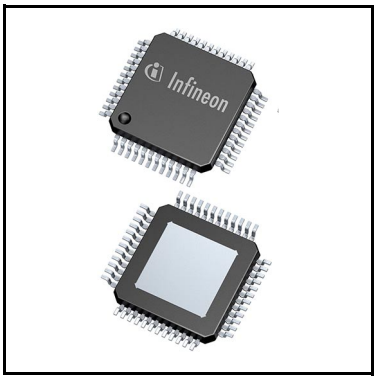
TLE9015QU BMS Transceiver IC - UART to iso UART

Datasheet



Features

- General
  - Two UART ports for serial communication to host microcontroller
  - Two iso UART interfaces for communication to other BMS ICs
  - 2 Mbit/s data rate for fast communication
  - Fully transparent communication scheme from UART to iso UART
  - Ring mode topology compatible
- Communication ports
  - Integrated internal logic to minimize pin count on the UART side
  - Differential current edge triggered iso UART communication interface
  - High robustness against external noise
- General purpose error pin
  - Two external fault inputs (EMM and ERRQ_ext)
  - Latching error output pin to trigger external microcontroller
- Supporting diagnosis features
  - Internal supply monitoring
- Green product (RoHS-compliant)

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE9015QU is a general purpose transceiver IC to be used in battery systems to enable the communication between the main host microcontroller and the cell supervision ICs which are usually connected to the battery module potential. The IC is designed for Li-Ion battery packs used in hybrid electric vehicles (HEV), plug-in hybrid electric vehicles (PHEV), battery electric vehicles (BEV) as well as stationary Lithium-Ion batteries.

Additionally to the physical layer translation, the TLE9015QU offers the possibility to communicate potential errors detected in a cell inside the battery pack to the main microcontroller.

Type	Package	Marking
TLE9015QU	PG-TQFP-48	TLE9015QU

Table of Contents

1 Block diagram

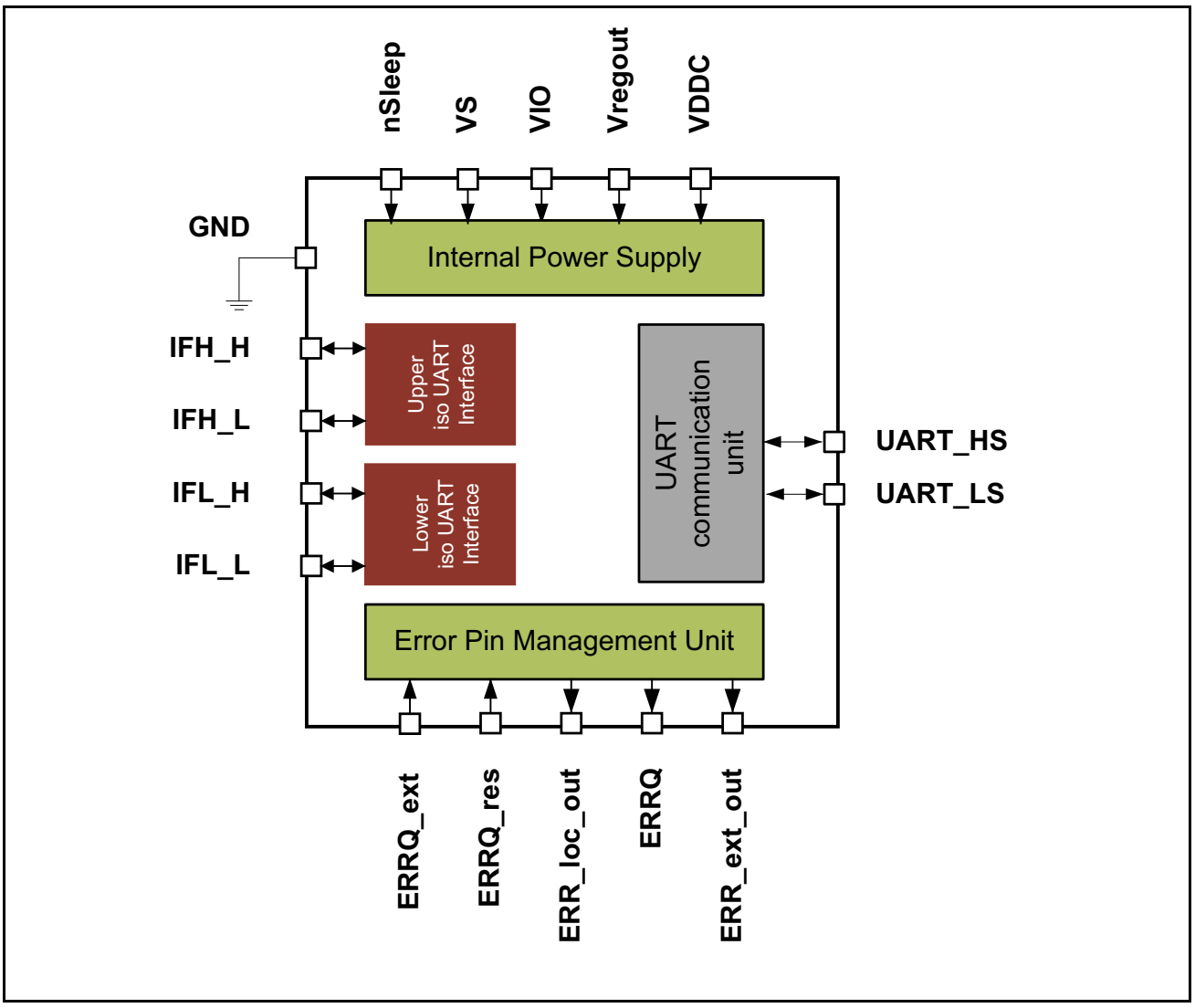


Figure 1-1 Block diagram

2 Pin configuration

2.1 Pin assignment

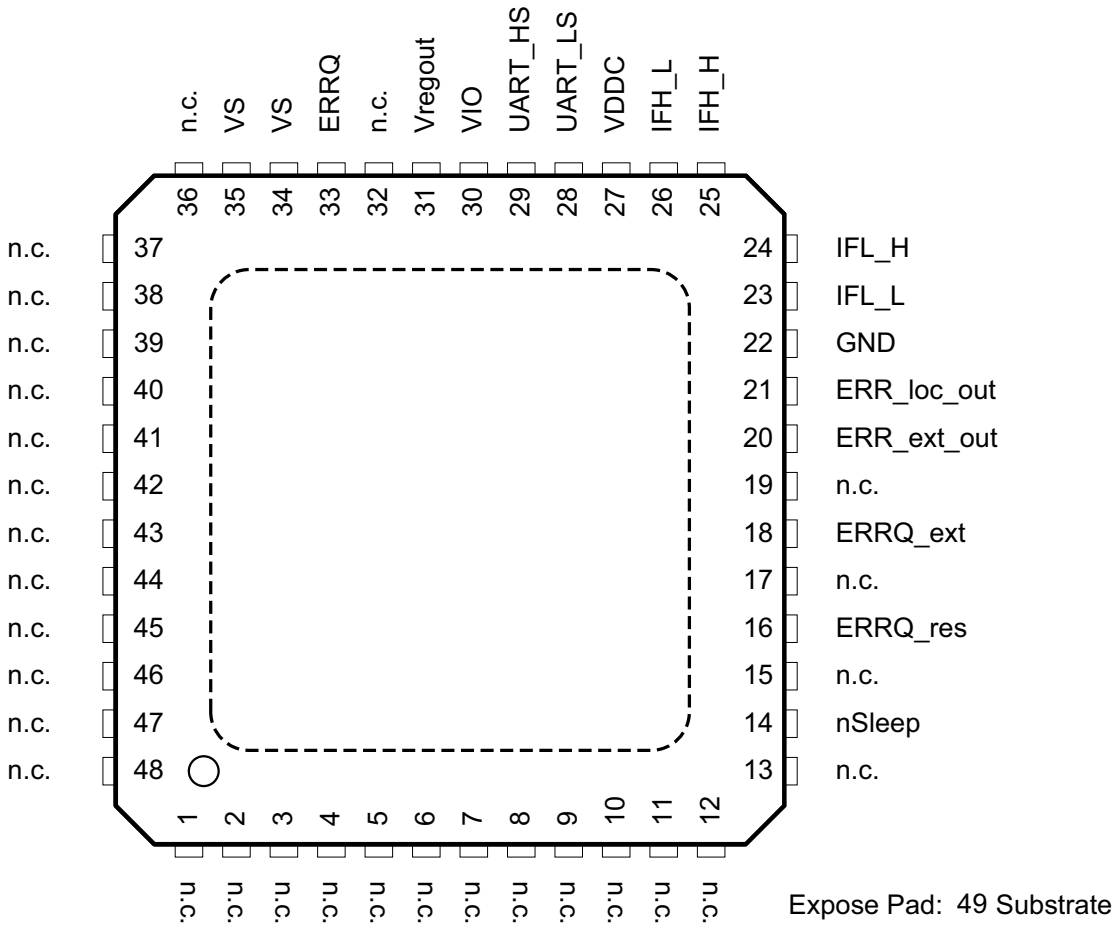


Figure 2-1 Pin configuration

2.2 Pin definitions and functions

Table 2-1 Pin assignment

Pin	Symbol	Function
1	n.c.	Not connected; this pin shall be connected to GND.
2	n.c.	Not connected; this pin shall be connected to GND.
3	n.c.	Not connected; this pin shall be connected to GND.
4	n.c.	Not connected; this pin shall be connected to GND.
5	n.c.	Not connected; this pin shall be connected to GND.
6	n.c.	Not connected; this pin shall be connected to GND.
7	n.c.	Not connected; this pin shall be connected to GND.
8	n.c.	Not connected; this pin shall be connected to GND.
9	n.c.	Not connected; this pin shall be connected to GND.
10	n.c.	Not connected; this pin shall be connected to GND.
11	n.c.	Not connected; this pin shall be connected to GND.
12	n.c.	Not connected; this pin shall be connected to GND.
13	n.c.	Not connected; this pin shall be connected to GND.
14	nSleep	Input pin to force the device to go to sleep; active low
15	n.c.	Not connected; recommended to be connected to GND
16	ERRQ_res	Reset the ERRQ pin; active low
17	n.c.	Not connected; this pin shall be connected to GND.
18	ERRQ_ext	Input for external ERRQ; If not used, connect to VREGOUT.
19	n.c.	Not connected; this pin shall be connected to GND.
20	ERR_ext_out	Output for external ERRQ; active high
21	ERR_loc_out	Output pin to indicate local ERRQ; active high
22	GND	Local GND of device
23	IFL_L	Lower Communication Bus (iso UART) L pin
24	IFL_H	Lower Communication Bus (iso UART) H pin
25	IFH_H	Upper Communication Bus (iso UART) H pin
26	IFH_L	Upper Communication Bus (iso UART) L pin
27	VDDC	Buffer capacitor pin for internal Communication Bus (iso UART) supply
28	UART_LS	UART_LS channel
29	UART_HS	UART_HS channel
30	VIO	Supply pin for UART interface.
31	VREGOUT	Output pin of the internal regulator
32	n.c.	Not connected; this pin shall be connected to GND.
33	ERRQ	Error pin; open drain NMOS. This pin is latching
34	VS	Supply pin.
35	VS	Supply pin.

Pin configuration

Table 2-1 Pin assignment

Pin	Symbol	Function
36	n.c.	Not connected; this pin shall be connected to GND.
37	n.c.	Not connected; this pin shall be connected to GND.
38	n.c.	Not connected; this pin shall be connected to GND.
39	n.c.	Not connected; this pin shall be connected to GND.
40	n.c.	Not connected; this pin shall be connected to GND.
41	n.c.	Not connected; this pin shall be connected to GND.
42	n.c.	Not connected; this pin shall be connected to GND.
43	n.c.	Not connected; this pin shall be connected to GND.
44	n.c.	Not connected; this pin shall be connected to GND.
45	n.c.	Not connected; this pin shall be connected to GND.
46	n.c.	Not connected; this pin shall be connected to GND.
47	n.c.	Not connected; this pin shall be connected to GND.
48	n.c.	Not connected; this pin shall be connected to GND.
49	EPAD	Cooling tab; should be connected to GND.

3 General product characteristics

3.1 Absolute maximum ratings

Table 3-1 Absolute maximum ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltages VS	V_{VS}	-0.3	–	45	V	–	
Supply voltage VIO	V_{VIO}	-0.3	–	5.5	V	–	
Supply voltage VS rel.	V_{VS}	V_{regout}-0.3	–	–	–	–	
Regulator output VREGOUT	V_{regout}	-0.3	–	3.6	V	–	
Regulator output VDDC	V_{VDDC}	-0.3	–	3.6	V	–	
Communication Bus (iso UART) interface IFH_x	V_{IFH_L} V_{IFH_H}	-3	–	5.5	V	[2)]BCI test max. 300 mA injected via twisted pair cable onto iso UART interface (max. pin current 150mA)	
Communication Bus (iso UART) interface IFL_x	V_{IFL_L} V_{IFL_H}	-3	–	5.5	V		
UART interface pins abs.	V_{UART_x}	-0.3	–	5.5	V	x -> LS or HS	
UART interface pins rel.	$V_{UART\_x\_rel}$	-0.3	–	V_{VIO}+ 0.3	V	x -> LS or HS	
High voltage input pin ERRQ_ext	V_{ERRQ_ext}	-0.3	–	V_{VS} + 0.3	V		
High voltage input pin ERRQ_res	V_{ERRQ_res}	-0.3	–	V_{VS} + 0.3	V		
High voltage input pin nSleep	V_{nSleep}	-0.3	–	V_{VS} + 0.3	V		
Digital output pin ERR_loc_out abs.	$V_{ERR\_loc\_out}$	-0.3	–	5.5	V		
Digital output pin ERR_loc_out rel.	$V_{ERR\_loc\_out\_rel}$	-0.3	–	V_{VIO}+ 0.3	V		
Digital output pin ERR_ext_out abs.	$V_{ERR\_ext\_out}$	-0.3	–	5.5	V		
Digital output pin ERR_ext_out rel.	$V_{ERR\_ext\_out\_rel}$	-0.3	–	V_{VIO}+ 0.3	V		
Open drain output pin ERRQ	V_{ERRQ}	-0.3	–	V_{VS}	V		
Ground pin GND	V_{GND}	0	–	0	V	absolute GND	
Temperatures							

Table 3-1 Absolute maximum ratings[1)] (cont'd)

T_j = -40 °C to +150 °C; all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction temperature Tj	T_j	-40	–	150	°C	–	
Storage temperature Tstg	T_{stg}	-55	–	150	°C	–	
ESD robustness							
ESD robustness 2 kV	V_{ESD}	-2	–	2	kV	HBM[3)]; all pins	
ESD robustness 4 kV	V_{ESD}	-4	–	4	kV	HBM[3)]; Robustness vs. GND for pins: VS, IFH_x, IFL_x	
ESD robustness CDM 500V	V_{ESD}	-500	–	500	V	CDM[4)]; all pins	
ESD robustness CDM 750V	V_{ESD_Corner}	-750	–	750	V	CDM[4)]; corner pins	

1) Not subject to production test, specified by design.
2) Positive and negative transients with a maximum duration of 100ns allowed between +/- 8 V; This should simulate ESD events; however, during normal and steady state condition voltage on these pins must stay inside the maximum ratings specified.
3) ESD robustness, according to Human Body Model "HBM" ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF)
4) ESD robustness, according to Charged Device Model "CDM" JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

3.2 Functional range

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

Table 3-2 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage regulator input	V_{VS}	4.75	–	45	V	–	
Other supply voltage	V_{VIO}	3	–	5.5	V	–	

3.3 Thermal resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3-3 Thermal resistance[1)]

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case RthJC	R_{thJC}	–	6	–	K/W		
Junction to ambient RthJA[2)]	R_{thJA}	–	30	–	K/W		

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (chip + package) was simulated on a 60 × 80× 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4 Power supply

4.1 Functional description

The TLE9015QU has an internal power supply which ensures proper functionality of the device. The power supply shall be connected to the local supply voltage (12 V in most of the systems). Additionally, external pins are available to buffer the internal voltage levels with a capacitor.

4.2 Power supply description

The following table contains a description of the power supply pins of the TLE9015QU.

Table 4-1 Power supply pins

Pin Name	Function
VS	VS are the main supply pins. These pins are the inputs for the internal regulator that is intended to supply the device.
Vregout	This pin is the output of the internal regulator. This pin shall always be connected to a buffer capacitor.
VIO	This pin is the supply for the UART interface. The voltage available on this pin will define the UART logic output levels. It should be connected to the same supply as the host microcontroller to ensure the same logic levels.
VDDC	VDDC is the output of the internal regulator which is used for the communication interface. This pin is used for buffering of the regulator; therefore, a capacitor must always be connected to ensure proper and robust communication.
GND	This is the main reference for the TLE9015QU on the board.
nSleep	Input pin to force the device to go to sleep mode. The pin is edge triggered from high to low; The pin has an internal pull-up resistor R_{nSleep_PU} implemented.

The main supply pin shall be connected to a source which is always providing voltage. This is necessary to keep the fault handling functionality of the TLE9015QU alive. The device has a sleep mode included to minimize current consumption. There is a built-in sleep mode regulator which ensures the detection of incoming iso UART and UART wake-up signals/EMM signal in sleep mode which will then trigger the start-up procedure (see also **Chapter 4.4**).

4.3 Using an external voltage regulator

It is necessary to use an external regulator to supply the UART logic level. This ensures common I/O voltage levels with the host controller.

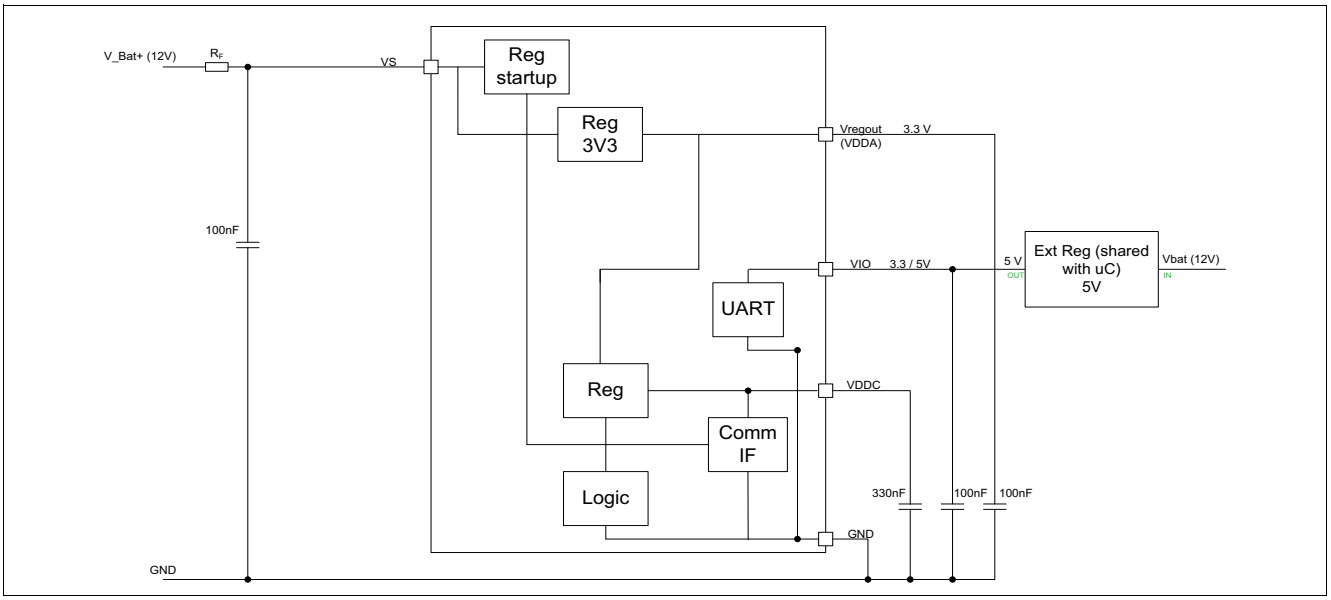


Figure 4-1 System using an external voltage regulator for VIO

4.4 Wake-up and sleep mode

After receiving power on VS, the IC will enter the sleep mode and starts monitoring the communication interfaces for a wake-up sequence.

In order to activate the TLE9015QU, a wake-up sequence as described in **Chapter 5.2.1** has to be sent via either the iso UART or UART interface. During sleep mode the TLE9015QU is only able to detect wake-up (and EMM) signals. As soon as the device detected a wake-up signal it will start the wake-up procedure and is – after finishing the wake-up procedure – in normal mode and able to forward normal speed communication data.

The TLE9015QU can be send to sleep mode via the nSleep pin. Initiating the sleep mode lowers the power consumption significantly.

4.5 Power supply monitoring

To ensure correct function of the TLE9015QU, the device has an internal monitoring unit for the different internal voltages. If important supplies go below secure levels to ensure correct functionality, the device will go into sleep mode.

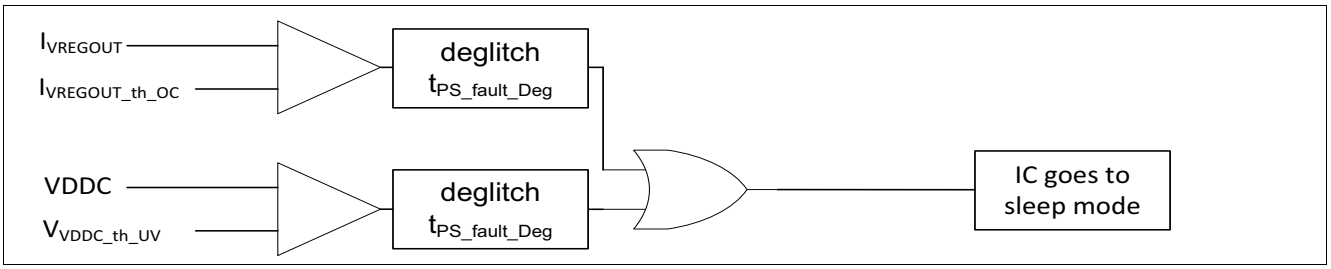


Figure 4-2 HW monitoring unit

4.6 Electrical characteristics power supply

Table 4-2 Electrical characteristics: power supply

V_{VS} = 4.75 V to 45 V, T_j = -40 °C to +150 °C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Internal regulators							
internal regulator output voltage VREGOUT	$V_{Vregout}$	3	3.45	3.6	V	–	
Overcurrent threshold VREGOUT	$I_{VREGOUT\_th\_OC}$	31	40	60	mA	–	
Undervoltage threshold falling VIO	$V_{VIO\_th\_UV\_fall}$	2.2	–	2.76	V	The UART interface is deactivated to avoid misinterpretations as long as VIO is in undervoltage	
Undervoltage threshold rising VIO	$V_{VIO\_th\_UV\_rise}$	2.24	–	2.8	V		
VIO undervoltage hysteresis VIO	$V_{VIO\_th\_UV\_hys}$	40	100	160	mV		
Output voltage VDDC	V_{VDDC}	2.42	2.5	2.75	V	–	
Undervoltage threshold VDDC	$V_{VDDC\_th\_UV}$	2.15	–	2.42	V	–	
Undervoltage threshold hysteresis VDDC	$V_{VDDC\_th\_UV\_hys}$	80	100	140	mV	–	
Power supply fault deglitch time	$t_{PS\_fault\_deg}$	8	15	24	µs	1)	
Supply currents							
Sleep mode current sleep supply VS	I_{VS_sleep}	0	6	23	µA	typ. @ T_j = 85°C; -40°C ≤ T_j ≤ 85°C; round robin in sleep mode deactivated	
Sleep mode leakage current VS	I_{VS_sleep}	-1	–	1	µA	-40°C ≤ T_j ≤ 85°C;	
Idle current VS	I_{VS_idle}	–	4.7	9.2	mA	IC in idle mode	
Current consumption during UART communication VIO	I_{VIO_comm}	–	–	5	mA	depending on load on UART	
Current consumption during communication VS	I_{VS_comm}	–	6.5	10.8	mA	Valid for UART or iso UART communication. Current to charge-up external interface components not included. Incl. idle consumption I_{VS_idle}	

Table 4-2 Electrical characteristics: power supply (cont'd)

V_{VS} = 4.75 V to 45 V, T_j = -40 °C to +150 °C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption during communication only for external iso UART interface components VS	$I_{VS\_comm\_ext}$	–	–	6	mA	$C_{isoUART\_ser}$ = 1 nF $BR_{isoUART}$ = 2 MBit $R_{isoUART\_ser}$ = 39 Ω This consumption needs to be added to I_{VS_comm} [1]	
nSleep pin							
nSleep input voltage range LOW	V_{nSleep_LOW}	0	–	0.99	V		
nSleep input voltage range HIGH	V_{nSleep_HIGH}	2.52	–	V_{VS}	V		
nSleep internal pull up resistor	R_{nSleep_PU}	200	300	400	kΩ	connected to an internal 3.3V supply	
nSleep input deglitch	$t_{nSleep\_deglitch}$	19.85	21.82	24	µs	[1]	

1) Not subject to production test, specified by design.

5 Housekeeping functions

5.1 Functional description

This chapter describes several functions that are required for the proper and safe function of the TLE9015QU.

These functions are:

- Sleep mode and wake-up
- Fault handling and emergency mode (EMM)

5.2 Sleep mode

The sleep mode pin (nSleep) is defined as active low and edge triggered. In case the microcontroller goes into sleep mode it can reset that input pin(1-->0) and the transceiver enters the sleep mode as well.

5.2.1 Sleep mode and wake-up function

When the device is in sleep mode, all iso UART and UART interfaces are disabled. In sleep mode the power dissipation of the receiver logic is very low, and the receiver is not able to receive normal-speed iso UART or UART datagrams. However, the TLE9015QU will continue to monitor all the communication interfaces (iso UART and UART) waiting for a wake-up sequence.

The wake-up sequence is a slowly alternating sequence (with frequency f_{WAKEUP}). This wake-up signal has n_{WAKE} cycles. After n_{WAKE_dect} complete cycles are detected in sleep mode, the TLE9015QU will trigger a wake-up and it will require a wake-up time t_{WAKE} before standard datagrams can be forwarded.

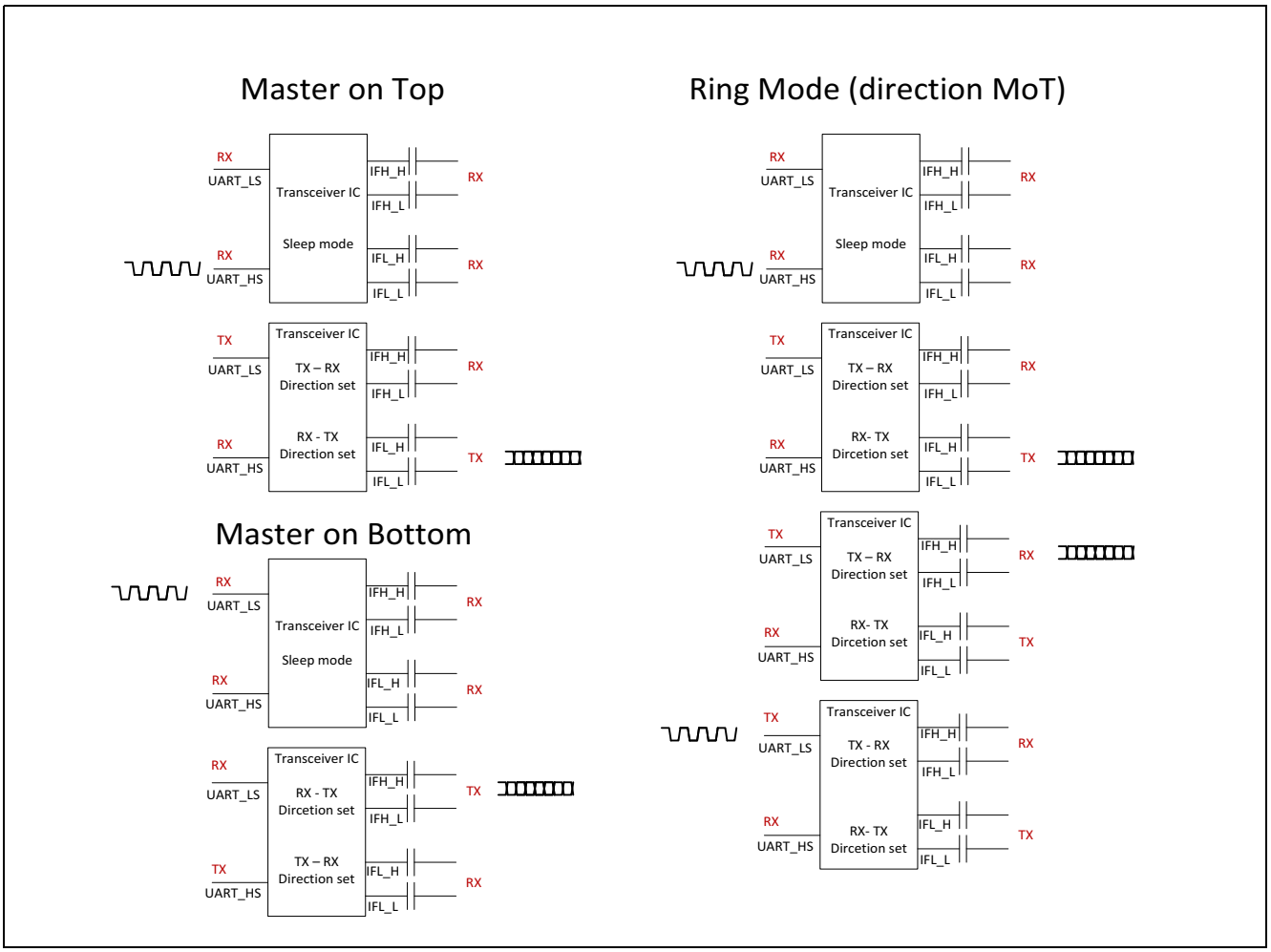


Figure 5-1 Wake-up signals

After t_{WAKE} the TLE9015QU is woken up and, if the wake-up came through UART, it will forward the wake-up signal to the sensing ICs via iso UART. Please keep in mind that the wake-up signal will be propagated through the entire network.

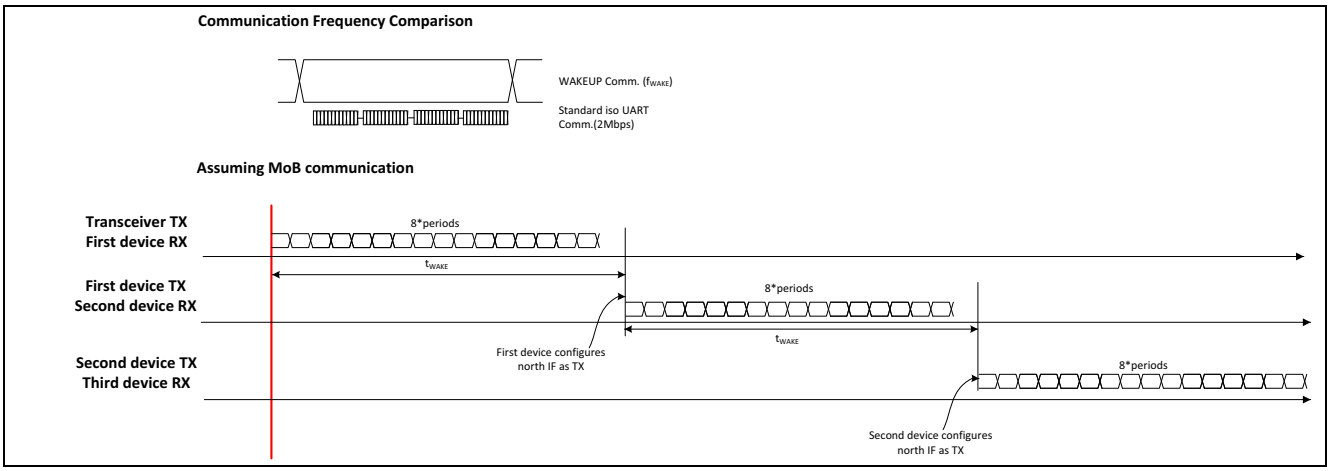


Figure 5-2 Wake-up signals through the daisy-chain

When the last node wakes up, it will send the wake-up signal to the next node, but in this case the signal will be received by the transceiver IC and will be forwarded to the microcontroller via UART interface. So the

microcontroller knows that the wake-up procedure of the entire chain was successful (only valid for ring mode topology).

If the wake-up signal approached the TLE9015QU via iso UART interface while the device was still in sleep mode, the signal was not a simple wake-up signal but an emergency mode (EMM) signal (same alternating frequency but n_{EMM} periods, see also **Chapter 5.3**) from one of the sensing ICs. In this case the wake-up signal will not be forwarded via UART to the host controller. Instead, the build-in fault handling in the TLE9015QU will process the fault (see also **Chapter 5.3**).

5.2.2 Electrical characteristics

Table 5-1 Electrical characteristics:

V_{VS} = 4.75 V to 45 V; T_j = -40 °C to +150 °C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Wake-up function							
Wake-up signal frequency iso UART	$f_{WAKEUP\_isoUART}$	48	50	1040	kHz		
Wake-up signal frequency UART	f_{WAKEUP_UART}	48	50	1040	kHz		
Device wake-up time	t_{WAKE}	200	370	500	µs		
Wake-up - number of detected periods	n_{WAKE_dect}	4	–	8	period		
Wake-up - length in periods	n_{WAKE}	8	–	8	period		

5.3 Emergency mode signals (EMM) and fault handling

The TLE9015QU fault handling procedure can be triggered by two different inputs:

- Emergency mode signal (EMM) via iso UART
- Fault input pin ERRQ_ext

The EMM signal arriving via iso UART at the TLE9015QU indicates that one of the sensing ICs connected to the transceiver via iso UART entered its EMM mode due to a fault. The fault handling procedure can also be started via the external fault pin ERRQ_ext. This might be useful in a multi transceiver application case.

5.3.1 Emergency mode (EMM) via iso UART

In case of an incoming EMM signal via iso UART, TLE9015QU goes into Emergency Mode (EMM) and starts the fault handling.

The EMM signal has a similar signature as the wake-up signal, however it has a longer duration. It contains a total of n_{EMM} periods. It is ensured that after t_{WAKE} still more than 4 periods will be remaining from the EMM signal of the contiguous device.

The following figures (**Figure 5-3** and **Figure 5-4**) show how the EMM signal is propagated through the chain to the transceiver IC.

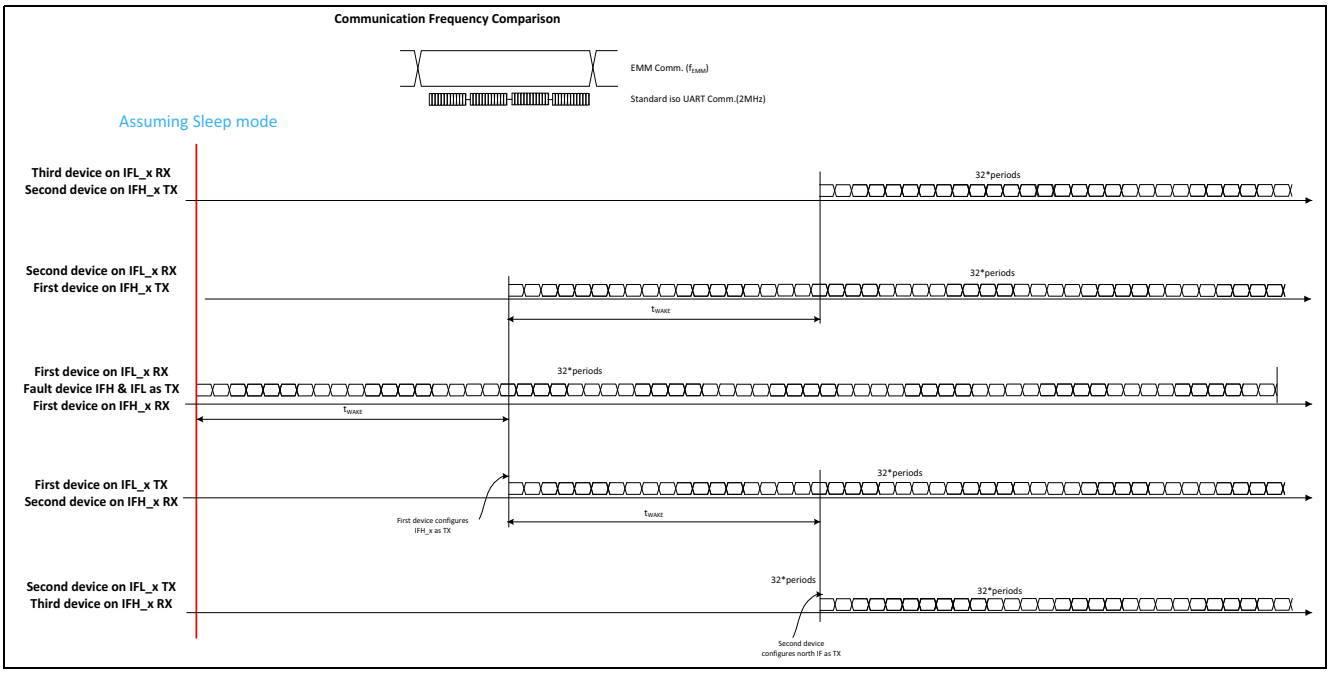


Figure 5-3 EMM signals during sleep mode

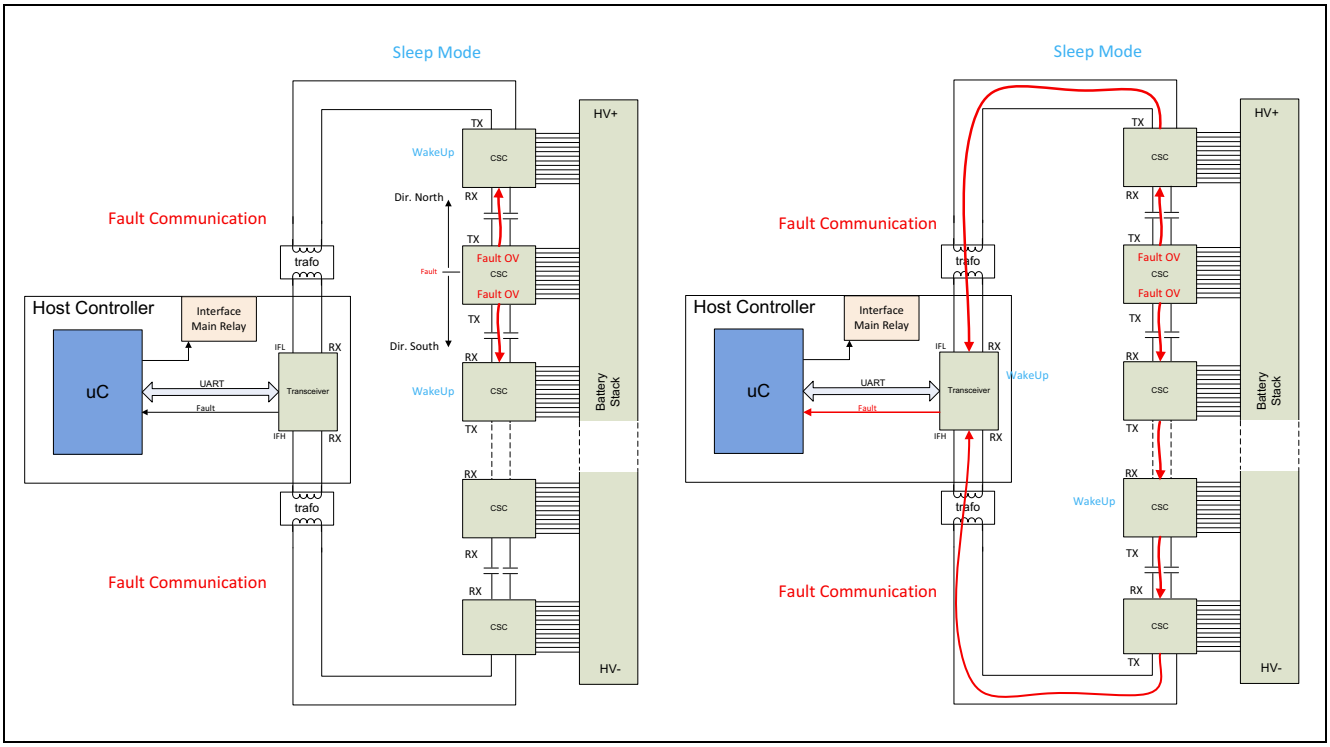


Figure 5-4 EMM during sleep mode

If the chain is in normal operation (i.e. communicating, measuring, etc.), a communication mode (MoT or MoB) is already defined. The affected device will also start transmitting the EMM signal. However, since the chain is already configured for either MoT or MoB communication, the contiguous devices will show either a TX interface or an RX interface. If the contiguous device shows a TX interface, the message will not be forwarded. Therefore, the EMM signal will follow the path that shows the RX interface back to the microcontroller. The following picture shows an EMM communication in case of MoB/MoT configuration:

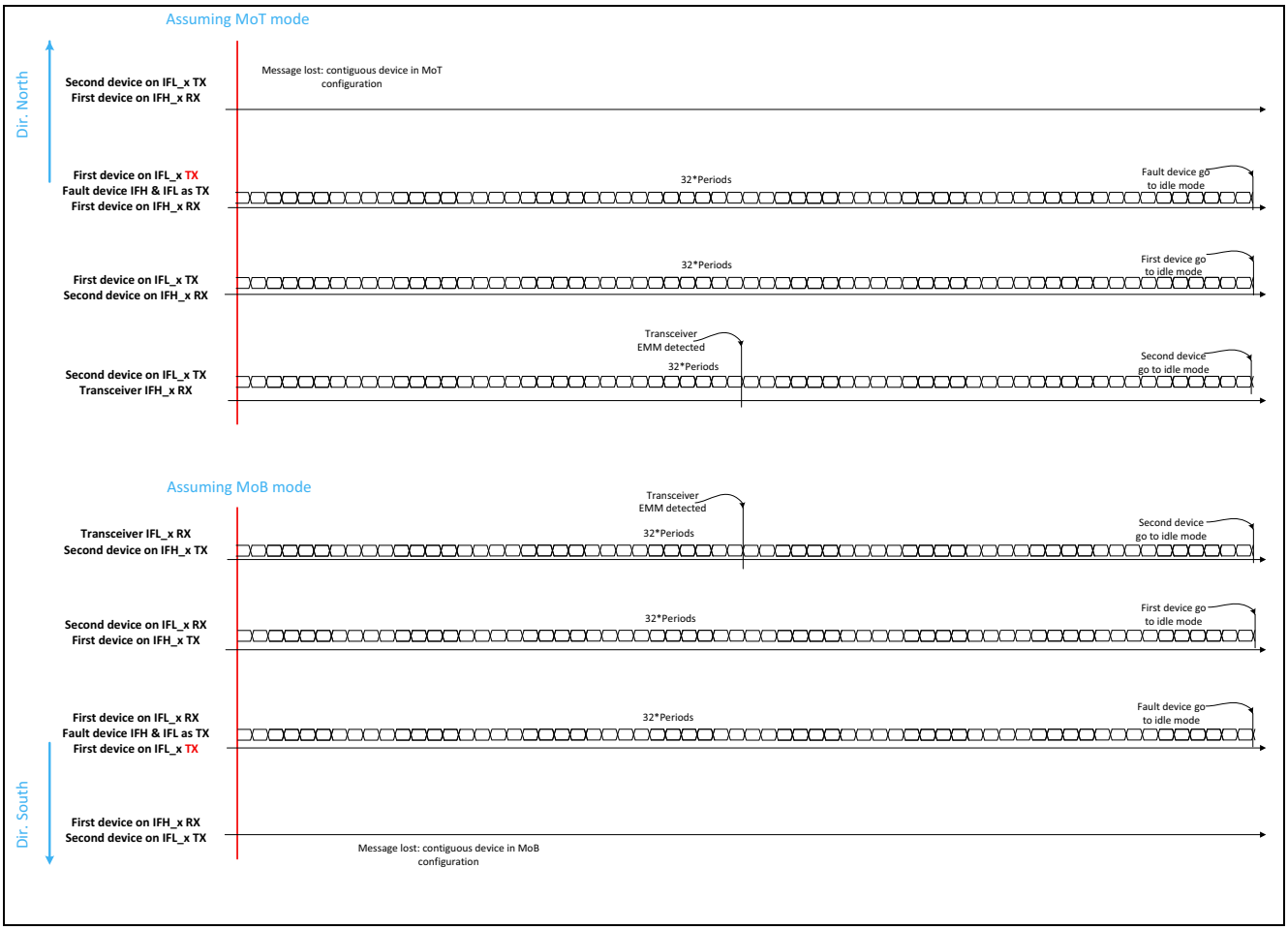


Figure 5-5 EMM signals during normal operation

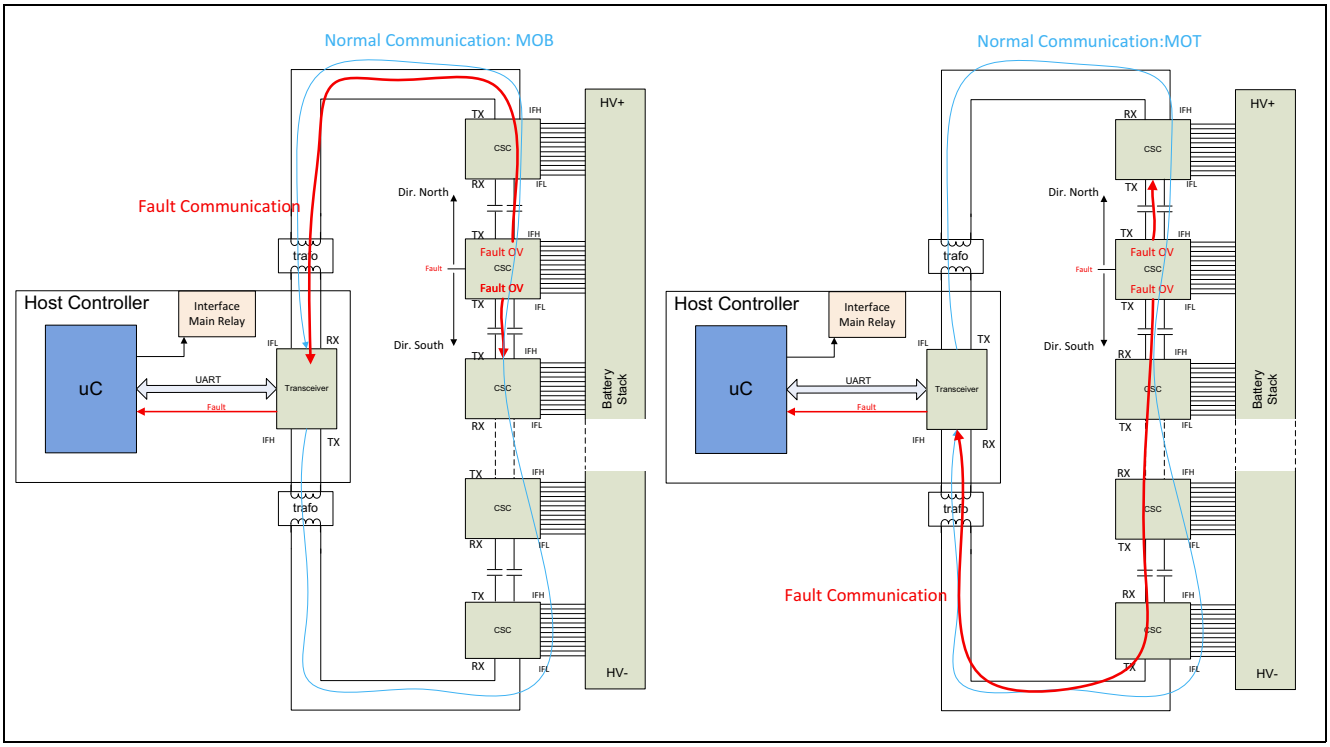


Figure 5-6 EMM during MoB/MoT configuration

For more details regarding the EMM signal transmission and the possible faults please see the sensing IC documentation.

5.3.2 Fault input pin & fault handling

In addition to the EMM signal via iso UART the TLE9015QU has also a fault input pin which triggers the fault handling as well. This might be useful in a multi-transceiver application. The following table gives an overview about the different fault pins and their function:

Table 5-2 Fault handling pins

Pin Name	Function
ERRQ	The ERRQ pin is an output pin. The pin is indicating a fault. The output is open drain and active low. The pin is latching.
ERR_loc_out	The ERR_loc_out pin is an output pin. It indicates that the fault indicated by ERRQ pin arrived the transceiver IC via EMM signal.The logic levels of the pin are VIO and GND. The pin is active high. After an EMM signal is detected, the ERR_loc_out pin will go high for $t_{ERR\_loc\_out}$.
ERR_ext_out	The ERR_ext_out pin is an output pin. It represents the deglitched and inverted ERRQ_ext signal. The logic levels of the pin are VIO and GND. The pin is active high (push-pull).
ERRQ_ext	The ERRQ_ext pin is an input pin to trigger the fault function (ERRQ pin) externally. The pin is level triggered active low with a deglitch time of terrq_ext_deglitch. The pin has an internal pull-up resistor $R_{ERRQ\_ext\_PU}$ implemented.
ERRQ_res	This pin is the input pin to reset the latched ERRQ pin function. The pin is level triggered active low with a deglitch time of terrq_res_deglitch. The pin has an internal pull-up resistor $R_{ERRQ\_res\_PU}$ implemented.

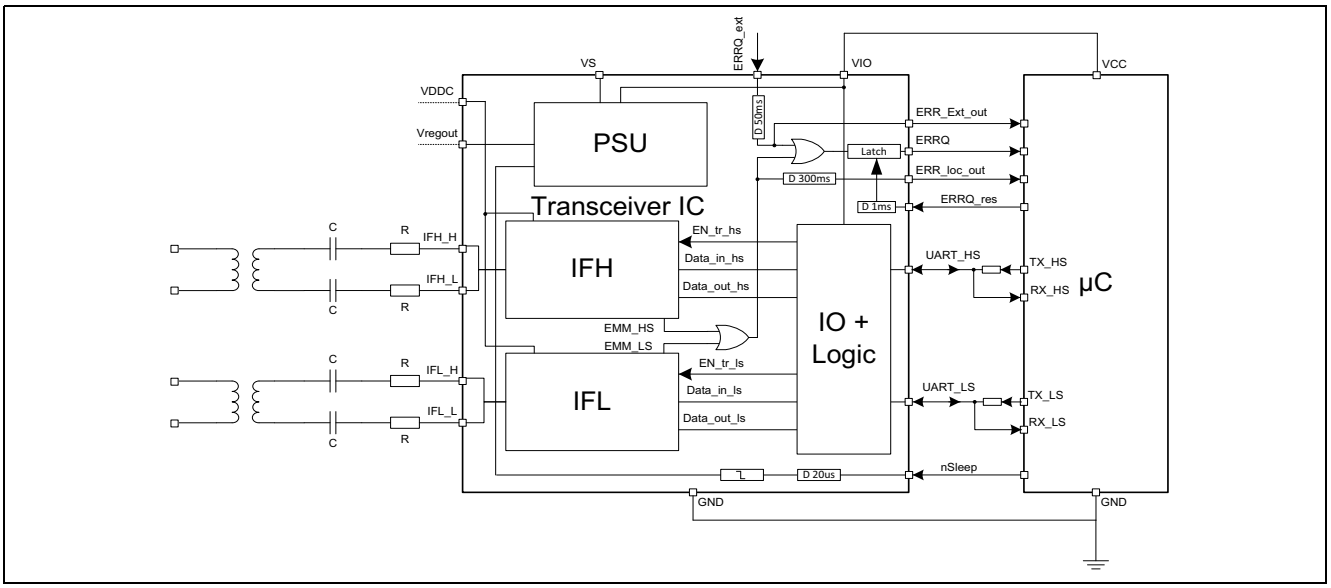


Figure 5-7 Transceiver block level and connections

5.3.3 Electrical characteristics

Table 5-3 Electrical characteristics:

V_{VS} = 4.75 V to 45 V; T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Emergency mode EMM							
EMM signal frequency	f_{EMM}	48	50	52	kHz	–	
Number of periods to detect EMM signal - straight after wake-up	$n_{EMM\_dect\_wake-up}$	4	–	4	periods	1)number of periods; valid only if IC just entered IDLE mode straight after wake-up procedure	
Number of periods to detect EMM signal - idle mode	n_{EMM_dect}	16	–	16	period	1)number of periods; valid while IC is in idle mode	
Length in periods for the EMM signal	n_{EMM}	32	–	32	period	1)	
ERRQ pins							
Functional range of ERRQ pin functions	V_{ERRQ}	4.75	–	V_{VS}	V	$V_{VS} \leq 20V$	
ERRQ activated output voltage	V_{ERRQ_LOW}	0	–	0.3	V	$I_{ERRQ} \leq 1.5$ mA	
Sink current	I_{ERRQ}	-1.5		0	mA	1)	
ERRQ_res input voltage range LOW	$V_{ERRQ\_res\_LOW}$	0	–	0.99	V	–	
ERRQ_res input voltage range HIGH	$V_{ERRQ\_res\_HIGH}$	2.52	–	V_{VS}	V	–	
ERRQ_ext input voltage range LOW	$V_{ERRQ\_ext\_LOW}$	0	–	0.99	V	–	
ERRQ_ext input voltage range HIGH	$V_{ERRQ\_ext\_HIGH}$	2.52	–	V_{VS}	V	–	
ERR_loc_out output voltage range LOW	$V_{ERRQ\_loc\_out\_LOW}$	0	–	0.45	V	$I_{ERRQ\_loc\_out} \leq 5$ mA	
ERR_loc_out output voltage range HIGH	$V_{ERRQ\_loc\_out\_HIGH}$	V_{VIO}-0.45	–	V_{VIO}	V	$I_{ERRQ\_loc\_out}$ >= -5 mA	
ERR_ext_out output voltage range LOW	$V_{ERRQ\_ext\_out\_LOW}$	0	–	0.45	V	$I_{ERRQ\_ext\_out} \leq 5$ mA	
ERR_ext_out output voltage range HIGH	$V_{ERRQ\_ext\_out\_HIGH}$	V_{VIO}-0.45	–	V_{VIO}	V	$I_{ERRQ\_ext\_out}$ >= -5 mA	
ERRQ_ext internal pull up resistor	$R_{ERRQ\_ext\_PU}$	200	300	400	kΩ	connected to an internal 3.3V supply	

Table 5-3 Electrical characteristics:

V_{VS} = 4.75 V to 45 V; T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ERRQ_res internal pull up resistor	$R_{ERRQ\_res\_PU}$	200	300	400	kΩ	connected to an internal 3.3V supply	
ERRQ_ext input deglitch	$t_{ERRQ\_ext\_deglitch}$	47.26	49.74	52.42	ms	1)	
ERRQ_res input deglitch	$t_{ERRQ\_res\_deglitch}$	844	951	1067	µs	1)	
ERR_loc_out active time	$t_{ERR\_loc\_out}$	281.32	293.74	307.2	ms	1)	

1) Not subject to production test, specified by design.

6 Communication interfaces

6.1 Physical layer

The TLE9015QU supports two types of physical layers: UART-based and iso UART-based. Both are point to point communication protocols and they can be used to communicate between the microcontroller in the system and the different slaves.

Each TLE9015QU contains four different units:

- iso UART IFH
- iso UART IFL
- UART HS
- UART LS

In the following sections each of these units will be described.

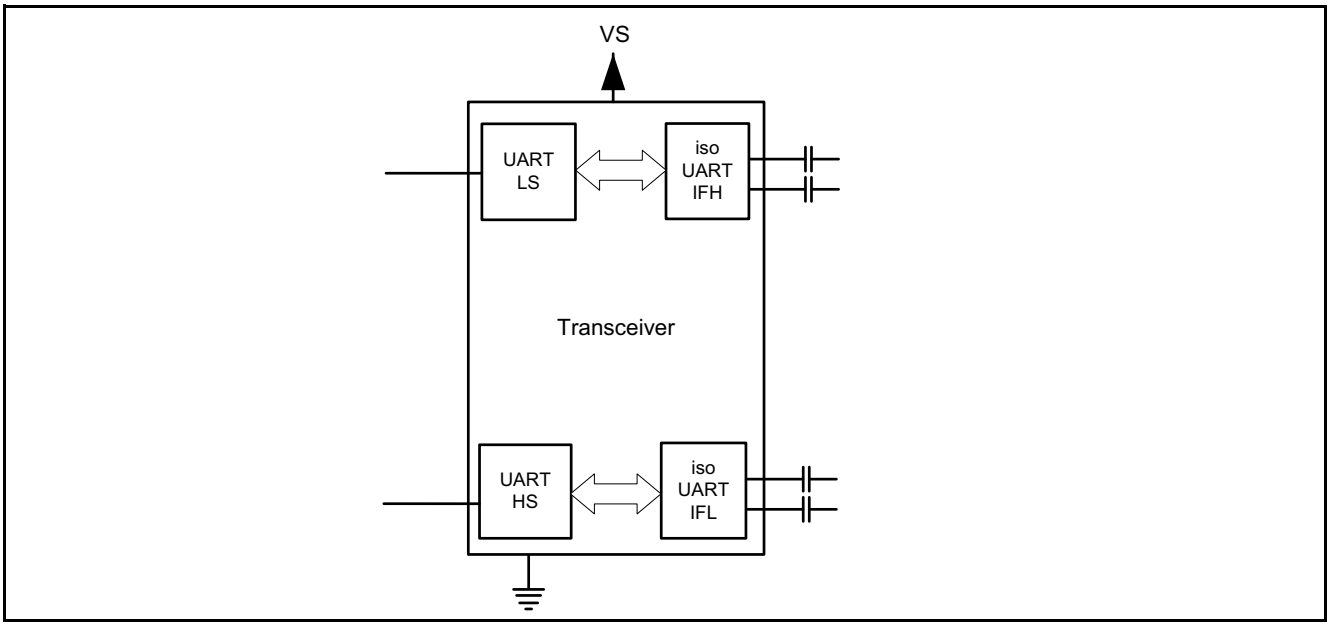


Figure 6-1 Typical communication block for the TLE9015QU

6.1.1 UART communication unit

The UART communication is logic-voltage-based. The voltage level for this communication is defined by the voltage between VIO to GND.

Due to the necessary GND connection the UART interface cannot be used for interblock communication if the devices are stacked (not galvanically isolated). Therefore the UART interface is the one communicating with the host controller.

Each UART communication interface needs only 1 pin on the TLE9015QU side since it has already integrated a logic controller which fulfills the function of switching between Tx and Rx mode. **Figure 6-2** shows a typical UART connection with 2 pins on the microcontroller side.

During sleep mode, the UART pins will stay in low power RX mode. If a wake-up signal is detected through the TLE9015QU UART pin, the transceiver starts a wake-up procedure. If a wake-up signal is detected at the UART HS, the wake-up signal will be forwarded to iso UART IFL interface and vice versa as soon as the device enters the normal mode.

Please note: In case of communication via UART the logic level of the UART pin in default state shall be static "1".

The only difference between UART and iso UART communication is the physical layer. On higher levels (OSI model), UART and iso UART are equal.

6.1.2 Communication Bus (iso UART) unit

The iso UART is a point to point communication bus designed by Infineon with a dedicated protocol. The TLE9015QU communicates via two physical links; high side interface (IFH) and low side interface (IFL).

The iso UART is based on differential bus lines. Both the high and low side interfaces are able to drive the differential lines (TX mode), and both have a differential receiver circuit (RX mode). Which of the interface modules is allowed to drive the bus lines is determined by the bus timing protocol.

The iso UART physical layer is a $\pm V_{VDDC}$ edge detection-based interface suitable for capacitive coupling as well as inductive coupling. This interface can offer the necessary galvanic isolation as well as the robustness to guarantee error free communication between the different CSCs in the battery system.

The iso UART communication physical layer supports wake-up and EMM communication as described in **Chapter 5.3**.

6.1.3 Electrical characteristics

Table 6-1 Electrical characteristics:

V_{VS} = 4.75 V to 45 V, T_j = -40 °C to +150 °C, all voltages with respect to GND, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
UART physical layer							
UART input threshold voltage LOW	$V_{UART\_th\_LOW}$	–	–	V_{VIO}* 0.3	V	–	
UART input threshold voltage HIGH	$V_{UART\_th\_HIGH}$	V_{VIO}* 0.7	–	-	V	–	
UART output voltage LOW	V_{UART_LOW}	0	–	0.45	V	I_{UART} <= 5 mA	
UART output voltage HIGH	V_{UART_HIGH}	V_{VIO}- 0.45	–	V_{VIO}	V	I_{UART} >= -5 mA	
UART to iso UART propagation delay	$t_{UART\_isoUART\_del}$	–	25	100	ns	propagation delay from UART to iso UART	
UART output current	I_{UART_x}	-5	–	5	mA	current capability of UART output; x -> LS or HS	
UART bitrate	BR_{UART}	1.45	2	2.1	Mbit/s	–	
External capacitance on UART pin	C_{UART_ext}	–	–	30	pF	1)	
iso UART physical layer							
iso UART current threshold HIGH	$I_{isoUART\_th\_HIGH}$	2.25	4.5	6.75	mA	(I_{IFx_H} - I_{IFx_L}) / 2	
iso UART current threshold LOW	$I_{isoUART\_th\_HIGH}$	-6.75	-4.5	-2.25	mA	(I_{IFx_H} - I_{IFx_L}) / 2	
Transceiver R_{ON} @100 mA	R_{ON}	–	22	–	Ω	–	
iso UART to UART propagation delay	$t_{isoUART\_UART\_del}$	–	25	100	ns	propagation delay from iso UART to UART	
iso UART bitrate	$BR_{isoUART}$	1.45	2	2.1	Mbit/s	–	
Series capacitor value	C_{SER}	0.95	1	1.05	nF	1)2)	
Series resistor value	R_{SER}	37.05	39	40.95	Ω	1)2)	

1) Not subject to production test, specified by design.

2) The external RC network may need to be adjusted depending on the application constraints (i.e. cable length)

6.2 Bus topology

The TLE9015QU support three different daisy-chain configurations:

- Master on Top/Master on Bottom
- Ring mode

6.2.1 Master on Top/Master on Bottom (MoT/MoB)

In this mode, the master (microcontroller) is always on the top or bottom of the chain and the transceiver IC TLE9015QU will be connected on one side to the master and on the other side to the first sensing IC in the chain.

For an MoT topology, the requests will be forwarded always from the IFH to IFL through the chain. For an MoB topology, the requests will be forwarded from the IFL to IFH. For the response message, the responding device will set both interfaces as TX. Further on, the rest of the chain will forward the message. Some nodes will need to switch their interfaces from TX to RX and RX to TX (this change in the iso UART interfaces is automatically controlled by the internal logic).

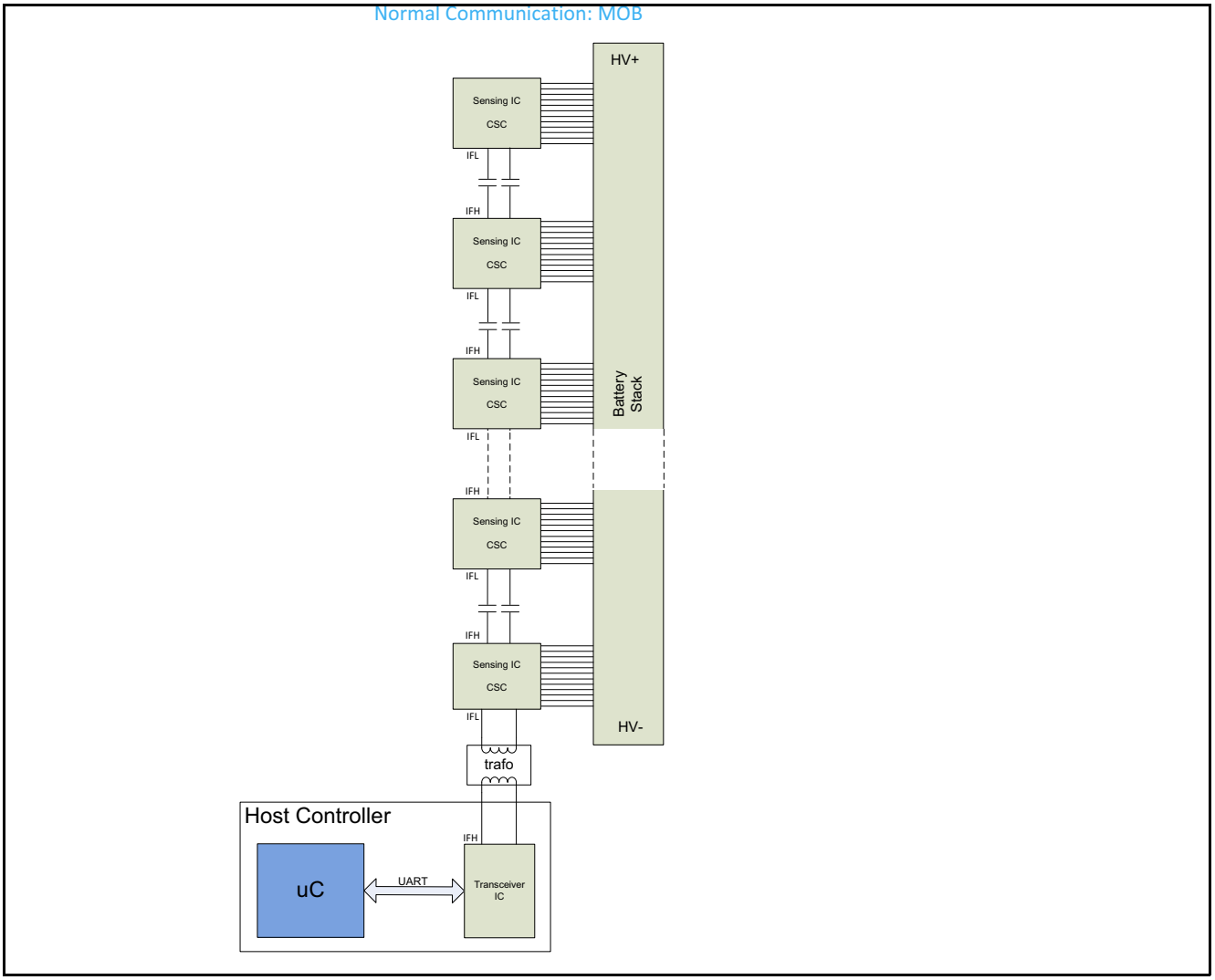


Figure 6-2 Network architecture for Master On Bottom configuration (simplified)

The MoT or MoB configuration within the daisy-chain can be selected depending on which interface is used for receiving the wake-up signal.

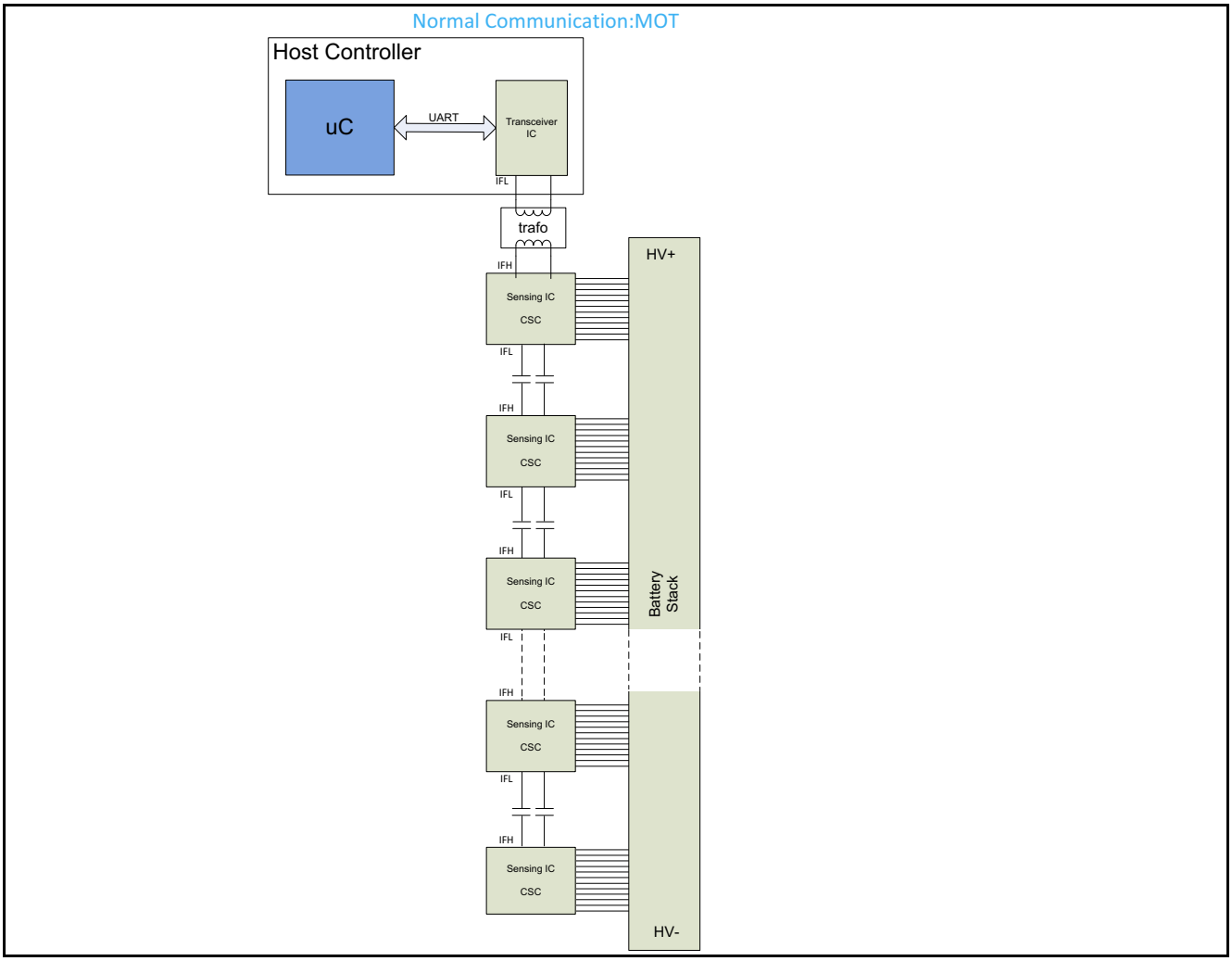


Figure 6-3 Network architecture for Master On Top configuration (simplified)

6.2.2 Ring topology

The TLE9015QU offers the possibility to connect all the sensing ICs in a system by using the so called ring topology. This topology is very similar to MoB or MoT, but the last node in the chain is also connected to the TLE9015QU.

When using a ring topology the host controller may wake-up the chain by using either UART HS or UART LS (MoB or MoT). Once the wake-up signal is sent, the direction must be kept until the next wake-up cycle. The requests will be forwarded through the chain respecting the direction set by wake-up. The TLE9015QU and the microcontroller will again receive the request from the opposite interface confirming that the full chain has no connection problems.

On the other side, the responses will be forwarded in both directions from the responding node. In this case, if the chain has no connection problems, the master will receive the same response from both interfaces.

The ring topology has significant advantages in terms of system availability under fault conditions.

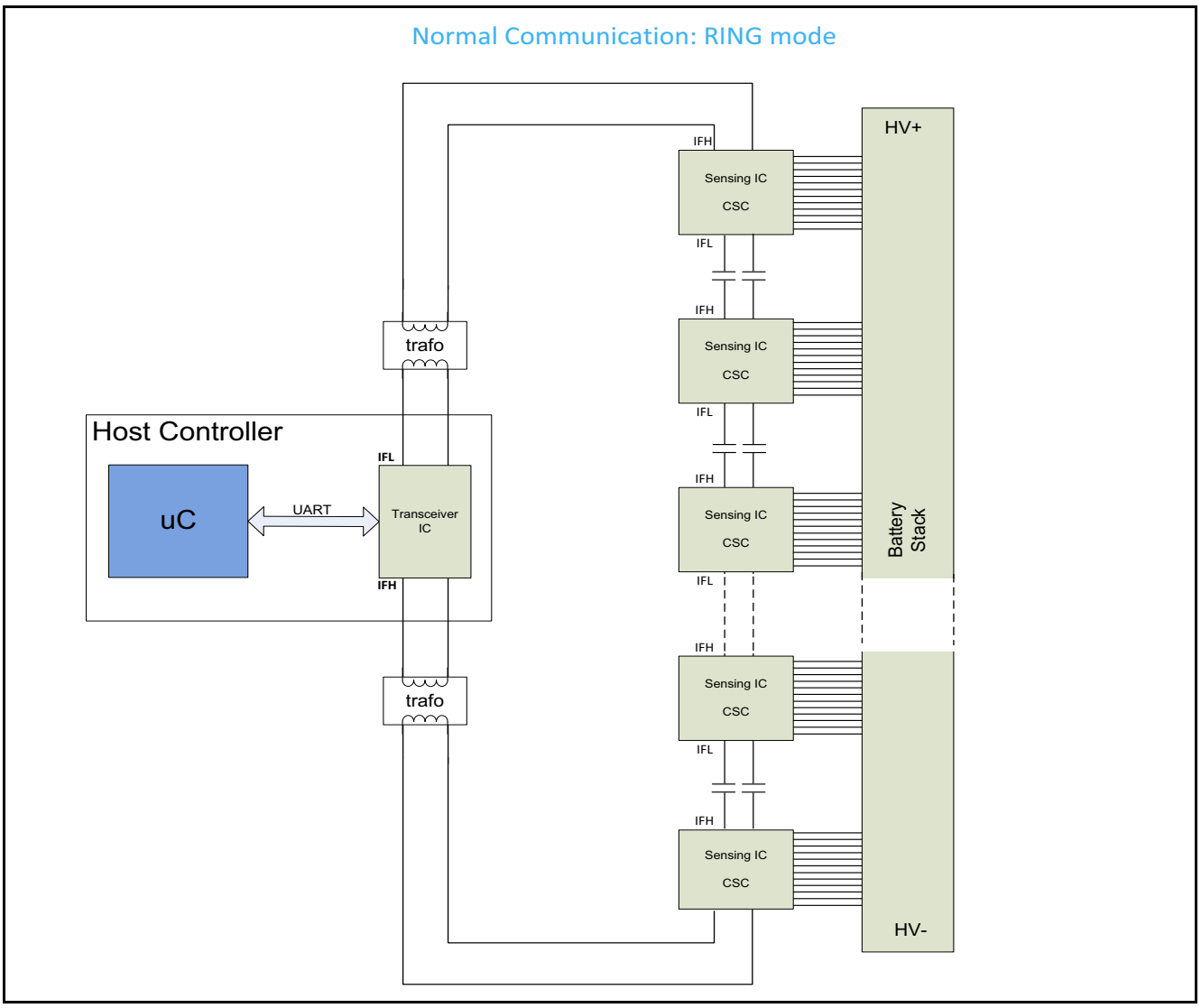


Figure 6-4 Network architecture for Ring mode configuration (simplified)

6.3 Frame description

For a detailed frame description please see the Sensing IC documentation. The transceiver IC only translates the frames from UART to iso UART and vice versa.

6.3.1 Timing

The chain timing is shown in **Figure 6-5**. The pass through time for each node is $t_{isoUART\_prop\_del}$. This means the microcontroller is still sending while the beginning of the message is already back at the microcontroller in ring mode.

There is a reply delay t_{reply_delay} implemented to make sure that all nodes can change their TX/RX direction properly before their reply frame is send.

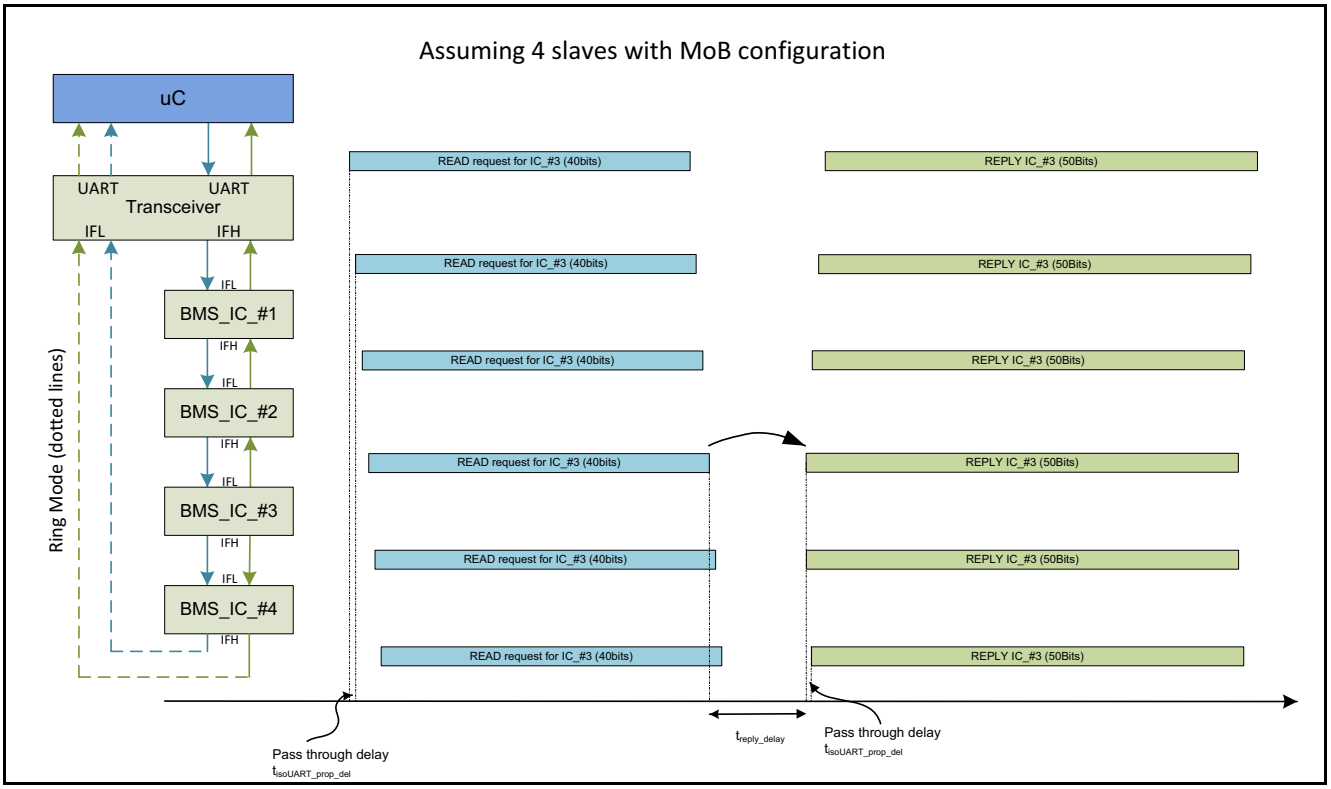


Figure 6-5 Timing

7 Application information

Note: The following information is given as an example for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device. The function of the circuit must be verified in the real application. Please ask for the Application Note regarding Application Information for more details.

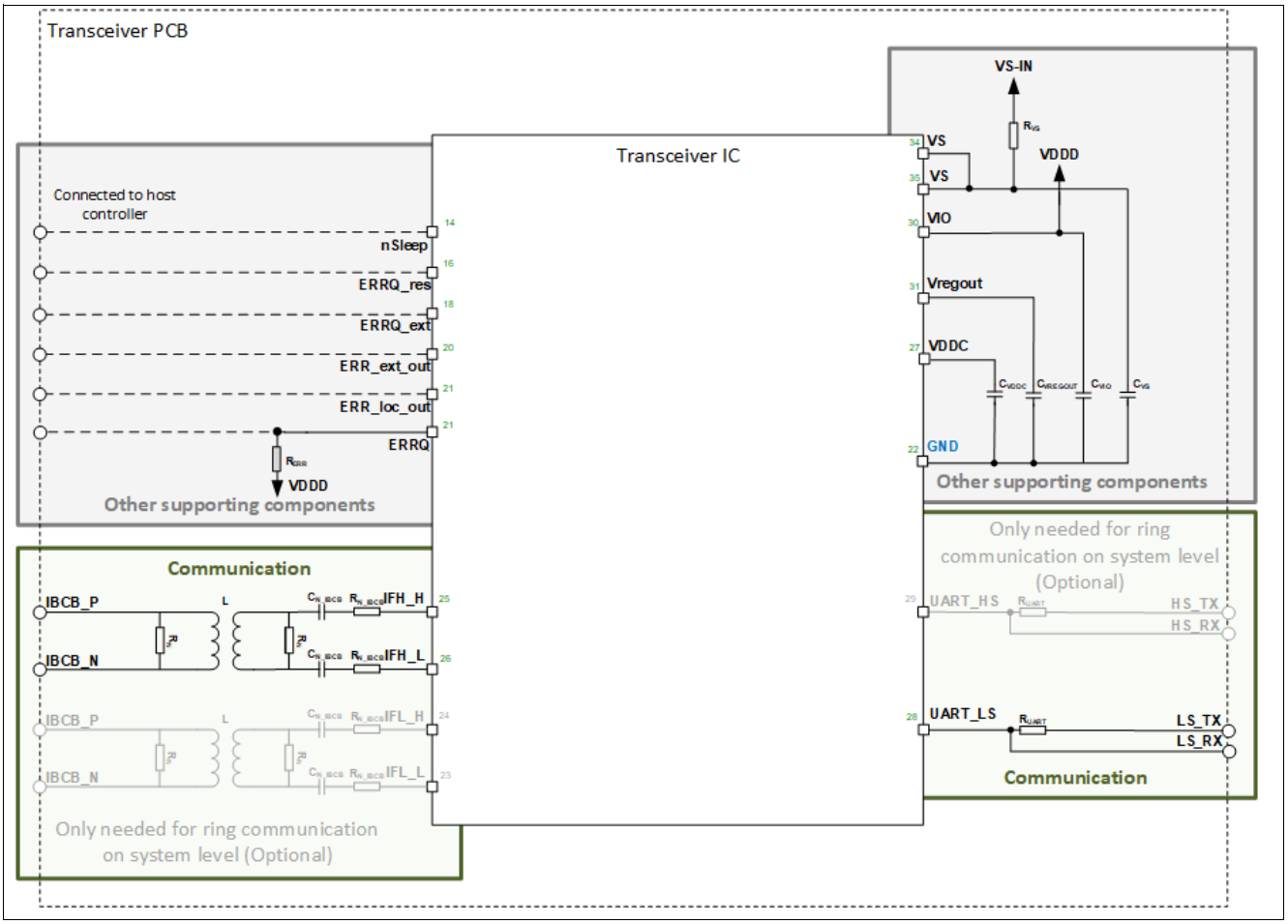


Figure 7-1 Application example

8 Package outlines

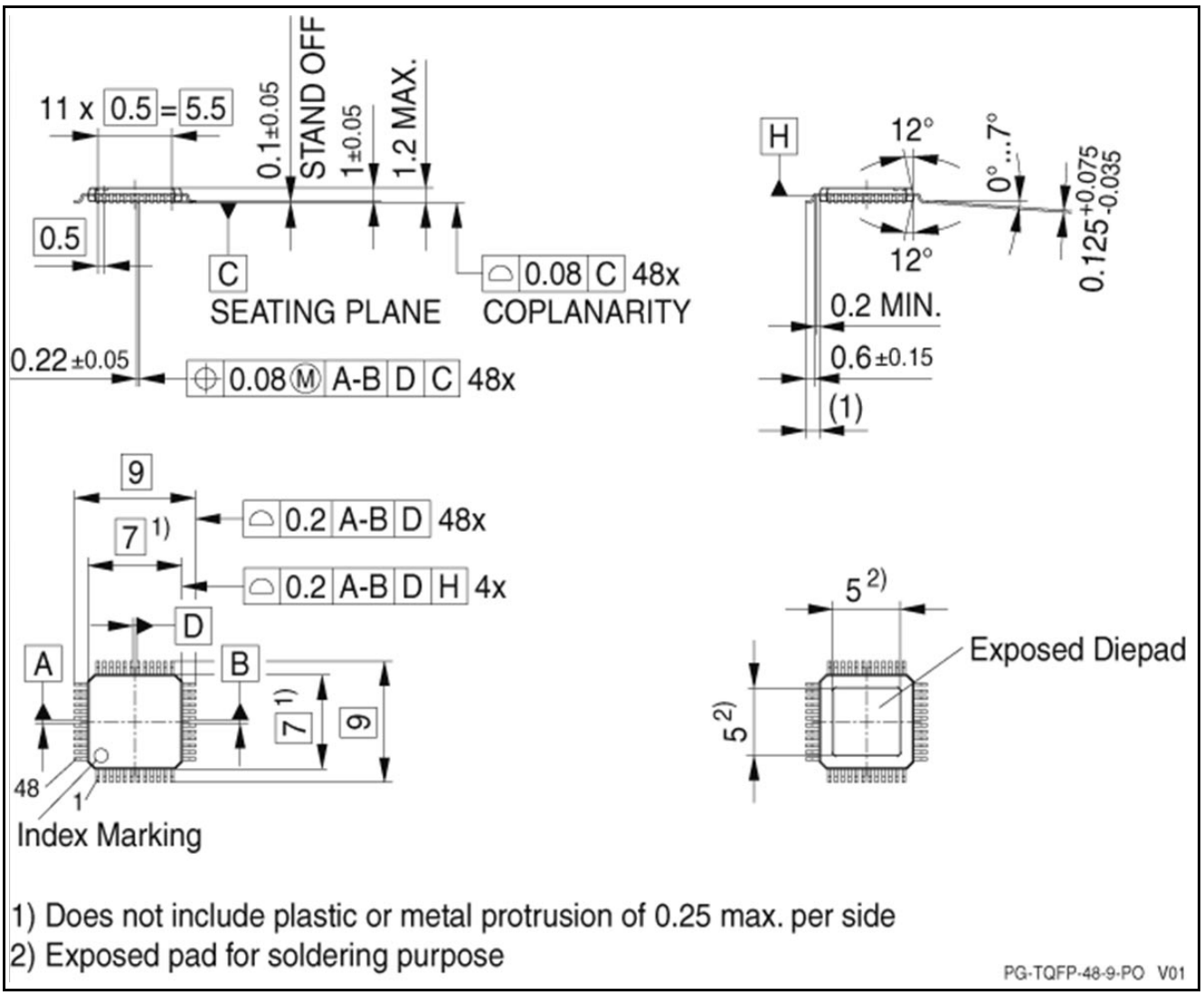


Figure 8-1 Package outlines and footprint PG-TQFP-48

Green product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision history

Revision	Date	Changes
1.0	2019-12-13	Initial Datasheet

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2019-12-13
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
<Doc_Number>

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.