TLE8110ED Switching Inductive Loads and External Clamping

Product Family: Flex Multichannel Low-Side Switches

About this document

Scope and purpose

This application note is intended to provide additional information regarding the Clamping Energy capabilities of the TLE8110ED. **Chapter 1** has to be considered as an addendum to the Application Note Multichannel Low-Side Switches - Switching Inductive Loads.

Chapter 2 of this application note is intended to demonstrate the external clamping behavior of the TLE8110ED with an external Zener Diode. The other two possibilities (external free wheeling diode and external free wheeling resistor) are not the focus of this application note but they are briefly illustrated. The test conditions, the lab setup, the measurements and differences between the methods are described.

The clamping energy which can be safely dissipated inside the TLE8110ED is restricted to the energy values given in the data sheet. When there are loads with a higher clamping energy it is necessary to have an external clamping unit. For an overview of the permitted loads for the TLE8110ED, please refer to the relevant section of the data sheet.

For a more detailed description of the capabilities of the TLE8110ED, please refer to the data sheet.

Note: *The following information is provided as advice for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

Intended audience

This document is aimed at users in need of additional information regarding the Clamping Energy capabilities of the TLE8110ED.

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1 TLE8110ED Switching Inductive Loads

1.1 Clamping Energy versus Current (SOA)

The TLE8110ED Switching Inductive Loads channels can be grouped as following **Table 1**, according to DMOS size and symmetry.

Table 1 TLE8110ED Switching Inductive Loads channel groups

Channel Group	$R_{DS(MAX)}$ [Ω]	$I_{LIM(MIN)}$ [A]	$I_{LIM(MAX)}$ [A]
CH1-4	0.6	2.6	5.0
CH5-6	0.5	3.7	6.0
CH7-10	1.2	1.7	2.9

In the following sections the energy SOA will be shown for each channel group in order to give the user the possibility to check the device capabilities in relation to his specific loads. For a detailed description on how to measure/calculate the operating point (I_L, E_{CL}) for each load and how to do the application check, please refer to the TLE8110ED Switching Inductive Loads Data Sheet and to the Application Note *Multichannel Low-Side Switches - Switching Inductive Loads*. Three areas of energy will be shown for a cumulative scenario:

- Normal Operation
  - 10^9 cycles
- Mid Energy[1)]
  - either 10^4 cycles
  - or 10^5 cycles
- High Energy
  - 10 single pulses

1) In the case of a mid energy area, two different plots are shown (10^4 and 10^5 cycles) for more flexibility to the user, but in no case it is allowed to combine both operations at the same time in a cumulative scenario, use either one or the other curve.

1.1.1 Channel Group 1-4[1) 2) 3)]

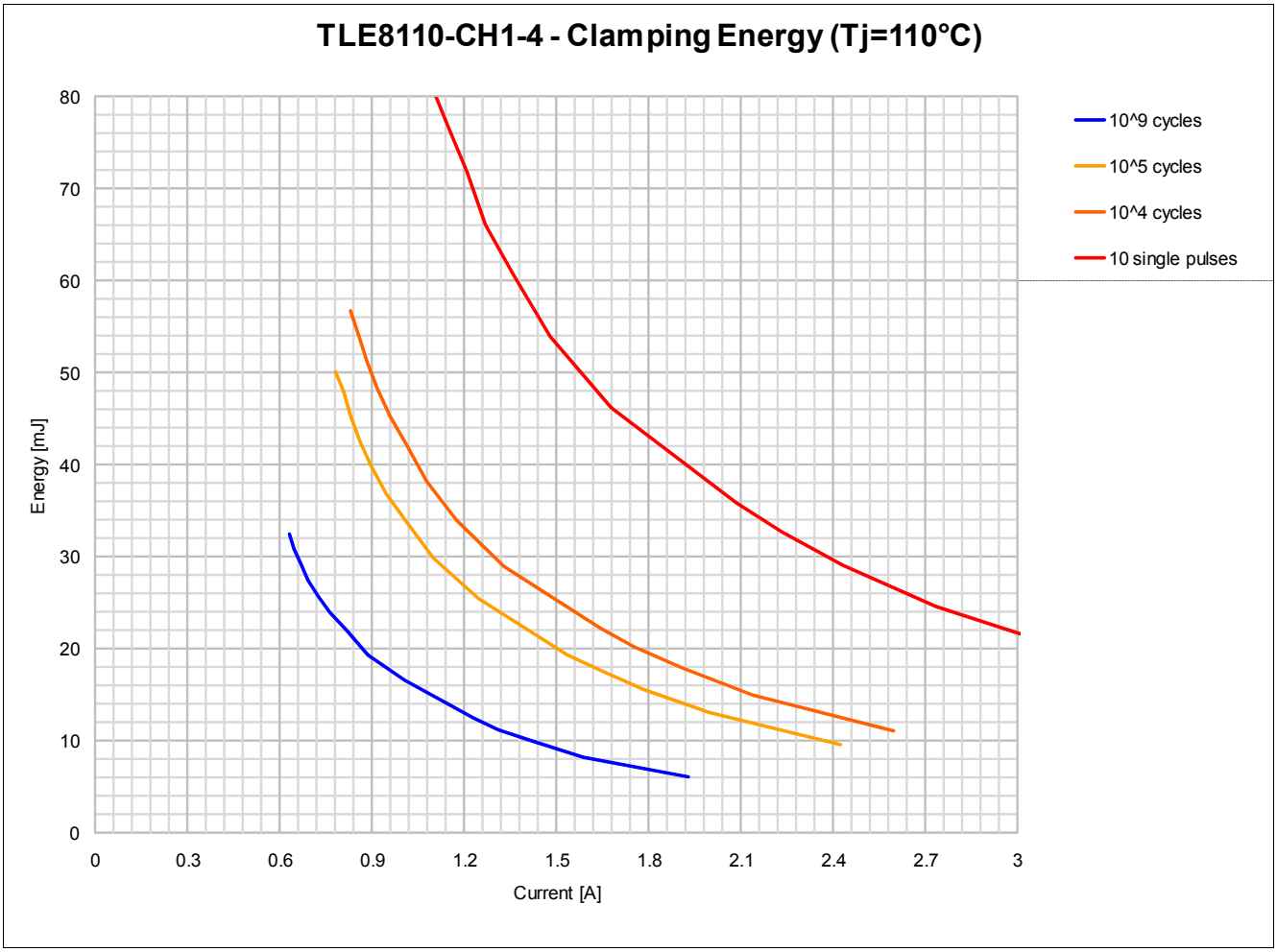

Figure 1 Energy SOA for TLE8110ED - CH1-4 (T_J = 110°C)

1) Data shown here for a starting temperature T_J = 110°C are based on extrapolation and not directly from measured data.

2) In the case of a mid energy area, two different plots are shown (10^4 and 10^5 cycles) for more flexibility to the user, but in no case it is allowed to combine both operations at the same time in a cumulative scenario, use either one or the other curve.

3) Several operating points could be grouped within the same energy level, in that case the total number of cycles allowed by the relative SOA has to be split among the operating points.

1.1.2 Channel Group 5-6[1) 2) 3)]

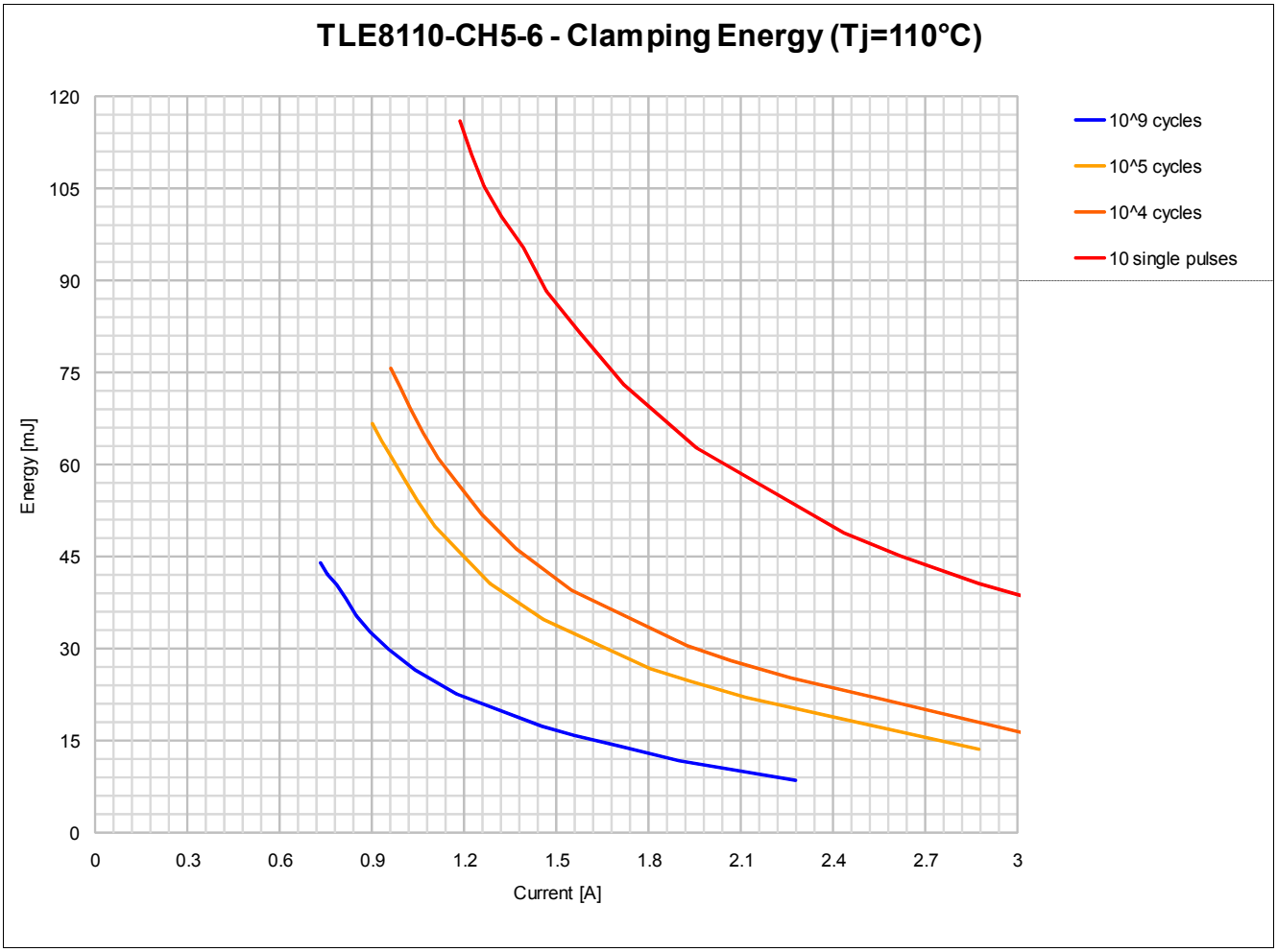

Figure 2 Energy SOA for TLE8110ED - CH5-6 (T_J = 110°C)

1) Data shown here for a starting temperature T_J = 110°C are based on extrapolation and not directly from measured data.
2) In the case of a mid energy area, two different plots are shown (10^4 and 10^5 cycles) for more flexibility to the user, but in no case it is allowed to combine both operations at the same time in a cumulative scenario, use either one or the other curve.
3) Several operating points could be grouped within the same energy level, in that case the total number of cycles allowed by the relative SOA has to be split among the operating points.

1.1.3 Channel Group 7-10[1) 2) 3)]

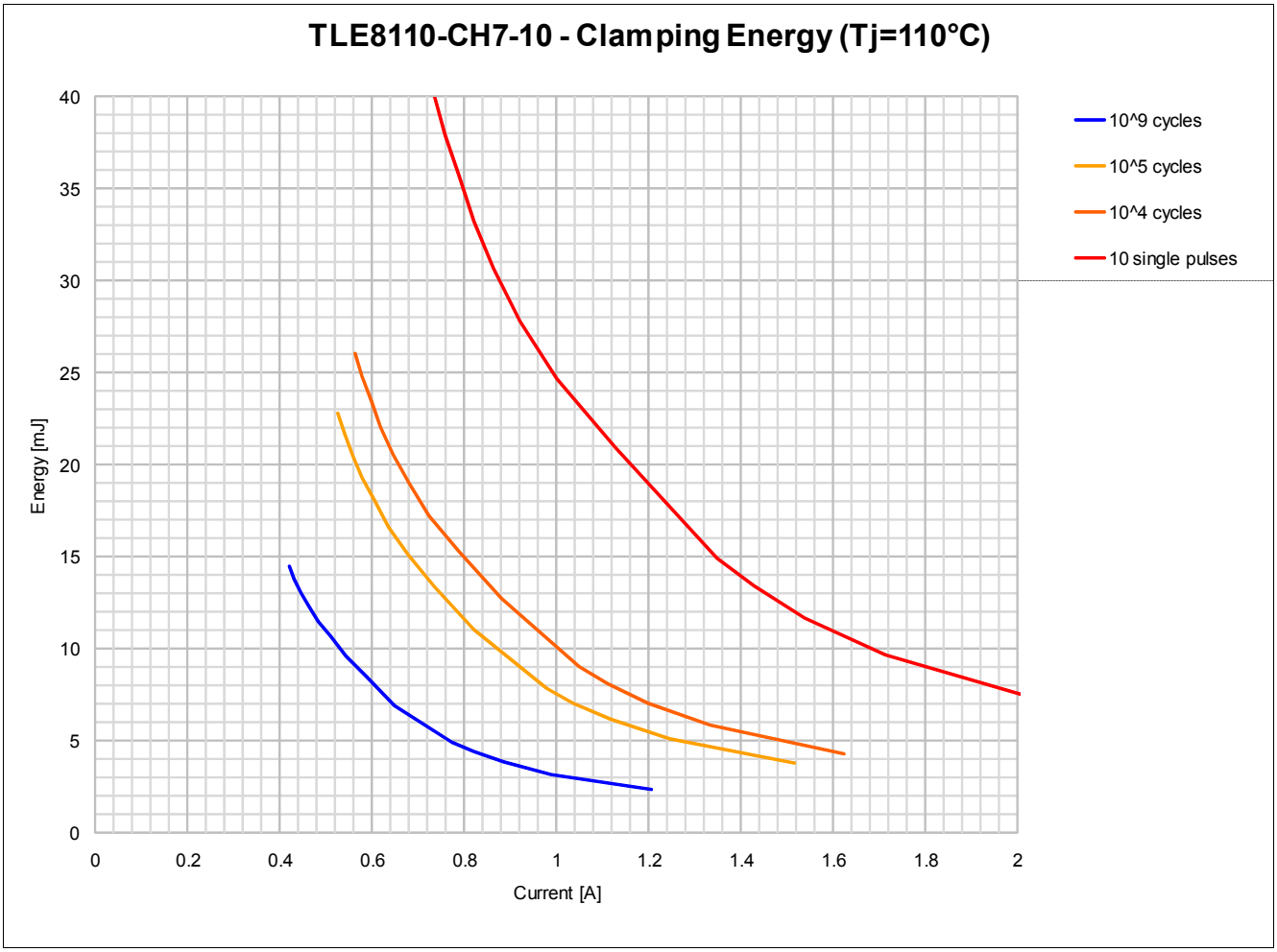

Figure 3 Energy SOA for TLE8110ED - CH7-10 (T_J = 110°C)

1) Data shown here for a starting temperature T_J = 110°C are based on extrapolation and not directly from measured data.
2) In the case of a mid energy area, two different plots are shown (10^4 and 10^5 cycles) for more flexibility to the user but, in no case it is allowed to combine both operations at the same time in a cumulative scenario, use either one or the other curve.
3) Several operating points could be grouped within the same energy level, in that case the total number of cycles allowed by the relative SOA has to be split among the operating points.

1.2 Clamping Energy for Parallel Mode Operation

The TLE8110ED Switching Inductive Loads is equipped with a structure which improves the performance of parallel-connected channels, for more details please refer to the TLE8110ED Switching Inductive Loads data sheet. The provided energy SOAs can be utilized to evaluate the capabilities of the device also for parallel connected channels. Three cases need to be distinguished:

- PM-bit set (PMx = 1[1)], improved parallel capabilities)
- PM-bit not set (PMx = 0)
- PM-bit lost after a reset

When DMOS switches are connected in parallel, the current is not necessarily equally shared, especially in a dynamic regime (e.g. clamping event) due to layout asymmetries, differences in timing and parameters shift overtemperature. Assuming that one of the two parallel connected channels will take a largest part of the current during the clamping event, we can express the sharing as:

(1.1)

$$I_{CHmax} = a \bullet I_{TOT} \; ; \quad I_{CHmin} = (1 - a) \bullet I_{TOT}$$

where I_{TOT} is the total current and I_{CHmax} I_{CHmin} are the currents flowing through the 2 channels and $a > 0.5$. The coefficient a depends on several factors and may vary device to device, channel to channel. For the TLE8110ED the value of a is show in **Table 2**.

Note: According to the TLE8110ED Switching Inductive Loads data sheet, a Reset[2)] input causes a reset of all registers to their default values and consequently PMx is set to 0, moreover the channels will be switched off causing a clamping event. After the reset pulse, the current sharing at the turn-off will be the same as per PMx = 0 condition, but while the reset pulse is still High, the sharing of the current shows an improved behavior. Therefore the third case (PM-bit lost) cannot be characterized as depending on the duration of the reset pulse, but it can be stated that the PM-bit lost condition can be better or equal to the PMx = 0 condition in terms of clamping energy.

Table 2 *TLE8110ED Switching Inductive Loads a*-coefficient

	PMx = 1	PMx = 0	PM-bit lost
a-coefficient[1)]	0.6	0.8	-[2)]

1) The coefficient is valid for dynamic conditions (e.g. clamping event) and takes into account variations of current sharing overtemperature and overcurrent, for all channel groups.
2) The coefficient cannot be extracted in this case as it depends on the duration of the reset pulse.

Similar to the current, the clamping energy will also be shared between channels:

(1.2)

$$E_{CHmax} = a \bullet E_{TOT} \; ; \quad E_{CHmin} = (1 - a) \bullet E_{TOT}$$

Knowing the total current and the total clamping energy of the load, with **Equation (1.1)** and **Equation (1.2)** we can evaluate the current and the clamping energy of the dominant channel (I_{CHmax}, E_{CHmax}) and use those values as entry point for the provided SOA. The same considerations made for single channel applies then also for the parallel-connected channels.

1) For the PMx register configuration, please refer to the data sheet of the device.
2) The reset can be also due to an undervoltage of the logic supply.

The same reasoning can be generalized and extended to more than 2 channels in parallel, in that case *a* has to be replaced by the coefficient λ:

(1.3)

$$I_{CHmax} = \lambda \bullet I_{TOT}\ ;\ E_{CHmax} = \lambda \bullet E_{TOT}\ ;\ \text{with}\ \lambda = \frac{a}{a + (n-1) \bullet (1-a)}$$

where n is the number of channels in parallel[1] with the same coefficient *a*[2].

1.2.1 Application Check example for Parallel Mode Operation

Let's consider an example (for simplicity we only analyze the normal operation) with a load showing following characteristics[3]:

- I_{TOT} = 1.5 A
- E_{TOT} = 30 mJ

applied on CH1 and CH2 in parallel.

Using **Equation (1.1)** and **Equation (1.2)** we obtain the values summarized in **Table 3**.

Table 3 *TLE8110ED Switching Inductive Loads a*-coefficient

	PM-bit set	PM-bit not set	PM-bit lost
I_{CHmax} [A]	0.9	1.2	-
E_{CHmax} [mJ]	18	24	-

If we project those values into the SOA of channel group 1-4 of the TLE8110ED Switching Inductive Loads, see **Figure 4**, we can draw the following conclusion:

- if the PM-bit is set: the load can be driven on CH1//CH2 for 10^9 cycles
- if the PM-bit is not set: the same load can be driven up to a maximum of 10^5 cycles

At the same time we could also draw some conclusion on the loss of the PM-bit configuration due to the following considerations:

- loss of the PM-bit configuration happens after a reset (or a logic supply undevoltage), therefore is a low probability event whose occurrence rate can be estimated
- during loss of the PM-bit the clamping capabilities can be approximated as worst case with the case of the PM-bit not set

In a cumulative scenario the PM-bit lost condition can be considered as an additional mid-energy condition, therefore we could state that the load can be driven on CH1//CH2 for:

- 10^9 cycles with PM-bit set
- + 10^5 cycles with the PM-bit lost + other mid-energy conditions (to be verified)
- + 10 single pulses in high-energy condition (to be verified)

1) The TLE8110ED allows to connect in channels in parallel via PM-bit only if belonging to the same group (1-4, 5-6, 7-10) and only if they are adjacent in numbering, please refer to the data sheet of the device.
2) **Equation (1.3)** is valid only if channels have the same a-coefficient, which is the case for the TLE8110ED.
3) In real application case also the mid-energy and high-energy could be considered applying the same equations.

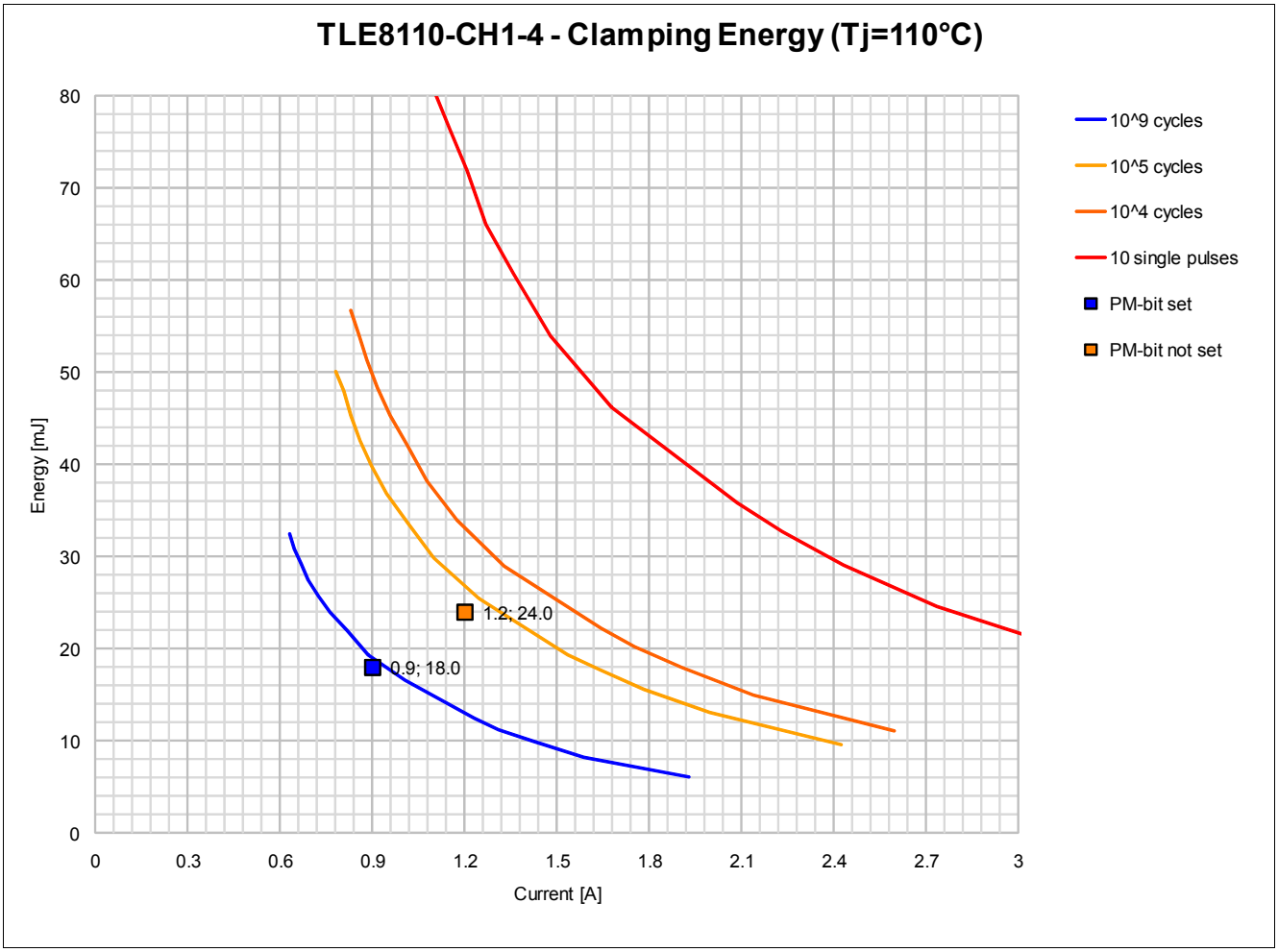

Figure 4 Clamping Energy in Parallel Mode

1.3 Conclusion

This section of the application note illustrated the clamping energy capabilities of the TLE8110ED Switching Inductive Loads. Subsequently, the Parallel Mode operation was considered for the clamping event and the specific condition of a Parallel Mode lost due to a reset was discussed.

The information provided, together with the more generic Application Note Multichannel Low-Side Switches - Switching Inductive Loads, represents a guideline for safe and efficient design using the TLE8110ED Switching Inductive Loads.

2 External Clamping with the TLE8110ED

This chapter demonstrates the external clamping behavior of the TLE8110ED with an external Zener Diode. The other two possibilities (external free wheeling diode and external free wheeling resistor) are not the focus of this application note but they are briefly illustrated. The test conditions, the lab setup, the measurements and differences between the methods are described.

The clamping energy which can be safely dissipated inside the TLE8110ED is restricted to the energy values given in the data sheet. When there are loads with a higher clamping energy it is necessary to have an external clamping unit. For an overview of the permitted loads for the TLE8110ED, please refer to the relevant section of the data sheet.

For a more detailed appreciation of the capabilities of the TLE8110ED, please refer to the data sheet.

2.1 Introduction

Note:

- All measurements in this application note have been undertaken accurately but the results are not guaranteed. This application note can be changed without prior notification
- Please refer to the official TLE8110ED data sheet for detailed technical descriptions.

2.1.1 Basic setup and graphical calculation of the clamping energy

Figure 5 shows the circuit with the TLE8110ED for the first measurements to declare the internal clamping behavior. The signals marked in color in **Figure 5** are plotted in **Figure 6**.

Basic setup (this setup is used as basic setup for all circuits in this application note):

- V_{bat}…14 V
- V_{dd}…5 V
- V_{cc}…5 V
- R…9 Ω
- L…15 mH
- Channel under test is Ch2
- Output current is in the range of 1.55 A

The reason to choose this load was that we are able to compare the behaviors from external clamping in a direct way with the TLE8110ED clamping. There are no problems for the TLE8110ED without external clamping with this load.

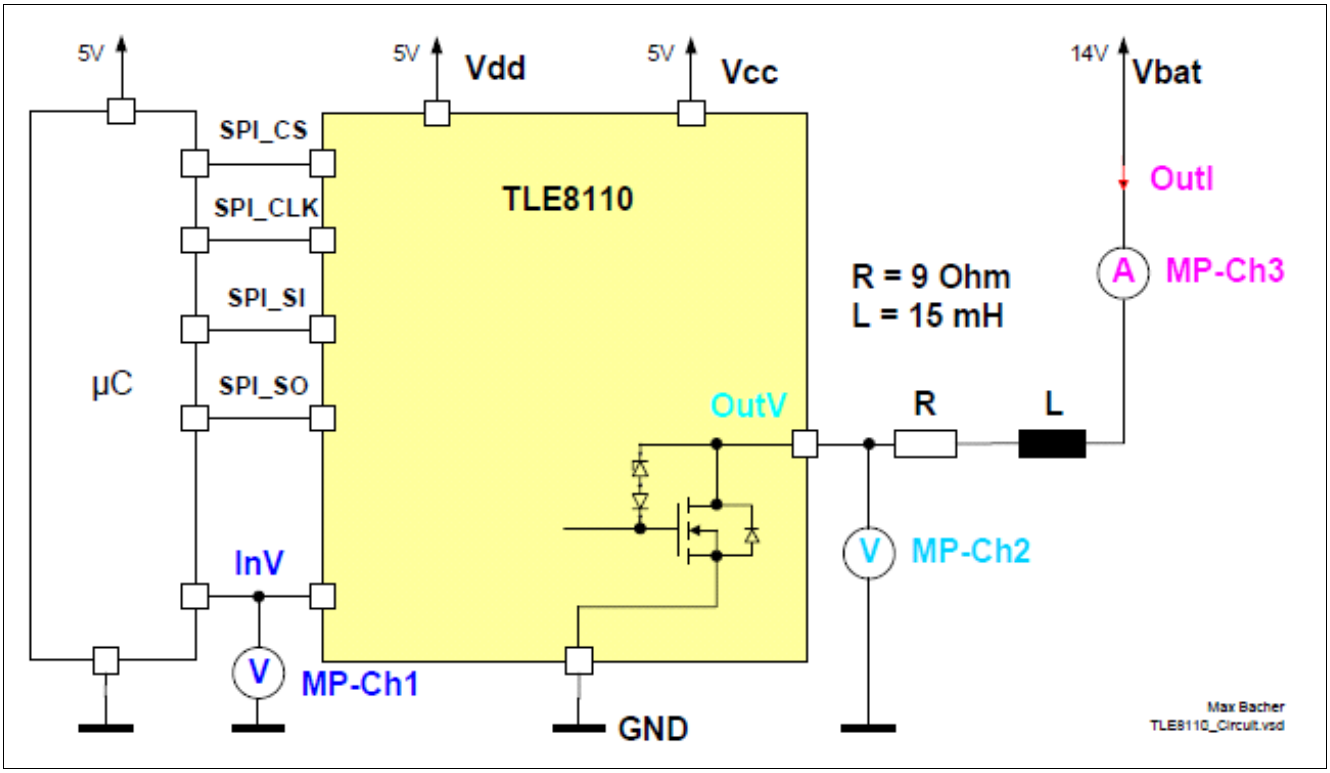

Figure 5 TLE8110ED connected to a load

Figure 6 shows the clamping behavior. The “Math Channel” (the red one) describes the clamping power and is calculated as channel 2 (output voltage) multiplied by channel 3 (the output current).

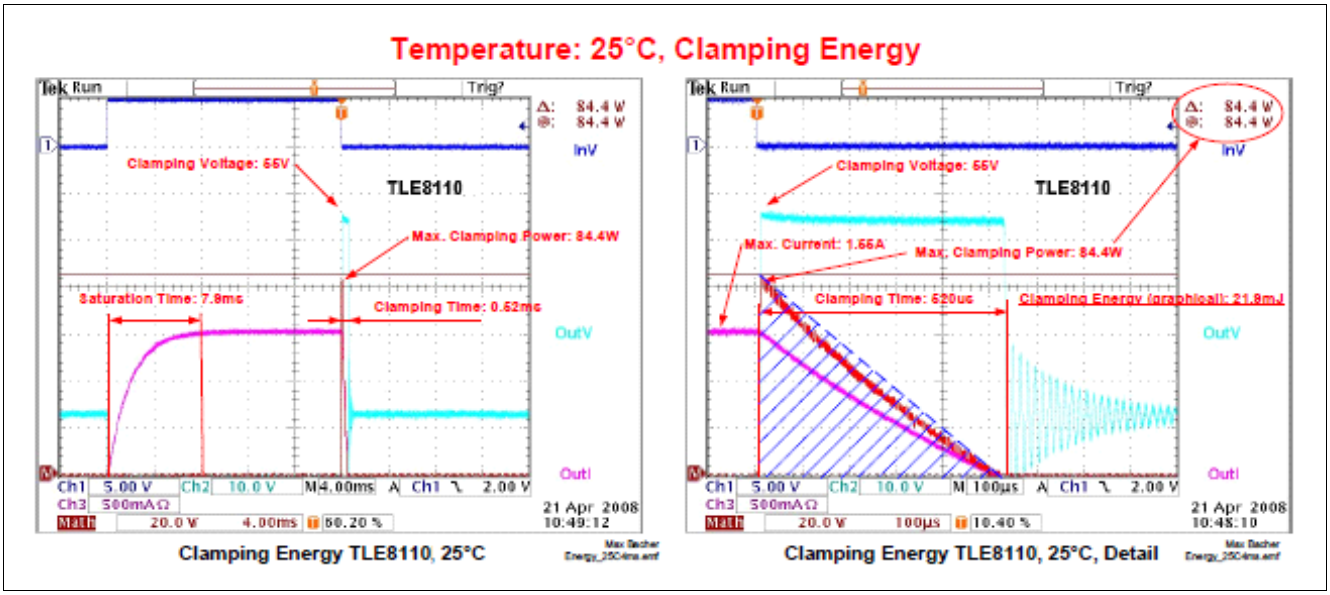

Figure 6 Clamping with inductive and ohmic load to show the clamping energy

The clamping energy can be calculated in a graphical way. The approximate clamping energy which is easy to calculate is the area below the dashed blue line marked with dotted blue lines, seen on the right side of **Figure 6**. When we calculate the energy graphical we get this value: **E = 21.94 mJ** (Max. clamping power × 0.5 × clamping time = 84.4 W × 520 µs × 0.5).

2.1.2 Calculate clamping energy

There are two well-known equations to calculate the clamping energy for an inductive load. Equation 1 has to be used when there is also an ohmic part for the load. Equation 2 could be used when there is no ohmic part - or the ohmic part is near zero - for the load.

Abbreviations for the Equations:

- V_{AZ}…Voltage Active Zener Clamping (for low-side switches: $V_{AZ} = V_{DS(CL)}$)
- $V_{DS(CL)}$…Voltage Drain Source during Clamping
- V_{bat}…Battery Voltage
- I_0…Saturation Current

$$E = V_{DS(CL)} \bullet \left[\frac{V_{bat} - V_{DS(CL)}}{R} \bullet \ln\left(1 - \frac{R \bullet I_0}{V_{bat} - V_{DS(CL)}} \right) + I_0 \right] \bullet \frac{L}{R}$$

Figure 7 Equation 1: For the clamping energy of a low-side switch with an ohmic part of the inductive load

$$E = \frac{1}{2} \bullet L \bullet {I_0}^2 \bullet \frac{V_{DS(CL)}}{V_{DS(CL)} - V_{bat}}$$

Figure 8 Equation 2: For the clamping energy of a low-side switch with no ohmic part of the inductive load

For the basic setup - shown in **Figure 5** - we calculate the clamping energy using Equation 1 : **E = 19.79 mJ**. Please be aware: We have to use Equation 1 because there is an ohmic part for the load. If we calculate using Equation 2, the result will be: **E = 24.17 mJ**.

An overview about the different possibilities to get a result for the clamping energy:

Table 4 Different possibilities for results for the clamping energy

With graphical calculation:	E = 21.94 mJ
With Equation 1:	E = 19.79 mJ
With Equation 2:	E = 24.17 mJ

2.2 External Zener diode

2.2.1 Application circuit

Figure 9 shows the circuit of the TLE8110ED with a Zener diode for external clamping. The signals marked in color in **Figure 9** are plotted in **Figure 10** to **Figure 21** to have a better overview.

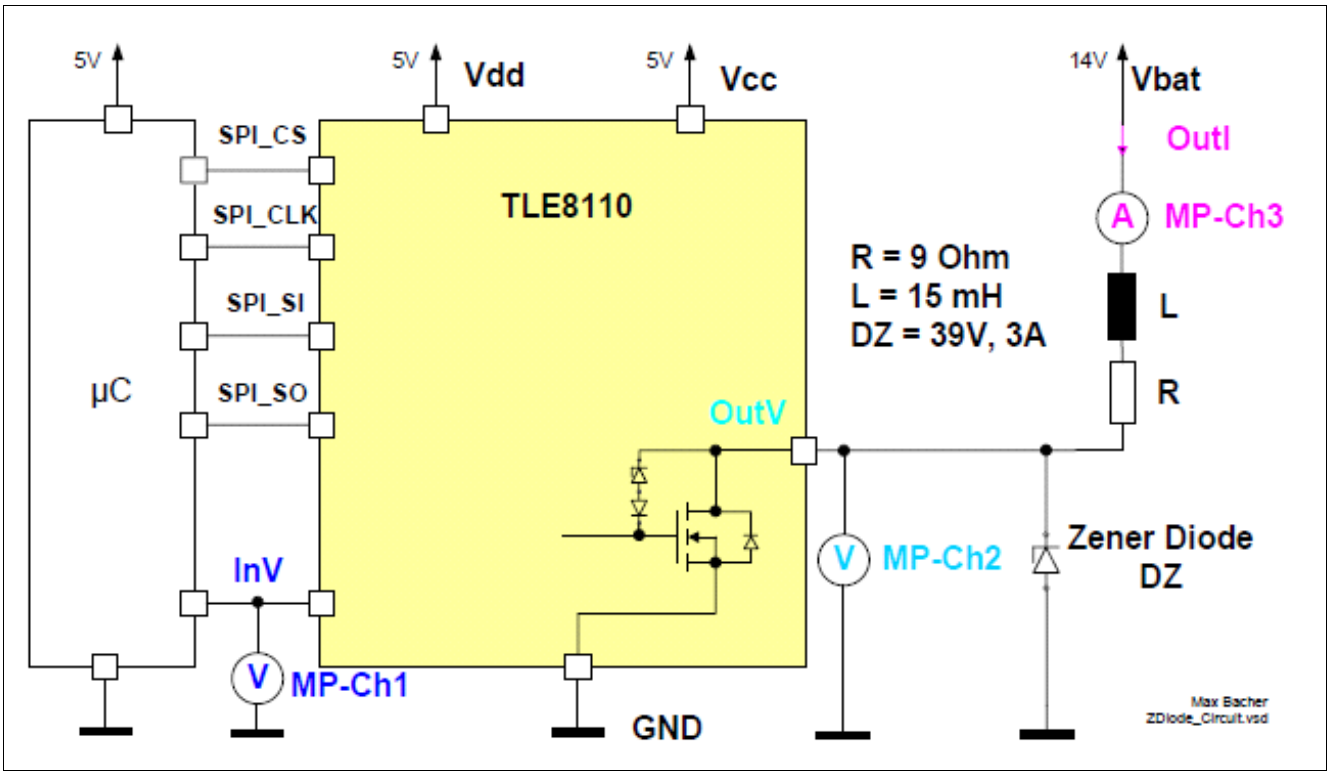

Figure 9 TLE8110ED with a Zener diode for external clamping

2.2.2 Measurements

Figure 10 to **Figure 12** show the clamping behavior with the Zener diode for -40°C. This is the temperature for the TLE8110ED and also for the Zener diode. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

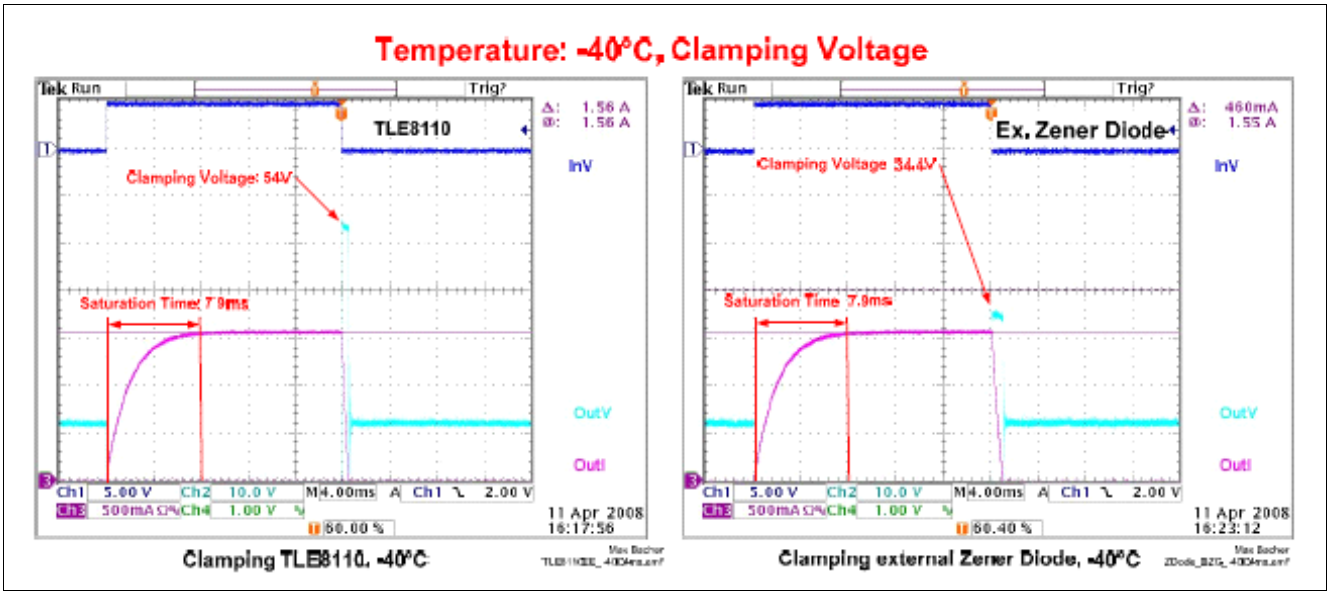

Figure 10 Comparing the clamping voltages for internal and external clamping with a Zener diode at -40°C

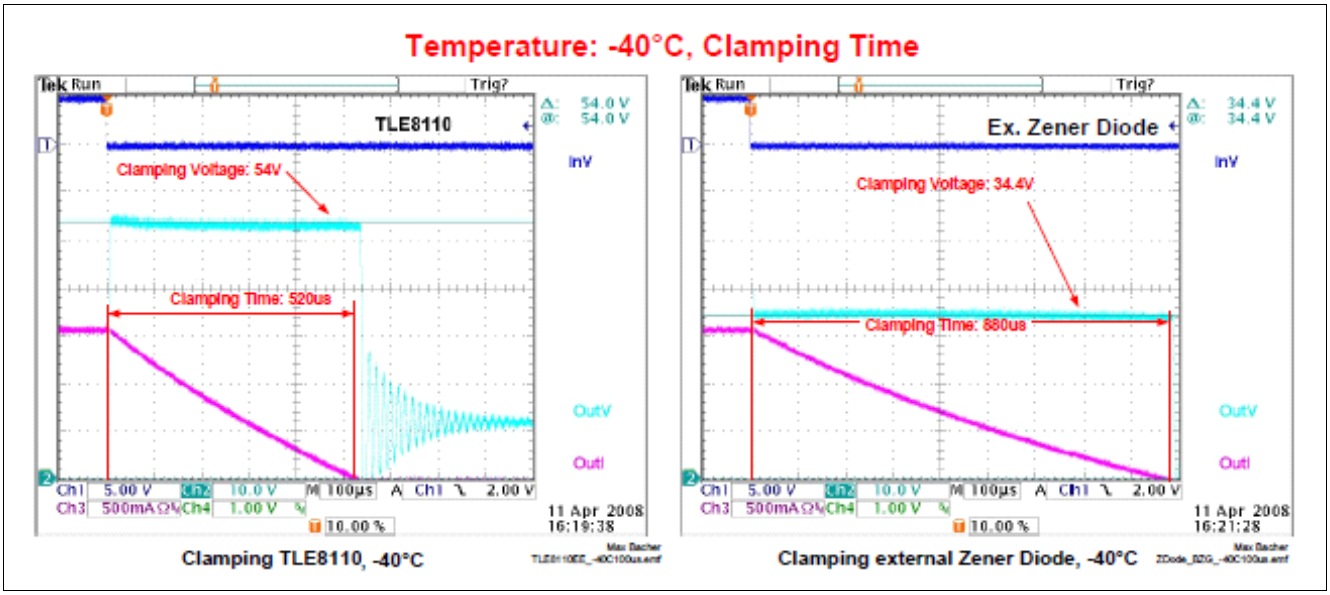

Figure 11 Comparing the clamping time for internal and external clamping with a Zener diode at -40°C

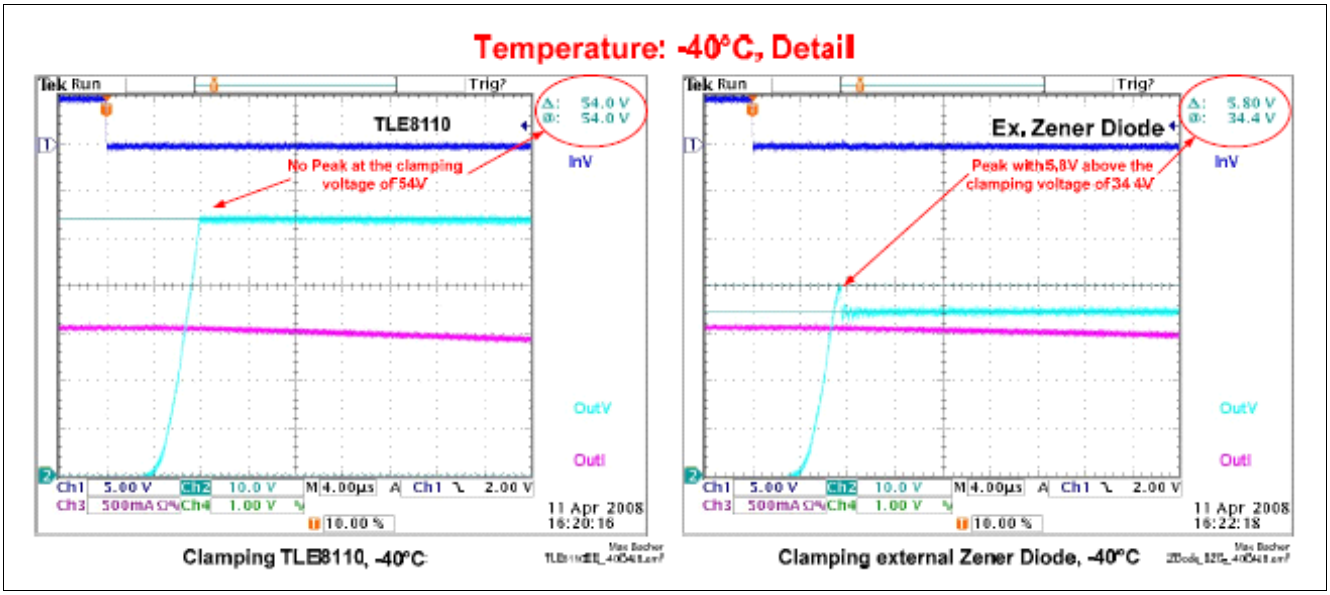

Figure 12 Comparing the voltage peak for internal and external clamping with a Zener diode at -40°C

Figure 15 to **Figure 15** show the clamping behavior with the Zener diode for 25°C. This is the temperature for the TLE8110ED and also for the Zener diode. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

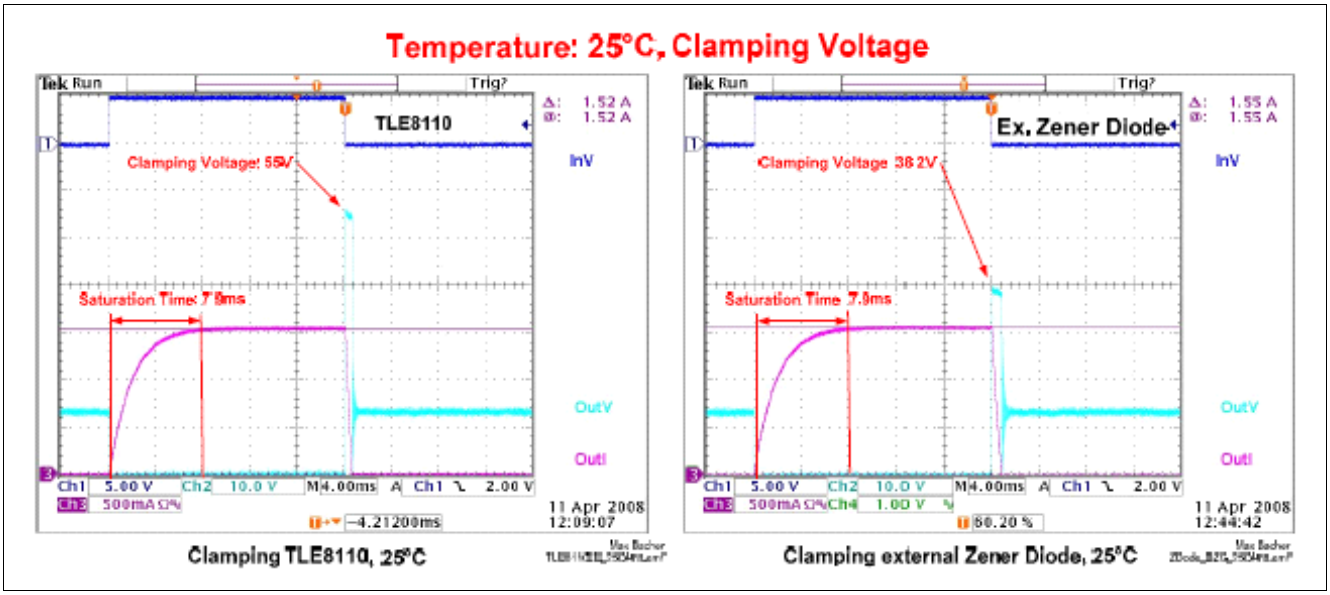

Figure 13 Comparing the clamping voltages for internal and external clamping with a Zener diode at 25°C

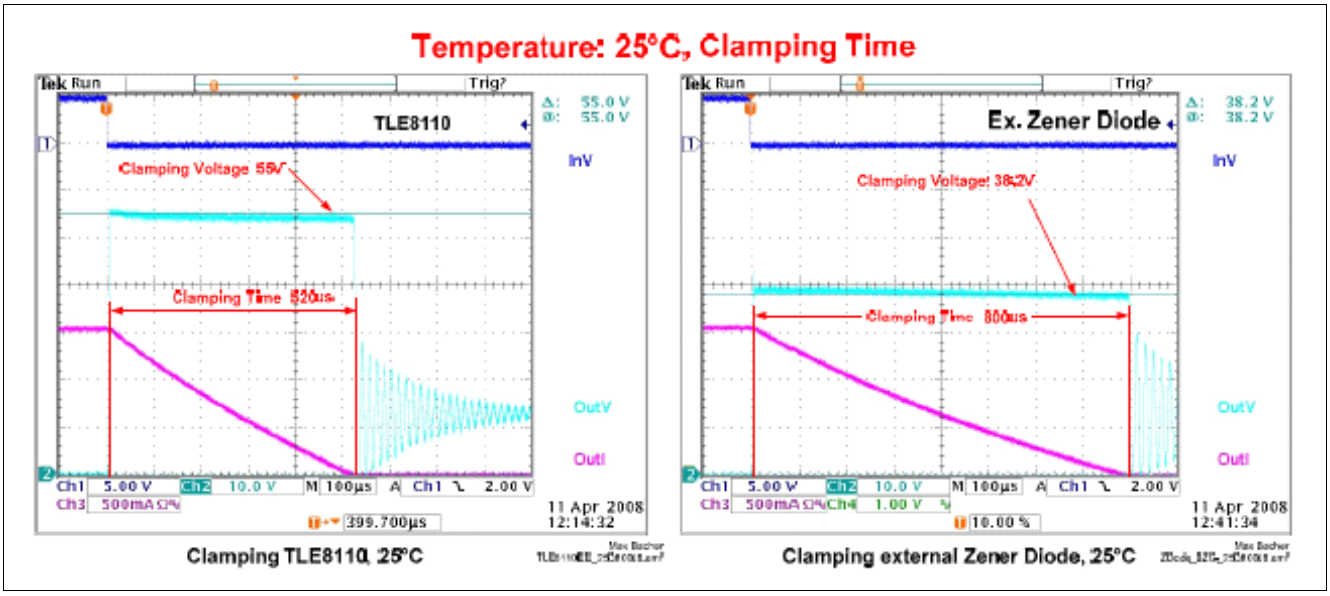

Figure 14 Comparing the clamping time for internal and external clamping with a Zener diode at 25°C

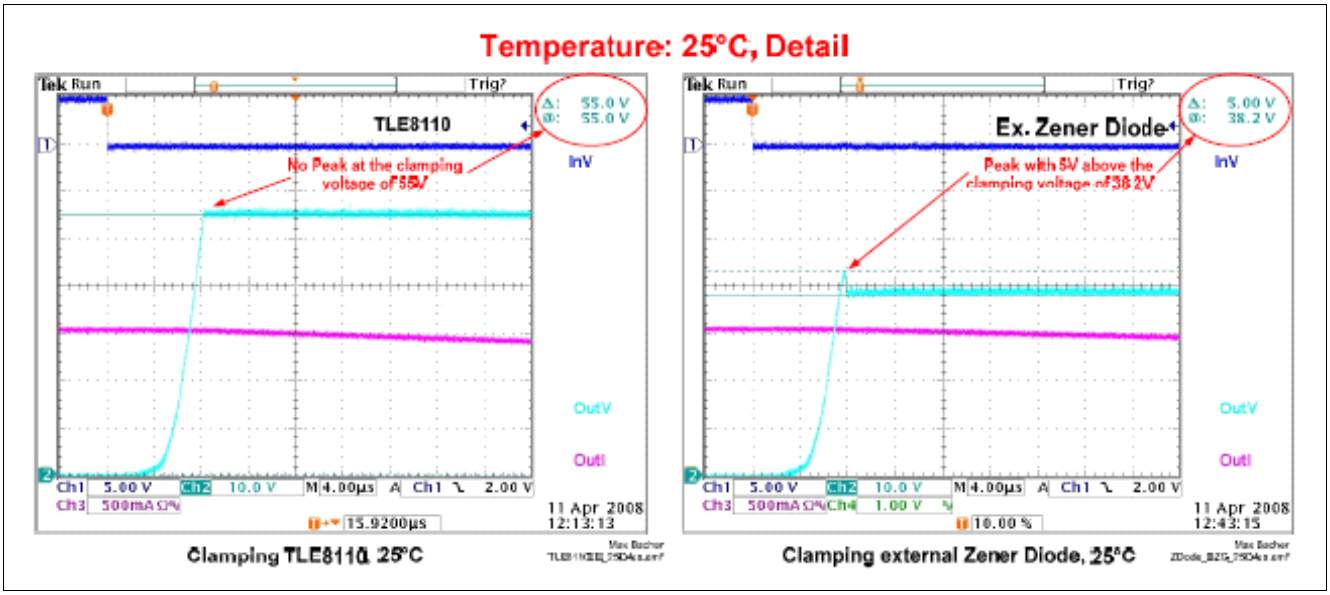

Figure 15 Comparing the voltage peak for internal and external clamping with a Zener diode at 25°C

Figure 16 to **Figure 18** show the clamping behavior with the Zener diode for 125°C. This is the temperature for the TLE8110ED and also for the Zener diode. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

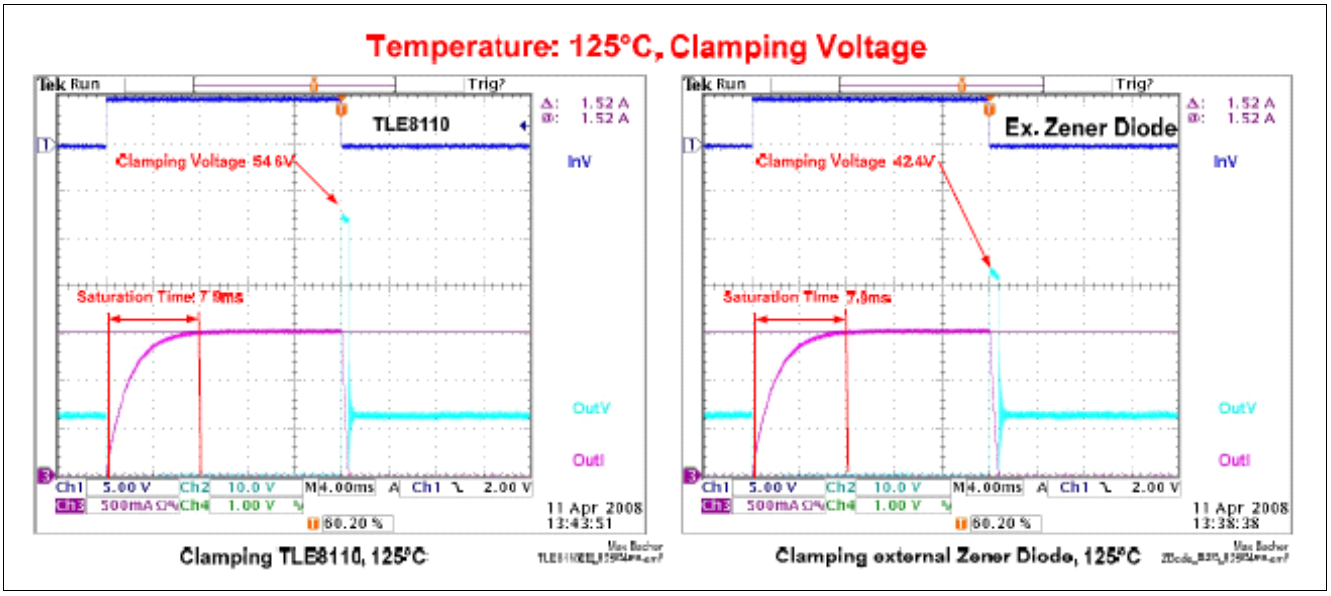

Figure 16 Comparing the clamping voltages for internal and external clamping with a Zener diode at 125°C

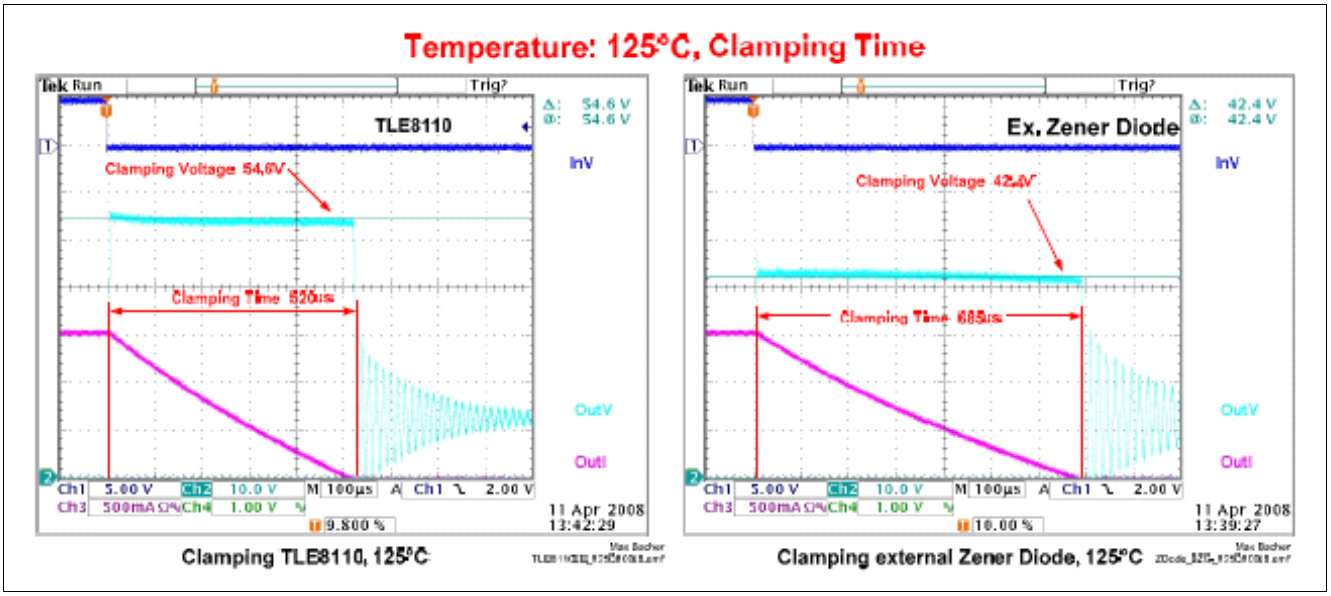

Figure 17 Comparing the clamping time for internal and external clamping with a Zener diode at 125°C

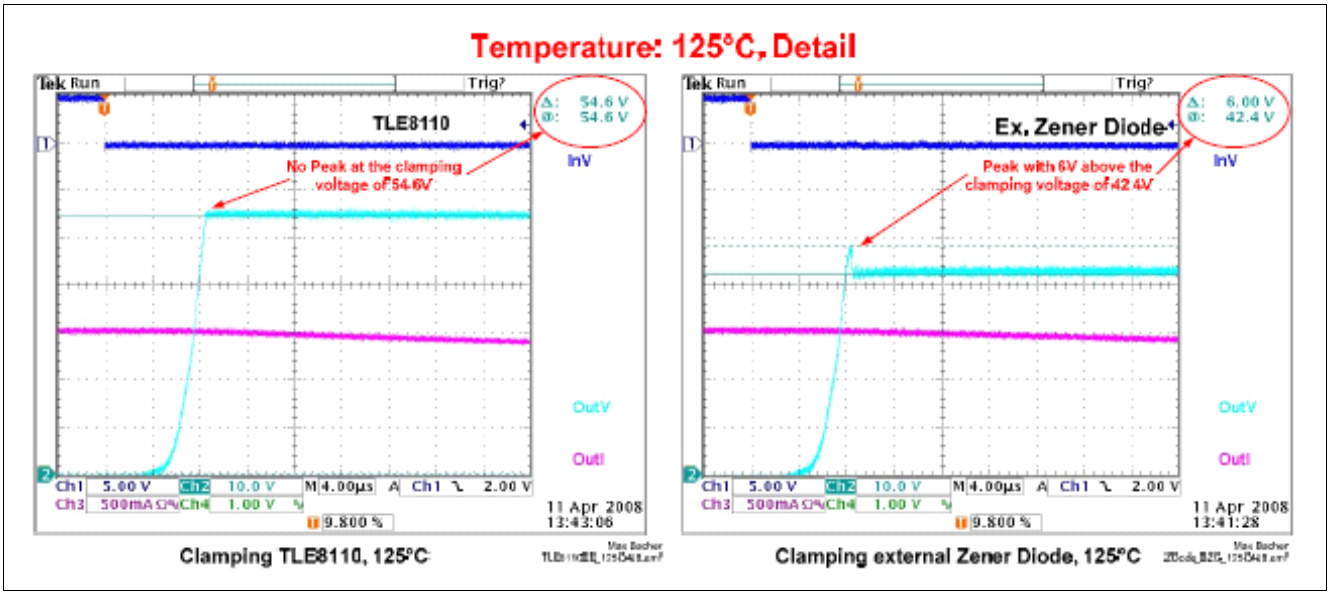

Figure 18 Comparing the voltage peak for internal and external clamping with a Zener diode at 125°C

Figure 19 to **Figure 21** show the clamping behavior with the Zener diode for 150°C. This is the temperature for the TLE8110ED and also for the Zener diode. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

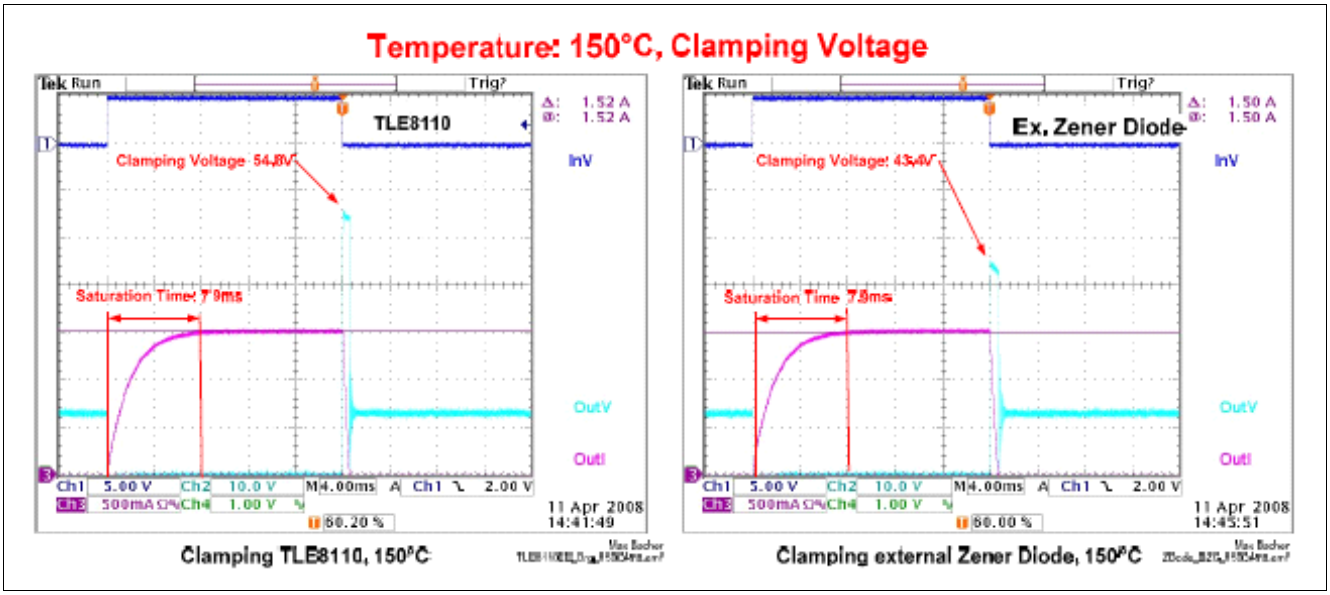

Figure 19 Comparing the clamping voltages for internal and external clamping with a Zener diode at 150°C

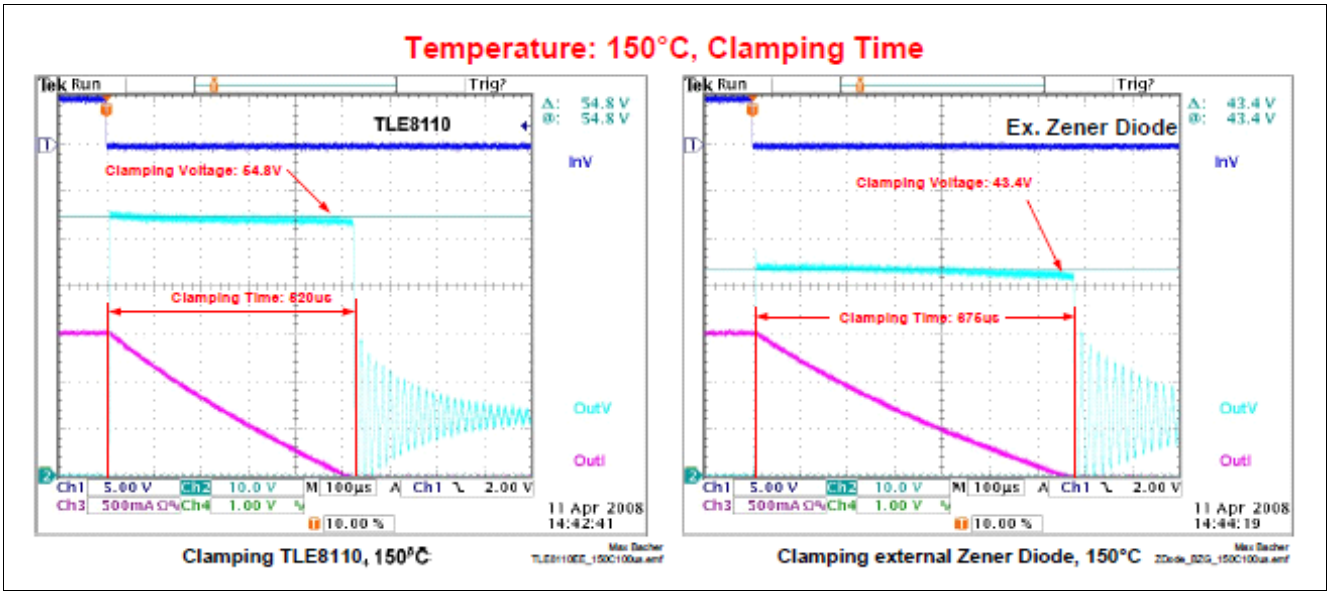

Figure 20 Comparing the clamping time for internal and external clamping with a Zener diode at 150°C

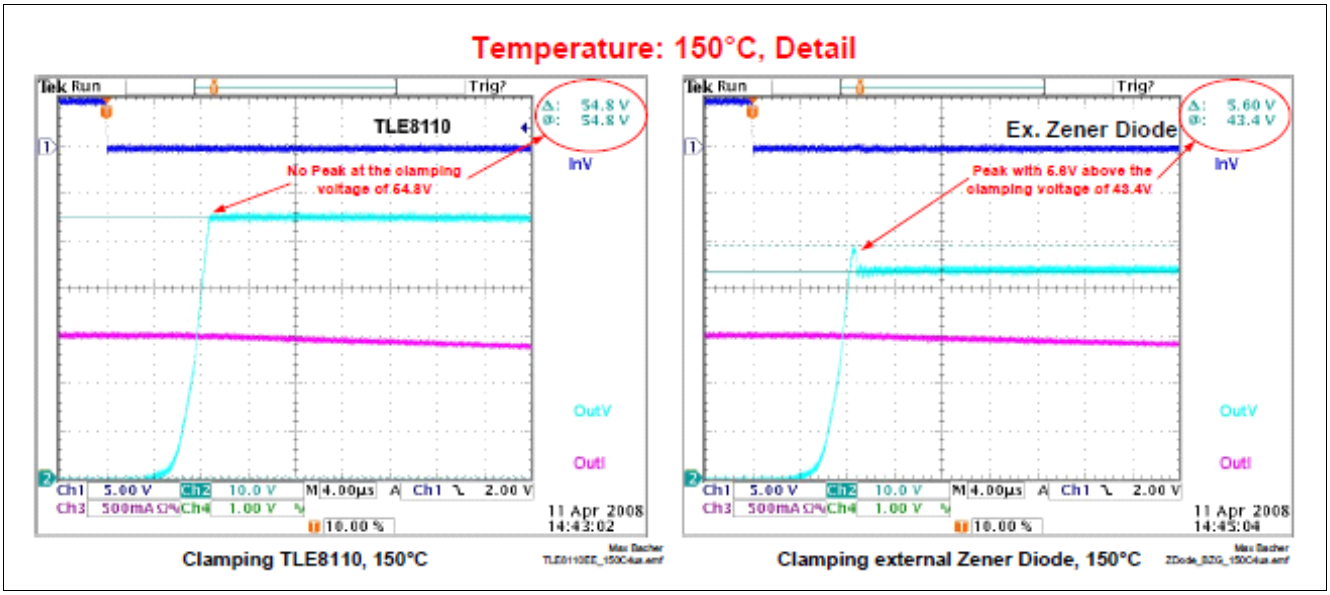

Figure 21 Comparing the voltage peak for internal and external clamping with a Zener diode at 150°C

2.2.3 Conclusion

A temperature-dependant behavior for external clamping with a Zener diode can be observed. **Figure 22** shows the characteristic curve of the used Zener diode at several temperatures. The Zener voltage increases with temperature, but clamping time decreases. There is always a voltage peak for 1 µs with nearly 5.5 V overvoltage when the clamping with Zener diode starts.

The worst behavior with the Zener diode for external clamping is measured at -40°C. With this temperature a clamping voltage in the range of 34.4 V is obtained. This voltage could be a problem with load dump when there is no lower load-dump protection such as additional clamping. Also the clamping time at 880 µs is much longer than the clamping time of the TLE8110ED which is 520 µs.

The use of this circuit is, however, not common. The use of a (Schottky) diode in series to the Zener diode is highly recommended. With this circuit it is possible to avoid problems with reverse currents – just like wrong polarity with the battery. In case of a reverse current, the Zener diode might be destroyed without without the polarity protection of an additional diode.

External Clamping with the TLE8110ED

A Zener diode with nominal 3 A and 39 V was selected to ensure operation is always below the minimum clamping voltage of the TLE8110ED. For the normal operating temperature of 125°C a clamping voltage in the range of 42.5 V is obtained from the 39 V Zener diode. With 150°C a clamping voltage in the range of 43.4 V is obtained - rather near the minimum clamping voltage for the TLE8110ED. For exact values and thresholds for the clamping voltages of the device, please refer to the data sheet of the TLE8110ED. The maximum clamping voltage of the Zener diode must not reach or exceed the minimum clamping voltage of the TLE8110ED. Calculation and comparison of the possible thresholds of the clamping voltages, to avoid destruction of the TLE8110ED through use of a setup which could reach a higher energy than permitted in the data sheet, is strongly recommended.

No distinct temperature-dependant behavior for the TLE8110ED clamping parameters, such as current behavior, clamping time and clamping voltage, was observed.

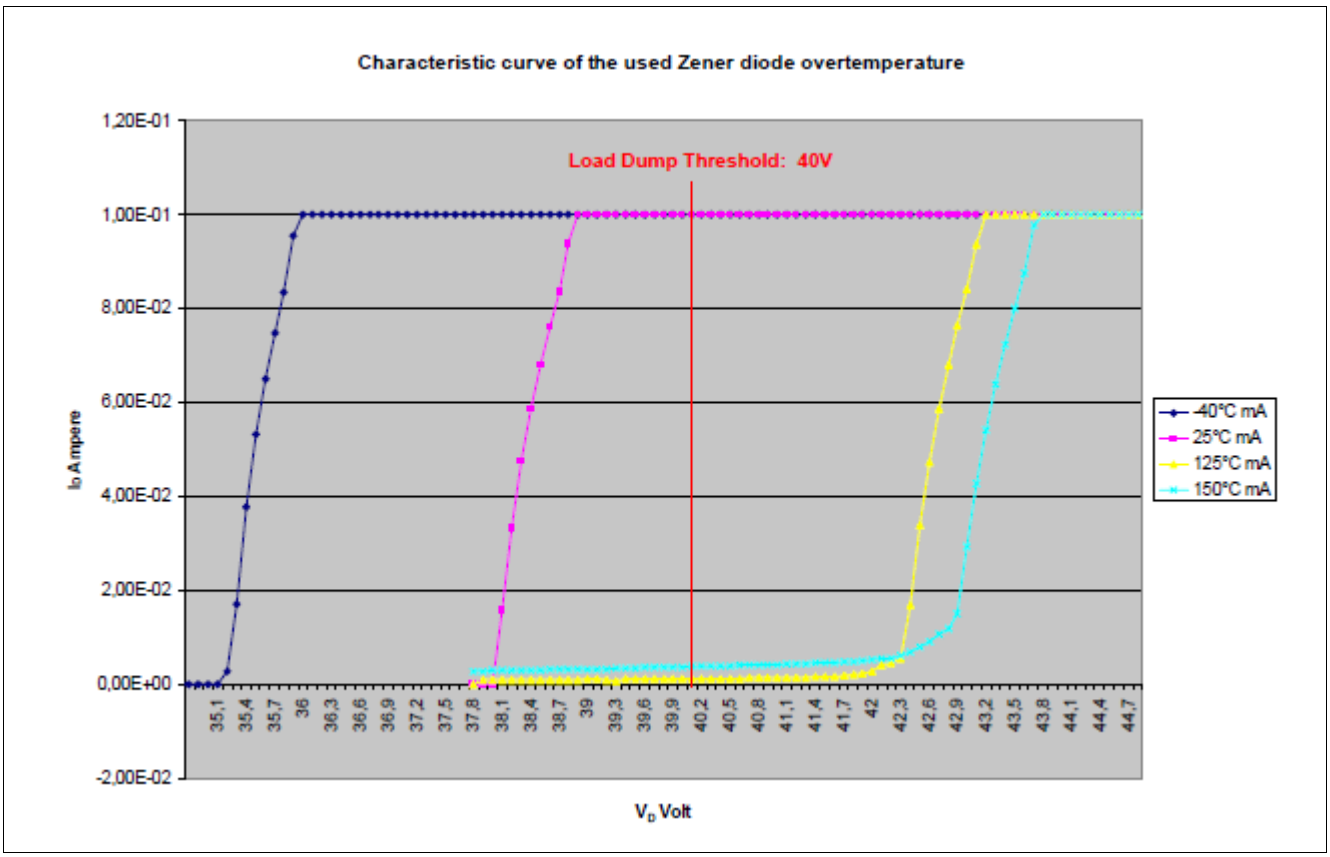

Figure 22 Characteristic curve of the used Zener diode at several temperatures

2.3 External free wheeling diode

2.3.1 Application circuit

Figure 23 shows the circuit of the TLE8110ED with an FWD (**F**ree **W**heeling **D**iode) for external clamping. The signals marked in color in **Figure 23** are plotted in **Figure 24** and **Figure 25** to have a better overview.

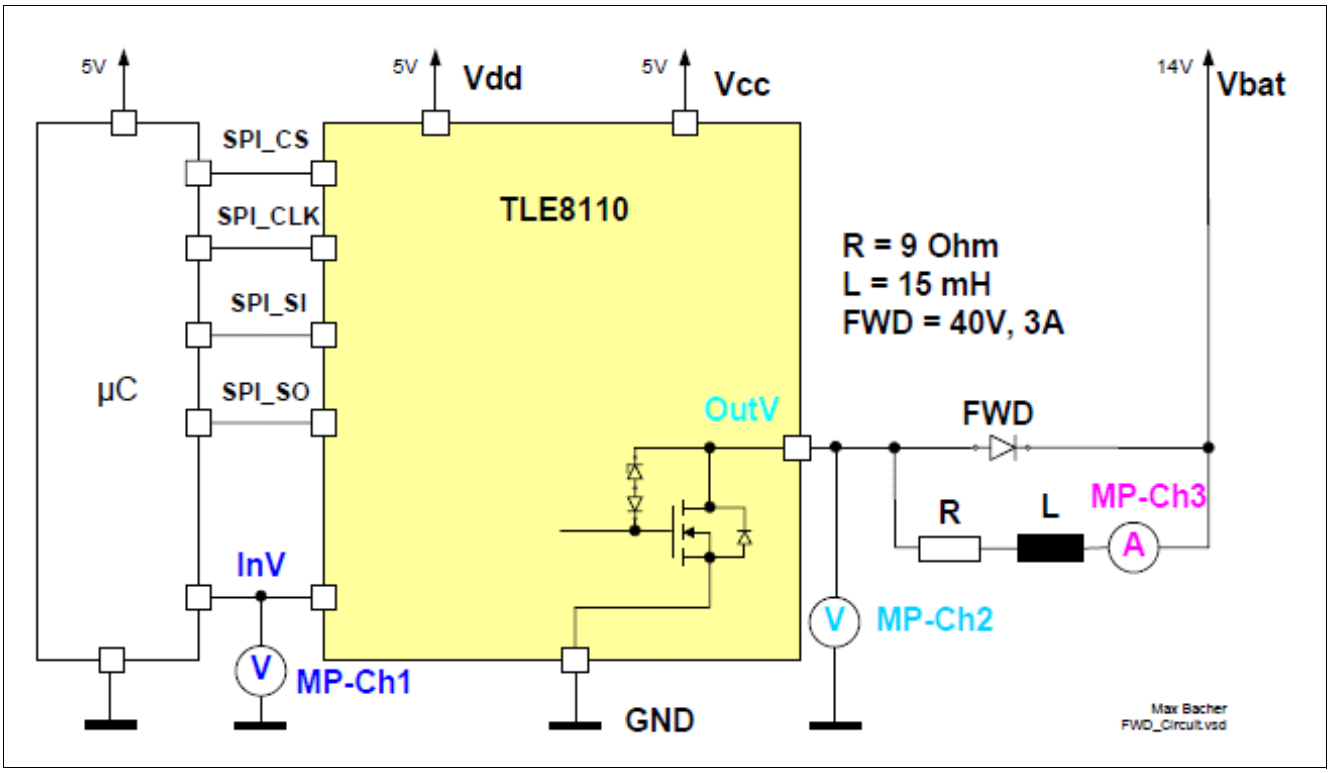

Figure 23 TLE8110ED with an FWD for external clamping

2.3.2 Measurements

Figure 24 and **Figure 25** show the clamping behavior with the FWD for 25°C. This is the temperature for the TLE8110ED and also for the FWD. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

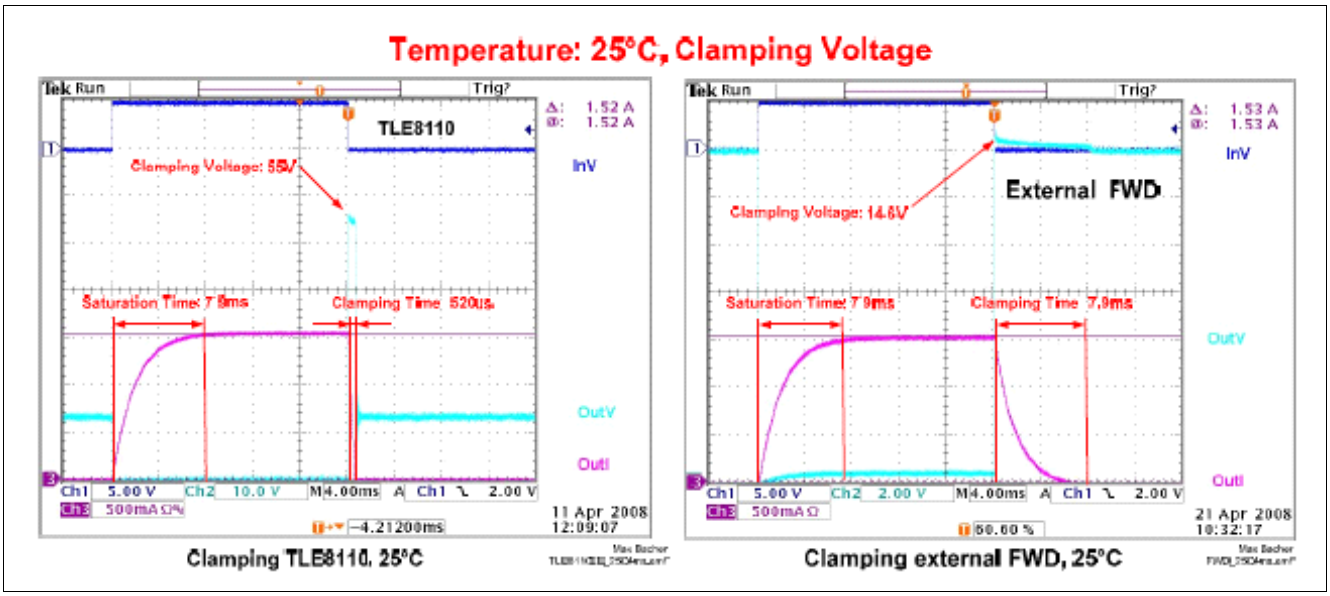

Figure 24 Comparing the clamping voltages for internal and external clamping with an FWD at 25°C

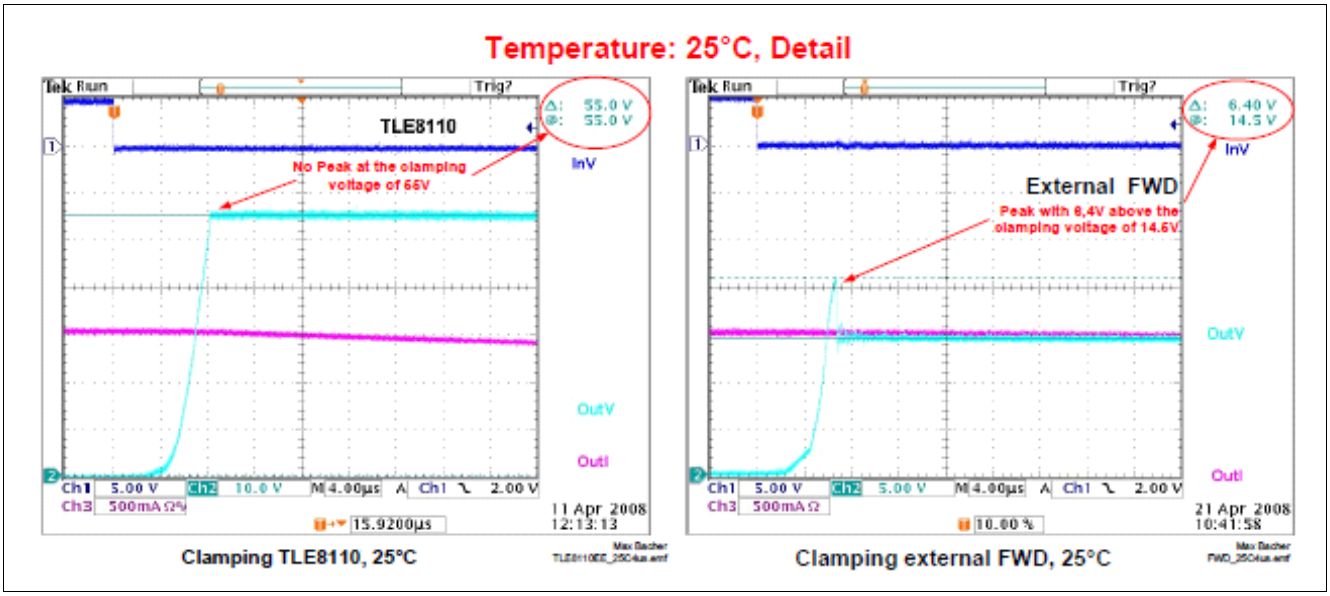

Figure 25 Comparing the voltage peak for internal and external clamping with an FWD at 25°C

2.3.3 Conclusion

With an FWD the expected behavior was observed. A 3 A Schottky diode with a maximum repetitive reverse voltage in the range of 40 V was used. **Figure 26** shows the characteristic curve of this Schottky diode for 25°C and from 0 to 1 A.

The clamping time has increased by an order of magnitude (15 times, to be more exact) compared to the TLE8110ED and is now in the same range as the saturation time. However, the clamping voltage is very small. There is always a voltage peak for 1 µs with nearly 6.5 V overvoltage when the clamping with the FWD starts.

The use of this circuit is, however, not common. In case of a wrong polarity of the battery, there could be a large reverse current which could destroy the devices.

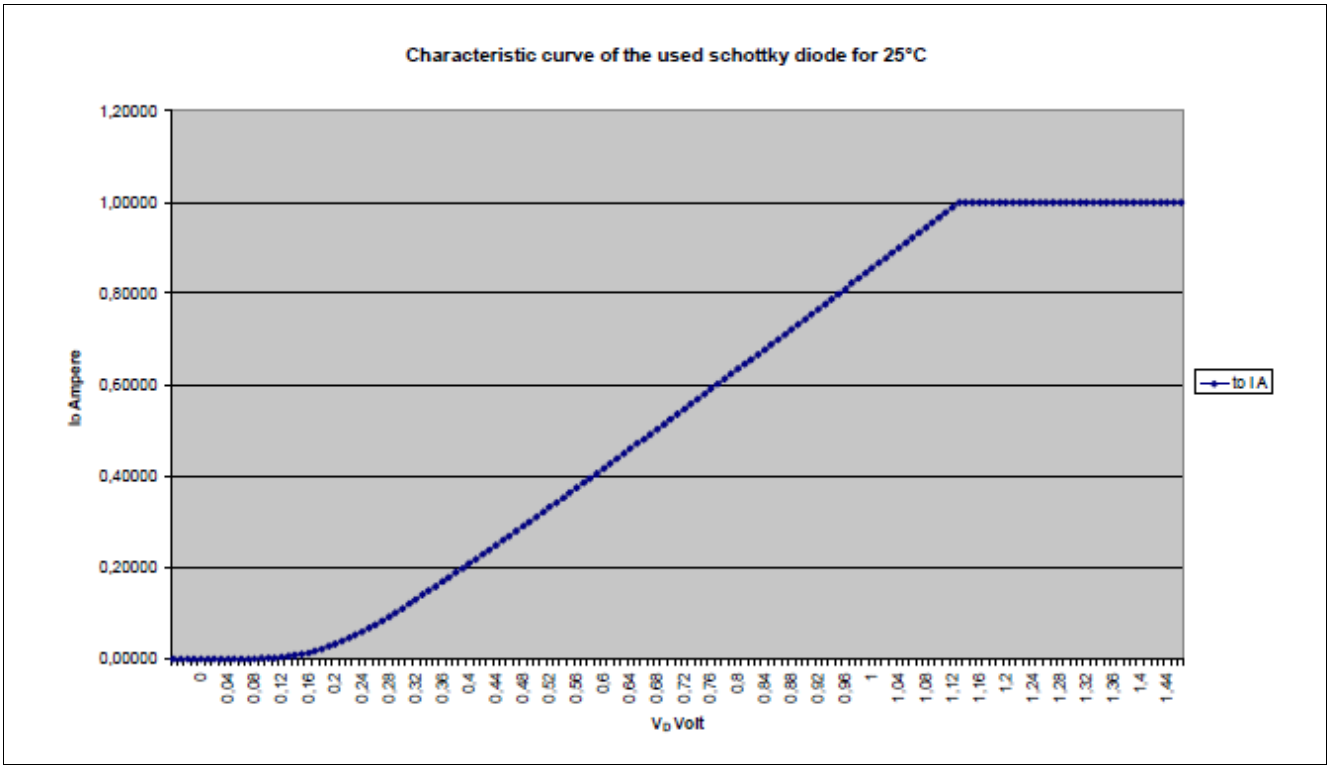

Figure 26 Characteristic curve of the used Schottky diode

2.4 External resistor

2.4.1 Application circuit

Figure 27 shows the circuit of the TLE8110ED with a parallel resistor (Rp) for external clamping. The signals marked in color in **Figure 27** are plotted in **Figure 28** to **Figure 33** to have a better overview.

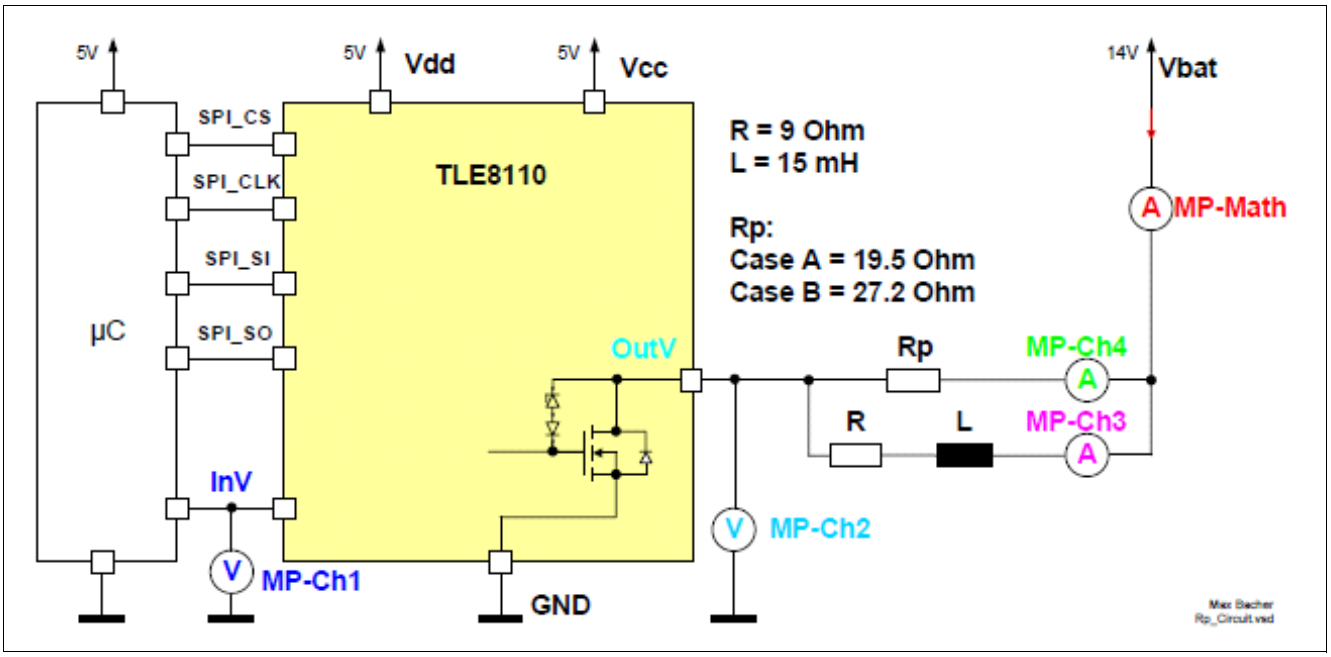

Figure 27 TLE8110ED with a parallel resistor for external clamping

2.4.2 Measurements

Figure 28 to **Figure 30** show the clamping behavior with a parallel resistor of 19.5 Ω at 25°C. This is the temperature for the TLE8110ED and also for Rp. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

The “Math Channel” (the red one) describes the current “MP-Math” in **Figure 27** and is calculated as channel 3 (MP-Ch3 – the load current) plus channel 4 (MP-Ch4 – the Rp current).

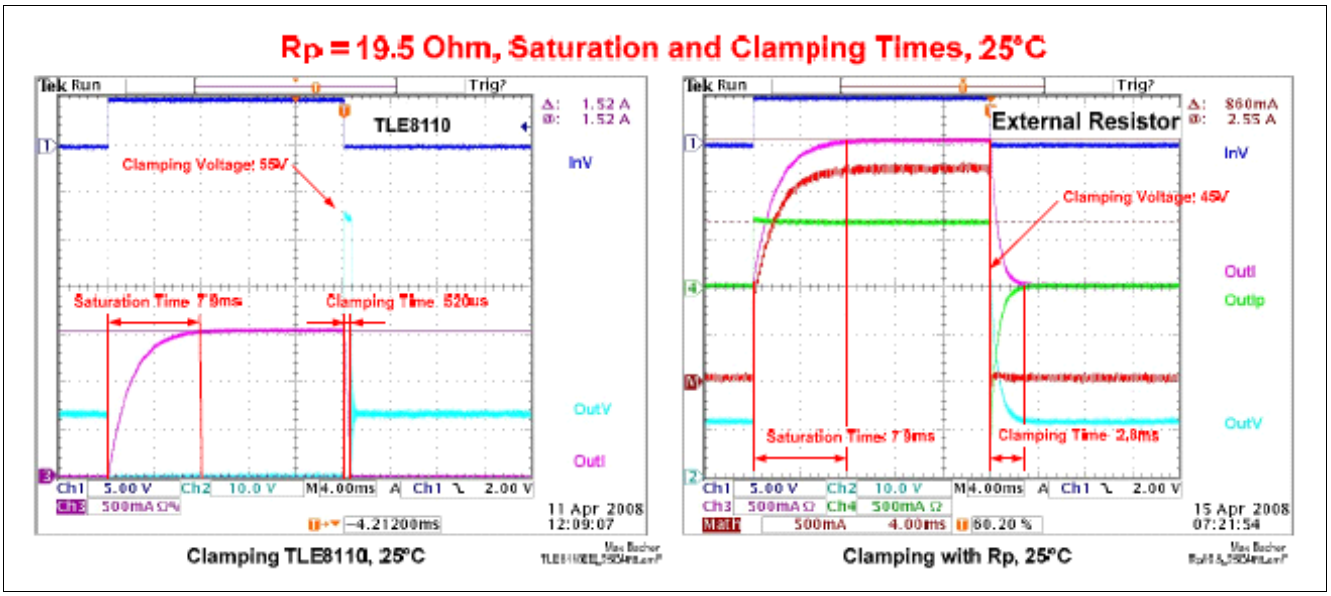

Figure 28 Comparing the clamping time for internal and external clamping with Rp = 19.5 Ω

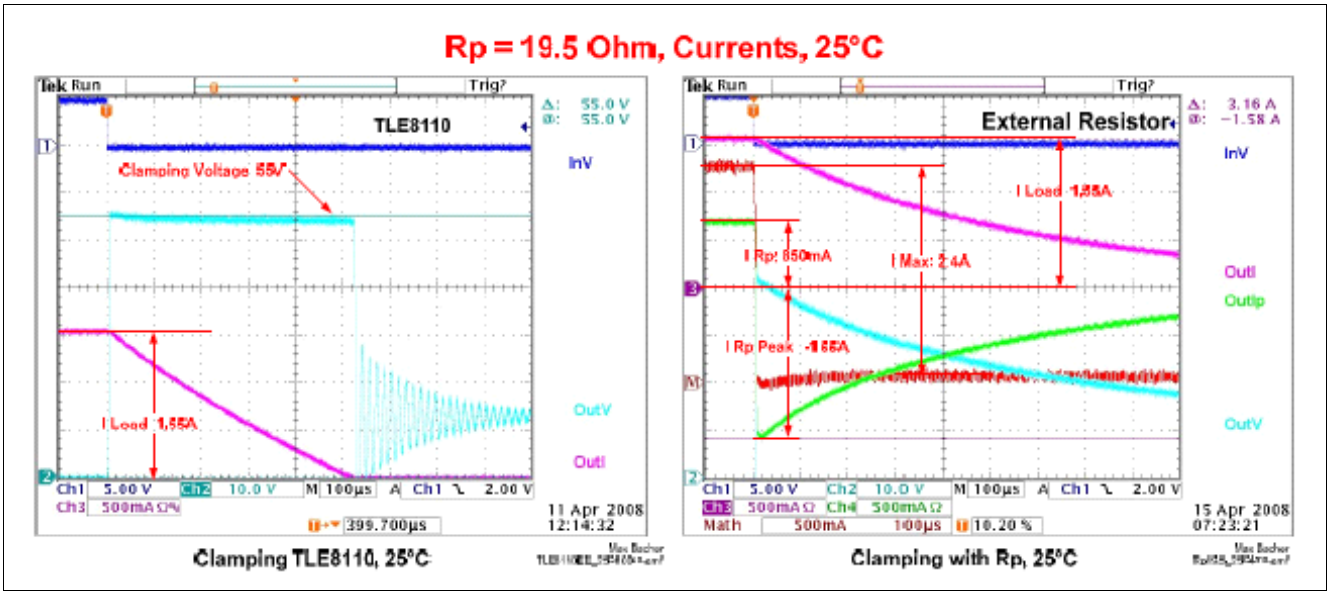

Figure 29 Comparing the currents for internal and external clamping with Rp = 19.5 Ω

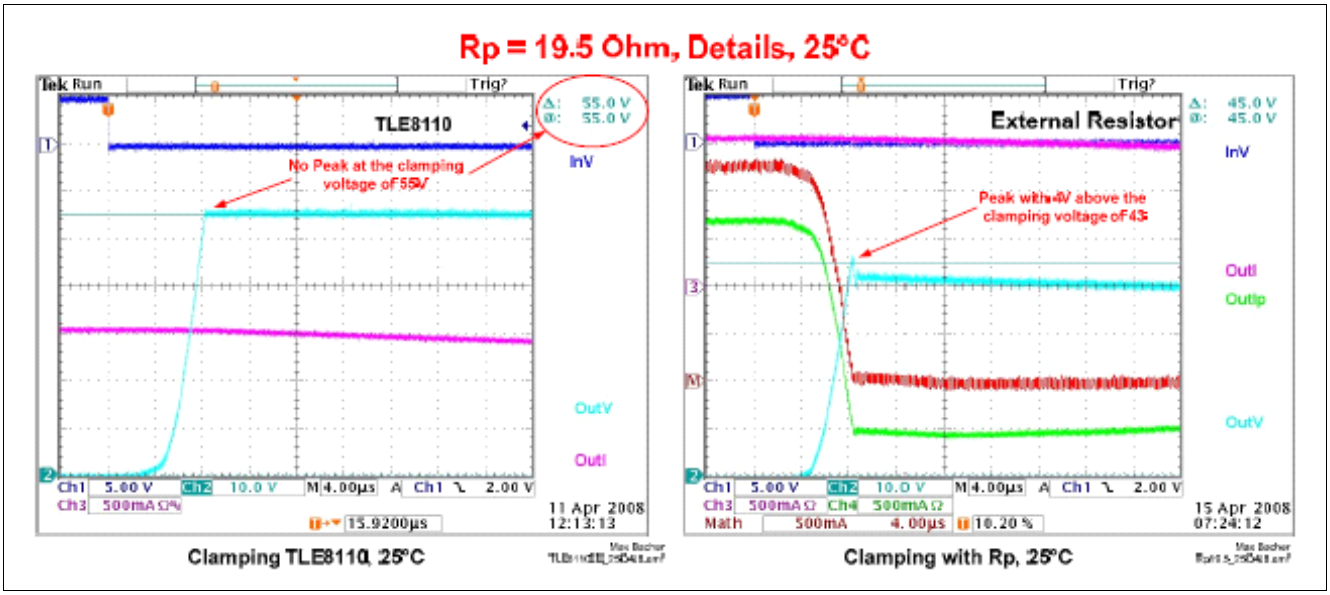

Figure 30 Comparing the voltage peak for internal and external clamping with Rp = 19.5 Ω

Figure 31 to **Figure 33** show the clamping behavior with parallel resistor of 27.2 Ω at 25°C. This is the temperature for the TLE8110ED and also for Rp. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

The “Math Channel” (the red one) describes the current “MP-Math” in **Figure 27** and is calculated as channel 3 (MP-Ch3 – the load current) plus channel 4 (MP-Ch4 – the Rp current).

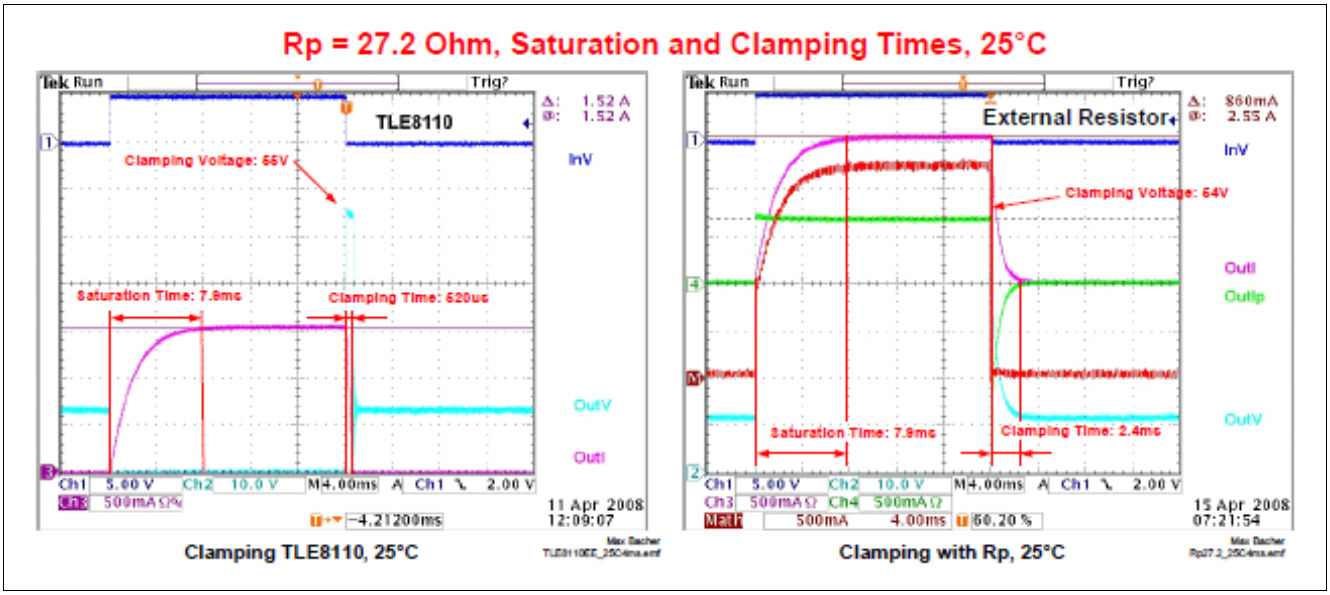

Figure 31 Comparing the clamping time for internal and external clamping with Rp = 27.2 Ω

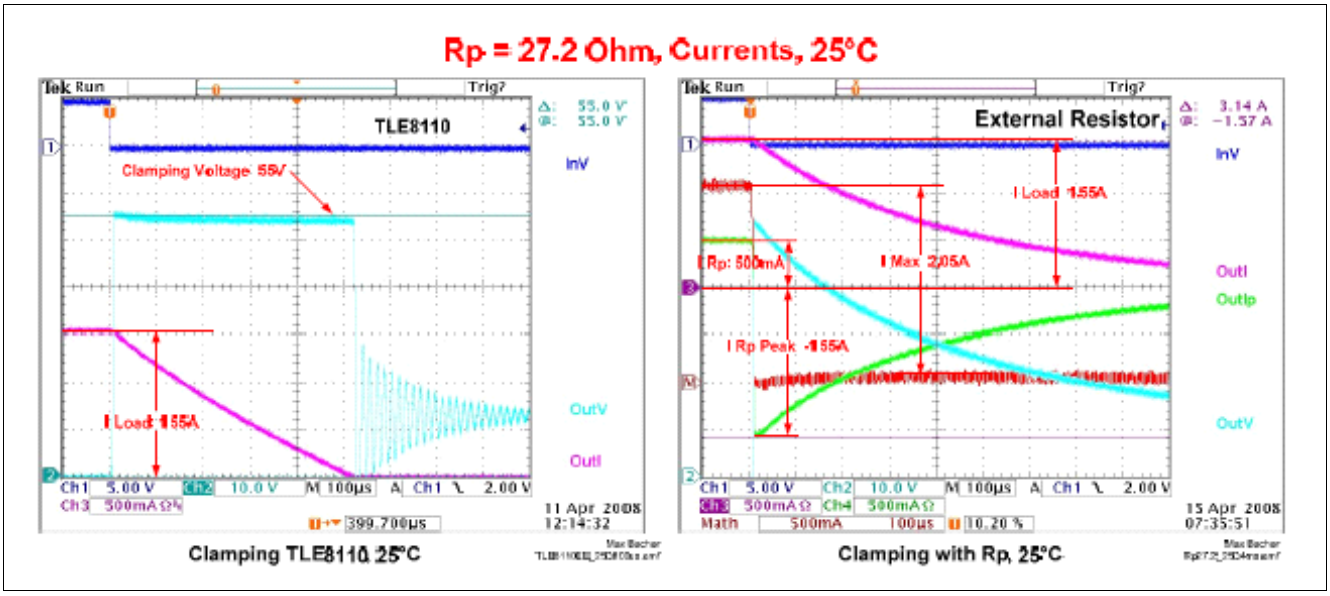

Figure 32 Comparing the currents for internal and external clamping with Rp = 27.2 Ω

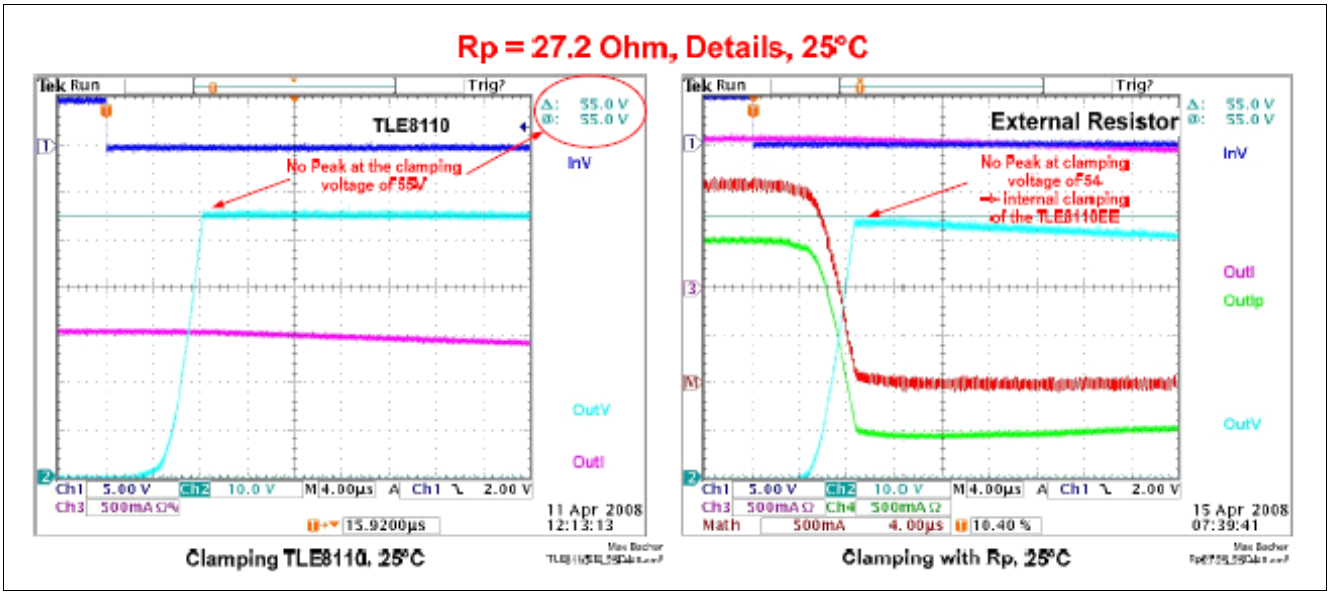

Figure 33 Comparing the voltage peak for internal and external clamping with Rp = 27.2 Ω

2.4.3 Conclusion

The expected behavior with the parallel resistor was observed. The output current for the channel is much higher because there is now the additional current of the parallel resistor. The amount of the additional current depends upon the value of the used parallel resistor and is easy to calculate ($I_L/I_p = R_p/R_L$).

To observe the effects resulting from the presence of different amounts of parallel resistance, the behavior with two different parallel resistors was measured.

The values of the resistors are chosen:

- to be under the minimum clamping voltage of the TLE8110ED. Rp = 19.5 Ω, which causes a clamping voltage of 43 V.
- to be under the typical clamping voltage of the TLE8110ED. Rp = 27.2 Ω, which causes a clamping voltage of 53 V.

Case A (Rp = 19.5 Ω)**:**

The clamping time has significantly increased (5.5 times, to be more exact) compared to the TLE8110ED. The additional current is in the range of 850 mA. A voltage peak for 1 µs with nearly 5 V overvoltage when the clamping with the parallel resistor starts, was observed.

Case B (Rp = 27.2 Ω)**:**

The clamping time has significantly increased (4.5 times, to be more exact) compared to the TLE8110ED. The additional current is in the range of 500 mA. No voltage peak was observed in this case because above 55 V the internal clamping from the TLE8110ED is activated.

2.5 External resistor with free wheeling diode

2.5.1 Application circuit

Figure 34 shows the circuit of the TLE8110ED with a parallel resistor (Rp) and an FWD for external clamping. The signals marked in color in **Figure 34** are plotted in **Figure 35** to **Figure 40** to have a better overview.

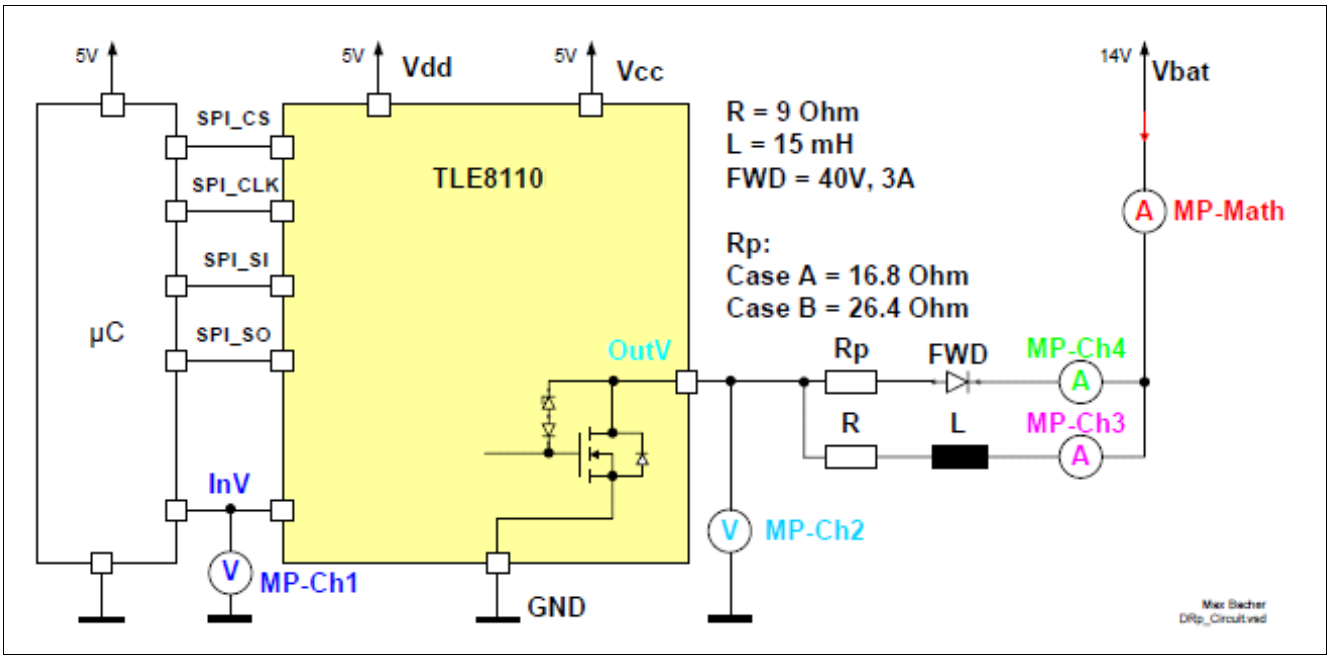

Figure 34 TLE8110ED with an FWD and a parallel resistor (Rp) for external clamping

2.5.2 Measurements

Figure 35 to **Figure 37** show the clamping behavior with a parallel resistor of 16.8 Ω and an FWD at 25°C. This is the temperature for the TLE8110ED and also for the Rp and the FWD. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

The “Math Channel” (the red one) describes the current “MP-Math” in **Figure 34** and is calculated as channel 3 (MP-Ch3 – the load current) plus channel 4 (MP-Ch4 – the FWD-Rp current).

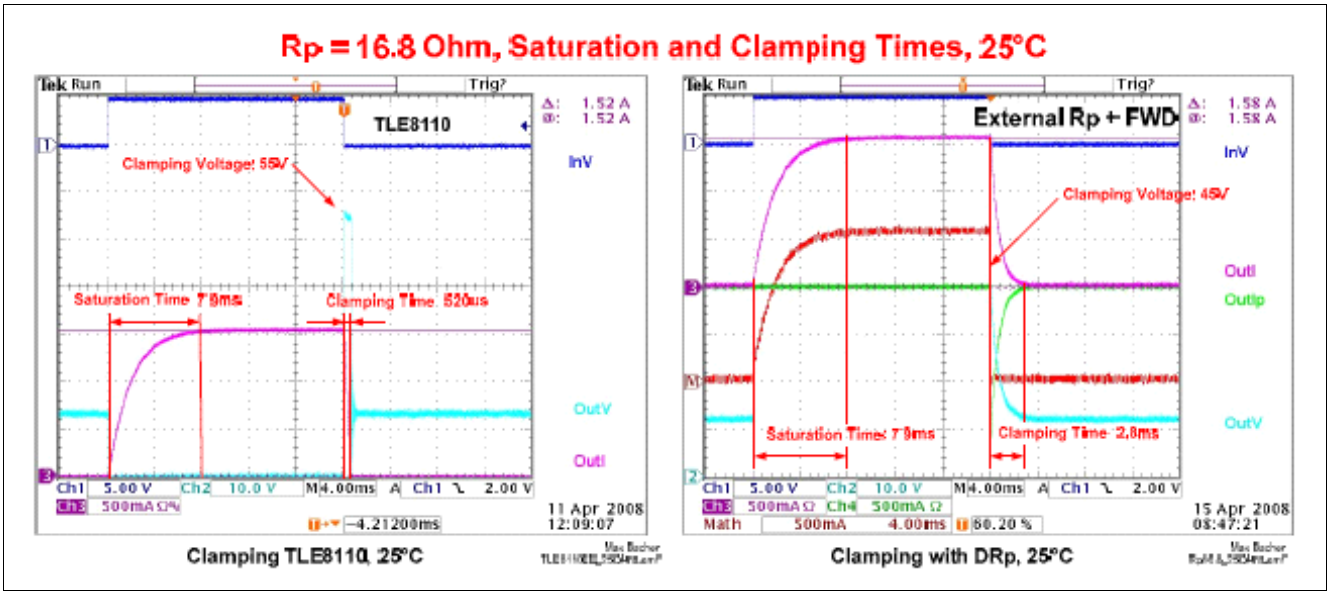

Figure 35 Comparing the clamping time for internal and external clamping with an FWD and Rp = 16.8 Ω

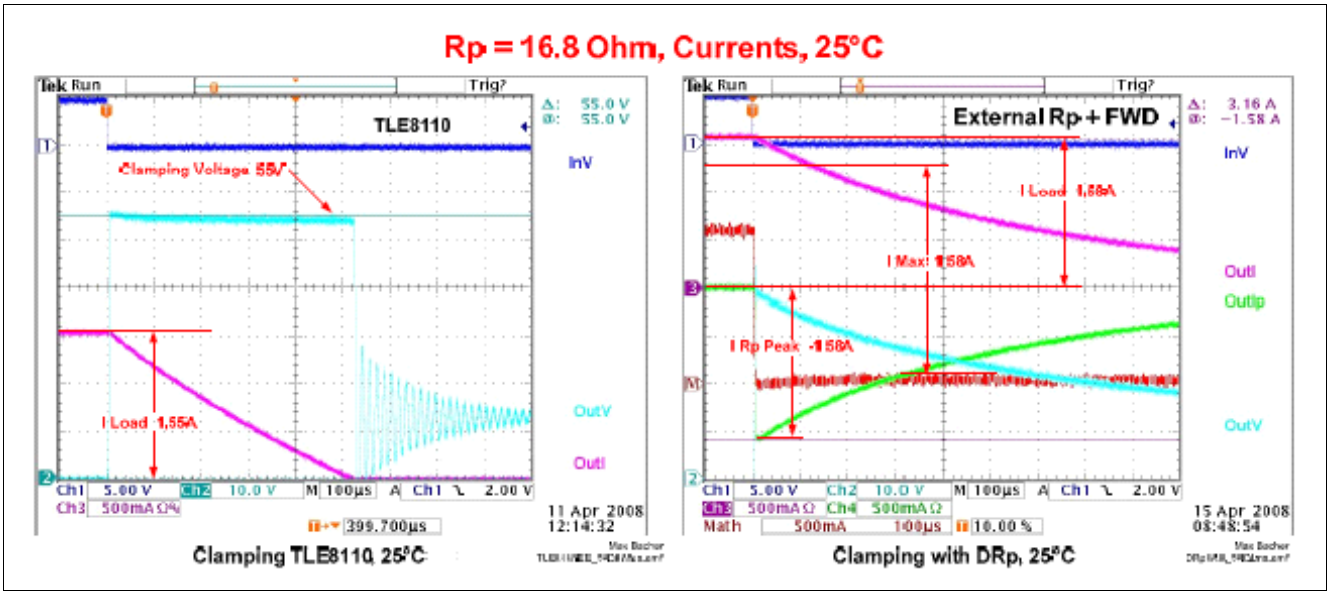

Figure 36 Comparing the currents for internal and external clamping with an FWD and Rp = 16.8 Ω

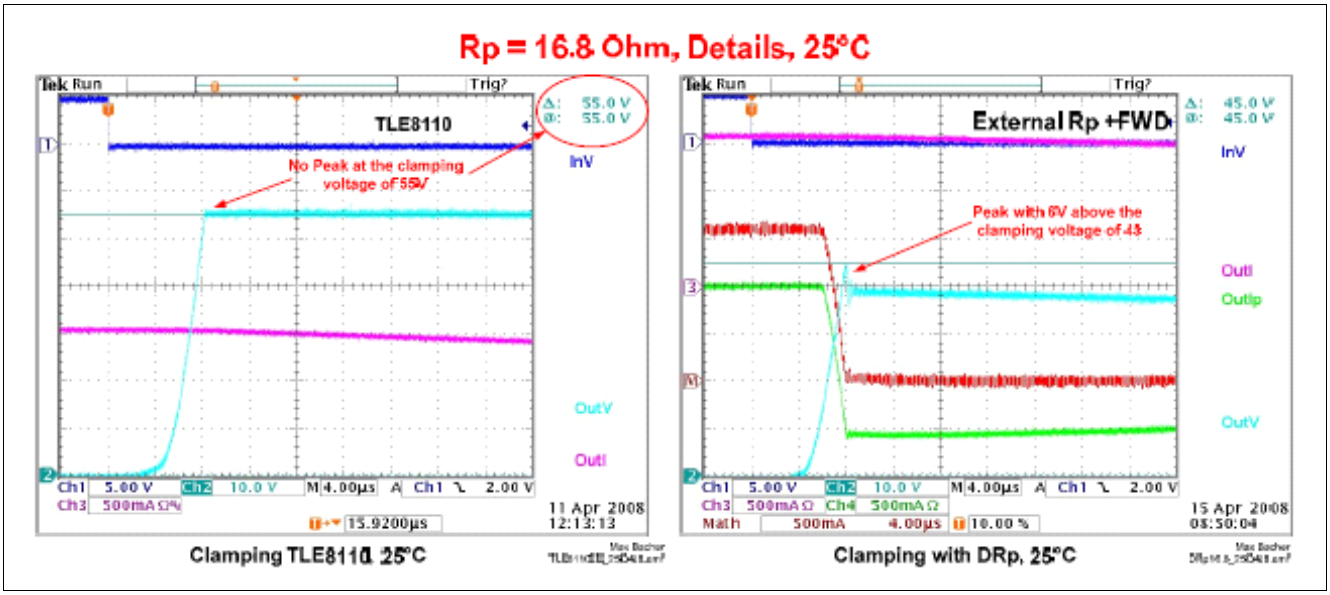

Figure 37 Comparing the voltage peak for internal and external clamping with an FWD and Rp = 16.8 Ω

Figure 38 to **Figure 40** show the clamping behavior with a parallel resistor of 26.4 Ω and an FWD at 25°C. This is the temperature for the TLE8110ED and also for the Rp and the FWD. The figures always show the comparisons with the original TLE8110ED clamping. The setup and the load are always the basic setup shown in **Chapter 2.1.1**.

The “Math Channel” (the red one) describes the current “MP-Math” in **Figure 34** and is calculated as channel 3 (MP-Ch3 – the load current) plus channel 4 (MP-Ch4 – the FWD-Rp current).

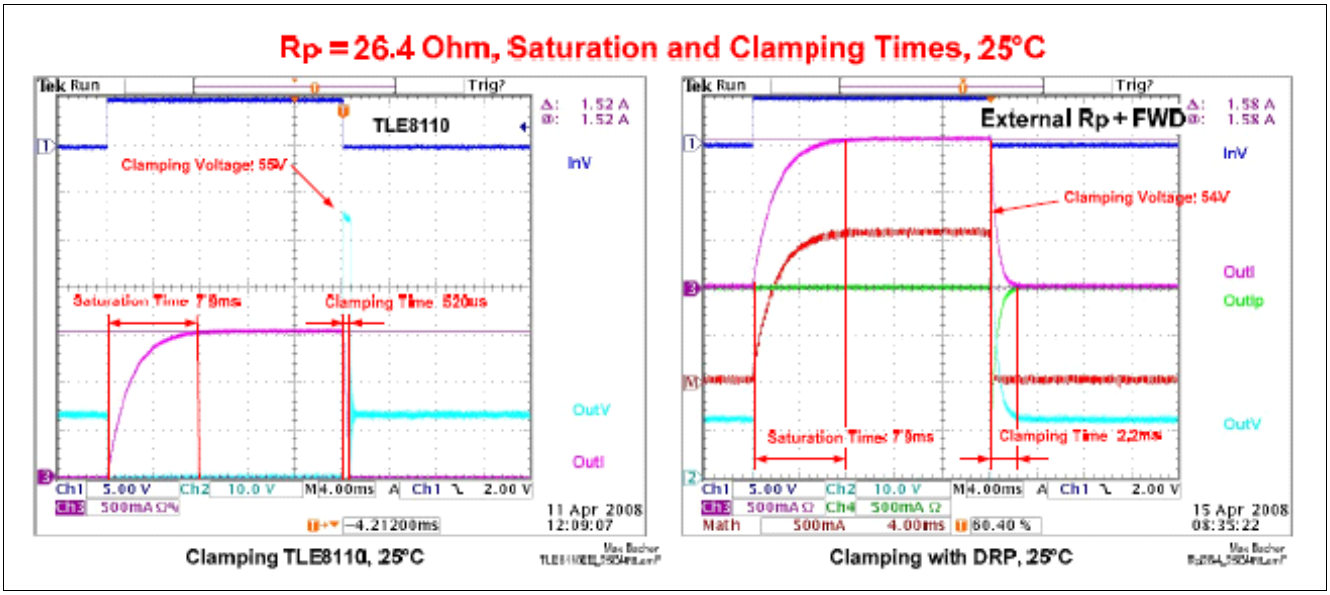

Figure 38 Comparing the clamping time for internal and external clamping with an FWD and Rp = 26.4 Ω

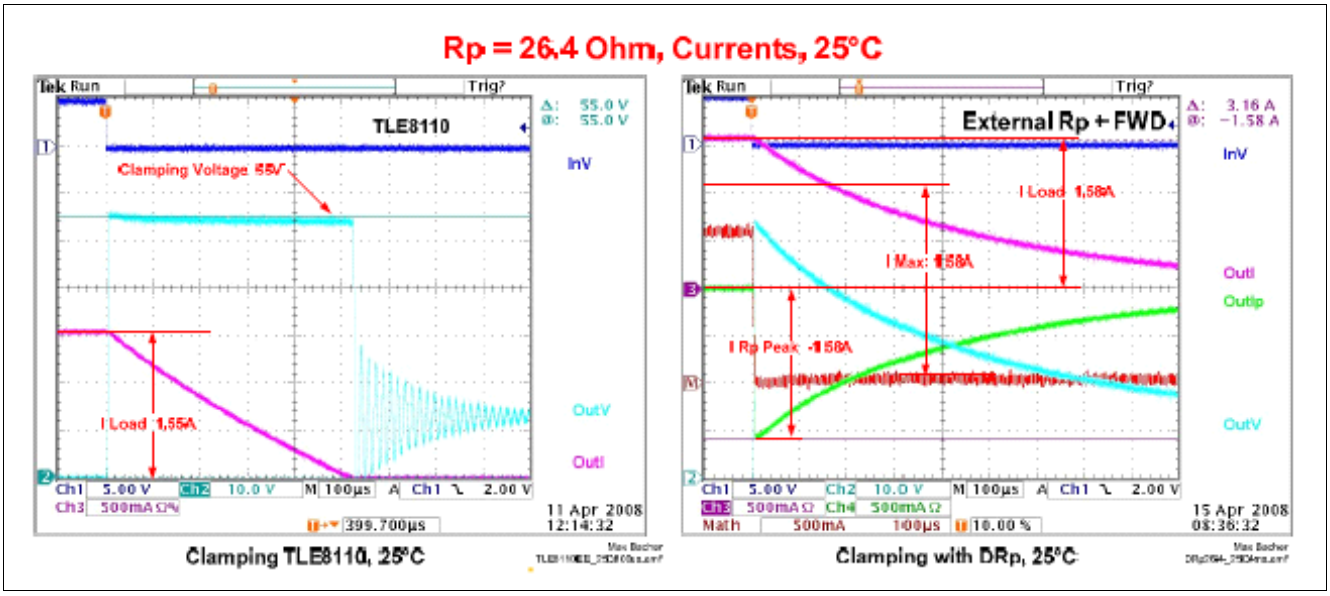

Figure 39 Comparing the currents for internal and external clamping with an FWD and Rp = 26.4 Ω

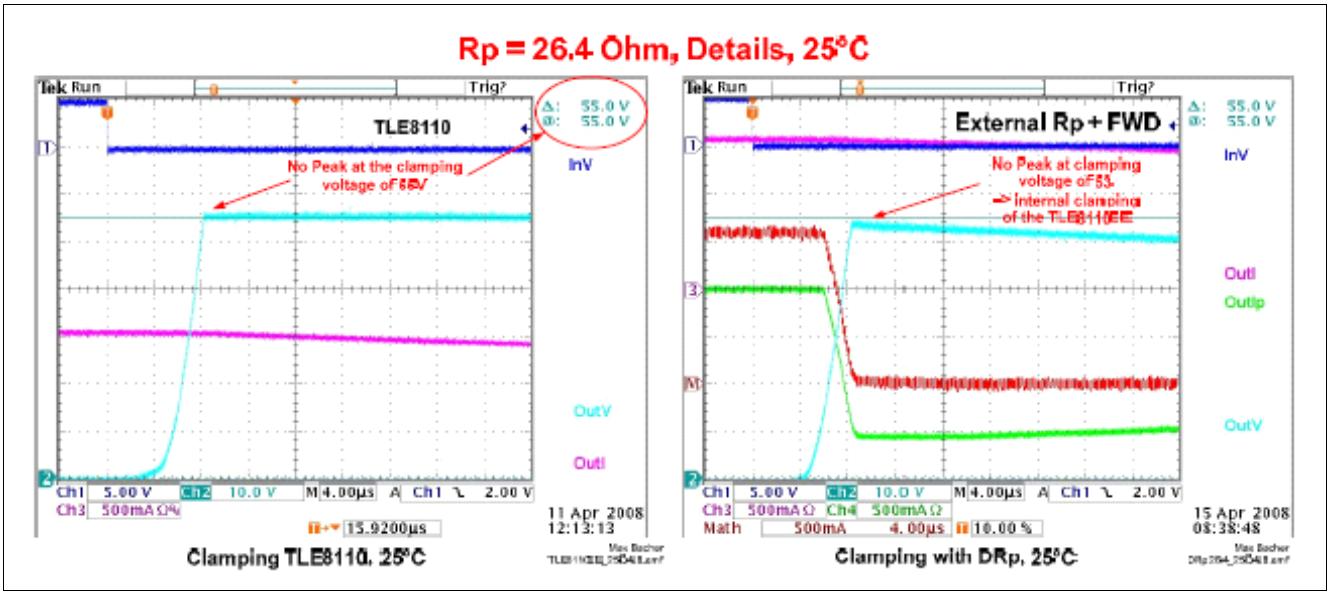

Figure 40 Comparing the voltage peak for internal and external clamping with an FWD and Rp = 26.4 Ω

2.5.3 Conclusion

The expected behavior with the parallel resistor and the FWD was observed. The big advantage against the external Rp clamping without an FWD is that there is now no additional current when the output is switched on. The other effect (longer clamping time) is still apparent. To observe the effects resulting from the presence of different amounts of parallel resistance, the behavior with two different parallel resistors was measured.

The values of the resistors are chosen:

- to be under the minimum clamping voltage of the TLE8110ED. Rp = 16.8 Ω, which causes a clamping voltage of 43 V.
- to be under the typical clamping voltage of the TLE8110ED. Rp = 26.4 Ω, which causes a clamping voltage of 53 V.

Case A (Rp = 16.8 Ω)**:**

The clamping time has significantly increased (5.5 times, to be more exact) compared to the TLE8110ED. A voltage peak for 1 µs with nearly 5 V overvoltage when the clamping with the parallel resistor starts, was observed.

Case B (Rp = 24.4 Ω)**:**

The clamping time has significantly increased (4 times, to be more exact) compared to the TLE8110ED. No voltage peak was observed in this case because above 55 V the internal clamping from the TLE8110ED is activated.

3 Additional Information

- Existing Application Notes:
  - SPI interface and use in a daisy-chain bus configuration
  - How to drive a unipolar stepper motor with the TLE8110ED
  - Switching Inductive Loads
- For further information you may contact **http://www.infineon.com/**

4 Revision History

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