Application note TLE4999Cx

Master nibble low time parameter and related tolerances

About this document

Scope and purpose

This application note is dedicated to the settings of the master nibble low time, that allow the correct triggering of the TLE4999Cx sensor.

Intended audience

This application note is intended for anyone who would like to use the TLE4999Cx in their application.

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1 Introduction

The triggering of sensors is a crucial task in nowadays applications consisting of sensors, signal processing units and actors.

One interface allowing sensor triggering is the Short PWM Code (SPC) interface. This interface is based on an extension to the SAE 2716 SENT Interface, which is encoding the transmitted data into nibbles.

Each of these nibbles is composed on a basic timing, which are called Unit Times. Sensor triggering is achieved by pulling the sensor interface line to low state for a certain amount of time and releasing the bus line.

The triggering functionality of the interface is sub-divided in a single sensor mode (synchronous mode/ bus mode off) and a multi-sensor mode (bus mode) depending on the system setup.

To allow very fast triggering with a single sensor configuration, the trigger pulse in this mode is very short so is does not introduce any additional delay. In bus mode, the triggering of the different sensors is based on introducing a constant length trigger pulse and differentiating the sensor addresses by modifying the low/high ratio of the trigger pulse.

2 Master nibble low time

To achieve correct triggering of the sensor, the system has to make a system tolerance computation to see that the trigger window for a correct trigger detection in the sensor is always achieved.

The triggering circuit typically consists of an open drain transistor which pulls the bus line to low state for a specified time controlled by a microcontroller.

For single sensor systems, this trigger low time is selected very short to have short delay of the trigger. The low time for a sensor is from 2 to 7 UT where the total trigger time is 13 UT.

In Bus mode, the total trigger length is fixed to 90UT where the address decoding is done with respect to the low time of the trigger pulse according to a logarithmic scale.

The master low times for the sensor are specified in **Table 1**

Table 1 SPC trigger parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Master nibble low time	t_{mlow}	2	–	7	UT	Bus mode off
Master nibble low time	t_{mlow}	8	–	15	UT	Bus mode on, ID = 0
Master nibble low time	t_{mlow}	16	–	28	UT	Bus mode on, ID = 1
Master nibble low time	t_{mlow}	29	–	49	UT	Bus mode on, ID = 2
Master nibble low time	t_{mlow}	50	–	82	UT	Bus mode on, ID = 3

This sensor detection window has to be hit by the ECU/Microcontroller trigger pulse. However, this generation of the transmitter pulse is subject to many parameters, which are narrowing down the detectability of the trigger by the sensor.

The contributors to this variation of the trigger master low time are as follows:

- *A:* External component accuracy
- *B:* Input trigger threshold level
- *C:* Asynchronous clock of receiver and transmitter

2.1 Calculation of the master nibble low time (ECU side)

This application note describes the calculation and analysis of the master nibble low time which is needed at the ECU side to address the sensor correctly.

A typical application circuit is shown on **Figure 1**

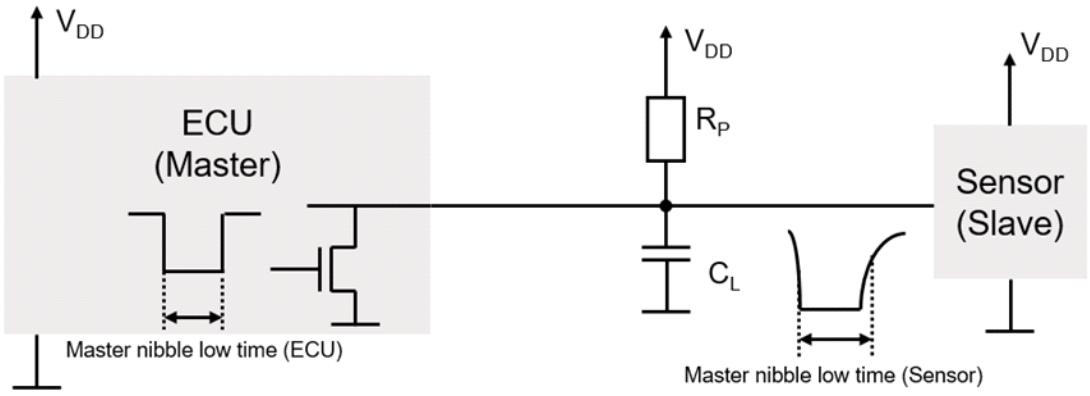

Figure 1 Application circuit

The ECU (Master) ideally generates a rectangular pulse to address and trigger the sensor.

With the output driver included in the ECU, usually only a pull down of the sensor line can be achieved. This means, the falling edge on the bus line is very fast but the release of the line is dominated by the RC time constant of the external circuitry. This implies, to the master nibble low time generated at the transmitter side, that an extra delay has to be added to determine the low time received at the sensor input.

On top of this delay, the application circuit external components have tolerances, these tolerances must also be considered in the system design (Influence A).

Furthermore, the input architecture of the sensor is starting a counter with the detection of the falling edge on the bus line. This counter is then stopped when the input reaches the high level again. However, this detection of the high level strongly depends on the detection threshold levels of the input Schmitt Trigger detection circuitry.

Due to process variations the detection threshold can vary between the upper and lower tolerance limits, and are listed in the **Table 2** (Influence B).

Table 2 Detection threshold

	Lower limit (% of V_{DD})	Nominal (% of V_{DD})	Upper limit (% of V_{DD})
Detection threshold high level	30	50	70
Detection threshold low level	10	30	50

Depending on the clock of the sensor, the counter that is used to count the trigger pulse unit times may not match to the clock of the master, which also introduces an error (Influence C). Due to the architecture of the master/slave system where the sensors response consists of a synchronization pulse which is explicitly denominated to an adjustment of the masters clock to adjust to the sensor Influence C is not further considered in this document.

Master nibble low time

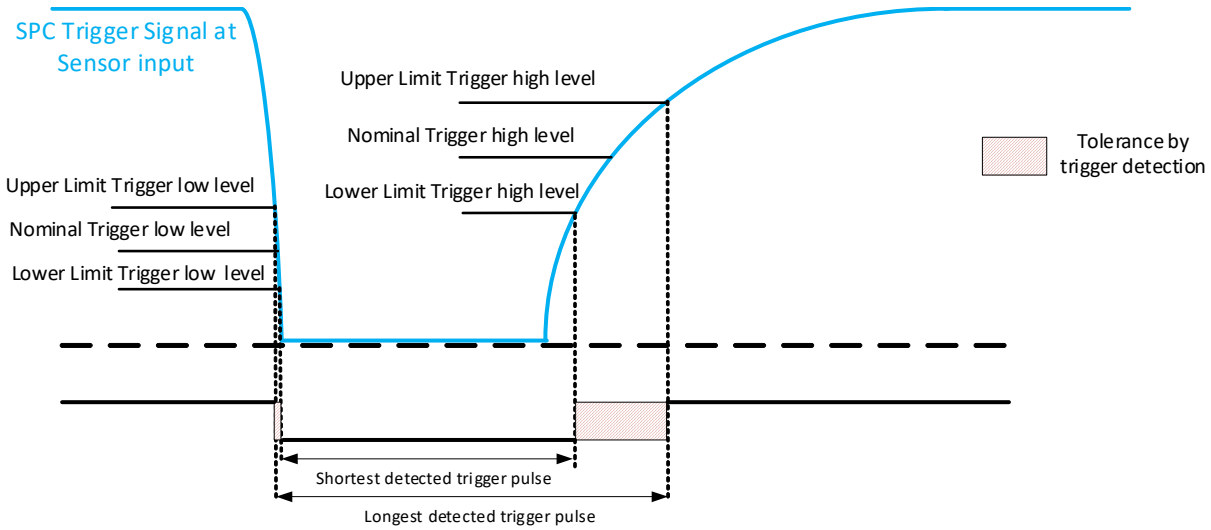

Figure 2 SPC trigger signal

The remaining tolerances need to be taken into account for a robust bus design. In this application note we present a tool where these external tolerances can be computed and considered in the system design. We will see, that even in some cases special combinations of C_L and R_P may prevent the use of some master low times due to increased output rise time.

3 Tolerance Calculator

To analyze the tolerances of a SPC System implementation Infineon generated an Excel spreadsheet (Krall & Lanschuetzer, 2019), see **References**.

On the left hand side of this Excel (see **Figure 3**), the user can configure the parameters of the system.

ECU Master nibble Low time	45	UT
Unit Time	1	µs
Bus Voltage	5	V
External Circuitry		
R	2700	Ohm
C	2,2	nF
Tolerance R	1	%
Tolerance C	10	%
Detector Threshold	60	%
Delay Adder (Tolerances)	6,1	µs
Delay Adder (Nominal)	4,2	µs
Total Master Nibble Low Time (Tolerances) at Sensor		
	51,1	µs
	51,10	UT
Total Master Nibble Low Time (Nominal) at Sensor		
	49,2	µs
	49,20	UT

Figure 3 Tolerance calculator

At the top, the ECU master nibble low time in Unit Times can be selected. Furthermore, the Unit Time can be entered to be able to compute the exact timing.

Then the external circuitry with its tolerances can be entered. The tool also makes a worst case computation with the specified tolerances based on the quality of the used components (i.e. +/-1% or +/-10%). In this computation it considers the tolerances such that the most delay is encountered. Also the detection threshold can be adjusted in a percentage of V_{DD}. With all this information the tool computes a worst case delay of the master nibble low time which has to be added to obtain the slave nibble low time and a nominal delay of the slave nibble low time. Both times are shown in UT and microseconds, see **Figure 4**.

On the right hand side of the interpretation of the slave for the nibble low time is shown where a user can immediately see, with the selected parameters what the sensor is doing.

Examples

Tolerances Consideration						
		min.	max.		min.	max.
0	Synchronous Mode	2	7	UT	2	7 µs
	Bus Mode					
0	Address 0	8	15	UT	8	15 µs
0	Address 1	16	28	UT	16	28 µs
0	Address 2	29	49	UT	29	49 µs
1	Address 3	50	82	UT	50	82 µs

Nominal Consideration						
		min.	max.		min.	max.
0	Synchronous Mode	2	7	UT	2	7 µs
	Bus Mode					
0	Address 0	8	15	UT	8	15 µs
0	Address 1	16	28	UT	16	28 µs
0	Address 2	29	49	UT	29	49 µs
0	Address 3	50	82	UT	50	82 µs

Figure 4 Calculation result

In the current example the master nibble low time is selected as such, that the nominal consideration results in no correct address decoding of the sensor. If the worst case is considered, Address 3 is considered (see **Figure 4**), which may be not desired because the selection of 45 UT for the master nibble low time may be interpreted as Address 2 for the bus system. To see the effect of the external circuitry and threshold tolerances, one may tune the ECU master nibble low time such that even in the worst case the sensor is reliably triggered.

4 Examples

In the following chapter, three examples are shown to explain how to use this tolerance calculator .

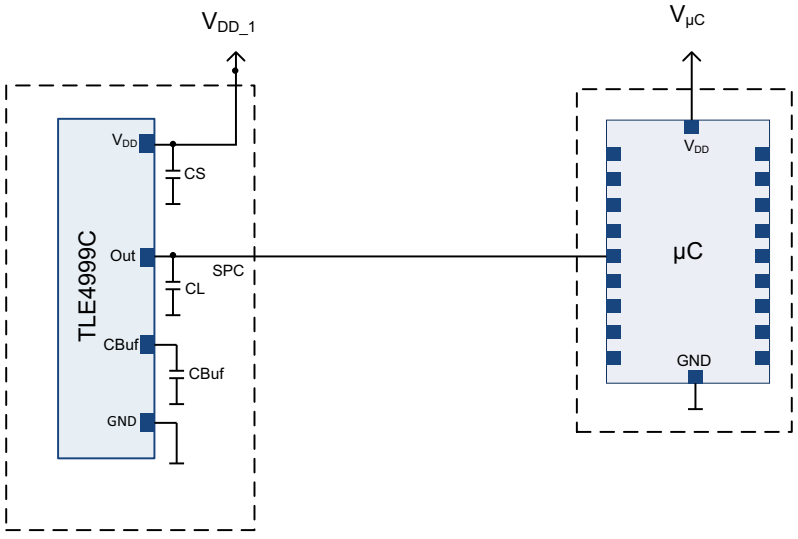

Figure 5 Application circuit

Examples

4.1 Example 1

Application circuit:

C_L=3.9nF (±10%); R_P=2k2(±1%), UT = 3µs

Supply voltage V_{DD}: 5V (±5%); C_{Buf}=68nF (±10%); C_S=100nF (±10%)

ECU master nibble low time for different ID's is give in **Table 3**

Table 3 SPC trigger parameters

Parameter	Symbol	Values				Unit	Note or Test Condition
		Min.	Max.	Min.	Max.		
Master nibble low time	t_{mlow}	1[1)]	3.9	1[1)]	4.87	UT	Bus mode off
Master nibble low time	t_{mlow}	4.93	11.93	5.87	12.87	UT	Bus mode on, ID = 0
Master nibble low time	t_{mlow}	12.93	24.93	13.87	25.87	UT	Bus mode on, ID = 1
Master nibble low time	t_{mlow}	25.93	45.93	26.87	47.87	UT	Bus mode on, ID = 2
Master nibble low time	t_{mlow}	46.93	78.93	47.87	79.87	UT	Bus mode on, ID = 3
		Worst case consideration		Nominal consideration			

1) Theoretically the value would be smaller than 1 UT but this is not realistic

4.2 Example 2

Application circuit:

C_L=2.2nF (±10%); R_P=2k2(±1%), UT = 1.5µs

Supply voltage V_{DD}: 5V (±5%); C_{Buf}=68nF (±10%); C_S=100nF (±10%)

ECU master nibble low time for different ID's is given **Table 4**

Table 4 SPC trigger parameters

Parameter	Symbol	Values				Unit	Note or Test Condition
		Min.	Max.	Min.	Max.		
Master nibble low time	t_{mlow}	1[1)]	3.49	1[1)]	4.56	UT	Bus mode off
Master nibble low time	t_{mlow}	4.49	11.49	5.56	12.56	UT	Bus mode on, ID = 0
Master nibble low time	t_{mlow}	12.49	24.49	13.56	25.56	UT	Bus mode on, ID = 1
Master nibble low time	t_{mlow}	25.49	45.49	26.56	47.56	UT	Bus mode on, ID = 2
Master nibble low time	t_{mlow}	46.49	78.49	47.56	79.56	UT	Bus mode on, ID = 3
		Worst case consideration		Nominal consideration			

1) Theoretically the value would be smaller than 1 UT but this is not realistic

4.3 Example 3

Application circuit:

C_L=1nF (±10%); R_P=2k2 (±1%), UT = 1µs

Supply voltage V_{DD}: 5V (±5%); C_{Buf}=68nF (±10%); C_S=100nF (±10%)

ECU master nibble low time for different ID's is given **Table 5**

Table 5 SPC trigger parameters

Parameter	Symbol	Values				Unit	Note or Test Condition
		Min.	Max.	Min.	Max.		
Master nibble low time	t_{mlow}	1[1)]	4.54	1[1)]	4.56	UT	Bus mode off
Master nibble low time	t_{mlow}	5.54	11.54	5.56	12.56	UT	Bus mode on, ID = 0
Master nibble low time	t_{mlow}	12.49	24.49	13.56	25.56	UT	Bus mode on, ID = 1
Master nibble low time	t_{mlow}	25.49	45.49	26.56	47.56	UT	Bus mode on, ID = 2
Master nibble low time	t_{mlow}	46.49	78.49	47.56	79.56	UT	Bus mode on, ID = 3
		Worst case consideration		Nominal consideration			

1) Theoretically the value would be smaller than 1 UT but this is not realistic

5 Conclusions

The impact for a system design of a SPC bus configuration was analyzed in this app note in detail. It has been shown that the external circuitry and the receiver threshold have significant impact on the signal timing of the SPC interface. Thus, this impact needs to be considered. To help analyzing the effects, an Excel Tool has been developed which shows, by entering the parameters of the input master nibble low time and the external components, how the sensor interprets the received trigger. This also shows that at very fast unit times (below 1µs) it is preferred to use the sensor in bus mode with address 0 instead of the conventional synchronous mode although the sensor is not used in a bus configuration

Note: References

1. *Krall, C., & Lanschuetzer, S. (2019). SPC Tolerance Calculator. Tool availabe on request please contact the nearest Infineon Technologies Office.*

Revision history

Document version	Date of release	Description of changes
v02_00	2021.05.18	Changed application note header
Page 9		Removed hyperlink

Edition 2021-5-18
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference
Z8F67433945

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