TLE4986C

EEPROM Programming Guide

Application Note

Rev 1.1, 2015-11-18

Sense & Control

Edition 2015-11-18

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Table of Contents

1 Supply Voltage Interface

All internal data is organized in a memory-like setup. Each data value or EEPROM parameter is located at a specific address. The data width is always 16 bit. The communication with the IC is done with a modulation of the supply voltage on the V_S pin. The sensor is initially switched to a communication mode and commands are sent in this way. The sensor responds with a modulated signal on the V_{OUT} pin.

1.1 Definition of interface timing

All timings and voltage levels for communication are specified in **Table 4-1** and **Table 4-2**.

One bit has the length t_{bit}. The length of the time for the HIGH level within t_{bit} determines whether it is considered as a “1” or a “0”. If the HIGH time is larger as the LOW time, it is considered as a “1”, otherwise it is a “0”. A ratio of 1/3 and 2/3 or 1/4 and 3/4 is recommended for safe communication.

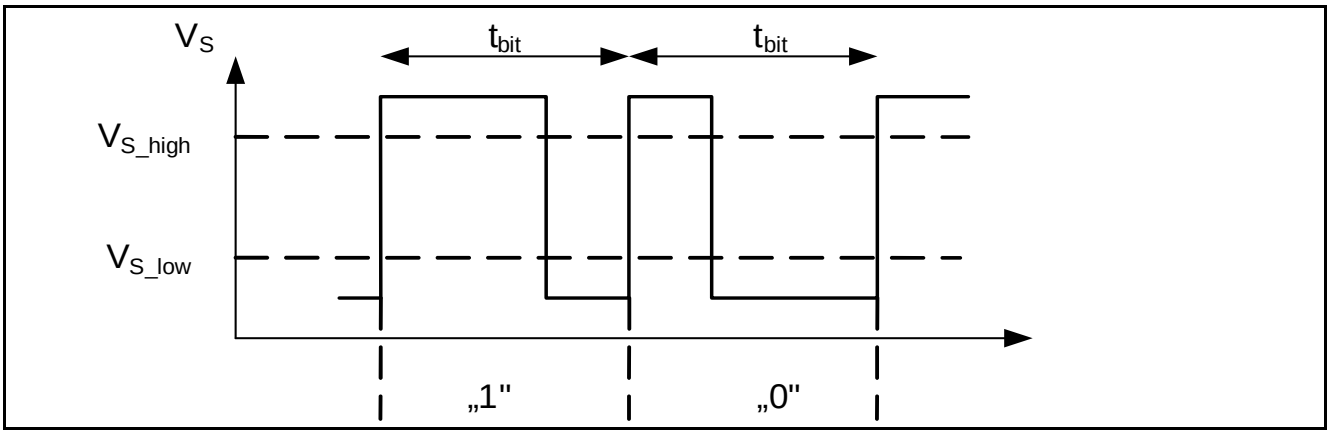

Figure 1-1 Definition of “1” and “0”

1.2 Enter Communication Mode

To enter the supply interface a special modulation sequence (1111 0001 0110 0001) has to be applied shortly after Power On (within $t_{SUPPLY,enter}$). After the last bit an additional pulse P has to be issued.

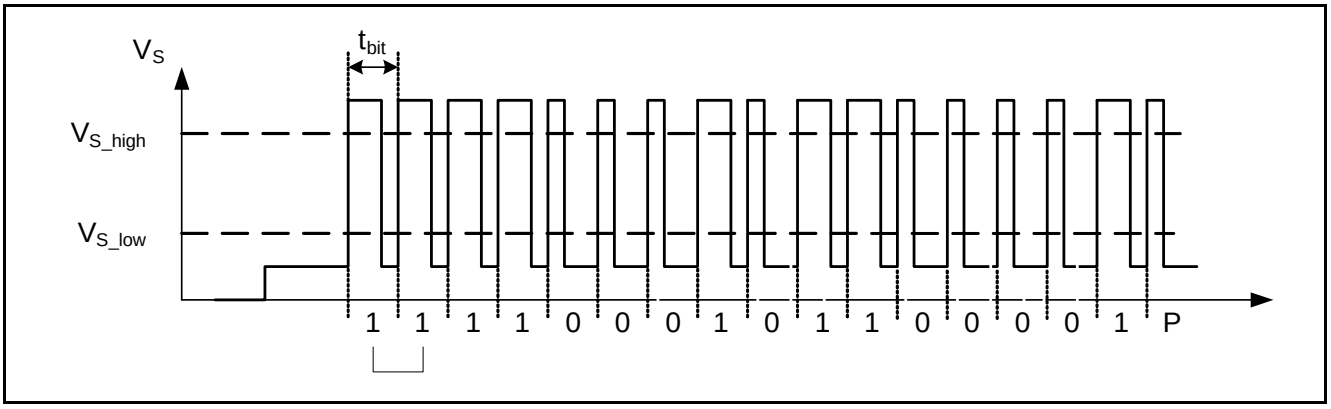

Figure 1-2 V_S sequence to enter communication mode

A second frame has to be sent within additional 43ms after the initial sequence which configures the IC to send data to the output pin V_{OUT} (write command to address 0x09 + additional pulse, 0000-0000-1001-0001-1000-0100-0000-0000-0).

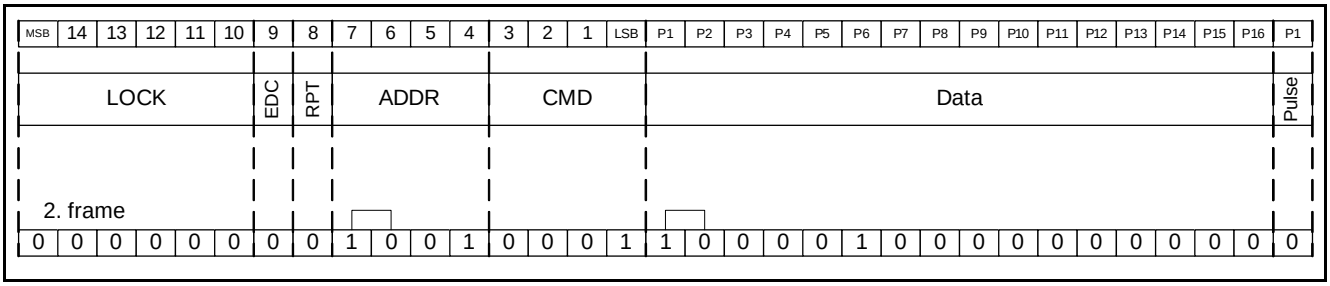

Figure 1-3 2. frame to be sent to enter communication mode: signal to V_{OUT}

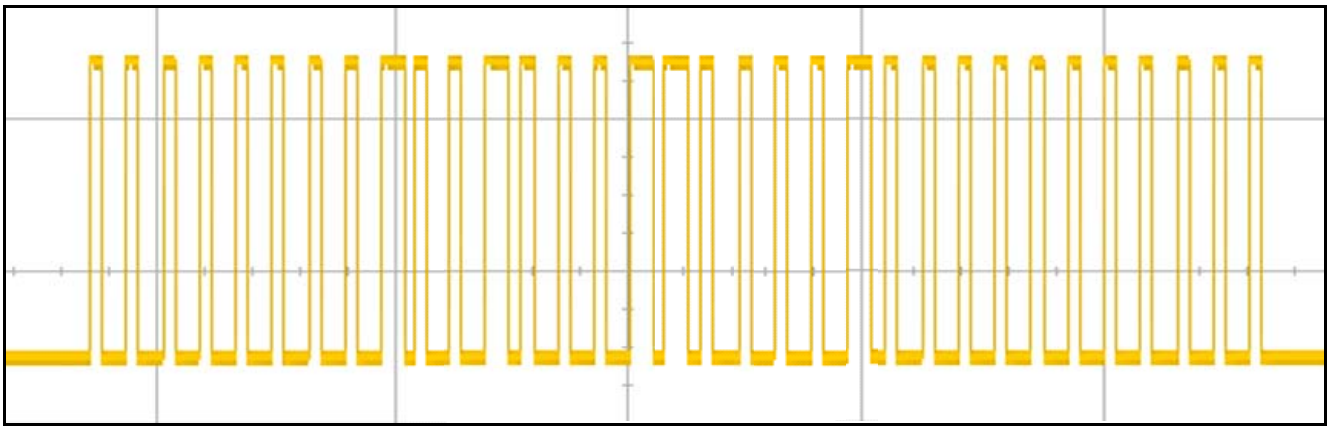

Figure 1-4 2. frame to be sent to enter communication mode: signal to V_{OUT}

Now the IC is in communication mode and the commands shown in **Table 2-1** can be sent. Content of EEPROM addresses can be read (**Chapter 5.1**) or new content can be written to specific addresses (**Chapter 5.2**). The EEPROM can be burned with the written content using a special sequence of frames explained in **Chapter 5.3**.

1.3 Terminate Communication Mode

To leave the communication mode, there are several possibilities:

- Set V_S voltage to high level V_{S_high} for a time longer than $t_{Supplyhigh,exit}$. This automatic exit function of the test mode will be ignored in case bit 15 of register 0x09 is set to “1” with the command (0000-0000-1001-0001-**1**000-0000-0000-0000-0).
- Disconnect V_S

2 Commands

Each command word consists of 16bit. An additional pulse (bit) has to be appended on each command. There are several possibilities where to place the additional pulse.

Single-command (e.g. EEPROM refresh):

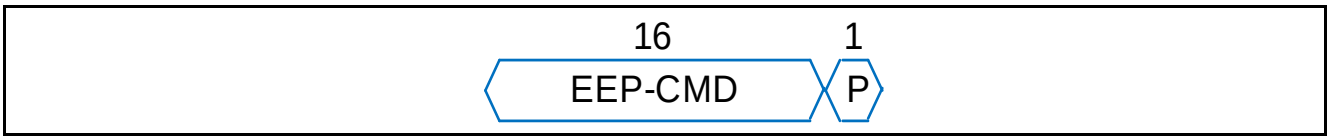

Figure 2-1 Single command

Single write command:

Simply append the additional pulse after the data. After that pulse the next command may follow immediately

Figure 2-2 Single write command

Single read-command: By appending the additional pulse after the command, the following 16 pulses will fit to the data word. After that pulse the next command may follow immediately

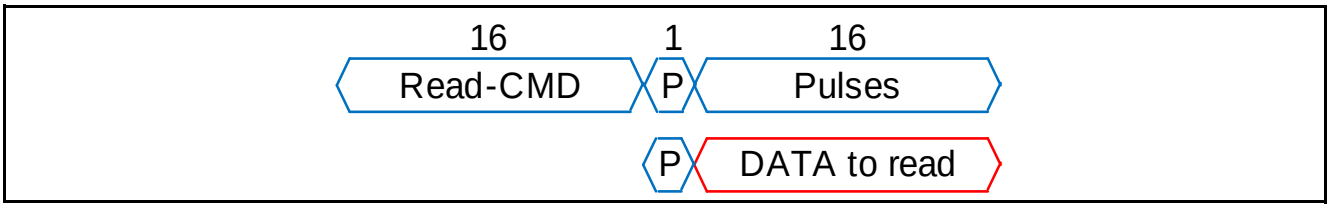

Figure 2-3 Single read command

The following table shows the structure of the 16bit Command word.

Table 2-1 Command Word

Bit	Name	Description
[15 .. 10]	0x00	unused bits, set to 0
[9]	0x0	set to 0
[8]	RPT	Read-CMD: Command sent in during read, will be executed Write-CMD: Continuous Write to the same address
[7 .. 4]	ADDR	Start address of read or write transfer
[3 .. 0]	CMD	Read/Write or EEPROM-Command
	0b0000 - 0x0	Normal read command
	0b0001 - 0x1	Normal write command
	0b1100 - 0xC	Refresh EEPROM register from EEPROM memory
	0b1101 - 0xD	--
	0b1110 - 0xE	Program Zeros of EEPROM
	0b1111 - 0xF	Program Ones of EEPROM

3 Register Map

The register values in the address 0x00 and 0x01 can be set by the user and specify the algorithm for the different operating modes of the sensor.The register mapping is valid for the B11 design step of TLE4986.

Table 3-1 Address Table for TLE4986 design step B11

0x00	EEPROM-Address 0x00 – Function parameter settings [15:0]
0x01	EEPROM-Address 0x01 – Function parameter settings [15:0]
0x02	EEPROM-Address 0x02 – Infineon internal (trimming) [15:0]
0x03	EEPROM-Address 0x03 – Infineon internal (trimming) [15:0]
0x04	Tracking (TADC) value [13:0]; [13:10] also used for programming pulse definition
0x05	Minimum value [13:0]
0x06	Maximum value [13:0]
0x07	SAR enable [14]; Software reset enable [11]; Offset (ODAC) value [10:0]
0x08	Verify programming, successful programming (no errors occurred during the procedure) if “1” [15]
0x09	Switch off automatic exit function [15]; Route the response of the IC to the received command to Vout [10]
0x0A	Infineon internal
0x0B	Infineon internal
0x0C	Disable open drain output [15]
0x0D	Infineon internal
0x0E	Infineon internal
0x0F	Infineon internal

3.1 EEPROM Register Map for TLE4986C-XAS-M47, TLE4986CB-XAN-F27(N)

Table 3-2 EEPROM address 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KFACT		MGN	PCAL		BTPO										

Table 3-3 Functional Description

Field	Bit	Type	Description
KFACT	15:14	rw	Defines threshold in calibrated phase 00_B: k = 38.67% 01_B: k = 51.17% 10_B: k = 63.67% 11_B: k = 69.92%
MGN	13	rw	Sets the possible range for threshold update during pre-calibration phase and the value of minimum noise constant DNC for a programmed device DNCmin: MGN=1_B: 5mT MGN=0_B: 2.5mT Maximum threshold update in pre-calibration phase: PROG=1_B, ADAPT=1_B: 96mT*(MGN+1)/PCAL_duration (PROG=0_B, pre-programmed: maximum threshold update 1.5mT, DNCmin=2.5mT)
PCAL	12:11	rw	Sets duration of pre-calibration phase 00_B: PCAL_duration= 2 output transitions 01_B: PCAL_duration= 2*(NTS+1) output transitions 10_B: PCAL_duration= 2*((NTS+1)/2) output transitions 11_B & AVG_EN = 1_B: PCAL_duration= 4*(NTS+1) output transitions 11_B & AVG_EN = 0_B: PCAL_duration= 64 output transitions Pre-programmed: pre-calibration duration 64 output transitions
BTPO	10:0	rw	Defines threshold for first switching

Table 3-4 EEPROM address 0x01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROG	ADAPT	INV	NTS					AVG_EN	EXTFILT_EN	HYS	ADHYS_EN	UPDFILT_EN	ADSTP_EN	FAST_EN	LOCK

Table 3-5 Functional Description

Field	Bit	Type	Description
PROG	15	rw	0_B: pre-programmed device, the chip starts an auto-search for the actual magnetic value. The initial threshold value is set to this magnetic value 1_B: customer programmed, takes BTPO as first threshold
ADAPT	14	rw	in case of a programmed device (PROG=1_B): 0_B: non-adaptive behavior (fixed threshold) 1_B: adaptive threshold
INV	13	rw	1_B: sets inverted output polarity
NTS	12:8	rw	Number of maxima between two ODAC corrections in calibrated phase when AVG_EN=1_B (number of teeth, length of calibration window). Number of output transitions between two ODAC corrections in calibrated phase when AVG_EN=0_B. It influences the number of output transitions to be considered in pre-calibrated phase 00000_B: 1 maxima/ 2 transitions 00001_B: 2 maxima/ 4 transitions 00010_B: 3 maxima/ 6 transitions 00011_B: 4 maxima/ 8 transitions ... 11111_B: 32 maxima/ 64 transitions
AVG_EN	7	rw	Set to “1” enables averaging algorithm
EXTFILT_EN	6	rw	Set to “1” enables extrema filtering algorithm
HYS	5	rw	Setting of fixed hysteresis level (ADHYS_EN = 0_B) or minimum hysteresis level (ADHYS_EN = 1_B) for programmed device 0_B: B_{Hys}_typ=0.9mT (hysteresis option 1) 1_B: B_{Hys}_typ=4mT (hysteresis option 2)
ADHYS_EN	4	rw	1_B: adaptive hysteresis, full hysteresis value is 25% of the peak-to-peak magnetic signal, minimum value given by setting of HYS bit 0_B: fixed hysteresis
UPDFILT_EN	3	rw	Set to “1” enables update filtering
ADSTP_EN	2	rw	Set to “1” enables adaptive steps feature
FAST_EN	1	rw	Set to “1” enables fast calibration feature
LOCK	0	rw	Locks EEPROM

3.2 EEPROM Register Map for TLE4986C-XTS-M47, TLE4986CB-XTN-F27(N)

Table 3-6 EEPROM address 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KFACT		MGN	PCAL/ KCAL		BTPO										

Table 3-7 Functional Description

Field	Bit	Type	Description
KFACT	15:14	rw	Defines threshold in calibrated phase 00_B: k = 38.67% 01_B: k = 51.17% 10_B: k = 63.67% 11_B: k = 69.92%
MGN	13	rw	Sets the possible range for threshold update during pre-calibration phase and the value of minimum noise constant DNC for a programmed device DNCmin: MGN=1_B: 5mT MGN=0_B: 2.5mT Maximum threshold update in pre-calibration phase: FUNC=11_B: 96mT*(MGN+1)/PCAL_duration FUNC=01_B: 20mT (FUNC=00_B, pre-programmed: maximum threshold update 1.5mT, DNCmin=2.5mT)
PCAL applicable for FUNC=11_B	12:11	rw	Sets duration of pre-calibration phase: 00_B: PCAL_duration= 2 output transitions 01_B: PCAL_duration= 2*(NTS+1) output transitions 10_B: PCAL_duration= 2*((NTS+1)/2) output transitions 11_B & AVG_EN = 1_B: PCAL_duration= 4*(NTS+1) output transitions 11_B & AVG_EN = 0_B: PCAL_duration 64 output transitions FUNC=00_B: pre-calibration duration 64 output transitions
KCAL applicable for FUNC=01_B	12:11	rw	Defines the target threshold in the pre-calibration phase (sub-phase 1) 00_B: k=6.25% 01_B: k=12.5% 10_B: k=25% 11_B: k=50%
BTPO	10:0	rw	Defines threshold for first switching

Table 3-8 EEPROM address 0x01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUNC		INV	NTS					AVG_EN	EXTFILT_EN	HYS	ADHYS_EN	UPDFILT_EN	ADSTP_EN	FAST_EN	LOCK

Table 3-9 Functional Description

Field	Bit	Type	Description
FUNC	15:14	rw	00_B: pre-programmed device 01_B: adaptive individual switching threshold (IST) 10_B: non-adaptive threshold 11_B: adaptive threshold
INV	13	rw	1_B: sets inverted output polarity
NTS bit 12:10 not used with FUNC=01_B	12:8	rw	Number of maxima between two ODAC corrections in calibrated phase when AVG_EN=1_B (number of teeth, length of calibration window). Number of output transitions between two ODAC corrections in calibrated phase when AVG_EN=0_B. It influences the number of output transitions to be considered in pre-calibrated phase 00000_B: 1 maxima/2 transitions 00001_B: 2 maxima/4 transitions 00010_B: 3 maxima/6 transitions 00011_B: 4 maxima/8 transitions ... 11111_B: 32maxima/ 64 transitions
AVG_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	7	rw	set to “1” enables averaging algorithm
EXTFILT_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	6	rw	set to “1” enables extrema filtering algorithm
HYS	5	rw	setting of fixed hysteresis level (ADHYS_EN = 0_B) or minimum hysteresis level (ADHYS_EN = 1_B) for programmed device 0_B: B_{Hys}_typ=0.9mT (hysteresis option 1) 1_B: B_{Hys}_typ=4mT (hysteresis option 2)
ADHYS_EN	4	rw	1_B: adaptive hysteresis, full hysteresis value is 25% of the peak-to-peak magnetic signal, minimum value given by setting of HYS bit 0_B: fixed hysteresis
UPDFILT_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	3	rw	set to “1” enables update filtering

Table 3-9 Functional Description

Field	Bit	Type	Description
ADSTP_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	2	rw	set to “1” enables adaptive steps feature
FAST_EN n.a. for FUNC=00_B FUNC=01_B FUNC=10_B	1	rw	set to “1” enables fast calibration feature
LOCK	0	rw	locks EEPROM

4 Timing & voltage levels for communication

The following tables show the timing and voltage levels which have to be applied for communication.

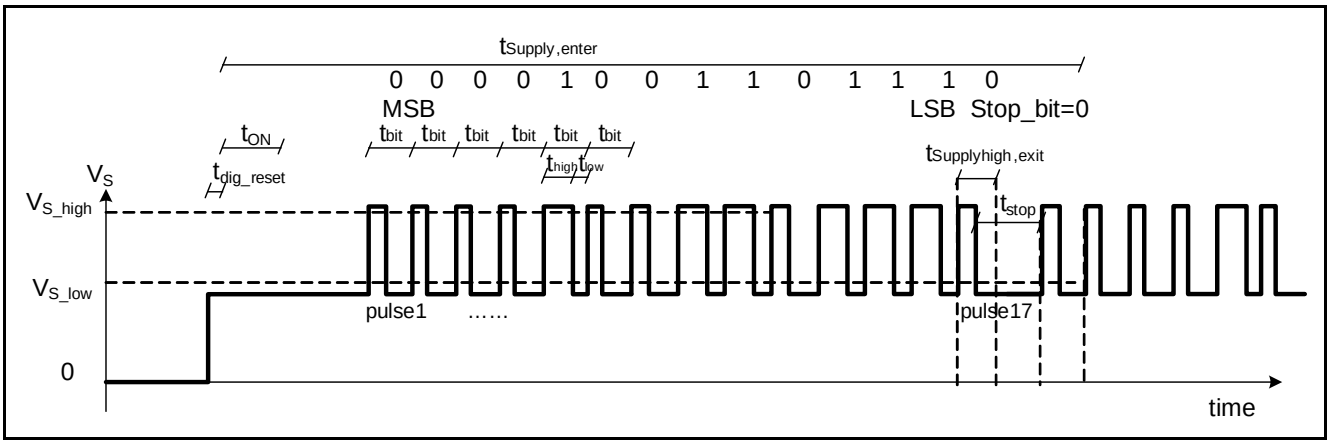

Figure 4-1 Supply voltage timing

Table 4-1 Timing requirements for communication

Parameter	Symbol	Limits			Unit	Notes
		MIN.	TYP.	MAX.		
Startup time	t_{ON}		100		µs	Startup_end signal
Time allowed to enter test-mode	$t_{Supply,enter}$		43		ms	
Bit length ‘0’	t_{bit_0}	33		1674	µs	$t_{bit} = t_{high} + t_{low}$
		47				R_{SERIES}=50Ω, $C1_{INT-PACKAGE}$=47nF
		93				R_{SERIES}=100Ω, $C1_{INT-PACKAGE}$=47nF
		436				R_{SERIES}=100Ω, $C1_{INT-PACKAGE}$=220nF
	t_{high_0}	11		558		
	t_{low_0}	22		1116		
Bit length ‘1’	t_{bit_1}	33		837	µs	
	t_{high_1}	22		558		
	t_{low_1}	11		279		
Exit communication pulse length	$t_{Supplyhigh,exit}$	748			µs	
Stop length	t_{stop}	748			µs	

For the communication with the IC two levels of the supply voltage V_S are needed to distinguish between a “1” and a “0”. The minimum value for the HIGH level and the maximum value for the LOW level are given in **Table 4-2**. These voltage levels must be available directly on the sensor pin. In case a series resistor is used the voltage drop on this resistor has to be taken into account. The minimum required bit length is dependent on the driving capability of the voltage supply to charge and discharge the capacitor. In **Table 4-1** examples are given for the minium required bit lengths for some different load conditions (R_{SERIES}, $C1_{INT-PACKAGE}$) on the supply line.

Table 4-2 Voltage thresholds for Interface on supply line

Parameter	Symbol	Limits			Unit	Notes
		MIN.	TYP.	MAX.		
High level	V_{S_high}	14.5		18.0	V	V_S to be recognized as HIGH level
Low level	V_{S_low}	5.0		8.5	V	V_S to be recognized as LOW level

To burn content from the registers to the EEPROM a programming voltage has to be applied directly on the V_{OUT} pin (without pull-up resistor). The value for this burning voltage is given in **Table 4-3**.

Table 4-3 Programming voltage on output pin

Parameter	Symbol	Limits			Unit	Notes
		MIN.	TYP.	MAX.		
EEPROM programming voltage on V_{OUT}	V_{OUT_PROG}	20.5	20.6	20.7	V	
EEPROM write and erase time	t_{WRITE_ERASE}	35.8			ms	Time for applied programming voltage on V_{OUT} during write or erase phase
EEPROM programming temperature (ambient)	T_{PROG}	15	25	80	°C	

5 Frame Structure for Communication

In this paragraph the structure of the frames for READ, WRITE and burning of EEPROM is shown.

5.1 Reading of EEPROM Content

To read the content of a specific address the following READ frame has to be send via supply line V_S after entering the communication mode as described in **Chapter 1.2**.

Frame structure is shown below:

MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB	P1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
LOCK						EDC	RPT	ADDR				CMD				Pulse	16 Pulses															
Read ADDR 0:																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read ADDR 1:																																
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-1 Structure of a READ frame

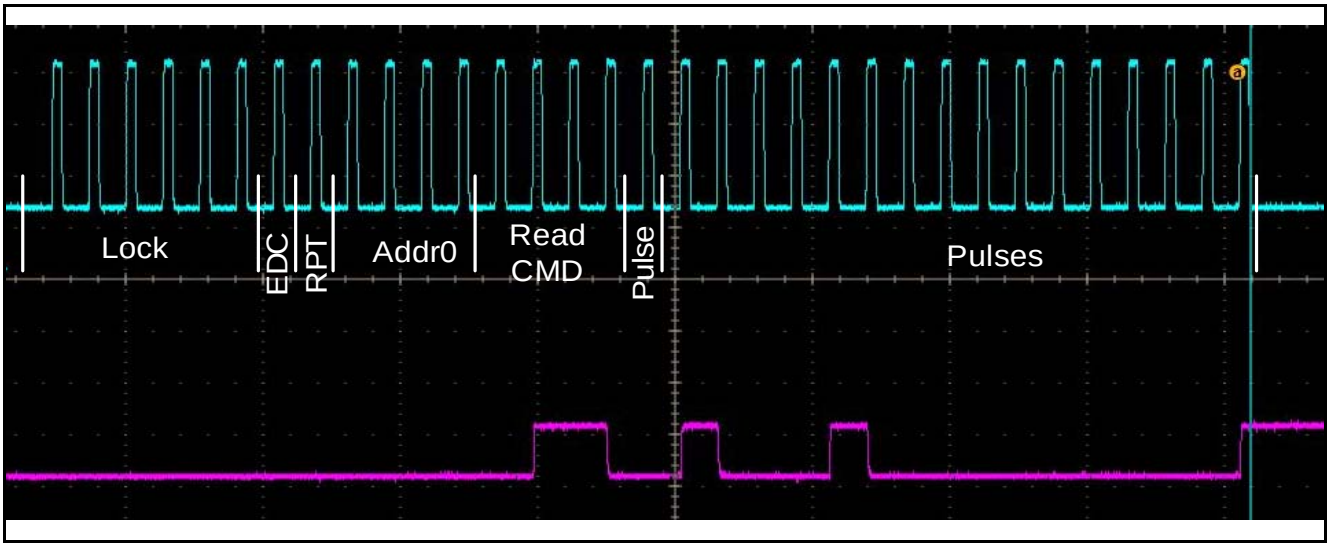

Figure 5-2 Read Addr0

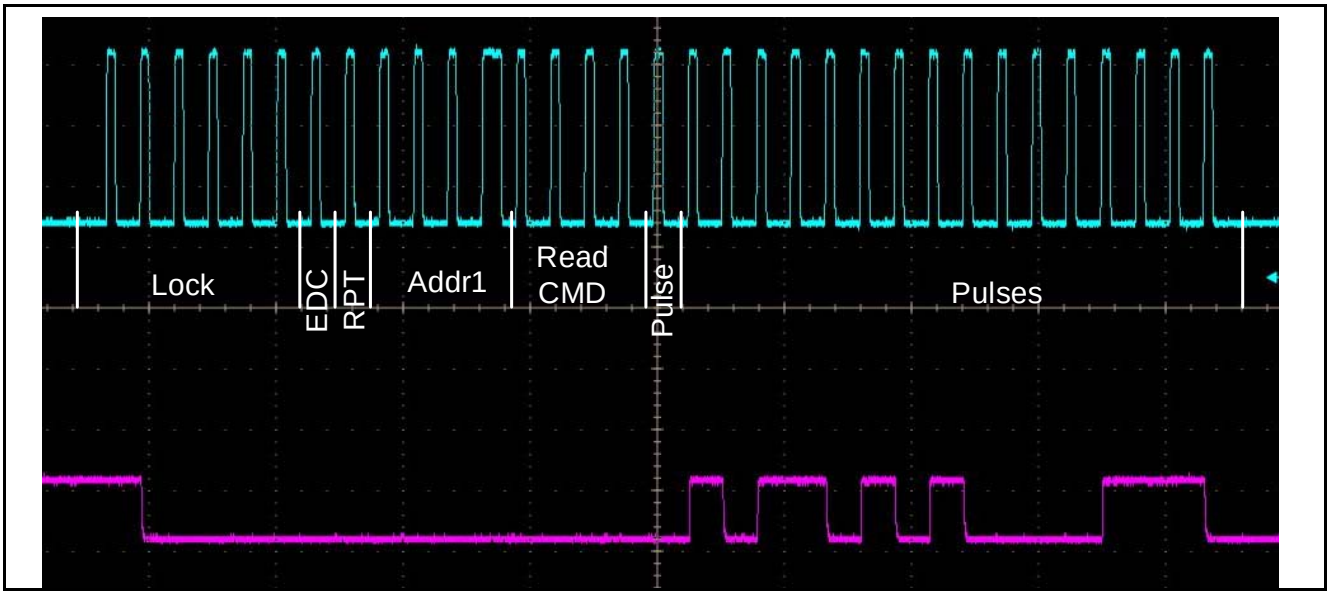

Figure 5-3 Read Addr1

After sending the READ command and the extra pulse, 16 pulses have to be provided at V_S to clock out the information on the V_{OUT} pin starting with the MSB. With each rising edge the V_{OUT} pin has the corresponding state of the specific register (“1” or “0”). To account for the settling time of the signal at the V_{OUT} pin (due to external circuitry for example), a delay should be used before taking the information on the V_{OUT} pin as valid. It is recommended to read the V_{OUT} information shortly before sending the next rising edge of the next pulse. In this way, the complete content of an address (16bit) is read.

5.2 Writing of EEPROM Content

To write content to an EEPROM address, the following 33bit frame must be used. Each WRITE frame writes the complete 16bit content of an address. The 16bit data word, which is sent after the WRITE command, contains the information which is written to the register. And additional pulse has to be appended at the end of the frame. In the example shown the 16bit word 1000-1000-0000-0000 is written to the specified address.

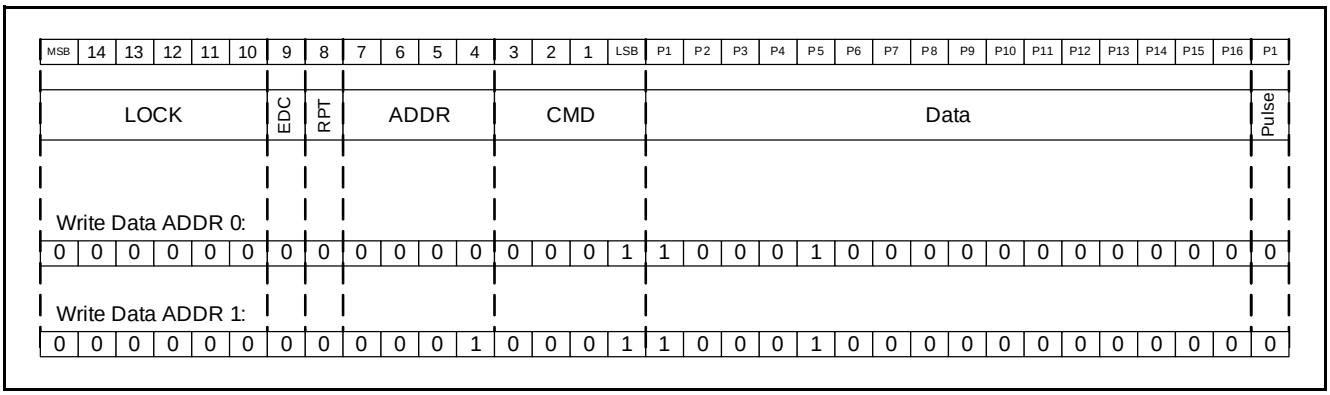

Figure 5-4 Structure of a WRITE frame

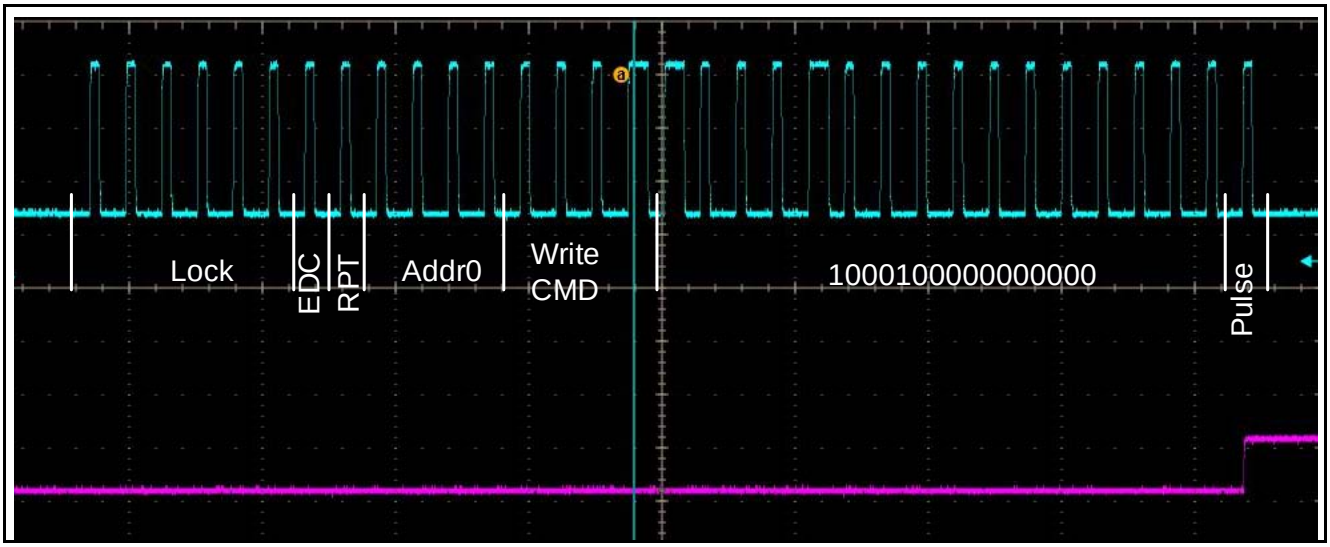

Figure 5-5 Write Addr0

5.3 Burning of EEPROM

After writing content to a EEPROM address, the EEPROM has to be burned sending a specific set of frames while the applied voltage at the V_{OUT} pin (directly on the pin without pull-up resistor) has to be in the range given by **Table 4-3** (typ. 20.6V). The ”0” and “1” values of the EEPROM have to be burned sequentially with the command 0b1110 (burn “0”) and 0b1111 (burn “1”).

The detailed sequence how to burn the EEPROM is as follows:

After entering the communication mode (3 frames as specified in **Chapter 1.2**), the desired content has to be written to the address 0x00 and 0x01 using the WRITE frame (**Chapter 5.2**). Before starting with the EEPROM burning sequence, the voltage at the V_{OUT} pin has to be applied according to the values given in **Table 4-3**. The first frame to be sent is the “Programming Pulse Definition” (+ appended pulse):
0000-0000-0100-0001-1000-1000-0000-0000-0.

The automatic exit function (see **Chapter 1.3**) must be disabled.

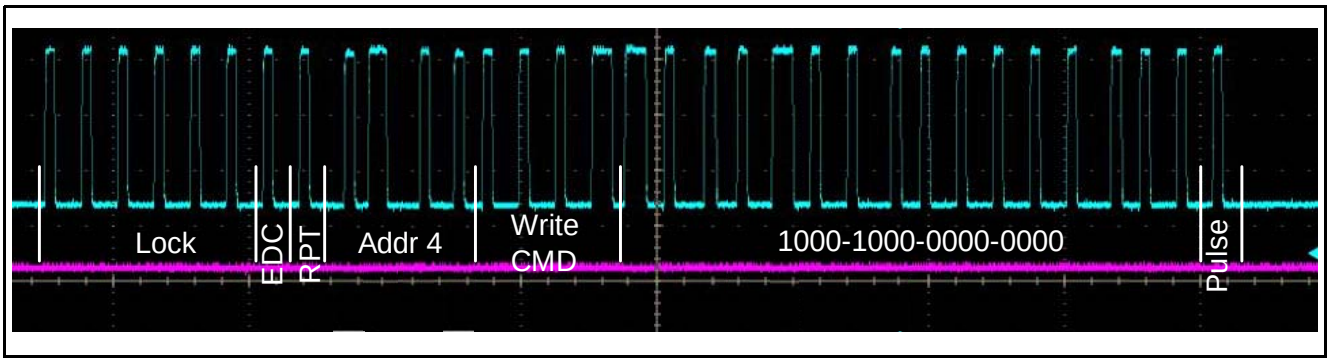

Figure 5-6 Programming Pulse Definition

As next, the frame “Burn0” has to be sent (0000-0000-0000-1110-0).

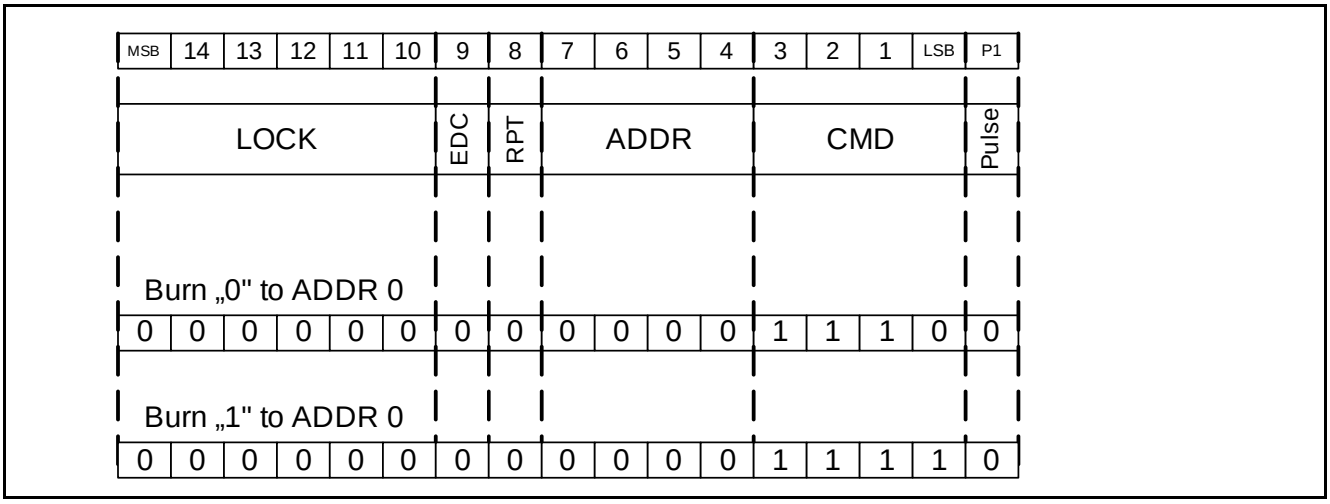

Figure 5-7 Structure of the frame: Burn EEPROM

After the “Burn0” command is sent it is important that the voltage level at V_S is kept at V_{S_high} while V_{OUT_PROG} is applied for 35.8ms. Afterwards, the V_S level must be set back to V_{S_low} before the next frame can follow.

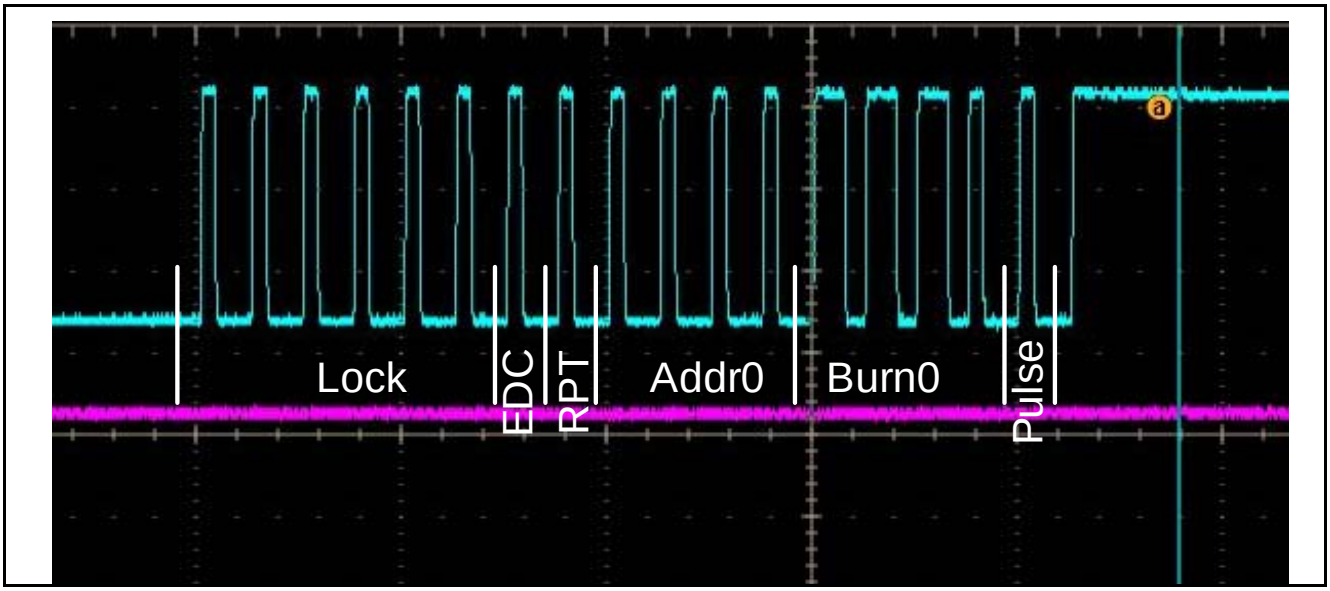

Figure 5-8 Burn “0” of EEPROM Address 0

Now, the WRITE commands have to repeated which write the desired content in the EEPROM addresses. This frame is followed by the “Burn1” frame (0000-0000-0000-1111-0).

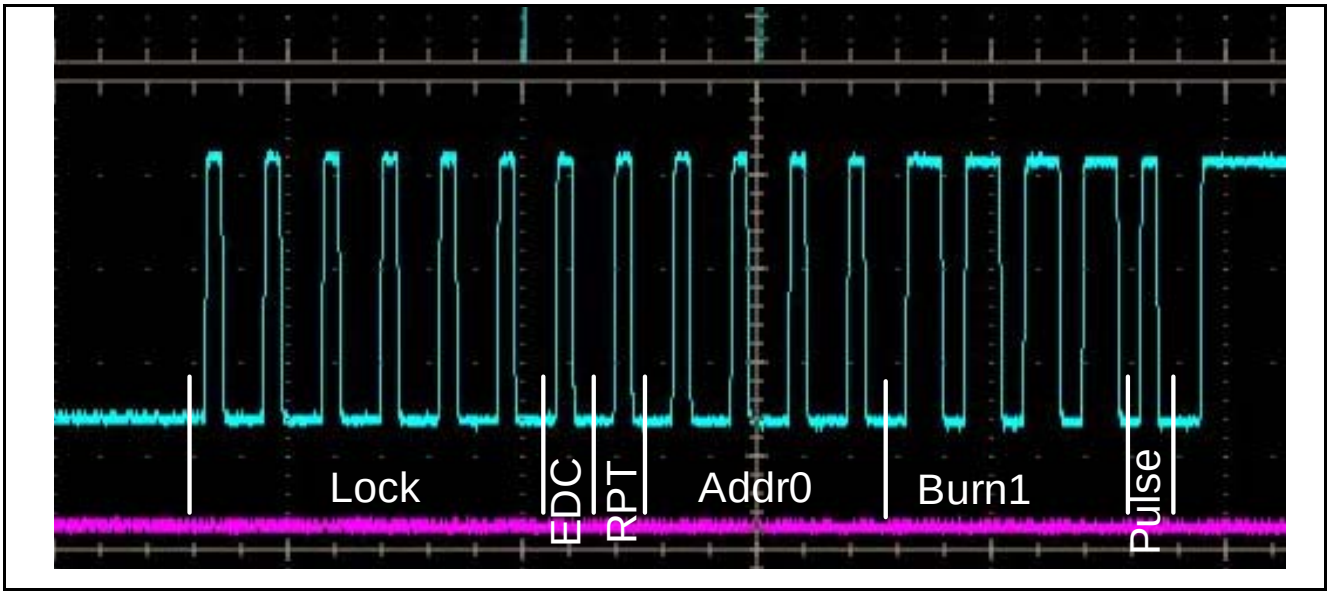

Figure 5-9 Burn “1” of EEPROM Address 0

Again, after the “Burn1” command is sent it is important that the voltage level at V_S is kept at V_{S_high} while V_{OUT_PROG} is applied for 35.8ms. Afterwards, the V_S level must be set back to V_{S_low} before the next frame can follow.

The burning of the EEPROM is now finished.

It is recommended, after a reset to read again the content of the programmed addresses to verify whether the EEPROM burning process was successfully.

The complete sequence of frames for the EEPROM burning is shown in **Figure 5-10**. The additional pulse is always included in the frame.

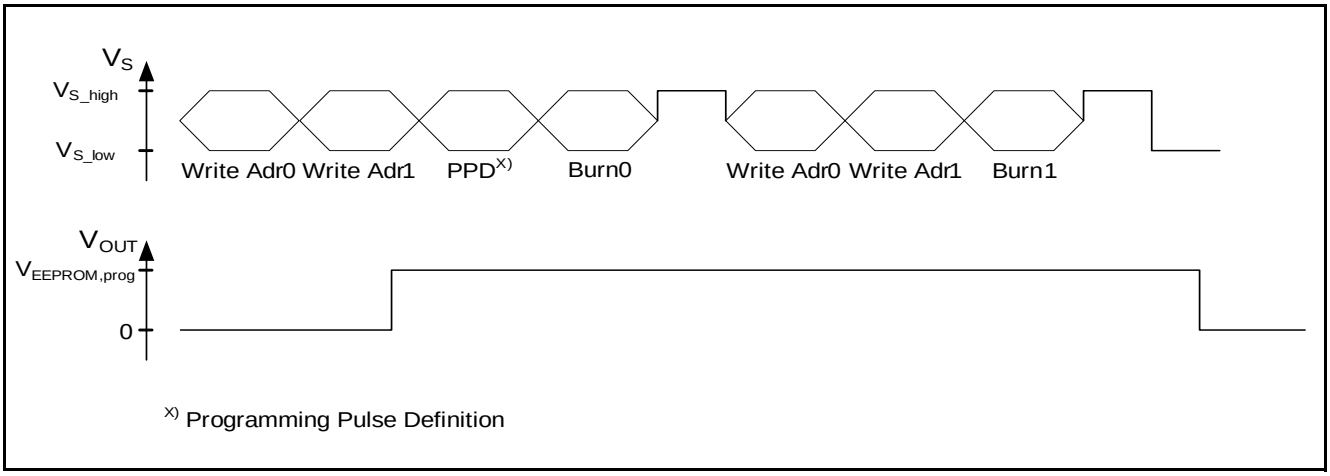

Figure 5-10 EEPROM burning sequence

6 Summary of IC Communication

The following tables summarize the sequence of frames which have to be used for switching into communication mode and for burning the EEPROM.

6.1 Switching the IC in Communication Mode

The following table shows the frames which have to be sent to switch the sensor in the programming mode. The appended pulse is included as a single “0” bit in the frame. In total, 2 frames have to be sent to enter the communication mode.

Table 6-1 Sequence of frames to switch into communication mode

Frame #	Description	Frame	Remark
1	Switch to communication mode	1111-0001-0110-0001-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
2	Switch digital signal to V_{OUT}	0000-0000-1001-0001-1000-0100-0000-0000-0	Route the response of the IC to the received command to Vout

6.2 Burning EEPROM

The following sequence of frames has to be sent to burn the EEPROM after having switched the sensor in communication mode. The programming voltage at V_{OUT} has to be applied before sending the Burn command and has to be maintained during the complete burning sequence. After the burn command V_S must kept at V_{S_high} while V_{OUT_PROG} is applied for 35.8ms and then set back to V_{S_low} before sending the next frame.

Table 6-2 Sequence of frames to burn EEPROM

Frame #	Description	Frame	Remark
1	Switch to communication mode	1111-0001-0110-0001-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
2	Switch digital signal to V_{OUT}	0000-0000-1001-0001-1000-0100-0000-0000-0	Route the response of the IC to the received command to Vout. Test mode will be exit automatically when V_S is set above 14.5V for typical 680µs. This command will disable the automatic exit functionality
3	Optionally read EEPROM Addr. 0x00	0000-0000-0000-0000-0 rrrr-rrrr-rrrr-rrrr	‘rrrr’ represents the initial16bit content of Addr. 0x00
4	Optionally read EEPROM Addr. 0x01	0000-0000-0001-0000-0 rrrr-rrrr-rrrr-rrrr	‘rrrr’ represents the initial16bit content of Addr. 0x01
5	Optionally keep data for later usage		
6	Change the read bit content of the two EEPROM lines to the desired, new bit content		
7	Write content to Addr 0x00	0000-0000-0000-0001-wwww-wwww-wwww-wwww-0	‘wwww’ represents the desired 16bit content of Addr. 0x00

Table 6-2 Sequence of frames to burn EEPROM

Frame #	Description	Frame	Remark
8	Write content to Addr 0x01	0000-0000-0001-0001-wwww-wwww-wwww-wwww-0	'wwww' represents the desired 16bit content of Addr. 0x01
9	Programming Pulse Definition	0000-0000-0100-0001-1000-1000-0000-0000-0	Definition of programming pulse length, set for typical 256µs
10	Disable open drain output	0000-0000-1100-0001-1000-0000-0000-0000-0	Avoids output switching during programming
11	Apply programming voltage V_{OUT_PROG} on sensor output pin		Set voltage of Vout pin to 20.6V
12	Burn "0" to EEPROM	0000-0000-0000-1110-0	Sending burn '0' command
13	After sending frame 12, keep V_S at V_{S_high} while V_{OUT_PROG} is applied for 35.8ms		
14	Set V_S back to V_{S_low}		
15	Remove programming voltage from Vout pin of sensor		
16	Enable open drain output	0000-0000-1100-0001-0000-0000-0000-0000-0	
17	Reading of register address 0x08	0000-0000-1000-0000-0 0000-0000-0000-0000	Reading of register address 0x08
18	Check bit number 15		If bit number 15 is set to '1' no error, otherwise error occurred
19	Write content to Addr 0x00	0000-0000-0000-0001-wwww-wwww-wwww-wwww-0	Repeat writing of desired content to Addr. 0x00
20	Write content to Addr 0x01	0000-0000-0001-0001-wwww-wwww-wwww-wwww-0	Repeat writing of desired content to Addr. 0x01. For complete locking of the EEPROM, bit 0 of Addr. 0x01 needs to be set to '1'
21	Disable open drain output	0000-0000-1100-0001-1000-0000-0000-0000-0	Avoids output switching during programming
22	Apply programming voltage V_{OUT_PROG} on sensor output pin		Set voltage of Vout pin to 20.6V
23	Burn "1" to EEPROM	0000-0000-0000-1111-0	Sending burn '1' command
24	After sending frame 23, keep V_S at V_{S_high} while V_{OUT_PROG} is applied for 35.8ms		
25	Set V_S back to V_{S_low}		
26	Remove programming voltage from Vout pin of sensor		
27	Enable open drain output	0000-0000-1100-0001-0000-0000-0000-0000-0	
28	Reading of register address 0x08	0000-0000-1000-0000-0 0000-0000-0000-0000	Reading of register Addr. 0x08

Table 6-2 Sequence of frames to burn EEPROM

Frame #	Description	Frame	Remark
29	Check bit number 15		If bit number 15 is set to ‘1’ no error, otherwise error occurred
30	Restart device		Power down and restart the sensor IC, most reliable method for subsequent check of proper progamming
31	Switch to communication mode	1111-0001-0110-0001-0	
32	Switch digital signal to V_{OUT}	0000-0000-1001-0001-1000-0100-0000-0000-0	
33	Refresh EEPROM register from EEPROM memory	0000-0000-0000-1100-0	Optional, instead step 30,31,32
34	Read EEPROM Addr. 0x00	0000-0000-0000-0000-0 rrrr-rrrr-rrrr-rrrr	
35	Read EEPROM Addr. 0x01	0000-0000-0001-0000-0 rrrr-rrrr-rrrr-rrrr	
36	If content of read EEPROM registers equal to that content that have been written during burn process the EEPROM cells have been written successfully. Optionally keep data for later usage		
37	Subsequent sensor functional check in normal operating mode requires a restart (reset) of the device		

Revision History	
Page or Item	**Subjects (major changes since previous revision)** **TLE4986 Programming Guide Rev 1.0, 2015-11-03**
Rev 1.1, 2015-11-18	
17	Chapter 5.3: Burning of EEPROM description and sequence complemented
general	Spelling and typos
<Revision X.Y>, <yyyy-mm-dd>	

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG

Doc_Number