Unipolar Hall Switch
High Precision Automotive Unipolar Hall Effect Switch
TLE4964-2M
SP000923330
Table of contents

Table of contents ................................................................. 2
List of tables ................................................................. 3
List of figures ............................................................... 4

1 Product description ........................................................... 5
1.1 Overview ............................................................... 5
1.2 Features ............................................................... 5
1.3 Target applications ..................................................... 6
1.4 Product validation ....................................................... 6

2 Functional description ........................................................ 7
2.1 General ............................................................... 7
2.2 Pin configuration (top view) ........................................... 7
2.3 Pin description ............................................................ 7
2.4 Block diagram ........................................................... 8
2.5 Functional block description ........................................... 9
2.6 Default start-up behavior ............................................. 10

3 Specification ................................................................. 11
3.1 Application circuit ....................................................... 11
3.2 Absolute maximum ratings ............................................ 12
3.3 Operating range .......................................................... 13
3.4 Electrical and magnetic characteristics ................................ 14
3.5 Electro magnetic compatibility ....................................... 16

4 Package information ........................................................ 18
4.1 Package outline PG-SOT23-3-15 ..................................... 18
4.2 Packing information PG-SOT23-3-15 ............................... 18
4.3 Footprint PG-SOT23-3-15 ............................................. 19
4.4 PG-SOT23-3-15 distance between chip and package ............ 19
4.5 Package marking .......................................................... 19

5 Graphs of the magnetic parameters ..................................... 20

6 Graphs of the electrical parameters ...................................... 21

7 Revision history ............................................................. 26
List of tables

Table 1  Ordering information ................................................................. 5
Table 2  Pin description PG-SOT23-3-15 .................................................. 7
Table 3  Absolute maximum rating parameters ....................................... 12
Table 4  ESD protection \( T_A = 25^\circ C \) ...................................................... 13
Table 5  Operating conditions parameters .............................................. 13
Table 6  General electrical characteristics ............................................. 14
Table 7  Magnetic characteristics .......................................................... 15
Table 8  Magnetic compatibility .............................................................. 16
Table 9  Electro magnetic compatibility .................................................. 17
List of figures

Figure 1  TLE4964-2M in the PG-SOT23-3-15 package .......................... 5
Figure 2  Pin configuration and center of sensitive area .......................... 7
Figure 3  Functional block diagram TLE4964-2M ................................. 8
Figure 4  Timing diagram TLE4964-2M ............................................. 9
Figure 5  Output signal TLE4964-2M ................................................. 9
Figure 6  Start-up behavior of the TLE4964-2M .................................... 10
Figure 7  Application circuit 1: with external resistor ............................ 11
Figure 8  Application circuit 2: without external resistor ....................... 11
Figure 9  Definition of magnetic field direction PG-SOT23-3-15 ............. 15
Figure 10  EMC test circuit ............................................................ 16
Figure 11  PG-SOT23-3-15 package outline (all dimensions in mm) .......... 18
Figure 12  Packing of the PG-SOT23-3-15 in a tape ........................... 18
Figure 13  Footprint PG-SOT23-3-15 .............................................. 19
Figure 14  Distance between chip and package .................................. 19
Figure 15  Marking of TLE4964-2M ................................................. 19
Figure 16  Operating point \( (B_{OP}) \) of the TLE4964-2M over temperature .... 20
Figure 17  Release point \( (B_{RP}) \) of the TLE4964-2M over temperature ........ 20
Figure 18  Hysteresis \( (B_{Hys}) \) of the TLE4964-2M over temperature ........ 20
Figure 19  Power on time \( t_{PON} \) of the TLE4964-2M over temperature ....... 21
Figure 20  Signal delay time of the TLE4964-2M over temperature ............ 21
Figure 21  Supply current of the TLE4964-2M over temperature ............... 21
Figure 22  Supply current of the TLE4964-2M over supply voltage .......... 22
Figure 23  Output current limit of the TLE4964-2M over temperature .......... 22
Figure 24  Output current limit of the TLE4964-2M over applied pull-up voltage .... 22
Figure 25  Output fall time of the TLE4964-2M over temperature .............. 23
Figure 26  Output fall time of the TLE4964-2M over applied pull-up voltage .... 23
Figure 27  Output rise time of the TLE4964-2M over temperature ............. 23
Figure 28  Output rise time of the TLE4964-2M over applied pull-up voltage .... 24
Figure 29  Output leakage current of the TLE4964-2M over temperature ....... 24
Figure 30  Saturation voltage of the TLE4964-2M over temperature .......... 24
Figure 31  Saturation voltage of the TLE4964-2M over output current ......... 25
Figure 32  Effective noise of the TLE4964-2M thresholds over temperature .... 25
Figure 33  Output signal jitter of the TLE4964-2M over temperature .......... 25
1 Product description

1.1 Overview

Figure 1 TLE4964-2M in the PG-SOT23-3-15 package

1.2 Features

- 3.0 V to 32 V operating supply voltage
- Operation from unregulated power supply
- Reverse polarity protection (-18 V)
- Overvoltage capability up to 42 V without external resistor
- Output overcurrent and overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 0.35 μs)
- High ESD performance
- Small SMD package PG-SOT23-3-15

Table 1 Ordering information

<table>
<thead>
<tr>
<th>Product name</th>
<th>Product type</th>
<th>Ordering code</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLE4964-2M</td>
<td>Unipolar Hall Switch</td>
<td>SP000923330</td>
<td>PG-SOT23-3-15</td>
</tr>
</tbody>
</table>
Target applications for the TLE496x Hall Switch family are all applications which require a high precision Hall Switch with an operating temperature range from -40°C to 170°C. Its superior supply voltage range from 3.0 V to 32 V with overvoltage capability (e.g. load-dump) up to 42 V without external resistor makes it ideally suited for automotive and industrial applications.

The TLE4964-2M is a unipolar switch with a typical operating point \( B_{\text{OP}} = 28 \text{ mT} \) and a hysteresis of \( B_{\text{HYS}} = 5.5 \text{ mT} \). It is ideally suited for various position detection applications.

1.4 Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.
2 Functional description

2.1 General
The TLE4964-2M is an integrated Hall effect switch designed specifically for highly accurate applications with superior supply voltage capability, operating temperature range and temperature stability of the magnetic thresholds.

2.2 Pin configuration (top view)

![Pin configuration and center of sensitive area](image)

Figure 2 Pin configuration and center of sensitive area

2.3 Pin description

Table 2 Pin description PG-SOT23-3-15

<table>
<thead>
<tr>
<th>Pin no.</th>
<th>Symbol</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>2</td>
<td>Q</td>
<td>Output</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground</td>
</tr>
</tbody>
</table>
2.4 Block diagram

Figure 3  Functional block diagram TLE4964-2M
### 2.5 Functional block description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.

![Timing diagram TLE4964-2M](image_url)

**Figure 4** Timing diagram TLE4964-2M

![Output signal TLE4964-2M](image_url)

**Figure 5** Output signal TLE4964-2M
2.6 Default start-up behavior

The magnetic thresholds exhibit a hysteresis $B_{\text{HYS}} = B_{\text{OP}} - B_{\text{RP}}$. In case of a power-on with a magnetic field $B$ within hysteresis ($B_{\text{OP}} > B > B_{\text{RP}}$) the output of the sensor is set to the pull up voltage level ($V_Q$) per default. After the first crossing of $B_{\text{OP}}$ or $B_{\text{RP}}$ of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

$V_{\text{DDA}}$ is the internal supply voltage which is following the external supply voltage $V_{\text{DD}}$.

This means for $B > B_{\text{OP}}$ the output is switching, for $B < B_{\text{RP}}$ and $B_{\text{OP}} > B > B_{\text{RP}}$ the output stays at $V_Q$.

![Figure 6 Start-up behavior of the TLE4964-2M](image)

The device always applies $V_Q$ level at start-up independent from the applied magnetic field!
3 Specification

3.1 Application circuit

The following Figure 7 shows one option of an application circuit. As explained above the resistor $R_S$ can be left out (see Figure 8). The resistor $R_Q$ has to be in a dimension to match the applied $V_S$ to keep $I_Q$ limited to the operating range of maximum 25 mA.

e.g.: $V_S = 12\, \text{V}; \, I_Q = 12\, \text{V}/1200\, \Omega = 10\, \text{mA}$

![Figure 7 Application circuit 1: with external resistor](image1)

![Figure 8 Application circuit 2: without external resistor](image2)
3.2 Absolute maximum ratings

Table 3 Absolute maximum rating parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note or Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>$V_{DD}$</td>
<td>-18 - 32</td>
<td>V</td>
<td>10h, no external resistor required</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_Q$</td>
<td>-0.5 - 32</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Reverse output current</td>
<td>$I_Q$</td>
<td>-70 - -</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Junction temperature</td>
<td>$T_J$</td>
<td>-40 - 155</td>
<td>°C</td>
<td>for 2000h (not additive)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>165 175 185</td>
<td>°C</td>
<td>for 1000h (not additive)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>°C</td>
<td>for 168h (not additive)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>°C</td>
<td>for 3 x 1h (additive)</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_S$</td>
<td>-40 - 150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Thermal resistance</td>
<td>$R_{th,JA}$</td>
<td>300</td>
<td>K/W</td>
<td>for PG-SOT23-3-15 (2s2p)</td>
</tr>
<tr>
<td>Junction lead</td>
<td>$R_{th,JL}$</td>
<td>100</td>
<td>K/W</td>
<td>for PG-SOT23-3-15</td>
</tr>
</tbody>
</table>

1) This lifetime statement is an anticipation based on an extrapolation of Infineon’s qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Calculation of the dissipated power $P_{DIS}$ and junction temperature $T_J$ of the chip (SOT23 example):
e.g. for: $V_{DD} = 12$ V, $I_S = 2.5$ mA, $V_{QAT} = 0.5$ V, $I_Q = 20$ mA
Power dissipation: $P_{DIS} = 12$ V x 2.5 mA + 0.5 V x 20 mA = 30 mW + 10 mW = 40 mW
Temperature $\Delta T = R_{th,JA} \times P_{DIS} = 300$ K/W x 40 mW = 12 K
For $T_A = 150$°C: $T_J = T_A + \Delta T = 150$°C + 12 K = 162°C
Data Sheet 13 Revision 1.2, 2019-12-20

TLE4964-2M

Specification

### Table 4  ESD protection\(^1\) \((T_A = 25^\circ\text{C})\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note or Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD voltage (HBM)(^2)</td>
<td>(V_{\text{ESD}})</td>
<td>-7</td>
<td>7</td>
<td>kV</td>
</tr>
<tr>
<td>ESD voltage (CDM)(^3)</td>
<td>(V_{\text{ESD}})</td>
<td>-1</td>
<td>1</td>
<td>kV</td>
</tr>
<tr>
<td>ESD voltage (system level)(^4)</td>
<td>(V_{\text{ESD}})</td>
<td>-15</td>
<td>15</td>
<td>kV</td>
</tr>
</tbody>
</table>

1) Characterization of ESD is carried out on a sample basis, not subject to production test.
2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.
3) Charge device model (CDM) tests according to JESD22-C101.
4) Gun test (2 k\(\Omega\) / 330 pF or 330 \(\Omega\) / 150 pF) according to ISO 10605-2008.

### 3.3  Operating range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4964-2M.

All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

The maximum tested magnetic field is 600 mT.

### Table 5  Operating conditions parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note or Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>(V_{\text{DD}})</td>
<td>3.0</td>
<td>–</td>
<td>32(^1)</td>
</tr>
<tr>
<td>Output voltage</td>
<td>(V_{\text{Q}})</td>
<td>-0.3</td>
<td>–</td>
<td>32</td>
</tr>
<tr>
<td>Junction temperature</td>
<td>(T_J)</td>
<td>-40</td>
<td>–</td>
<td>170</td>
</tr>
<tr>
<td>Output current</td>
<td>(I_{\text{Q}})</td>
<td>0</td>
<td>–</td>
<td>25</td>
</tr>
<tr>
<td>Magnetic signal input frequency(^2)</td>
<td>(f_{\text{SW}})</td>
<td>0</td>
<td>–</td>
<td>10</td>
</tr>
</tbody>
</table>

1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.
2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3 dB corner frequency of the internal low-pass filter in the signal path.
3.4 Electrical and magnetic characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to $V_{DD} = 12$ V and $T_A = 25^\circ$C. The below listed specification is valid in combination with the application circuit shown in Figure 7 and Figure 8.

### Table 6 General electrical characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Values</th>
<th>Unit</th>
<th>Note or Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current</td>
<td>$I_S$</td>
<td>1.1</td>
<td>1.6</td>
<td>2.5 mA</td>
</tr>
<tr>
<td>Reverse current</td>
<td>$I_{SR}$</td>
<td>–</td>
<td>0.05</td>
<td>1 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>for $V_{DD} = -18$ V</td>
</tr>
<tr>
<td>Output saturation voltage</td>
<td>$V_{QSAT}$</td>
<td>–</td>
<td>0.2</td>
<td>0.5 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$I_O = 20$ mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$I_O = 25$ mA</td>
</tr>
<tr>
<td>Output leakage current</td>
<td>$I_{QLEAK}$</td>
<td>–</td>
<td>–</td>
<td>10 μA</td>
</tr>
<tr>
<td>Output current limitation</td>
<td>$I_{QLIMIT}$</td>
<td>30</td>
<td>56</td>
<td>70 mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>internally limited and thermal shutdown</td>
</tr>
<tr>
<td>Output fall time$^{1)}$</td>
<td>$t_f$</td>
<td>0.17</td>
<td>0.4</td>
<td>1 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.2 kΩ / 50 pF, see Figure 4</td>
</tr>
<tr>
<td>Output rise time$^{1)}$</td>
<td>$t_r$</td>
<td>0.4</td>
<td>0.5</td>
<td>1 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.2 kΩ / 50 pF, see Figure 4</td>
</tr>
<tr>
<td>Output jitter$^{1)(2)}$</td>
<td>$t_{QJ}$</td>
<td>–</td>
<td>0.35</td>
<td>1 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>for square wave signal with 1 kHz</td>
</tr>
<tr>
<td>Delay time$^{1)(3)}$</td>
<td>$t_d$</td>
<td>12</td>
<td>15</td>
<td>30 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>see Figure 4</td>
</tr>
<tr>
<td>Power-on time$^{1)(4)}$</td>
<td>$t_{PON}$</td>
<td>–</td>
<td>80</td>
<td>150 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V_{DD} = 3$ V, $B \leq B_{RP} - 0.5$ mT or $B \geq B_{OP} + 0.5$ mT</td>
</tr>
<tr>
<td>Chopper frequency$^{1)}$</td>
<td>$f_{OSC}$</td>
<td>–</td>
<td>350</td>
<td>kHz</td>
</tr>
</tbody>
</table>

1) Not subject to production test, verified by design/characterization.
2) Output jitter is the 1 σ value of the output switching distribution.
3) Systematic delay between magnetic threshold reached and output switching.
4) Time from applying $V_{DD} = 3.0$ V to the sensor until the output is valid.
Table 7  Magnetic characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>T (°C)</th>
<th>Values</th>
<th>Unit</th>
<th>Note / Test Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Operating point</td>
<td>(B_{\text{OP}})</td>
<td>-40</td>
<td>21.6</td>
<td>30.2</td>
<td>38.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td>20.0</td>
<td>28.0</td>
<td>36.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>170</td>
<td>16.3</td>
<td>23.1</td>
<td>29.9</td>
</tr>
<tr>
<td>Release point</td>
<td>(B_{\text{RP}})</td>
<td>-40</td>
<td>17.1</td>
<td>24.2</td>
<td>31.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td>15.9</td>
<td>22.5</td>
<td>29.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>170</td>
<td>12.9</td>
<td>18.6</td>
<td>24.3</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>(B_{\text{HYS}})</td>
<td>-40</td>
<td>4.4</td>
<td>5.9</td>
<td>8.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td>4.1</td>
<td>5.5</td>
<td>7.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>170</td>
<td>3.4</td>
<td>4.6</td>
<td>6.3</td>
</tr>
<tr>
<td>Effective noise value of the</td>
<td>(B_{\text{Neff}})</td>
<td>25</td>
<td>–</td>
<td>62</td>
<td>–</td>
</tr>
<tr>
<td>magnetic switching points(^1)</td>
<td></td>
<td>25</td>
<td>–</td>
<td>62</td>
<td>–</td>
</tr>
<tr>
<td>Temperature compensation of</td>
<td>(T_{\text{C}})</td>
<td>–</td>
<td>–</td>
<td>-1200</td>
<td>–</td>
</tr>
<tr>
<td>magnetic thresholds(^2)</td>
<td></td>
<td>25</td>
<td>–</td>
<td>-1200</td>
<td>–</td>
</tr>
</tbody>
</table>

1) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents the rms-value and corresponds therefore to a 1 \(\sigma\) probability of normal distribution. Consequently a 3 \(\sigma\) value corresponds to 99.7% probability of appearance.

2) Not subject to production test, verified by design/characterization.

Field direction definition

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.

Figure 9  Definition of magnetic field direction PG-SOT23-3-15
3.5 Electro magnetic compatibility

Characterization of electro magnetic compatibility is carried out on a sample basis from one qualification lot. Not all specification parameters have been monitored during EMC exposure.

![EMC test circuit](image)

**Figure 10** EMC test circuit

Ref: ISO 7637-2 (Version 2004), test circuit **Figure 10** (with external resistor, $R_S = 100 \, \Omega$)

**Table 8 Magnetic compatibility**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Level / Type</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Testpulse 1</td>
<td>$V_{EMC}$</td>
<td>-100 V</td>
<td>C</td>
</tr>
<tr>
<td>Testpulse 2a(^1)</td>
<td></td>
<td>60 V/110 V</td>
<td>A/C</td>
</tr>
<tr>
<td>Testpulse 2b</td>
<td></td>
<td>10 V</td>
<td>C</td>
</tr>
<tr>
<td>Testpulse 3a</td>
<td></td>
<td>-150 V</td>
<td>A</td>
</tr>
<tr>
<td>Testpulse 3b</td>
<td></td>
<td>100 V</td>
<td>A</td>
</tr>
<tr>
<td>Testpulse 4(^2)</td>
<td></td>
<td>-7 V / -5.5 V</td>
<td>A</td>
</tr>
<tr>
<td>Testpulse 5b(^3)</td>
<td></td>
<td>$U_S = 86.5 , V / U_S^* = 28.5 , V$</td>
<td>A</td>
</tr>
</tbody>
</table>

---

1) ISO 7637-2 (2004) describes internal resistance = 2 \, \Omega (former 10 \, \Omega).
2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V ±0.2 V.
3) A central load dump protection of 42 V is used. $U_S^* = 42 \, V - 13.5 \, V$. 

---

Data Sheet 16 Revision 1.2, 2019-12-20
Ref: ISO 7637-2 (Version 2004), test circuit Figure 10 (without external resistor, $R_s = 0 \Omega$)

Table 9  Electro magnetic compatibility

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Level / Type</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Testpulse 1</td>
<td>$V_{EMC}$</td>
<td>-50 V</td>
<td>C</td>
</tr>
<tr>
<td>Testpulse 2a$^1$</td>
<td></td>
<td>50 V</td>
<td>A</td>
</tr>
<tr>
<td>Testpulse 2b</td>
<td></td>
<td>10 V</td>
<td>C</td>
</tr>
<tr>
<td>Testpulse 3a</td>
<td></td>
<td>-150 V</td>
<td>A</td>
</tr>
<tr>
<td>Testpulse 3b</td>
<td></td>
<td>100 V</td>
<td>A</td>
</tr>
<tr>
<td>Testpulse 4$^2$</td>
<td></td>
<td>-7 V / 5.5 V</td>
<td>A</td>
</tr>
<tr>
<td>Testpulse 5b$^3$</td>
<td></td>
<td>$U_s = 86.5 V / U_s^* = 28.5 V$</td>
<td>A</td>
</tr>
</tbody>
</table>

1) ISO 7637-2 (2004) describes internal resistance = 2 $\Omega$ (former 10 $\Omega$).
2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V ±0.2 V.
3) A central load dump protection of 42 V is used. $U_s^* = 42 V - 13.5 V$. 

---

**Note:**
- Table 9 lists the electro magnetic compatibility parameters for the TLE4964-2M, including test pulses with designated levels and types, along with their respective statuses.
- Testpulse 1 uses $V_{EMC}$ level with values of -50 V and 50 V, and status C.
- Testpulse 2a uses 50 V, with status A.
- Testpulse 2b uses 10 V, with status C.
- Testpulse 3a uses -150 V, with status A.
- Testpulse 3b uses 100 V, with status A.
- Testpulse 4 uses -7 V / 5.5 V, with status A.
- Testpulse 5b uses $U_s = 86.5 V / U_s^* = 28.5 V$, with status A.

---

**Reference:**
- ISO 7637-2 (Version 2004), test circuit Figure 10.
4 Package information

The TLE4964-2M is available in the small halogen-free SMD package PG-SOT23-3-15.

4.1 Package outline PG-SOT23-3-15

Figure 11  PG-SOT23-3-15 package outline (all dimensions in mm)

4.2 Packing information PG-SOT23-3-15

Figure 12  Packing of the PG-SOT23-3-15 in a tape
4.3 Footprint PG-SOT23-3-15

![Footprint PG-SOT23-3-15](image)

Figure 13 Footprint PG-SOT23-3-15

4.4 PG-SOT23-3-15 distance between chip and package

![Distance between chip and package](image)

Figure 14 Distance between chip and package

4.5 Package marking

![Marking of TLE4964-2M](image)

Figure 15 Marking of TLE4964-2M
5  Graphs of the magnetic parameters

Figure 16  Operating point ($B_{op}$) of the TLE4964-2M over temperature

Figure 17  Release point ($B_{rp}$) of the TLE4964-2M over temperature

Figure 18  Hysteresis ($B_{Hys}$) of the TLE4964-2M over temperature
6 Graphs of the electrical parameters

Figure 19  Power on time $t_{\text{PON}}$ of the TLE4964-2M over temperature

Figure 20  Signal delay time of the TLE4964-2M over temperature

Figure 21  Supply current of the TLE4964-2M over temperature
Graphs of the electrical parameters

Figure 22  Supply current of the TLE4964-2M over supply voltage

Figure 23  Output current limit of the TLE4964-2M over temperature

Figure 24  Output current limit of the TLE4964-2M over applied pull-up voltage
Graphs of the electrical parameters

Figure 25  Output fall time of the TLE4964-2M over temperature

Figure 26  Output fall time of the TLE4964-2M over applied pull-up voltage

Figure 27  Output rise time of the TLE4964-2M over temperature
TLE4964-2M

Graphs of the electrical parameters

Figure 28  Output rise time of the TLE4964-2M over applied pull-up voltage

Figure 29  Output leakage current of the TLE4964-2M over temperature

Figure 30  Saturation voltage of the TLE4964-2M over temperature
Graphs of the electrical parameters

Figure 31  Saturation voltage of the TLE4964-2M over output current

Figure 32  Effective noise of the TLE4964-2M thresholds over temperature

Figure 33  Output signal jitter of the TLE4964-2M over temperature
7 Revision history

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Revision 1.2</td>
<td>2019-12-20</td>
<td>Updated text and figure in Chapter 2.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated standards in Table 4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added maximum tested magnetic field in Chapter 3.3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Editorial changes</td>
</tr>
<tr>
<td>Revision 1.0</td>
<td>2013-07-20</td>
<td>Initial release</td>
</tr>
</tbody>
</table>