TLE4929Cx / TLE4959x EEPROM Programming Guide

Application Note

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Rev 0.90, 2017-06-22	Initial version
Rev 0.91, 2018-01-29	Page 11: Bit 12 was removed from “PW_CHOICE” to “not used”
Rev 1.00, 2018-02-14	Official releasetogether with datasheet version 1.0
Rev 1.10, 2018-09-11	Combine derivaties TLE4929Cx and TLE4959x into one programming guide / editorial updates / clarification on margin test
Rev 1.20, 2019-06-04	Page 17: Table 4-3: Max limit of EEPROM programming voltage increased / . . . . . . Page 26: Table 7-1: Steps 4 and 8 added: Disable/Enable open drain output
Rev 1.30, 2020-03-23	Page 5 / chapter 1.2: new derivative TLE4929C-XHA added Page 9 / chapter 2: in table 2-1, line 0b1010 - 0xA, “set” changed to “reset” Page 15 / chapter 3.1: table 3-8 added for new derivative TLE4929C-XHA Page 16 / chapter 3.1: table 3-9 added for new derivative TLE4929C-XHA Page 25 / chapter 6.1: in table 6-1 new derivative TLE4929C-XHA added Page 25 / chapter 6.2: in table 6-2 new derivative TLE4929C-XHA added Page 28 / chapter 7: in table 7-1 new derivative TLE4929C-XHA added

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1 Supply Voltage Interface

All internal data is organized in a memory-like setup. Each data value or EEPROM parameter is located at a specific address. The data width is always 16 bit. The communication with the IC is done with a modulation of the supply voltage on the VS pin. The sensor is initially switched to a communication mode and commands are sent in this way. The sensor responds with a modulated signal on the VOUT pin.

1.1 Definition of interface timing

All timings and voltage levels for communication are specified in **Table 4-1** and **Table 4-2**.

One bit has the length tbit. The length of the time for the HIGH level within tbit determines whether it is considered as a “1” or a “0”. If the HIGH time is larger as the LOW time, it is considered as a “1”, otherwise it is a “0”. A ratio of 1/3 and 2/3 or ¼ and ¾ is recommended for save communication.

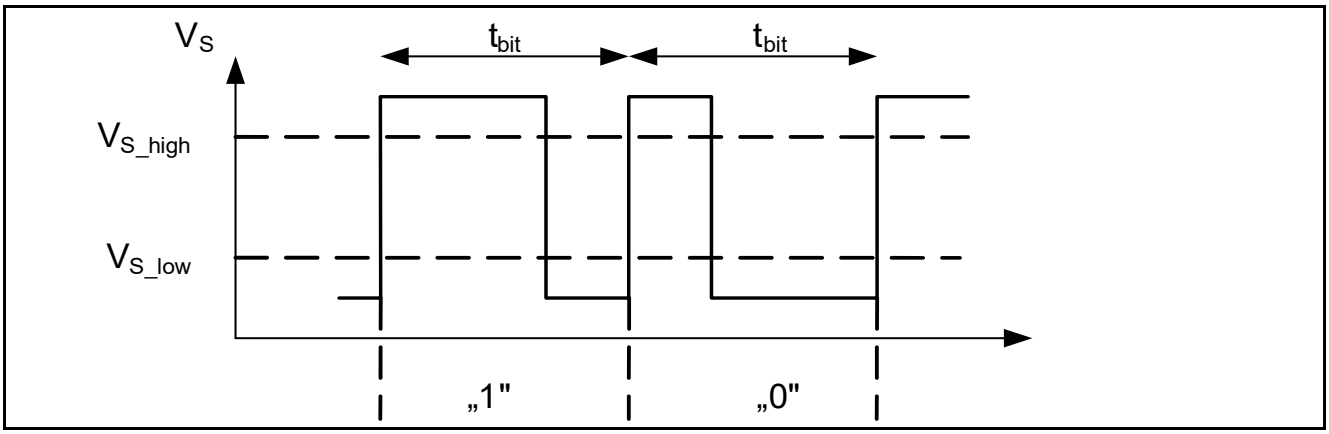

Figure 1-1 Definition of “1” and “0”

1.2 Enter Communication Mode

To enter the supply interface a special modulation sequence (**TLE4929C-XAx/TLE4959x:**"1111-0000-1100-1101" / **TLE4929C-XVAx:** “1101-1100-0000-1101” / **TLE4929C-XHAx:** "1110-1100-0000-1101") has to be applied shortly after Power On (within tSUPPLY,enter). After the last bit an additional pulse “P” has to be issued.

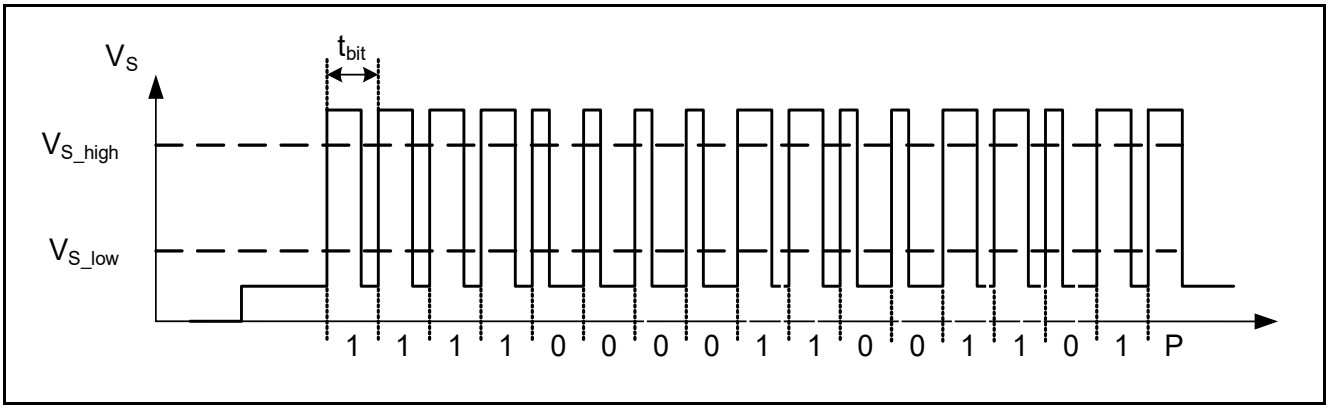

Figure 1-2 VS sequence to enter communication mode

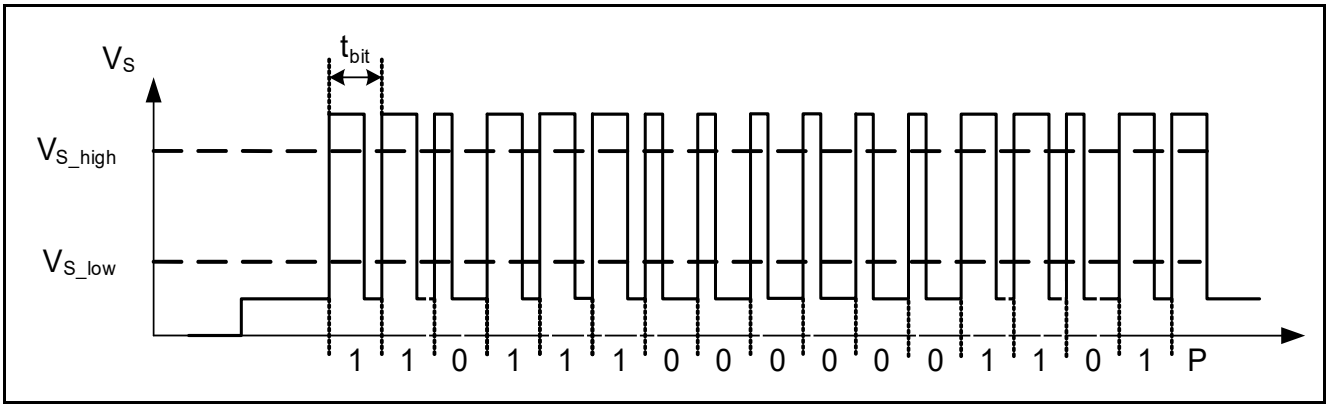

Figure 1-3 VS sequence to enter communication mode

A second frame has to be send which configures the IC to send data to the output pin VOUT. This command is 0x00D15000 +additional pulse (= 0000-0000-1101-0001-0101-0000-0000-0000-0)

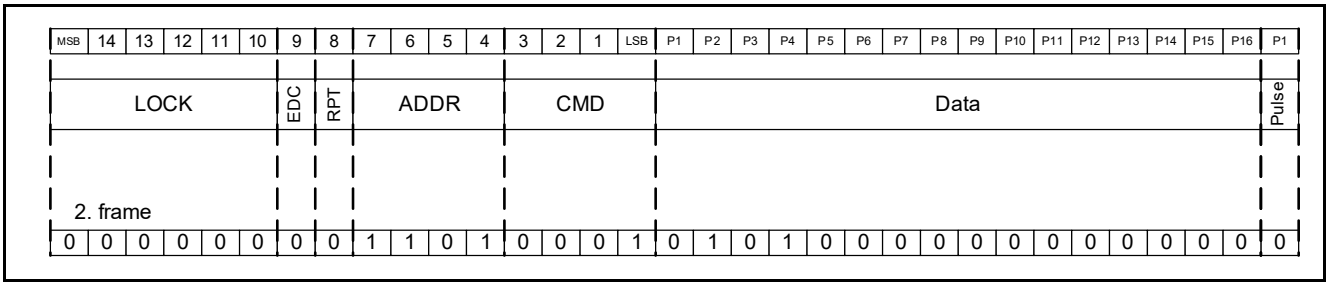

Figure 1-4 2. frame to be sent to enter communication mode: signal to VOUT

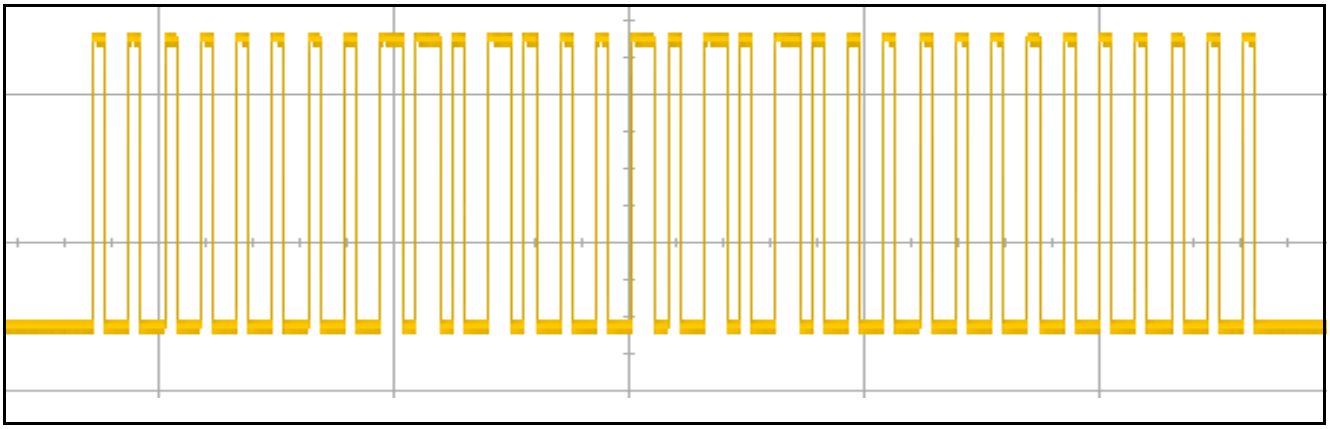

Figure 1-5 2. frame to be sent to enter communication mode: signal to VOUT

After the 2.frame a 3.frame has to be sent which is the command “EEPROM refresh”.

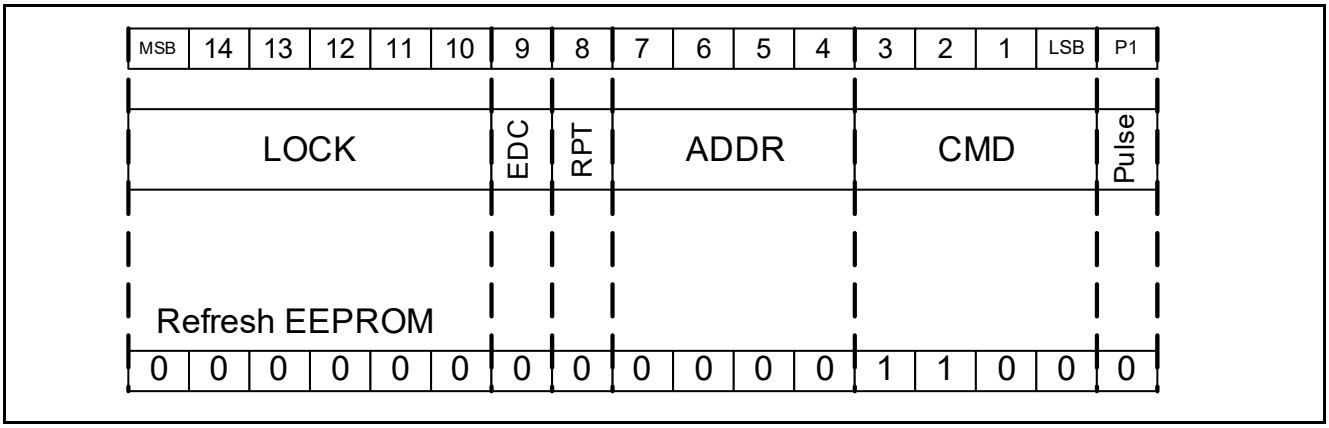

Figure 1-6 3. frame: EEPROM refresh

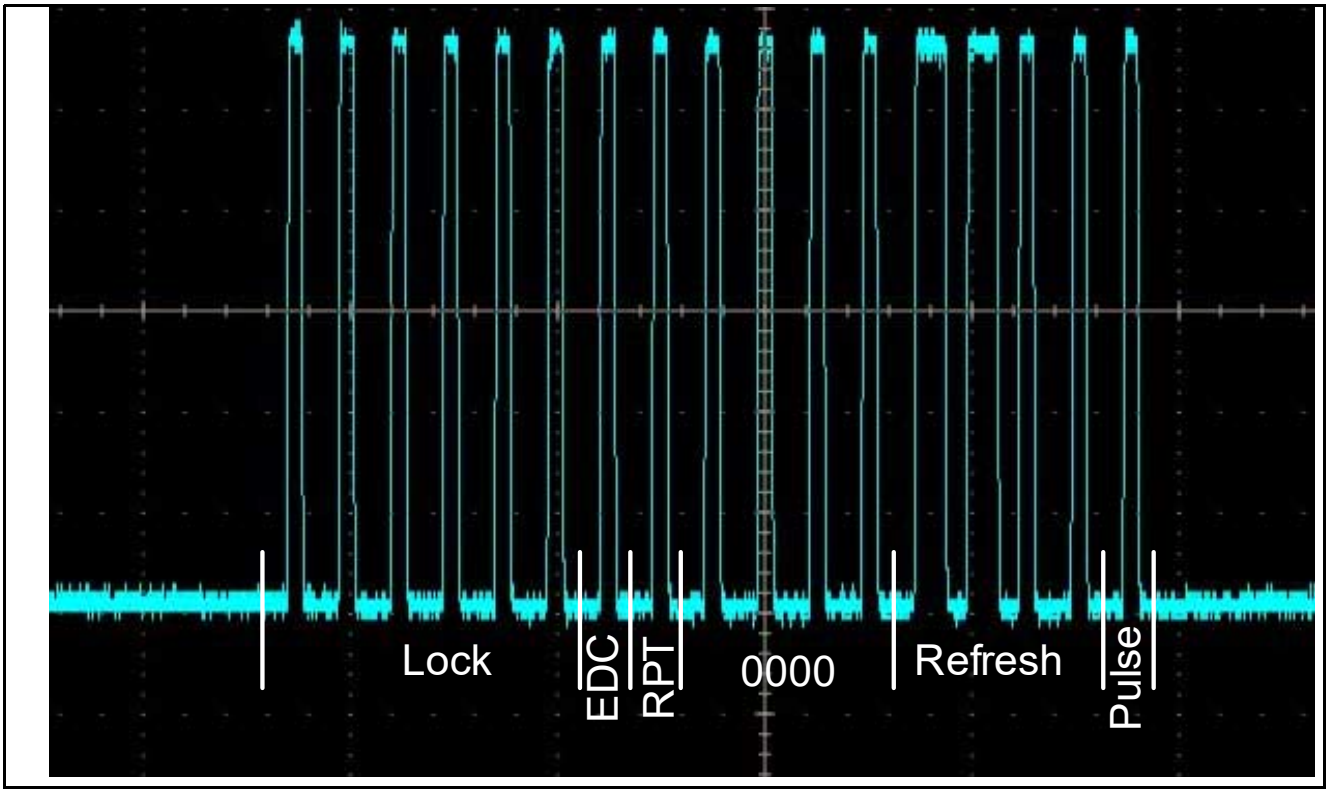

Figure 1-7 3. frame: EEPROM refresh

Now the IC is in communication mode and the commands shown in **Table 2-1** can be sent. Content of EEPROM addresses can be read (**Chapter 5.1**) or new content can be written to specific addresses (**Chapter 5.2**). The EEPROM can be burned with the written content using a special sequence of frames explained in **Chapter 5.3**.

1.3 Terminate Communication Mode

To leave the communication mode, there are several possibilities:

Set VS voltage to high level VS_high for a time longer than tSupplyhigh,exit. This automatic exit function of the test mode will be ignored in case the command (0000-0000-1101-0001-0101-0000-0000-0000-0) is sent

Disconnect VS

2 Commands

Each command word consists of 16 bit. An additional pulse (bit) has to be appended on each command. There are several possibilities where to place the additional pulse.

Single-command (e.g. EEPROM refresh):

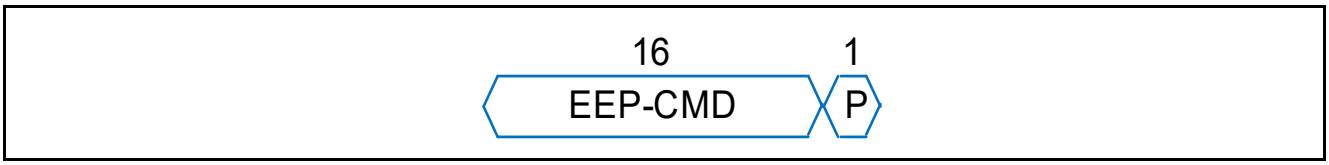

Figure 2-1 Single command

Single write command:

Simply append the additional pulse after the data. After that pulse the next command may follow immediately

Figure 2-2 Single write command

Single read-command: By appending the additional pulse after the command, the following 16 pulses will fit to the data word. After that pulse the next command may follow immediately

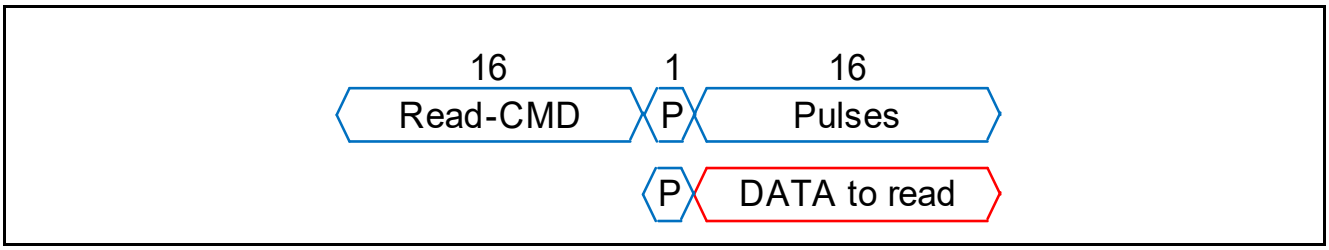

Figure 2-3 Single read command

EEPROM margin command: After the command an additional pulse has to be add. After that the trigger-pulse is necessary, but before triggering the margin, the margin-voltage has to be applied at VOUT. Keep Vmargin stable for tstop after the trigger pulse. Then use a stop-pulse to be able to execute the readout commands for reading the result (**Chapter 7**).

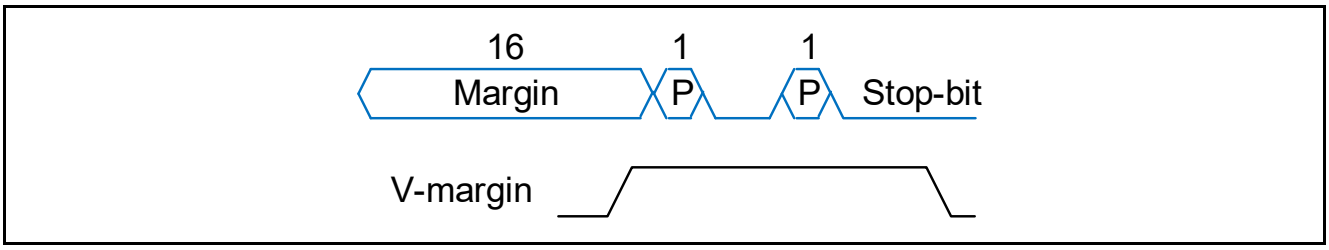

Figure 2-4 EEPROM margin command

The following table shows the structure of the 16-bit command word.

Table 2-1 Command Word

Bit	Name	Description
[15 .. 10]	LOCK	
	0x00	default operating access
[9]	EDC-OFF	1: At read or write of EEPROM-Data, Error correction will be switched off. No correction and no EDC-generation 0: Error correction is on
[8]	RPT	Read-CMD: Command sent in during read, will be executed Write-CMD: Continuous Write to the same address until CS will abort the transfer
[7 .. 4]	ADDR	Start address of read or write transfer
[3 .. 0]	CMD	Read/Write or EEPROM-Command
	0b0000 - 0x0	Normal read command
	0b0001 - 0x1	Normal write command
	0b0010 - 0x2	Read command - reads EDC-Bits of addressed EEPROM-line and EDC-Status
	0b0011 - 0x3	Write command - writes EDC-Bits of addressed EEPROM -line (EDC should be off)
	0b0100 - 0x4	Margin Test
	0b0101 - 0x5	Margin Zero Test
	0b0110 - 0x6	Program Zeros of EEPROM - stupid
	0b0111 - 0x7	Program Ones of EEPROM - stupid
	0b1000 - 0x8	Set: EVEN reset / ODD reset
	0b1001 - 0x9	Set: EVEN reset / ODD set (Checkerboard)
	0b1010 - 0xA	Set: EVEN set / ODD reset (inverted checkerboard)
	0b1011 - 0xB	Set: EVEN set / ODD set
	0b1100 - 0xC	Refresh EEPROM
	0b1101 - 0xD	--
	0b1110 - 0xE	Program Zeros of EEPROM - intelligent
	0b1111 - 0xF	Program Ones of EEPROM - intelligent

3 Register Map

The register values in the address 0x00 and 0x01 can be set by the user and specify the algorithm of the sensor.

Table 3-1 Adress Table

0x00	EEPROM-Address 0x00 – **Crank/Cam/Transmission setting [15:0]**
0x01	EEPROM-Address 0x01 – **Crank/Cam/Transmission setting [15:0]**
0x02	EEPROM-Address 0x02 – oscillator-rise/fall-temperature coefficient trimming [15:0]
0x03	EEPROM-Address 0x03 – full scale – hall supply trimming [15:0]
0x04	Tracking Value Differential [13:0]
0x05	Found_min_diff [15], Differential Minima [13:0]
0x06	Found_max_diff [15], Differential Maxima [13:0]
0x07	Differential offset [10:0]
0x08	Found_min_cent [15], Center Minima [13:0]
0x09	Found_max_cent[15], Center Maxima [13:0]
0x0A	Center offset [10:0]
0x0B	Backbias DAC [7:0]
0x0C	EEPROM programming status [15:0]
0x0D	Testsettings / Bist / Dither [15:0]
0x0E	Analog-Digital Testmux / PowerDowns / HTM [15:0]
0x0F	Tracking Value Center [13:0]

Found_min*/Found_max* = 1 signals a valid extrema in differential or center path.

3.1 EEPROM Register Map

Table 3-2 TLE4929C-XAx: EEPROM Register 0x00

bit	name	description	r/w	remark
[15]	not used		r	read as “0”
[14]	STOP_ENABLE	0 = Disable start/stop mode 1 = Enable start/stop mode	rw	
[13]	HIGH SPEED	0 = Enabled motion detection 1 = same pulse and phase as before when above 1.5 kHz	rw	
[12]	DIR CHANGE	0 = 1/4 Criteria 1 = 1/8 Criteria	rw	
[11]	WATCHDOG ENABLE	0 = Watchdog off 1 = Watchdog on	rw	
[10:2]	not used	to be set to “000000000”	rw	
[1]	PULSE_WIDTH	0 = default length for all pulses 1 = all pulse lengths shortened by 4 µs	rw	
[0]	POLE_WHEEL	0 = self calibration on start up - back bias application 1 = center and differential path set to 0 mT on start up - pole wheel application	rw	

Table 3-3 TLE4929C-XAx: EEPROM Register 0x01

bit	name	description	r/w	remark
[15:14]	not used	to be set to “00”	rw	
[13]	PW_CHOICE	Choice of pulse length at direction detection forwards / backwards time, pulse length is 3 µs shorter by default and can be shortened by additional 4µs with the PULSE_WIDTH bit 0 = 45/90 µs 1 = 45/135 µs	rw	
[12]	not used	to be set to “0”	rw	
[11]	FORWARD_DEF	0 = none invertion of forward definition 1 = invertion of forward definition	rw	
[10]	EDGE_POLAR	0 = non-inverted 1 = inverted	rw	
[9]	HYST_ADAPT	0 = 25% 1 = 31.5%	rw	
[8]	HYST	0 = 0.75 mT_{pkpk} 1 = 1.5 mT_{pkpk}	rw	
[7]	HYST_TYPE	0 = Hidden adaptive hysteresis 1 = Visible adaptive hysteresis	rw	
[6:5]	DNC_MIN	Following value is used for uncalibrated mode: 00 = 0.75 mT_{pkpk} 01 = 1.5 mT_{pkpk} 10 = 2.5 mT_{pkpk} 11 = 5 mT_{pkpk}	rw	
[4]	DNC_ADAPT	Following value is used for uncalibrated mode: 0 = 25% 1 = 31.5%	rw	
[3]	CRANK_TEETH	0 = 58 teeth 1 = 32 teeth	rw	
[2]	DIR_ENABLE	0 = Direction detection off 1 = Direction detection on	rw	
[1]	ADAPT_FILT	0 = slow adaptation tracking: average over 32/58 (CRANK_TEETH) edges… 1 = fast adaptation tracking: each valid min/max is considered if the extremes are bigger 5 times, with a full update of the ODAC	rw	
[0]	LOCK	0 = User area of EEPROM is unlocked 1 = User area of EEPROM is locked (no reprogramming possible)	rw	

Table 3-4 TLE4959xx-FX: EEPROM Register 0x00

bit	name	description	r/w	remark
[15]	not used		r	read as “0”
[14]	not used	to be set to “0”	rw	
[13]	HIGH SPEED	0 = Enabled motion detection 1 = According selected protocol when above 4.3 kHz	rw	

Table 3-4 TLE4959xx-FX: EEPROM Register 0x00

bit	name	description	r/w	remark
[12]	not used	to be set to “0”	rw	
[11]	STAND_EN	0=disable stand-still pulse 1=enable stand-still pulse Stand still pulse is provided, if enabled, only if PW_CHIOICE=00	rw	
[10:0]	not used	to be set to “00000000000”	rw	

Table 3-5 TLE4959xx-FX: EEPROM Register 0x01

bit	name	description	r/w	remark
[15:14]	not used	to be set to “01”	rw	
[13:12]	PW_CHOICE	Choice of PWM protocol for direction detection. 00 = Option 1 01 = Option 2 10 = Option 3 11 = Option 4	rw	
[11]	FORWARD_DEF	0 = none invertion of forward definition 1 = invertion of forward definition	rw	
[10]	EDGE_POLAR	0 = non-inverted 1 = inverted	rw	
[9]	HYST_ADAPT	0 = 25% 1 = 12.5%	rw	
[8:5]	not used	to be set to “1101”	rw	
[4]	DNC_ADAPT	DNC Adaption: 0 = 25% 1 = 12.5%	rw	
[3]	not used	to be set to “0”	rw	
[2]	DIR_ENABLE	0 = Direction detection off 1 = Direction detection on	rw	
[1]	not used	to be set to “1”	rw	
[0]	LOCK	0 = User area of EEPROM is unlocked 1 = User area of EEPROM is locked (no reprogramming possible)	rw	

Table 3-6 TLE4929C-XVAx: EEPROM Register 0x00

bit	name	description	r/w	remark
[15]	not used		r	read as “0”
[14]	STOP_ENABLE	0 = Disable start/stop mode 1 = Enable start/stop mode	rw	
[13]	HIGH SPEED	0 = Enabled motion detection 1 = Same pulse and phase as before when above 1.5 kHz when TSS=‘0’ 1 = Always short pulse or high speed pulse on last direction dependent phase above 4 kHz when TSS=‘1’	rw	

Table 3-6 TLE4929C-XVAx: EEPROM Register 0x00

bit	name	description	r/w	remark
[12]	DIR CHANGE	0 = 1/4 Criteria for direction change 1 = 1/8 Criteria for direction change	rw	
[11]	WATCHDOG ENABLE	0 = Watchdog off 1 = Watchdog on Not enabled if TSS='1'. If TSS='1' this bit activates the stand still pulse for protocol 00	rw	
[10:9]	DELAY_TIME	Programmable delay time in speed-signal path 00 = 14 µsec 01 = 17 µsec 10 = 20 µsec 11 = 23 µsec	rw	
[8:6]	PW_CHOICE	Choice of pulse length at direction detection forwards/backwards time: Protocol available in TSS=0: xxx = forward/reverse/standstill 000 = 45/90/180 µs 001 = 45/180/360 µs 010 = 45/135/180 µs 011 = 75/600/360 µs 100 = 22/45/90 µs 101 = 60/120/360 µs 110 = 30/60 µs/ - (specification VW) 111 = 90/135/360 µs	rw	
[8:6]	PW_CHOICE	Protocol available in TSS=1: xxx = forward / reverse / start up / opt. high speed / opt. standstill 000 = 60/120/30/30/360 µs 001 = 45/180/ - /45/360 µs 010 = 45/135/ - /45/360 µs 011 = 45/135/180/45/360 µs 100 = 45/90/180/45/180 µs 101 = 22/45/90/22/180 µs 110 = 90/135/180/30/60 µs 111 = 90/135/180/30/180 µs	rw	
[5]	STAND_STILL_TIMEOUT	Only used when STAND_STILL_ENABLE=1: 0 = 40 msec delaytime after the last sent pulse 1 = 80 msec delaytime after the last sent pulse	rw	
[4]	WATCHDOG_TIMEOUT	Only used in TSS=0: 0 = WATCHDOG_TIMEOUT off 1 = 1.4 sec time out at power on to remain in calibration state	rw	
[3]	VW_FW_START	Only used when VW-crankshaft-protocol is enabled 0 = No pulse on first edge, on second edge delayed or active edge 1 = First edge is issued according forward-direction	rw	
[2]	not used	to be set to "0"	rw	

Table 3-6 TLE4929C-XVAx: EEPROM Register 0x00

bit	name	description	r/w	remark
[1]	PULSE_WIDTH	0 = default length for all pulses 1 = all pulse lengths shortened by 4 µs	rw	
[0]	POLE_WHEEL	0 = self calibration on start up - back bias application 1 = center and differential path set to 0mT on start up - pole wheel application	rw	

Table 3-7 TLE4929C-XVAx: EEPROM Register 0x01

bit	name	description	r/w	remark
[15]	not used	to be set to “0”	rw	
[14]	FILTER_SELECT	0 = Speed path optimized for low jitter-performance 1 = Speed path optimized for frequency above 8 kHz	rw	
[13]	TSS	0 = forward-pulses and reverse-pulses are issued in case of vibration and passing switching-point (crankshaft application) 1 = alternating forward- and reverse-pulses are suppressed (transmission application)	rw	
[12]	STAND_STILL_ENABLE	0 = no optional stand still pulse 1 = optional stand still pulse activated	rw	
[11]	FORWARD_DEF	0 = none invertion of forward definition 1 = invertion of forward definition	rw	
[10]	EDGE_POLAR	0 = non-inverted 1 = inverted	rw	
[9]	HYST_ADAPT	0 = 25% 1 = 31.5%	rw	
[8]	not used	to be set to “0”	rw	
[7]	HYST_TYPE	0 = Hidden adaptive hysteresis 1 = Visible adaptive hysteresis	rw	
[6:5]	DNC_MIN	Following value is used for uncalibrated mode: 00 = 0.75 mT_{pkpk} 01 = 1.5 mT_{pkpk} 10 = 2.5 mT_{pkpk} 11 = 5 mT_{pkpk}	rw	
[4]	DNC_ADAPT	Following value is used for uncalibrated mode: 0 = 25% 1 = 31.25% (TSS=’0’) = 12.5% (TSS=’1’)	rw	
[3]	CRANK_TEETH	0 = 58 teeth 1 = 32 teeth	rw	
[2]	DIR_ENABLE	0 = Direction detection off 1 = Direction detection on	rw	

Table 3-7 TLE4929C-XVAx: EEPROM Register 0x01

bit	name	description	r/w	remark
[1]	ADAPT_FILT	0 = slow adaptation tracking: average over 32/58 (CRANK_TEETH / active edges) 1 = fast adaptation tracking: each valid min/max is considered if the extremes are bigger 5 times, with a full update of the ODAC	rw	
[0]	LOCK	0 = User area of EEPROM is unlocked 1 = User area of EEPROM is locked (no reprogramming possible)	rw	

Table 3-8 TLE4929C-XHAx: EEPROM Register 0x00

bit	name	description	r/w	remark
[15]	DNC_ADAPT	Following value is used for uncalibrated mode: 0 = 25% 1 = 31.25%	rw	read as “0”
[14]	STOP_ENABLE	0 = Disable stop mode 1 = Enable stop mode	rw	
[13]	HIGH SPEED	0 = Enabled motion detection 1 = Same pulse and phase as before when above 1.5 kHz	rw	
[12]	DIR CHANGE	0 = 1/4 Criteria for direction change 1 = 1/8 Criteria for direction change	rw	
[11]	WATCH_DOG_EN	0 = Watchdog off 1 = Watchdog on	rw	
[10:9]	DELAY_TIME	Programmable delay time in speed-signal path: 00 = 14 µsec 01 = 17 µsec 10 = 20 µsec 11 = 23 µsec	rw	
[8:6]	PW_CHOICE	Choice of pulse length at direction detection forwards/backwards time: xxx = forward/reverse/otional standstill 000 = 45/90 /180 µs 001 = 45/180/360 µs 010 = 45/135/180 µs 011 = 75/600/360 µs 100 = 22/45/90 µs 101 = 60/120/360 µs 110 = 30/60 µs / - (OEM specific) 111 = 90/135/360 µs	rw	
[5]	STAND_STILL_TIMEOUT	Only used when STAND_STILL_ENABLE = 1: 0 = 40 msec delaytime after the last sent pulse 1 = 80 msec delaytime after the last sent pulse	rw	
[4]	WATCHDOG_TIMEOUT	0 = WATCHDOG_TIMEOUT off 1 = 1.4 sec time out at power on to remain in calibration state	rw	
[3]	OEM_FW_START	When “PW_CHOICE” is “110”: 0 = No pulse on first edge, on second edge delayed or active edge 1 = First edge is issued according forward-direction	rw	

Table 3-8 TLE4929C-XHAx: EEPROM Register 0x00

bit	name	description	r/w	remark
[2]	WATCHDOG_HYBRID	0 = WATCHDOG_HYBRID off 1 = No calibration during electric drive of hybrid vehicle	rw	
[1]	STAND_STILL_ENABLE	0 = No optional stand still pulse 1 = Optional stand still pulse activated	rw	
[0]	POLE_WHEEL	0 = Back bias self calibration on start up - back bias application 1 = Back bias center and differential path set to ~0 mT	rw	

Table 3-9 TLE4929C-XHAx: EEPROM Register 0x01

bit	name	description	r/w	remark
[15:12]	K-FACTOR	Programmable switching threshold: 0000 = 39.1% 0001 = 40.6% 0010 = 42.2% 0011 = 43.8% 0100 = 45.3% 0101 = 46.9% 0110 = 48.4% 0111 = 50.0% 1000 = 51.6% 1001 = 53.1% 1010 = 54.7% 1011 = 56.3% 1100 = 57.8% 1101 = 59.4% 1110 = 60.9% 1111 = 62.5%	rw	
[11]	FORWARD_DEF	0 = None invertion of forward definition 1 = Invertion of forward definition	rw	
[10]	EDGE_POLAR	0 = Non-inverted 1 = Inverted	rw	
[9]	HYST_ADAPT	0 = 25% 1 = 31.25%	rw	
[8]	FILTER_SELECT	0 = Speed path optimized for low jitterperformance 1 = Speed path optimized for frequency above 8 kHz	rw	
[7]	HYST_TYPE	0 = Hidden adaptive hysteresis 1 = Visible adaptive hysteresis	rw	
[6:5]	DNC_MIN	Minimal DNC (Digital Noise Constant): 00 = 0.75 mT_{pkpk} 01 = 1.5 mT_{pkpk} 10 = 2.5mT_{pkpk} 11 = 5 mT_{pkpk}	rw	
[4:3]	CRANK_TEETH	00 = 58 teeth 01 = 56 teeth 10 = 34teeth 11 = 32 teeth	rw	

Table 3-9 TLE4929C-XHAx: EEPROM Register 0x01

bit	name	description	r/w	remark
[2]	DIR_ENABLE	0 = Direction detection off 1 = Direction detection on	rw	
[1]	ADAPT_FILT	0 = Slow adaptation tracking: average over 32/34/56/58 (CRANK_TEETH/active edges) 1 = Fast adaptation tracking: each valid min/max is considered if the extremes are bigger 5 times, with a full update of the ODAC	rw	
[0]	LOCK	0 = User area of EEPROM is unlocked 1 = User area of EEPROM is locked (no reprogramming possible)	rw	

4 Timing & voltage levels for communication

The following tables show the timing and voltage levels which have to be applied for communication.

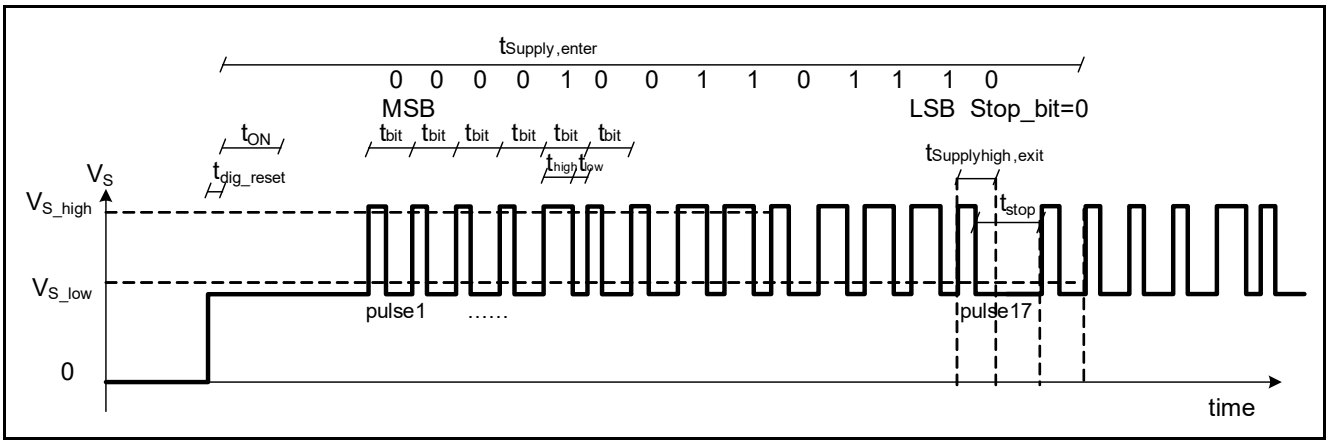

Figure 4-1 Supply voltage timing

Table 4-1 Timing requirements for communication

Parameter	Symbol	Limits			Unit	Notes
		MIN.	TYP.	MAX.		
Startup time	t_{dig_reset}		16		clocks	Duration of digital reset (prolonged analog reset)
Startup time	t_{ON}		100		µs	Startup_end signal
Time allowed to enter test-mode	$t_{Supply,enter}$		43		ms	2^18 * 6 MHz Period
High/Low decision threshold			1			If high time is longer than low a 1 is decoded
Bit length	t_{bit}	2		1860	µs	thigh + tlow
	t_{high}	1		620	µs	
	t_{low}	1		1240	µs	
Bit length tolerance	t_{bit}	-10		10	%	
Duty cycle “0” bit	t_{high_0}	15		43	%	
Duty cycle “1” bit	t_{high_1}	57		85	%	
Exit communication pulse length	$t_{Supplyhigh,exit}$	748			µs	
Stop length	t_{stop}	748			µs	

For the communication with the IC two levels of the supply voltage VS are needed to distinguish between a “1” and a “0”. The minimum value for the HIGH level and the maximum value for the LOW level are given in **Table 4-2**. These voltage levels must be available directly on the pin. In case a series resistor is used the voltage drop on this resistor has to be taken into account. The minimum required bit length is dependent on the driving capability of the voltage supply to charge and discharge the capacitor.

Table 4-2 Voltage thresholds for Interface on supply line

Parameter	Symbol	Limits			Unit	Notes
		MIN.	TYP.	MAX.		
High level	V_{S_high}	10.5		18.0	V	V_S to be recognized as HIGH level
Low level	V_{S_low}	5.0		7.5	V	V_S to be recognized as LOW level

To burn content from the registers to the EEPROM a programming voltage has to be applied directly on the VOUT pin (without pull-up resistor). The value for this burning voltage is given in **Table 4-3**.

Table 4-3 Programming voltage on output pin

Parameter	Symbol	Limits			Unit	Notes
		MIN.	TYP.	MAX.		
EEPROM programming voltage on V_{OUT}	V_{OUT_PROG}	20.5	20.6	21.0	V	
EEPROM write and erase time	t_{WRITE_ERASE}	35.8			ms	write or erase
EEPROM programming temperature (ambient)	T_{PROG}	15	25	80	°C	

5 Frame Structure for Communication

In this paragraph the structure of the frames for READ, WRITE and burning of EEPROM is shown.

5.1 Reading of EEPROM Content

To read the content of a specific address the following READ frame has to be send via supply line VS after entering the communication mode as described in **Chapter 1.2**.

Frame structure is shown below:

MSB	14	13	12	11	10	9	8	7	6	5	4	3	2	1	LSB	P1	P1	P2	P3	P4	P5	P6	P7	P8	P9	P10	P11	P12	P13	P14	P15	P16
LOCK						EDC	RPT	ADDR				CMD				Pulse	16 Pulses															
Read ADDR 0:																																
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Read ADDR 1:																																
0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Figure 5-1 Structure of a READ frame

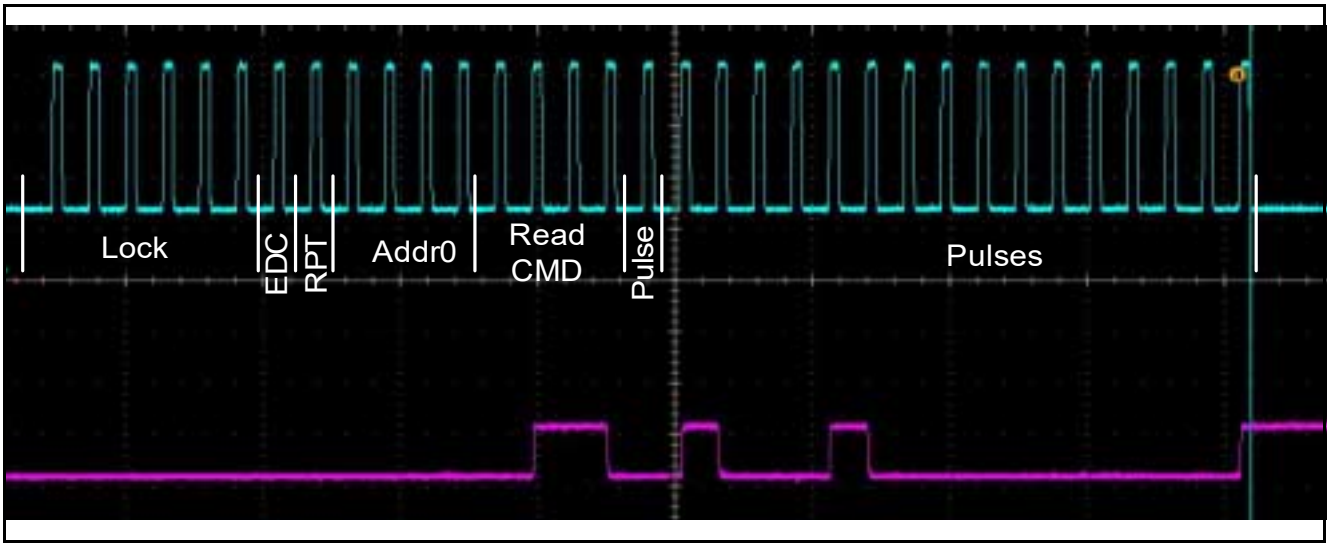

Figure 5-2 Read Addr0

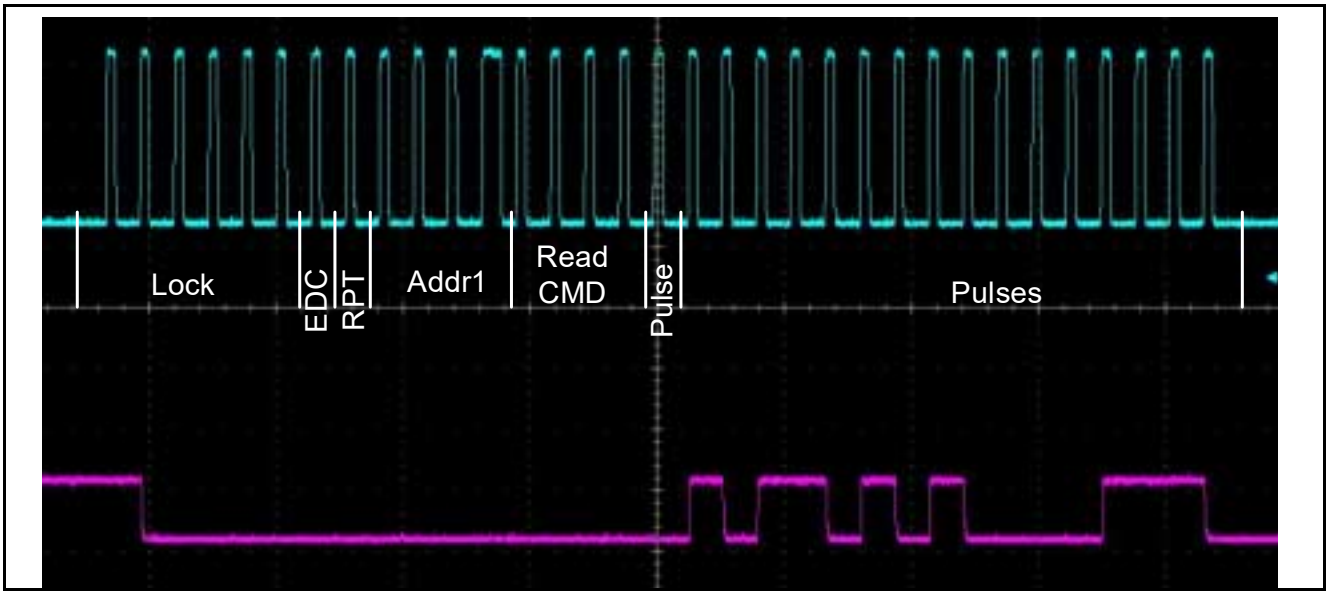

Figure 5-3 Read Addr1

After sending the READ command and the extra pulse, 16 pulses have to be provided at V_S to clock out the information on the V_{OUT} pin starting with the MSB. With each rising edge the V_{OUT} pin has the corresponding state of the specific register (“1” or “0”). To account for the settling time of the signal at the V_{OUT} pin (due to external circuitry for example), a delay should be used before taking the information on the V_{OUT} pin as valid. It is recommended to read the V_{OUT} information shortly before sending the next rising edge of the next pulse. In this way, the complete content of an address (16 bit) is read.

5.2 Writing of EEPROM Content

To write content to an EEPROM address, the following 33-bit frame must be used. Each WRITE frame writes the complete 16-bit content of an address. The 16-bit data word, which is sent after the WRITE command, contains the information which is written to the register. And additional pulse has to be appended at the end of the frame. In the example shown the 16-bit word 1000-1000-0000-0000 is written to the specified address.

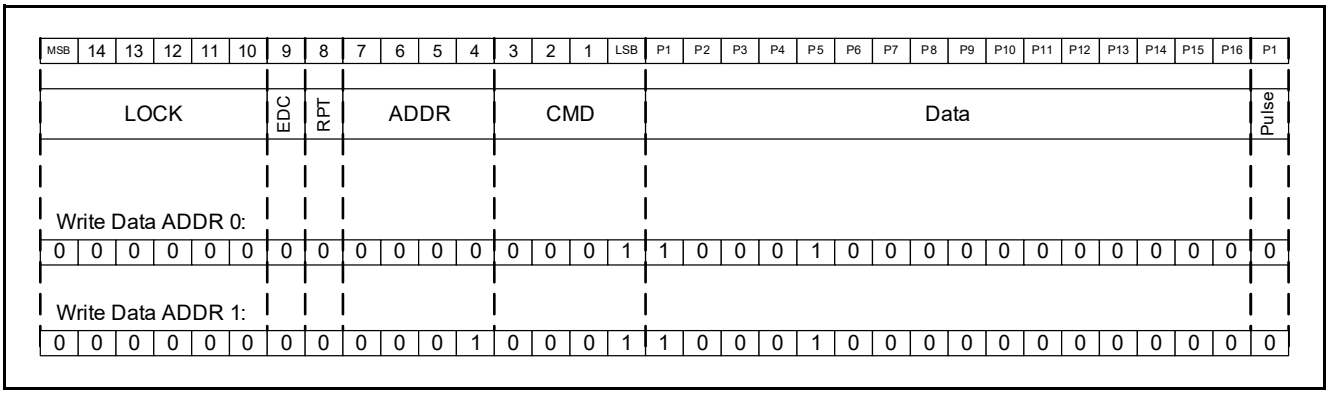

Figure 5-4 Structure of a WRITE frame

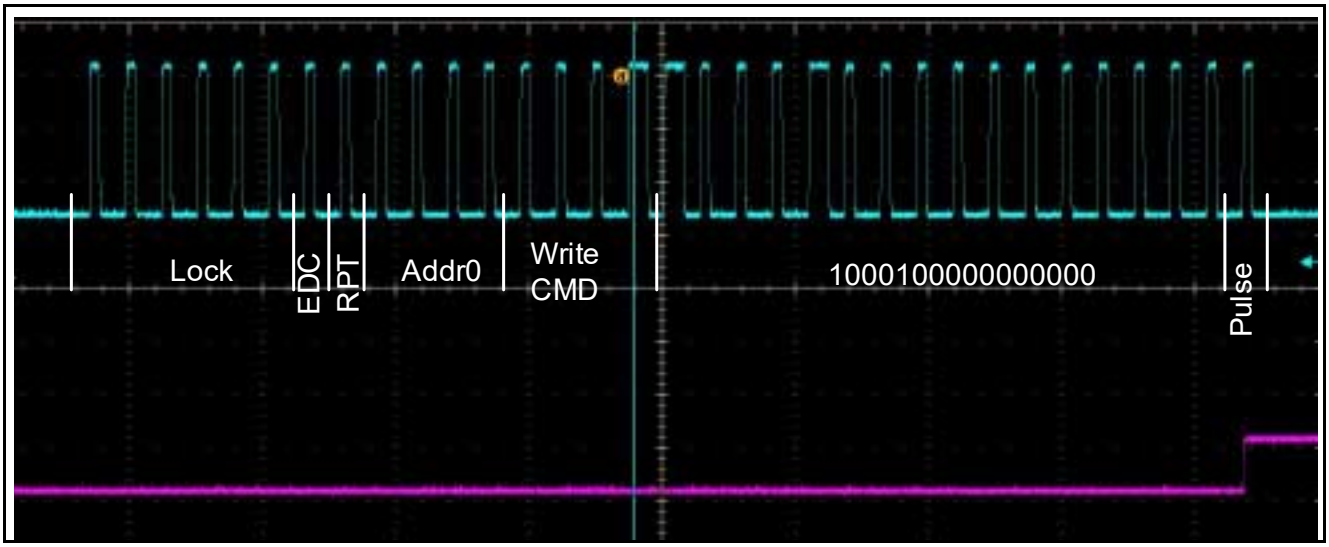

Figure 5-5 Write Addr0

5.3 Burning of EEPROM

After writing content to a EEPROM address, the EEPROM has to be burned sending a specific set of frames while the applied voltage at the VOUT pin (directly on the pin without pull-up resistor) has to be in the range given by **Table 4-3** (VOUT_PROG). The ”0” and “1” values of the EEPROM have to be burned sequentially with the command 0b1110 (burn “0”) and 0b1111 (burn “1”).

The detailed sequence how to burn the EEPROM is as follows:

After entering the communication mode (3 frames as specified in **Chapter 1.2**), the desired content has to be written to the address 0x00 and 0x01 using the WRITE frame (**Chapter 5.2**). Before starting with the EEPROM burning sequence, the voltage at the V_{OUT} pin has to be applied according to the values given in **Table 4-3**. The first frame to be sent is the “Programming Pulse Definition” (+ appended pulse):
0000-0000-1011-0001-0000-0001-0000-0010-0.

The automatic exit function (see **Chapter 1.3**) must be disabled.

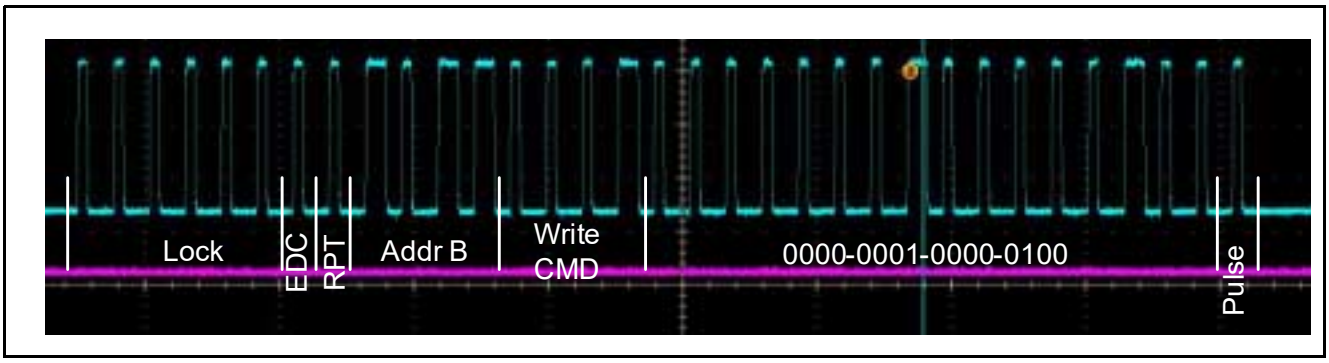

Figure 5-6 Programming Pulse Definition

As next, the frame “Burn0” has to be sent (0000-0000-0000-1110-0).

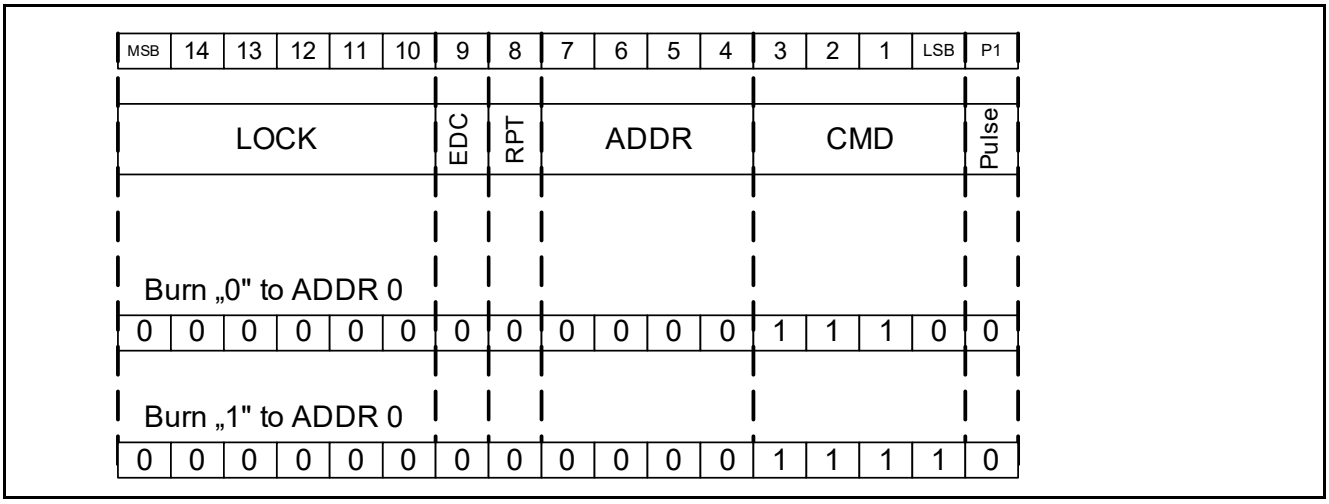

Figure 5-7 Structure of the frame: Burn EEPROM

After the “Burn0” command s sent it is important that the voltage level at V_S is kept at V_{S_high} while V_{OUT_PROG} is applied for 35.8 ms. Afterwards the V_S level must be set back to V_{S_low} before the next frame can follow.

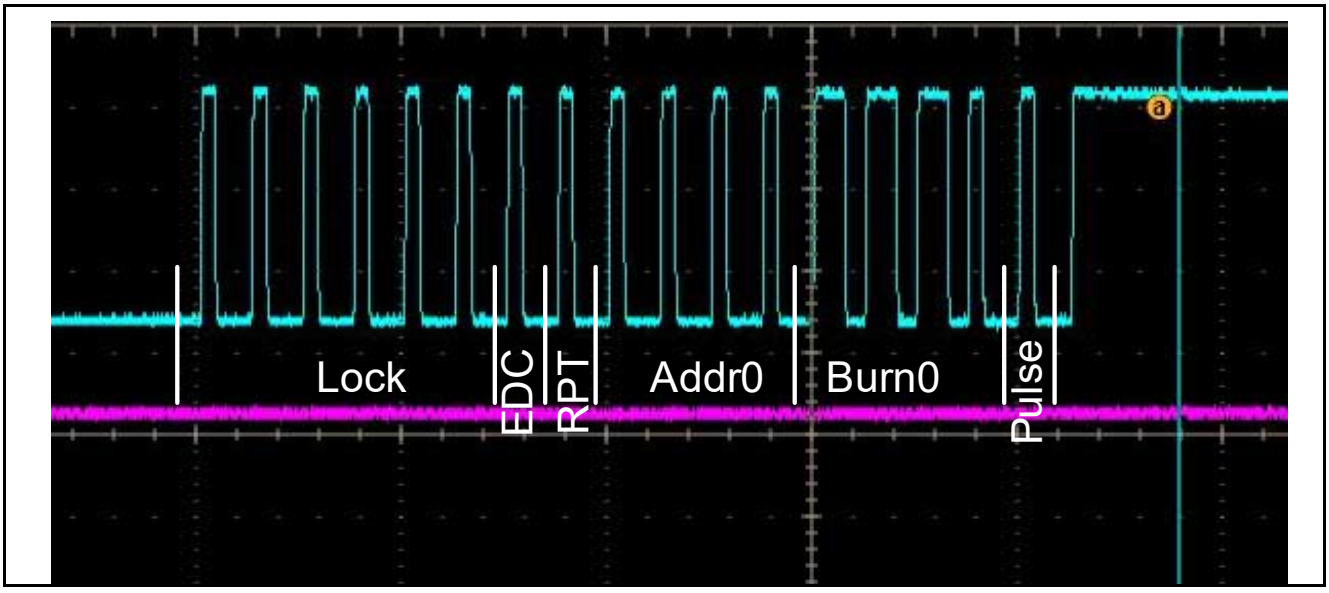

Figure 5-8 Burn “0” of EEPROM Address 0

Now, the WRITE commands have to repeated which write the desired content in the EEPROM addresses. This frame is followed by the “Burn1” frame (0000-0000-0000-1111-0).

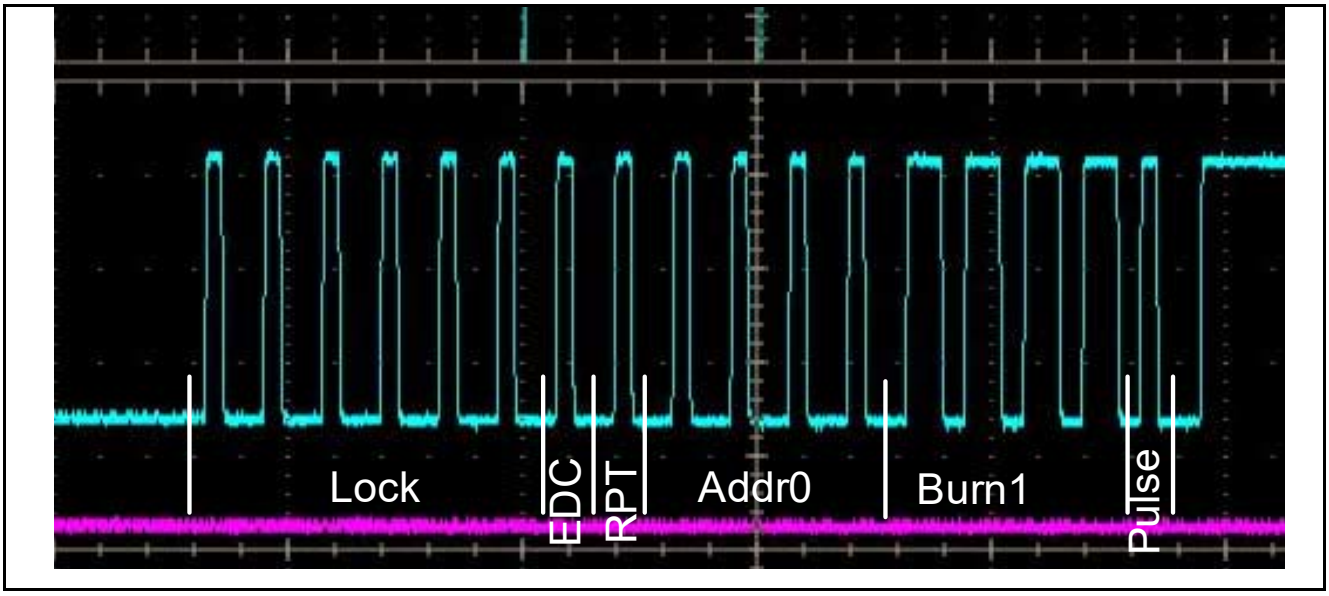

Figure 5-9 Burn “1” of EEPROM Address 0

Again, after the “Burn1” command is sent it is important that the voltage level at V_S is kept at V_{S_high} while V_{OUT_PROG} is applied for 10 ms. Afterwards, the V_S level must be set back to V_{S_low} before the next frame can follow.The burning of the EEPROM is now finished.

It is recommended, to read again the content of the programmed addresses to verify whether the EEPROM burning process was successfully.

The complete sequence of frames for the EEPROM burning is shown in **Figure 5-10**. The additional pulse is always included in the frame.

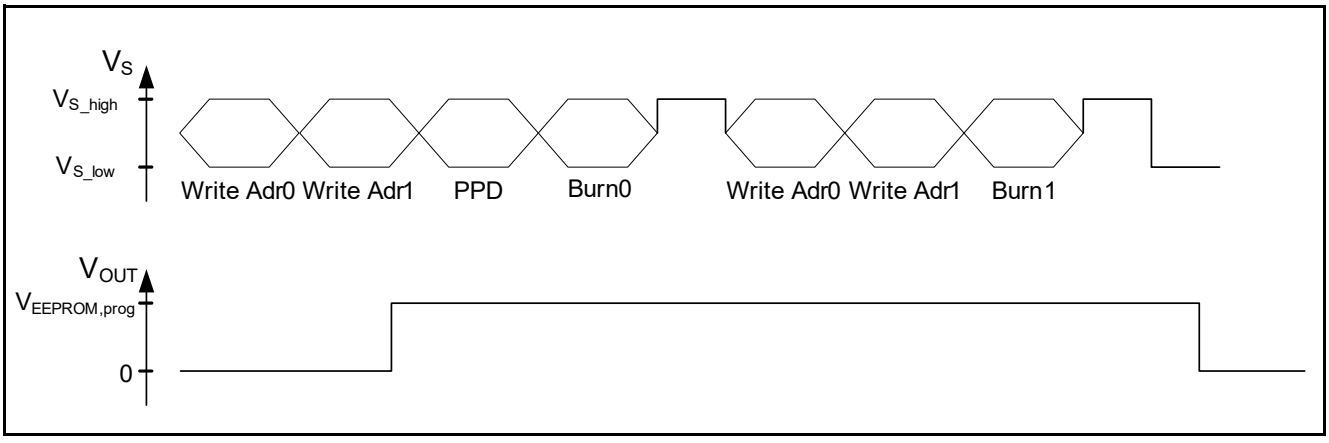

Figure 5-10 EEPROM burning sequence

6 Summary of IC Communication

The following tables summarize the sequence of frames which have to be used for switching into communication mode and for burning the EEPROM.

6.1 Switching the IC in Communication Mode

The following table shows the frames which have to be sent to switch the sensor in the programming mode. The appended pulse is included as a single “0” bit in the frame. In total, 3 frames have to be sent to enter the communication mode.

Table 6-1 Sequence of frames to switch into communication mode

Frame #	Description	Frame	Remark
1	Switch to communication mode for derivative **TLE4929C-XAx** and for derivative **TLE4959xx-FX**	1111-0000-1100-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
1	Switch to communication mode for derivative **TLE4929C-XVAx**	1101-1100-0000-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
1	Switch to communication mode for derivative **TLE4929C-XHAx**	1110-1100-0000-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
2	Switch digital signal to V_{OUT}	0000-0000-1101-0001-0101-0000-0000-0000-0	
3	Refresh EEPROM	0000-0000-0000-1100-0	

6.2 Burning EEPROM

The following sequence of frames has to be sent to burn the EEPROM after having switched the sensor in communication mode. The programming voltage at VOUT has to be applied before sending the Burn command and has to be maintained during the complete burning sequence. After that, VS must kept at VS_high while VOUT_PROG is applied for 35.8 ms and then set back to VS_low before sending the next frame.

Table 6-2 Sequence of frames to burn EEPROM

Frame #	Description	Frame	Remark
1	Switch to communication mode for derivative **TLE4929C-XAx** and for derivative **TLE4959xx-FX**	1111-0000-1100-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
1	Switch to communication mode for derivative **TLE4929C-XVAx**	1101-1100-0000-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
1	Switch to communication mode for derivative **TLE4929C-XHAx**	1110-1100-0000-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}

Table 6-2 Sequence of frames to burn EEPROM

Frame #	Description	Frame	Remark
2	Switch digital signal to V_{OUT}	0000-0000-1101-0001- 0101-0000-0000-0000-0	Testmode will be exit automatically when V_S is set above V_{S_high} for 680 us. This command will disable the automatic exit functionality
3	Read EEPROM Addr. 0x00	0000-0000-0000-0000-0 rrrr-rrrr-rrrr-rrrr	rrrr represents the initial16bit content Addr. 0x00
4	Read EEPROM Addr. 0x01	0000-0000-0001-0000-0 rrrr-rrrr-rrrr-rrrr	rrrr represents the initial16bit content Addr. 0x01
5	Optionally keep data for later usage		
6	Change the read bit content of the two EEPROM lines to the desired, new bit content		
7	Write to Addr 0x00	0000-0000-0000-0001- wwww-wwww-wwww-wwww-0	wwww represents the desired 16-bit content of 0x00
8	Write to Addr 0x01	0000-0000-0001-0001- wwww-wwww-wwww-wwww-0	wwww represents the desired 16-bit content of 0x01
9	Programming Pulse Definition	0000-0000-1011-0001- 0000-0001-0000-0010-0	Definition of programming pulse length. Set for typ. 255 µs
10	Disable open drain output	0000-0000-1110-0001- 0000-0000-1110-0000-0	Avoids output switching during programming
11	Apply programming voltage on sensor output pin		Set voltage of V_{out} pin to V_{OUT_PROG}
12	Burn “0” to EEPROM	0000-0000-0000-1110-0	Sending burn zeros command
13	Keep V_S at V_{S_high} while V_{OUT_PROG} is applied for 35.8 ms		
14	Set V_S back to V_{S_low}		
15	Remove programming voltage from Vout pin of sensor		
16	Enable open drain output	0000-0000-1110-0001- 0000-0000-0000-0000-0	
17	Reading of register address 0x0C	0000-0000-1100-0000-0 0000-0000-0000-0000	Reading of register address 0x0c.
18	Check bit number 15		If bit number 15 is set to ‘1’ no error otherwise error occurred
19	Write content to Addr 0x00	0000-0000-0000-0001- wwww-wwww-wwww-wwww-0	Repeat writing desired content to address 0x00
20	Write content to Addr 0x01	0000-0000-0001-0001- wwww-wwww-wwww-wwww-0	Repeat writing desired content to address 0x01. For complete locking of the EEPROM, bit 0 of Addr. 0x1 needs to be set to ‘1’

Table 6-2 Sequence of frames to burn EEPROM

Frame #	Description	Frame	Remark
21	Disable open drain output	0000-0000-1110-0001- 0000-0000-1110-0000-0	Avoids output switching during programming
22	Apply programming voltage on sensor output pin		Set voltage of Vout pin to V_{OUT_PROG}
23	Burn “1” to EEPROM	0000-0000-0000-1111-0	Sending burn ones command
24	Keep V_S at V_{S_high} while V_{OUT_PROG} is applied for 35.8 ms		
25	Set V_S back to V_{S_low}		
26	Remove programming voltage from Vout pin of sensor		
27	Enable open drain output	0000-0000-1110-0001- 0000-0000-0000-0000-0	
28	Reading of register address 0x0C	0000-0000-1100-0000-0 0000-0000-0000-0000	reading of register address 0x0c.
29	Check bit number 15		if bit number 15 is set to ‘1’ no error otherwise error occurred
30	Refresh EEPROM	0000-0000-0000-1100-0	
31	Reading back of EEPROM Addr. 0x00	0000-0000-0000-0000-0 rrrr-rrrr-rrrr-rrrr	
32	Reading back of EEPROM Addr. 0x01	0000-0000-0001-0000-0 rrrr-rrrr-rrrr-rrrr	
33	If content of read EEPROM registers is equal to that content that have been written during burn process the EEPROM cells have been written successfully. Optionally keep data for later usage		

7 EEPROM Margin Test

The margin command can be used in order to check the threshold voltages of the programmed EEPROM cells. For reliable sensor EEPROM operation the threshold level of the cell's have to be kept within the specification (Table 7-2). After sending the margin test command an external margin voltage can be switched to the control gates while refreshing the EEPROM-registers by a external trigger, so that the switching threshold of the EEPROM cell's can be identified (Table 7-1). EEPROM cell's programmed to '0' or to '1' need to be tested separately. For the '1' programmed cells a threshold voltage smaller than the applied margin voltage a '0' will be stored to the EEPROM registers, for those with a higher threshold a '1'. Vice versa the procedure when testing '0' programmed cells, for a margin voltage smaller then the threshold a '1' and for those higher than the threshold a '0' is stored in the EEPROM registers. By sweeping the external margin voltage the effective threshold voltages of each EEPROM cell can be identified. The threshold voltages of cells programmed to '1' can be found in this way. The smallest possible margin voltage is 0V, it is therefore not possible to determine the threshold voltages below 0V for the cells programmed to '0'.

Table 7-1 Sequence of frames for EEPROM margin test

Frame	Description	Frame	Remark
1	Switch to communication mode for derivative **TLE4929C-XAx** and for derivative **TLE4959xx-FX**	1111-0000-1100-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
1	Switch to communication mode for derivative **TLE4929C-XVAx**	1101-1100-0000-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
1	Switch to communication mode for derivative **TLE4929C-XHAx**	1110-1100-0000-1101-0	This frame has to be sent after power on of the sensor within t_{SUPPLY_enter}
2	Set SDO_to_VOUT bit 14 to “1” in Addr. 0x0D	0000-0000-1101-0001- 0100-0000-0000-0000-0	Sends stream of SDO (serial data out) also to VOUT pin
3	Read the initial content of EEPROM, Addr. 0x00 to 0x01	0000-0000-0000-0000-0 0000-0000-0000-0000 0000-0000-0000-0001-0 0000-0000-0000-0000	Memorize for later reference
4	Disable open drain output	0000-0000-1110-0001- 0000-0000-1110-0000-0	
5	Margin test command	0000-0000-0000-0100-0	‘0100’ margin test ‘0101’ margin zero test
6	Apply margin voltage at V_{OUT} and keep for tstop after trigger pulse	n.a.	Voltage level depending on “0” or “1” needs to be checked
7	Apply trigger pulse and wait tstop	0	
8	Enable open drain output	0000-0000-1110-0001- 0000-0000-0000-0000-0	
9	Read the content of EEPROM	0000-0000-0000-0000-0 0000-0000-0000-0000 0000-0000-0000-0001-0 0000-0000-0000-0000	Depending on the margin voltage some or more bit states possibly changed
10	Compare readout step 3 with readout step 9, memorize margin voltages of toggled bit’s	n.a.	

Table 7-1 Sequence of frames for EEPROM margin test

Frame	Description	Frame	Remark
11	If margin voltage < max. margin voltage, then increase margin voltage and continue with step 4	n.a.	
12	Report maximum and minimum margin voltage, end	n.a.	

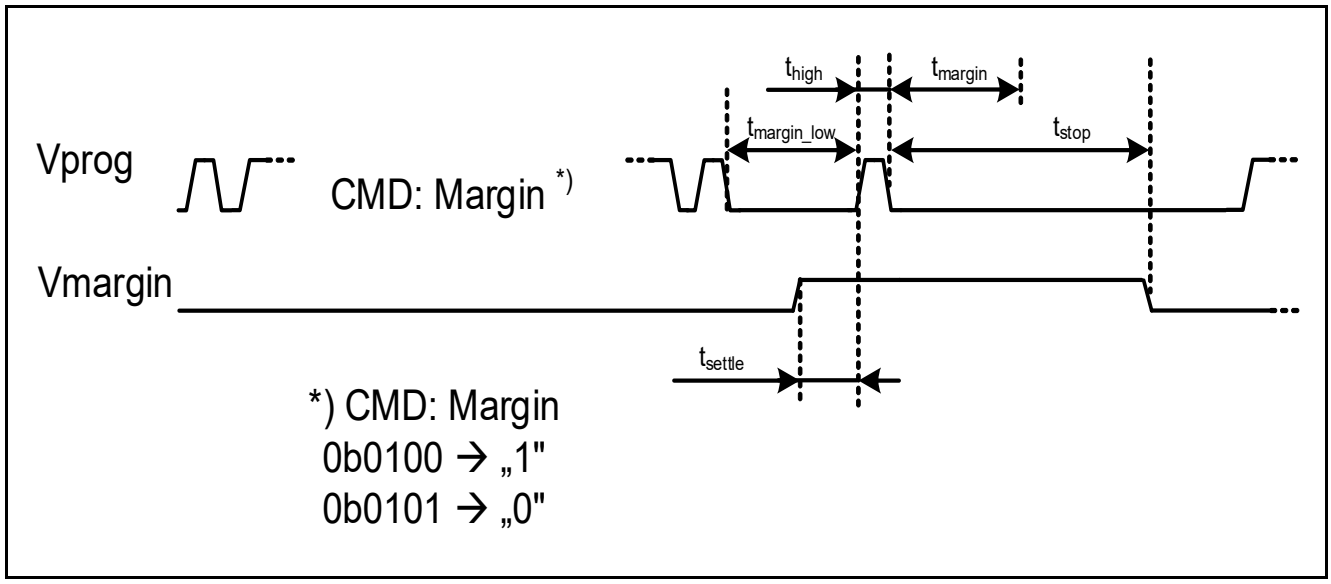

Figure 7-1 EEPROM Margin test

Table 7-2 Margin voltage specification and timing requirements

Parameter	Symbol	Limits			Unit	Notes
		MIN.	TYP.	MAX.		
EEPROM threshold margin level at start of lifetime[1)]	V_{TH_0h}	3.55	3.8	4.15	V	“1” programmed cells
				0.25	V	“0” programmed cells
EEPROM threshold margin level after lifetime	V_{TH_LT}	1.9			V	“1” programmed cells
				1.1	V	“0” programmed cells
Margin settle time	t_{settle}	10		620	µs	
Trigger pulse high length	t_{high}	11		558	µs	
Margin time	t_{margin}	10			µs	
Margin trigger wait time	t_{margin_low}	10		620	µs	Wait time after margin command
Stop length	t_{stop}	748			µs	

Table 7-2 Margin voltage specification and timing requirements (cont'd)

Parameter	Symbol	Limits			Unit	Notes
Margin voltage sweep range, test of "1" bits	V_{margin}	1.3		4.3	V	0.025 V step size recommended
Margin voltage sweep range, test of "0" bits		0		1.7	V	

1) Limits for EEPROM programming and margin level test at the same temperature. Alternatively the temperature characteristics of the margin level test needs to be considered: VTH(T)=VTH(WRITE_ERASE)+0.0016V/K*(TPROG-T). Please note that only a typical temperature coefficient is used.

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