



## Low drop voltage tracking regulator

### Features

- 50 mA output current capability
- Tiny SMD-package PG-SCT595-5 with lowest thermal resistance
- Low output tracking tolerance
- Stable with small ceramic output capacitor
- Low dropout voltage
- Combined reference/enable input
- Low current consumption in stand-by mode
- Maximum input voltage  $V_I = -42\text{ V to }+45\text{ V}$
- Reverse polarity protection
- Output short circuit proof to ground and supply
- Overtemperature protection
- Temperature range  $T_j = -40^\circ\text{C to }150^\circ\text{C}$
- Green Product (RoHS-compliant)



### Potential applications

General automotive applications.

### Product validation

Qualified for automotive applications.

Product validation according to AEC-Q100.

### Description

The OPTIREG™ linear TLE4250-2G is a monolithic integrated low dropout voltage tracker in a tiny SMD package PG-SCT595-5 with excellent thermal resistance. It is designed to supply off-board loads (for example, sensors) in automotive environments. The IC protects itself in case of overload, overtemperature, reverse polarity as well as output short circuit to battery and ground. Supply voltages up to  $V_I = 45\text{ V}$  are regulated to a reference voltage applied at the adjust input “ADJ” with high accuracy. The output “Q” is able to drive loads up to 50 mA.

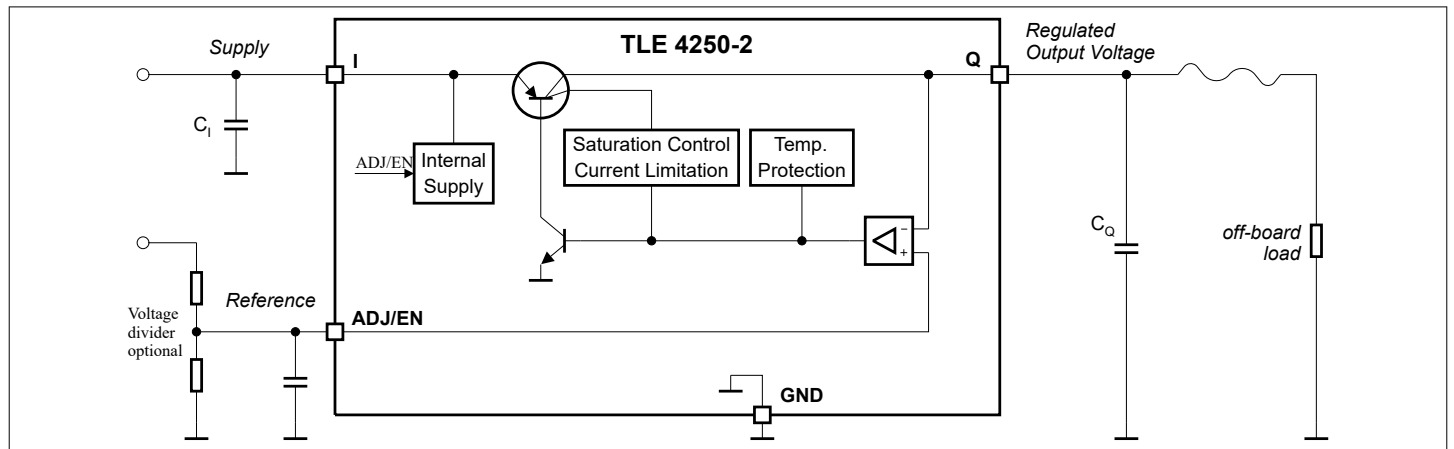
In order to reduce the quiescent current to a minimum, the TLE4250-2G can be switched to stand-by mode by setting the adjust/enable input “ADJ/EN” to “low”.

Type	Package	Marking
TLE4250-2G	PG-SCT595-5	52

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# 1 Block diagram



**Figure 1** Block diagram and simplified typical application

## 2 Pin configuration

### 2.1 Pin assignment

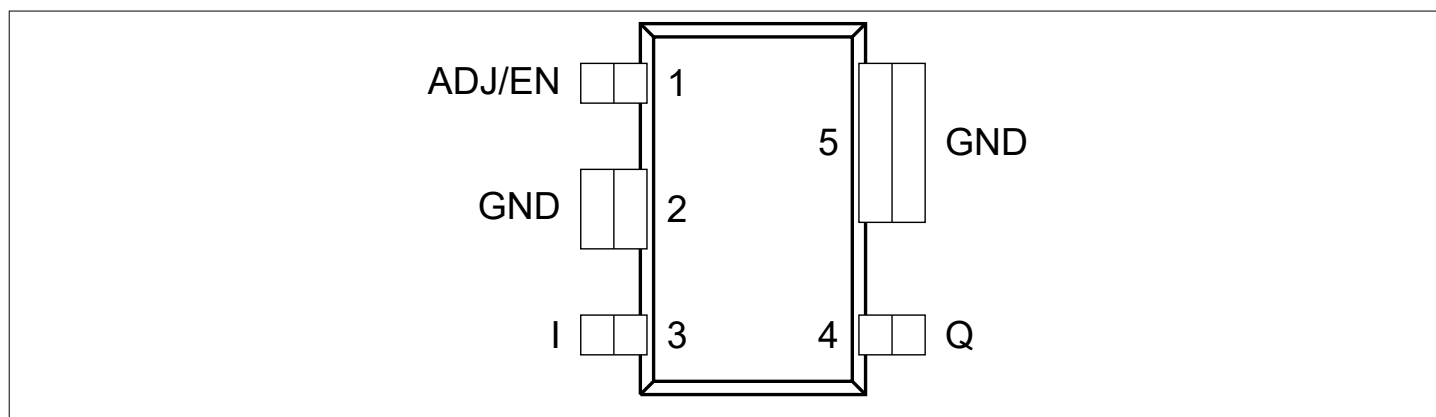


Figure 2 Pin configuration package PG-SCT595-5

### 2.2 Pin definitions and functions

Pin	Symbol	Function
1	ADJ/EN	<b>Adjust/enable.</b> Connect the reference to this pin. A low signal disables the IC; a high signal switches it on. The reference voltage can be connected directly or by a voltage divider for lower output voltages. For compensating line influences, a capacitor close to the IC pins is recommended.
2	GND	<b>Ground reference.</b> Internally connected to Pin 5. Connect to heatsink area.
3	I	<b>Input.</b> IC supply. For compensating line influences, a capacitor close to the IC pins is recommended.
4	Q	<b>Tracker output.</b> Block to GND with a capacitor close to the IC terminals, respecting capacitance and ESR requirements given in the table <a href="#">Functional range</a> .
5	GND	<b>Ground reference.</b> Internally connected to Pin 2. Connect to heatsink area.

### 3 General product characteristics

#### 3.1 Absolute maximum ratings

**Table 1** Absolute maximum ratings <sup>1)</sup>

$T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			

##### Voltages

Input voltage	$V_I$	-42	–	45	V	–	P_3.1.1
Output voltage	$V_Q$	-1	–	40	V	–	P_3.1.2
Adjust/enable input	$V_{\text{ADJ/EN}}$	-0.3	–	40	V	–	P_3.1.3

##### Temperatures

Junction temperature	$T_j$	-40	–	150	$^\circ\text{C}$	–	P_3.1.4
Storage temperature	$T_{\text{stg}}$	-50	–	150	$^\circ\text{C}$	–	P_3.1.5

##### ESD robustness

ESD robustness all pins (HBM)	$V_{\text{ESD,HBM}}$	-3	–	3	kV	<sup>2)</sup>	P_3.1.6
ESD robustness all pins (CDM)	$V_{\text{ESD,CDM}}$	-2	–	2	kV	<sup>3)</sup>	P_3.1.7

1) Not subject to production test, specified by design.

2) Human body model (HBM) robustness according to EIA/JESD 22-A114B.

3) Charged device model (CDM) robustness according to EIA/JESD22-C101 or ESDA STM5.3.1.

##### Notes:

1. Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

## 3.2 Functional range

**Table 2** Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Input voltage	$V_I$	4	–	40	V	–	P_3.2.1
Adjust/enable input voltage (Voltage tracking range)	$V_{ADJ/EN}$	2.5	–	36	V	–	P_3.2.2
Junction temperature	$T_j$	-40	–	150	°C	–	P_3.2.3
Output capacitor requirements	$C_Q$	1	–	–	μF	<sup>1)</sup>	P_3.2.4
Output capacitor requirements	$ESR_{CQ}$	–	–	3	Ω	<sup>2)</sup>	P_3.2.5

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%.

2) Relevant ESR value at  $f = 10$  kHz.

**Note:** Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

## 3.3 Thermal resistance

**Table 3** Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to ambient	$R_{thJA}$	–	81	–	K/W	<sup>1)</sup> 2s2p board	P_3.3.1
Junction to ambient	$R_{thJA}$	–	217	–	K/W	<sup>2)</sup> Footprint only	P_3.3.2
Junction to ambient	$R_{thJA}$	–	117	–	K/W	<sup>2)</sup> 300 mm <sup>2</sup> PCB heatsink area	P_3.3.3
Junction to ambient	$R_{thJA}$	–	103	–	K/W	<sup>2)</sup> 600 mm <sup>2</sup> PCB heatsink area	P_3.3.4
Junction to soldering point	$R_{thJSP}$	–	30	–	K/W	Pins 2, 5 fixed to $T_A$	P_3.3.5

1) Specified  $R_{thJA}$  value is according to JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The product (chip+package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 μm Cu, 2 × 35 μm Cu). Where applicable a thermal via array under the package contacted the first inner copper layer.

2) Package mounted on PCB FR4; 80 × 80 × 1.5 mm; 35 μm Cu, 5 μm Sn; horizontal position; zero airflow. Not subject to production test; specified by design.

## 4 Electrical characteristics

### 4.1 Tracking regulator

The output voltage  $V_Q$  is controlled by comparing it to the voltage applied at pin ADJ/EN and driving a PNP pass transistor accordingly. The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the poles/zeros introduced by the integrated circuit. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in the table [Functional range](#) have to be maintained. For details see also the typical performance graph [Output capacitor equivalent series resistance  \$ESR\_{CQ}\$  vs. output current  \$I\_Q\$](#)  graph. The output capacitor shall also be sized to buffer load transients.

An input capacitor  $C_I$  is recommended to buffer line influences. Connect the capacitors close to the IC terminals.

Protection circuitry prevent the IC as well as the application from destruction in case of catastrophic events. These safeguards contain output current limitation, reverse polarity protection as well as thermal shutdown in case of overtemperature.

In order to avoid excessive power dissipation that could never be handled by the pass element and the package, the maximum output current is decreased at high input voltages. The overtemperature protection circuit prevents the IC from immediate destruction under fault conditions (e. g. output continuously short-circuited) by reducing the output current. A thermal balance below 200°C junction temperature is established. Please note that a junction temperature above 150°C is outside the maximum ratings and reduces the IC lifetime.

The TLE4250-2G allows a negative supply voltage. However, several small currents are flowing into the IC. For details see electrical characteristics table and typical performance graphs. The thermal protection circuit is not operating during reverse polarity condition.

**Table 4 Electrical characteristics tracking regulator**

$V_I = 13.5\text{ V}$ ;  $V_{ADJ/EN} \geq 2.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$

all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Output voltage tracking accuracy	$\Delta V_Q$	-5	-	5	mV	$1\text{ mA} \leq I_Q \leq 10\text{ mA}$ ; $6\text{ V} \leq V_I \leq 16\text{ V}$	P_4.1.1
Output voltage tracking accuracy	$\Delta V_Q$	-25	-	25	mV	$1\text{ mA} I_Q \leq 50\text{ mA}$ ; $6\text{ V} \leq V_I \leq 28\text{ V}$	P_4.1.2
Output voltage tracking accuracy	$\Delta V_Q$	-25	-	25	mV	$1\text{ mA} \leq I_Q \leq 10\text{ mA}$ ; $6\text{ V} \leq V_I \leq 40\text{ V}$	P_4.1.3
Load regulation steady-state	$ \Delta V_{Q,load} $	-	-	15	mV	$I_Q = 1\text{ mA}$ to $30\text{ mA}$ ;	P_4.1.4
Line regulation steady-state	$ \Delta V_{Q,line} $	-	-	10	mV	$V_I = 6\text{ V}$ to $40\text{ V}$ ; $I_Q = 10\text{ mA}$	P_4.1.5
Power supply ripple rejection	$PSRR$	-	48	-	dB	<sup>1)</sup> $f_{ripple} = 100\text{ Hz}$ ; $V_{ripple} = 1\text{ Vpp}$	P_4.1.6
Dropout voltage $V_{dr} = V_I - V_Q$	$V_{dr}$	-	100	300	mV	<sup>2)</sup> $I_Q = 10\text{ mA}$ ; $V_{ADJ} \geq 4\text{ V}$	P_4.1.7
Output current limitation	$I_{Q,max}$	51	85	120	mA	$V_Q = (V_{ADJ} - 0.1\text{ V})$	P_4.1.8

(table continues...)

4 Electrical characteristics

**Table 4 (continued) Electrical characteristics tracking regulator**

$V_I = 13.5\text{ V}$ ;  $V_{ADJ/EN} \geq 2.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$

all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Reverse current	$I_Q$	-5	-1	-	mA	$V_I = 0\text{ V}$ ; $V_Q = 16\text{ V}$ ; $V_{ADJ} = 5\text{ V}$	P_4.1.9
Reverse current at negative input voltage	$I_I$	-10	-2	-	mA	$V_I = -16\text{ V}$ ; $V_Q = 0\text{ V}$ ; $V_{ADJ} = 5\text{ V}$	P_4.1.10

**Overtemperature protection**

Junction temperature	$T_{j,eq}$	151	-	200	$^\circ\text{C}$	<sup>1)</sup> $T_j$ increasing due to power dissipation generated by the IC	P_4.1.11
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1) Parameter not subject to production test; specified by design.

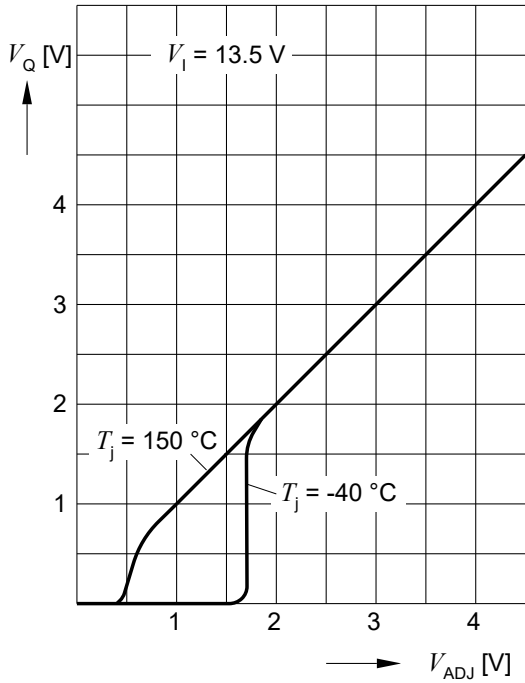
2) Measured when the output voltage  $V_Q$  has dropped 100 mV from its nominal value.



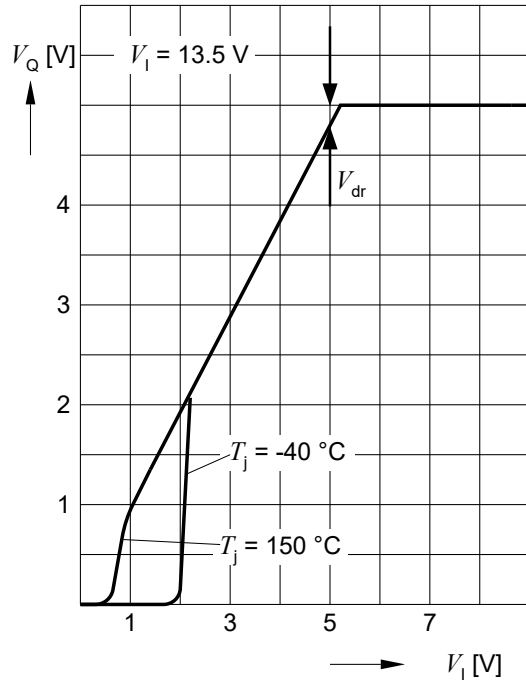
4 Electrical characteristics

**Typical performance characteristics tracking regulator  $V_{ADJ/EN} = 5\text{ V}$  (unless otherwise noted)**

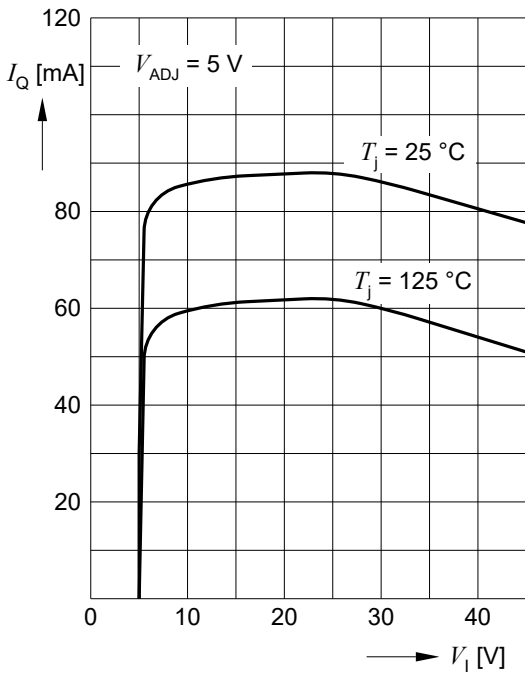
Output voltage  $V_Q$  vs.  
 adjust voltage  $V_{ADJ}$



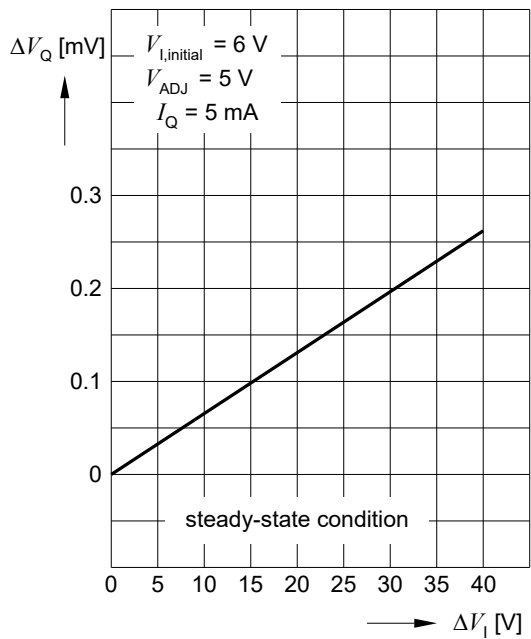
Output voltage  $V_Q$  vs.  
 input voltage  $V_I$



Maximum output current  $I_Q$  vs.  
 input voltage  $V_I$

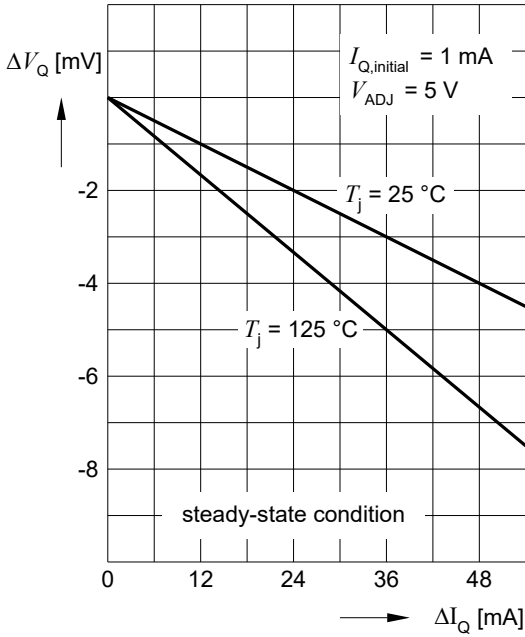


Line regulation  $\Delta V_{Q,line}$  vs.  
 input voltage change  $\Delta V_I$

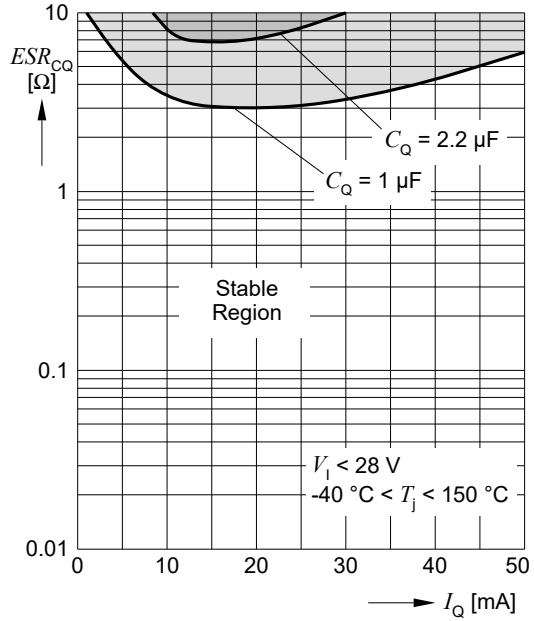


**4 Electrical characteristics**

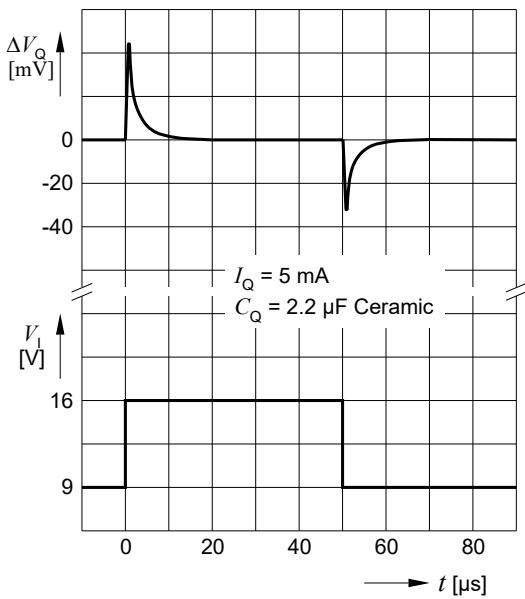
Load regulation  $\Delta V_{Q,line}$  vs. output current change  $\Delta I_Q$



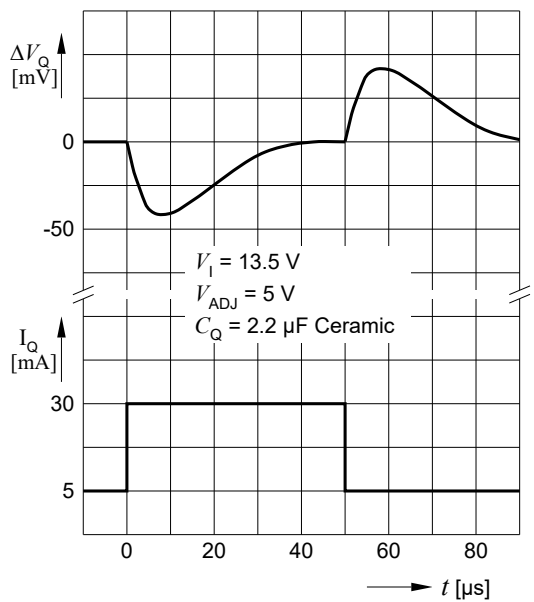
Output capacitor equivalent series resistance  $ESR_{CQ}$  vs. output current  $I_Q$



Line transient response

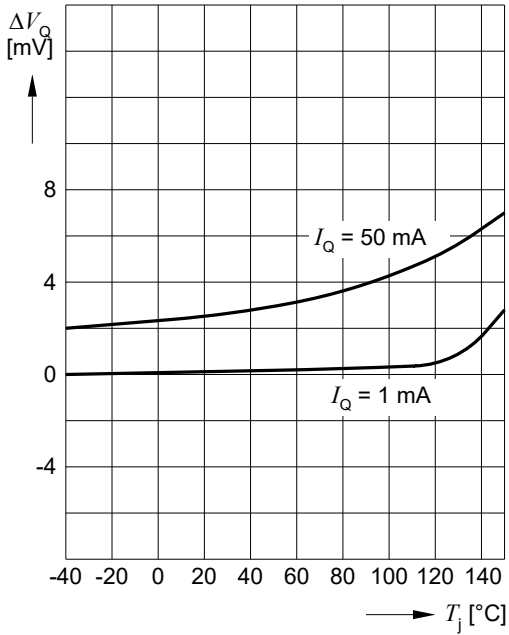


Load transient response

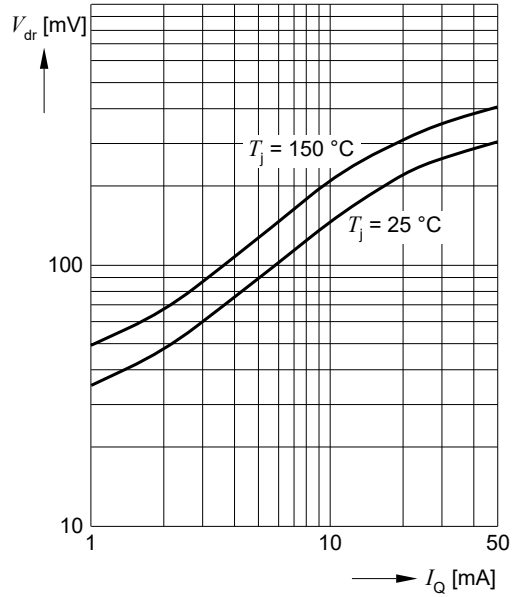


**4 Electrical characteristics**

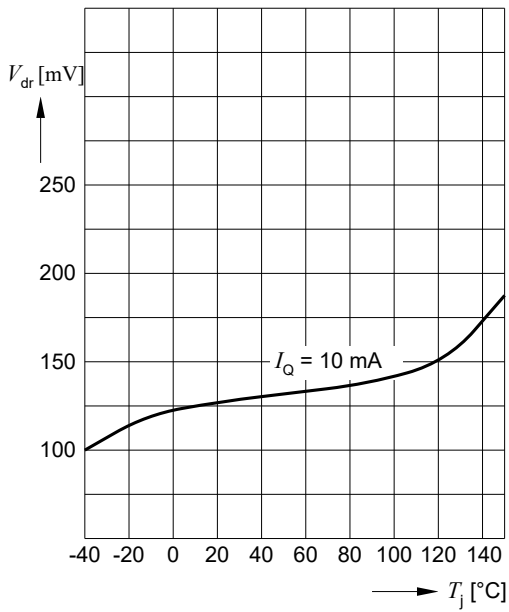
Tracking accuracy  $\Delta V_Q$  vs. junction temperature  $T_j$



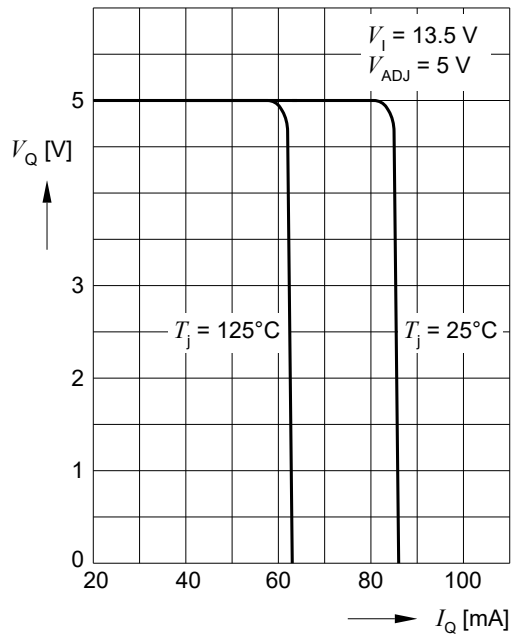
Dropout voltage  $V_{dr}$  vs. output current  $I_Q$



Dropout voltage  $V_{dr}$  vs. junction temperature  $T_j$

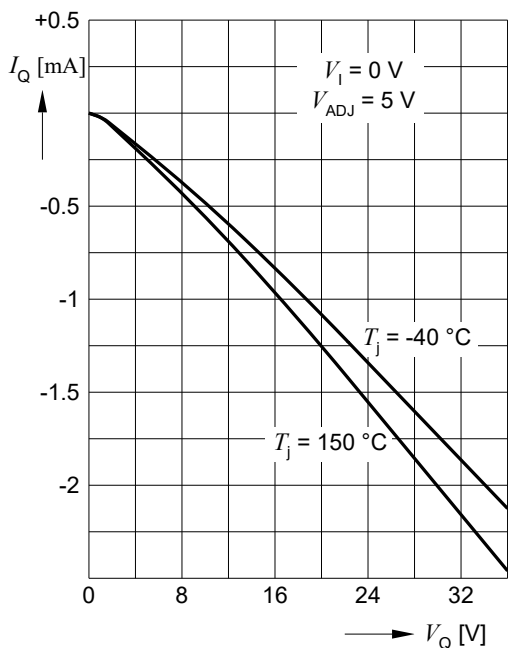


Output current limitation  $I_{Q,max}$  vs. output voltage  $V_Q$

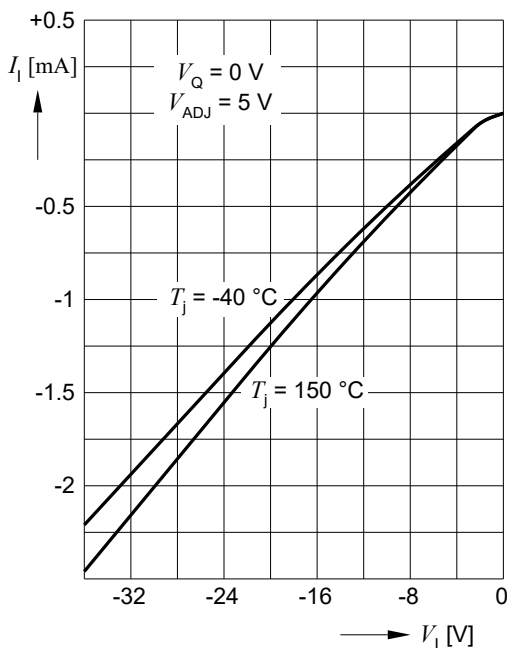


**4 Electrical characteristics**

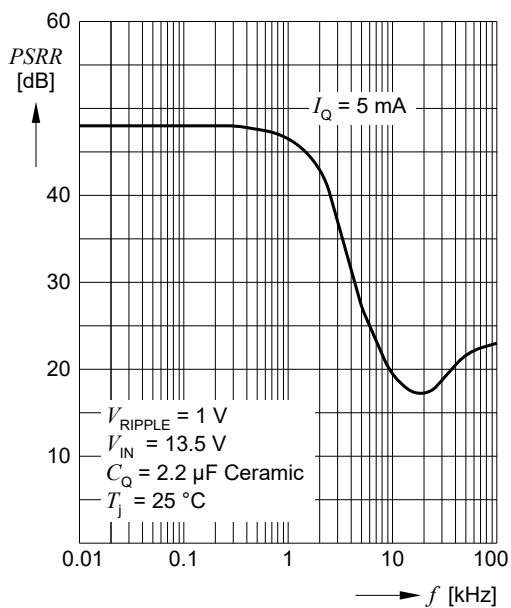
Reverse output current  $I_Q$  vs. output voltage  $V_Q$



Reverse current  $I_I$  vs. input voltage  $V_I$



Power supply ripple rejection  $PSRR$  vs. frequency  $f$



## 4.2 Current consumption

**Table 5** Electrical characteristics current consumption

$V_I = 13.5\text{ V}$ ;  $V_{ADJ/EN} \geq 2.5\text{ V}$ ;  $T_j = -40^\circ\text{C}$  to  $150^\circ\text{C}$

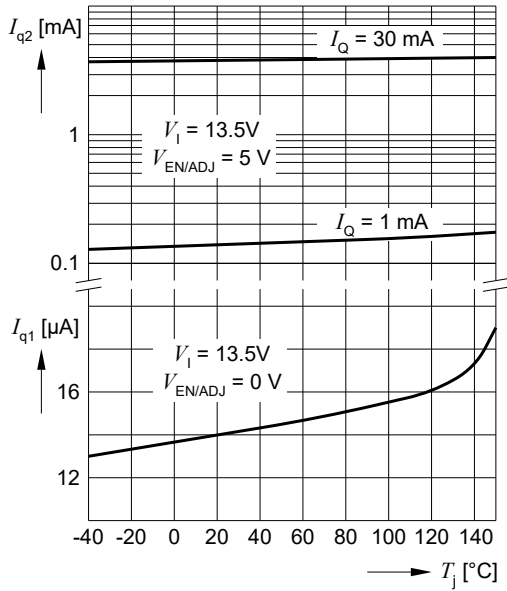
all voltages with respect to ground (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Quiescent current stand-by mode	$I_{q1}$	–	10	20	$\mu\text{A}$	$V_{ADJ/EN} \leq 0.4\text{V}$ ; $T_j \leq 85^\circ\text{C}$	P_4.2.1
Current consumption $I_q = I_I - I_Q$	$I_{q2}$	–	140	200	$\mu\text{A}$	$I_Q \leq 1\text{ mA}$	P_4.2.2
Current consumption $I_q = I_I - I_Q$	$I_{q2}$	–	3	5	$\text{mA}$	$I_Q \leq 30\text{ mA}$	P_4.2.3
Current consumption dropout region; $I_q = I_I - I_Q$	$I_{q3}$	–	1	2	$\text{mA}$	$V_{ADJ} = V_I = 5\text{V}$ ; $I_Q = 0\text{ mA}$	P_4.2.4

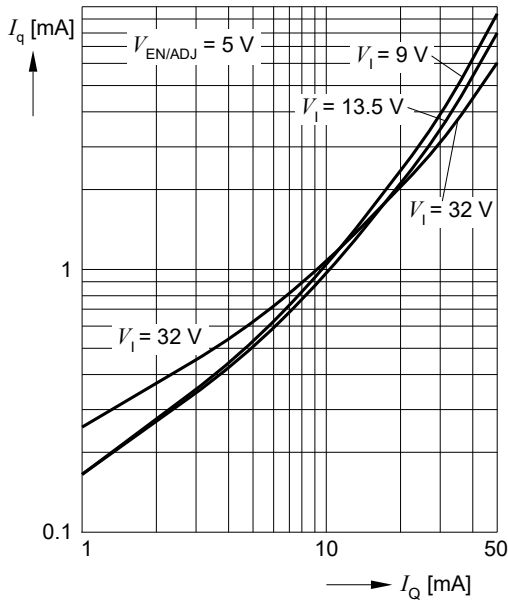
**4 Electrical characteristics**

**Typical performance characteristics current consumption  $V_{ADJ/EN} = 5\text{ V}$  (unless otherwise noted)**

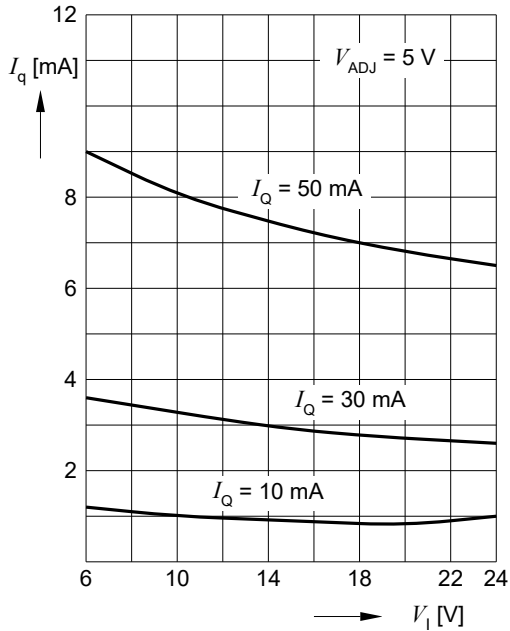
Current consumption  $I_{q1}, I_{q2}$  vs.  
 junction temperature  $T_j$



Current consumption  $I_{q2}$  vs.  
 output current  $I_Q$



Current consumption  $I_{q2}$  vs.  
 input voltage  $V_1$



### 4.3 Adjust/enable input

In order to reduce the quiescent current to a minimum, the TLE4250-2G can be switched to stand-by mode by setting the adjust/enable input “ADJ/EN” to “low”.

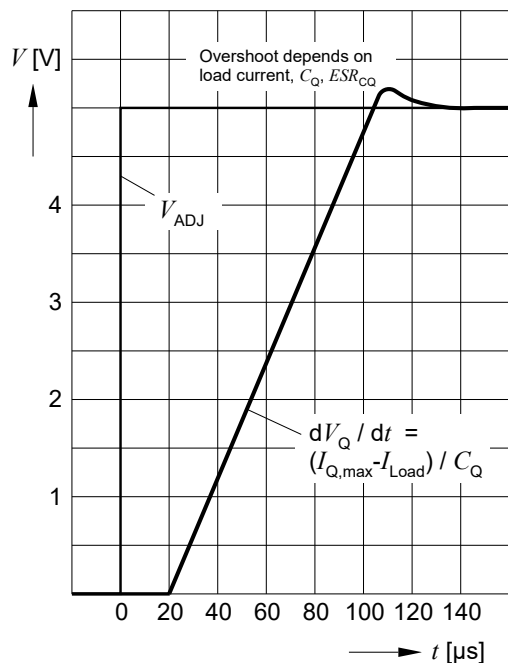
**Table 6 Electrical characteristics adjust/enable**

$V_I = 13.5\text{ V}$ ;  $V_{ADJ/EN} \geq 2.5\text{ V}$  all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Adjust/enable input current	$I_{ADJ}$	–	0.1	0.5	$\mu\text{A}$	$V_{ADJ} = 5\text{ V}$	P_4.3.1
Adjust/enable low signal valid	$V_{ADJ,low}$	–	–	0.4	V	$V_Q = 0\text{ V}$	P_4.3.2
Adjust/enable high signal valid (tracking region)	$V_{ADJ,high}$	2.5	–	36	V	$ V_Q - V_{ADJ}  < 25\text{ mV}$	P_4.3.3

#### Typical performance characteristics adjust/enable input $V_{ADJ/EN} = 5\text{ V}$ (unless otherwise noted)

Startup sequence



## 5 Package information

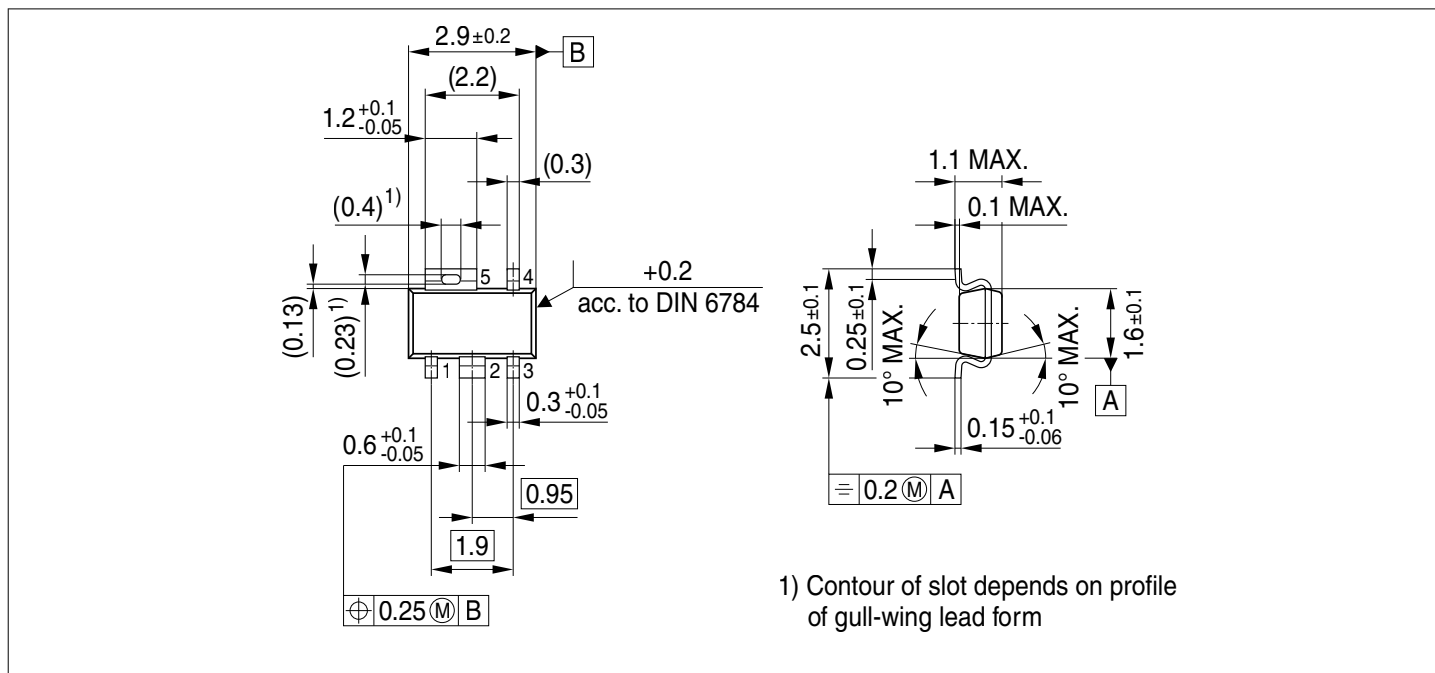


Figure 3 Outline PG-SCT595-5 <sup>1)</sup>

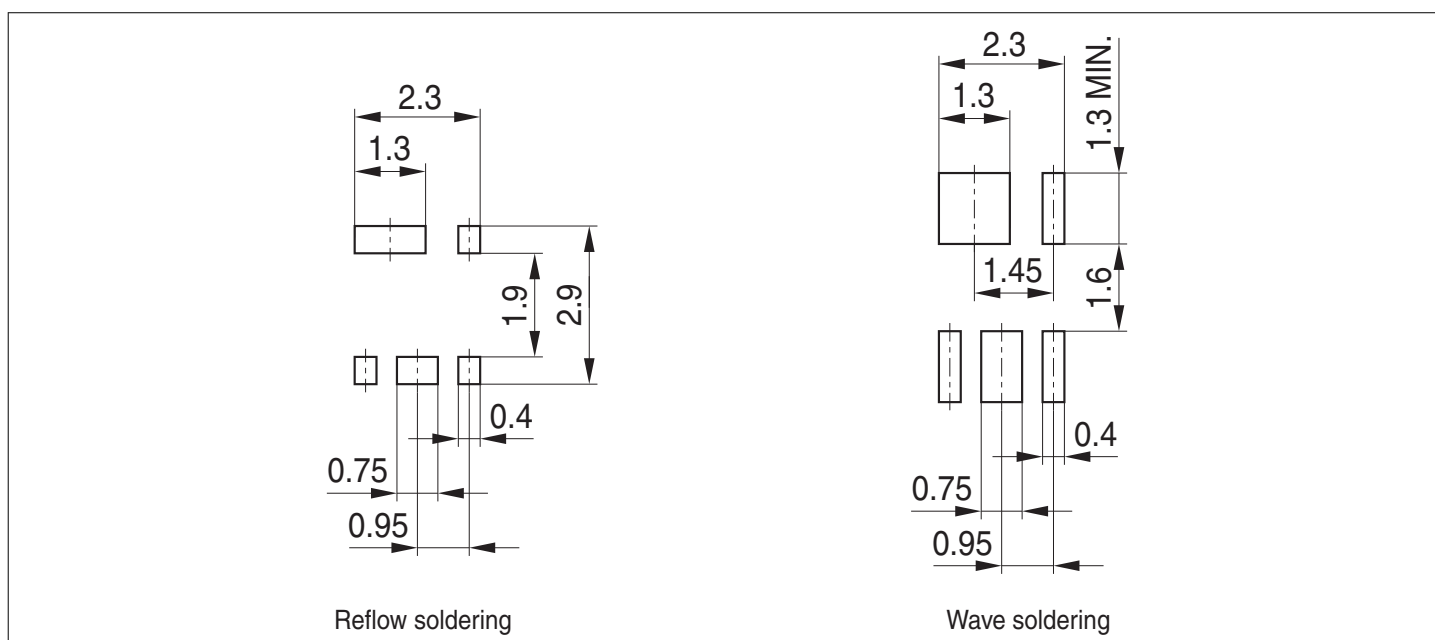


Figure 4 Footprint PG-SCT595-5 (Plastic dual small outline) <sup>1)</sup>

### Green Product (RoHS-compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green Products are RoHS-compliant (Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

### Further information on packages

<https://www.infineon.com/packages>

<sup>1)</sup> Dimensions in mm



## 6 Revision history

Revision	Date	Changes
1.11	2025-02-12	Editorial changes and template update
1.10	2022-03-08	Update layout, editorial changes
1.00	2007-07-24	Final datasheet initial version

## Trademarks

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