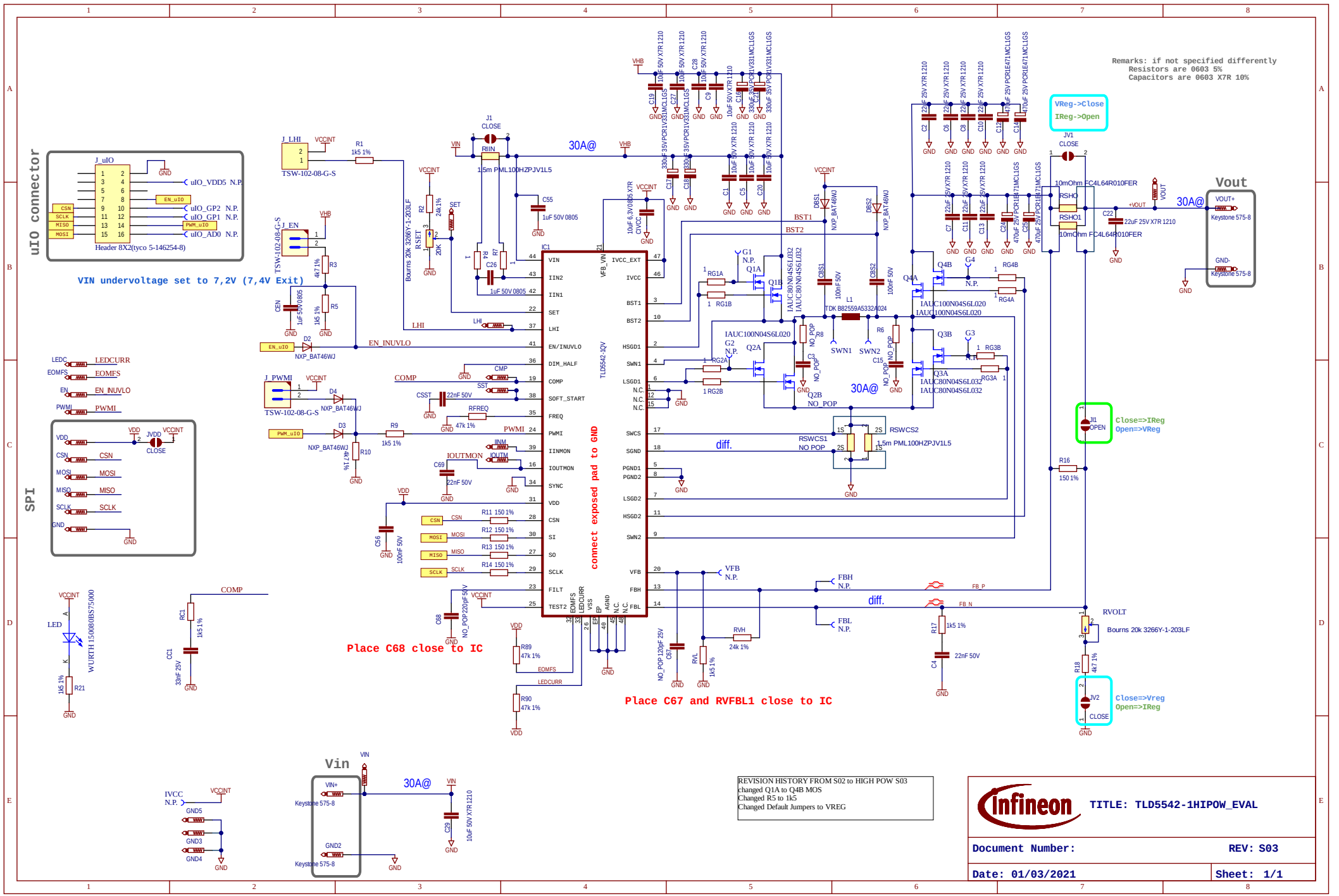
uIO connector
J_uIO
Header 8X2(tyco 5-146254-8)
uIO_VDD5 N.P.
uIO_GP2 N.P.
uIO_GP1 N.P.
uIO_AD0 N.P.
VIN undervoltage set to 7,2V (7,4V Exit)
SPI
LEDCURR
EOMFS
EN_INUVLO
PWMI
CSN
MOSI
MISO
SCLK
J_LHI
TSW-102-08-G-S
J_EN
J_PWMI
J1
CLOSE
RIIN
1.5m PML100HZPJV1L5
30A@
VHB
VCCINT
BST1
BST2
IC1
TLD5542-1QV
connect exposed pad to GND
Place C68 close to IC
Place C67 and RVFBL1 close to IC
IAUC100N04S6L020
IAUC80N04S6L032
TDK B82559A5332A024
RSWCS1
RSWCS2
NO POP
diff.
Vout
VOUT+
VOUT-
Keystone 575-8
10mOhm FC4L64R010FER
RSHO
RSHO1
VReg->Close
IReg->Open
Close=>IReg
Open=>VReg
Close=>Vreg
Open=>IReg
RVOLT
Bourns 20k 3266Y-1-203LF
Vin
IVCC
LED
WURTH 150080BS75000
REVISION HISTORY FROM S02 to HIGH POW S03
changed Q1A to Q4B MOS
Changed R5 to 1k5
Changed Default Jumpers to VREG
Remarks: if not specified differently
Resistors are 0603 5%
Capacitors are 0603 X7R 10%
TITLE: TLD5542-1HIPOW_EVAL
Document Number:
REV: S03
Date: 01/03/2021
Sheet: 1/1