

Introduction to Simulation Model - IFX Designer

LITIX™ Power TLD5191ES

About this document

Scope and purpose

This document outlines the main features of LITIX™ Power TLD5191ES by means of its digital twin. The digital twin is the simulation model. In typical application setups, the simulation model aims to be an easy, time-efficient and cost-reduced solution for exploring device capabilities and integration in complex applications.

Information covered in this document does not substitute datasheet content and shall be regarded as complementary to it. For a more precise description of the device and its features, please consult the datasheet[1].

Intended audience

This application note, along with the simulation model itself, offers an interactive solution targeted at anybody who aims to explore the functionality and “what if” scenarios for the TLD5191ES device.

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1 LITIX™ Power TLD5191ES

The LITIX™ Power **TLD5191ES** is a synchronous MOSFET H-Bridge DC/DC controller with built-in protection features. This concept of a synchronous and seamless buck-boost regulation provides a very efficient solution for circuits where the output (load) voltage is on the same level as the input voltage, such as in short chains with 2 to 3 high power LEDs or laser diodes connected to a 12 V electrical system.

The available online circuits are:

- 12V Automotive LED synchronous H-Bridge topology with LITIX™ Power controller TLD5190 (input voltage ramping)
- 12V Automotive LED synchronous H-Bridge topology with LITIX™ Power controller TLD5190 (soft start and dimming)
- 12V Automotive LED synchronous H-Bridge topology with LITIX™ Power controller TLD5190 (pwm engine)
- 12V Automotive LED synchronous H-Bridge topology with LITIX™ Power controller TLD5190 (slow switch)
- 12V Automotive LED synchronous H-Bridge topology with LITIX™ Power controller TLD5190 (short circuit)

[Click here to open the circuits.](#)

Simulation model features

2 Simulation model features

- Perform transient simulations: observe and analyze the transient device response to different stimuli. The number of stimuli and probes is unlimited
- Measure the device's electrical parameters in typical conditions with increased precision at small resolution (such as 100 ns/1 uV/1 uA)
- Integrate the simulation model in complex applications and explore new possibilities
- Explore main features of the real device (for more details, consult the datasheet[1]): shortest time to obtain results, zero-error cost (no harm to physical components), can be done by anyone such as engineers, and students.
 - Regulation loop
 - Analog and digital dimming including the embedded PWM generator
 - Soft start behavior
 - Fault management (short circuit, overvoltage, input undervoltage)
 - Spread spectrum
 - Internal LDO (IVCC)
- To keep the usability and simulation speed in a reasonable range, the simulation model does not cover all features of the real device:
 - BST1,2 and SWN1,2 pins not available (no real external MOSFETs, only ideal switches)
 - External Clock Sync (no FREQ pin, frequency controlled via model parameter)
 - Thermal Network and self-heating not available, no overtemperature detection and protection
 - The current consumption of the IC is not considered (A realistic power efficiency calculation is not possible)
 - There are no ESD, EMC, AC, DC, and Monte Carlo analysis simulation capabilities
 - There are possible convergence issues for using DC sources, steep ramps, or high frequency sources within the setup.

2.1 Details on the implementation

Gate Drivers controlling the four external MOSFETs in an H-Bridge configuration provides ideal 0V-5V logic signals independent of switching nodes levels SWN1,2. Due to this, it is only possible to drive ideal switches instead of real MOSFETs. This in turn reduces the number of calculations per cycle and highly improves the total simulation time. Therefore, bootstrap pins BST1,2 and SWN1,2 are not present on the symbol. Dead time between low-side and high-side switching is implemented and for the ideal switches the ON threshold, $R_{DS(ON)}$ and body diode have been considered.

The internal oscillator has not been modeled as in the real device, hence the FREQ pin is not present on the blue symbol on the schematics. The main reason is to reduce the complexity of the model and optimize performance speed. Instead of modeling the frequency pin as in the real device the frequency of the controller is specified directly in [Hz] units via the model parameter {frequency} available on the test bench (check Table 1 below).

Important: for correct functioning of the controller, the maximum time step cannot exceed 150ns. Values above this limit affect the generation of the internal clock.

Table 1 Model parameter list

Parameter name	Description	Range
frequency	Specifies directly the controller's oscillator frequency	200 kHz to 700 kHz

3 Model performance

3.1 Input voltage ramping – transient

This test bench shows how the regulator reacts to changes in the input voltage (V_{IN}) while the circuit is in a steady state. Output current is monitored while the regulator tries to compensate for input voltage variation below or above the nominal output voltage. The load is fixed by 4 LEDs driven by 1 A average current.

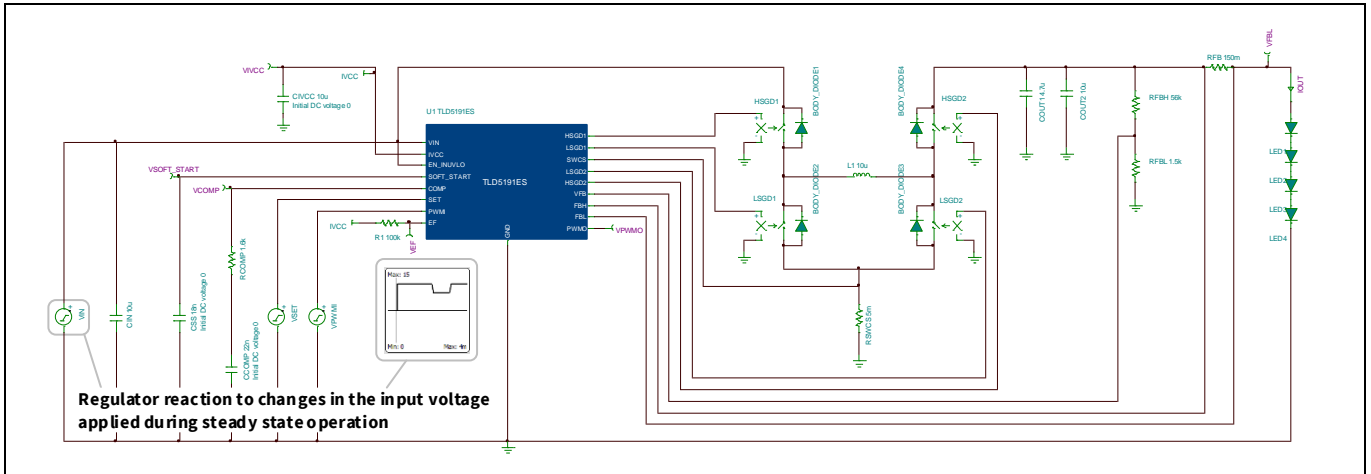


Figure 1 Test setup for input voltage ramping [click to open](#)

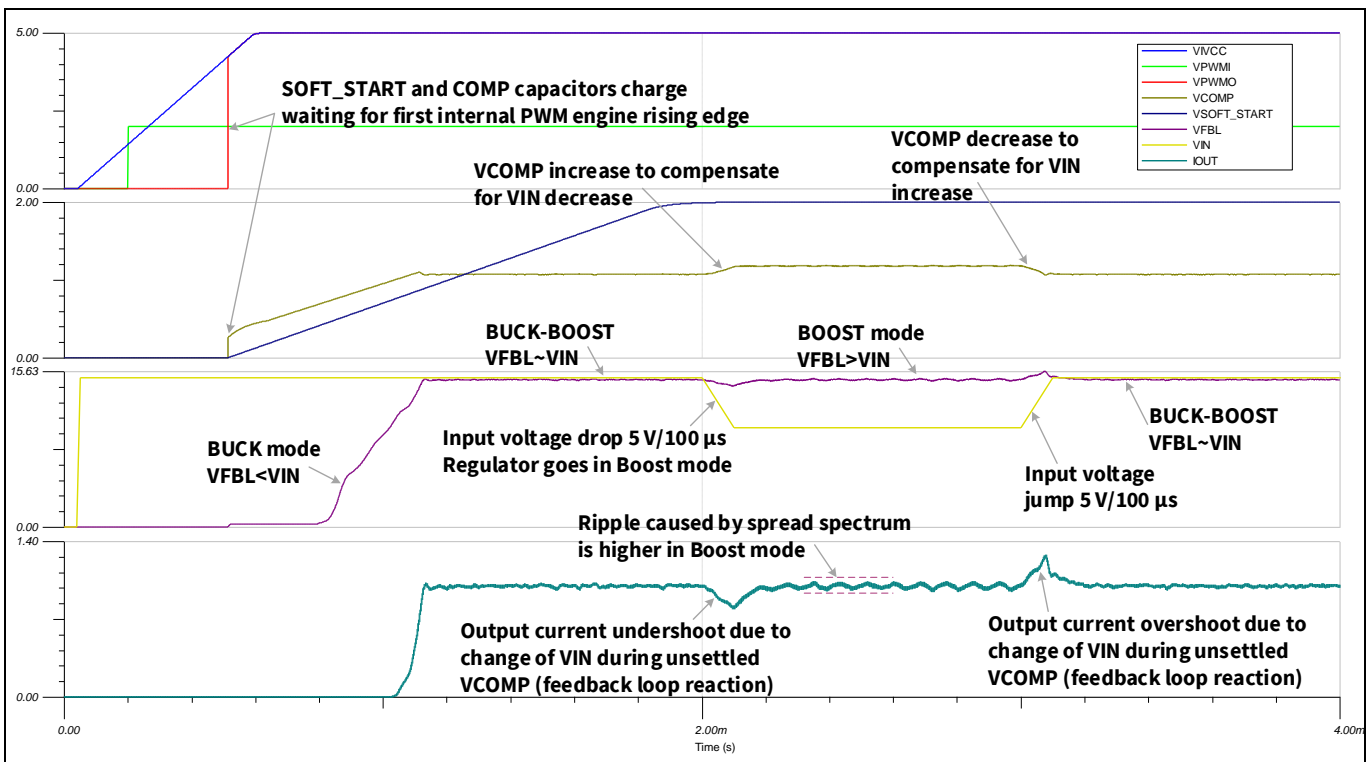


Figure 2 Simulation results

3.2 Soft start, analog and digital dimming – transient

This test bench shows three functions:

- Soft start: This is the start up sequence of the device. During the rising edge of SOFT_START, the internal PWM signal is extended until one of the two following conditions is reached:
 - VSOFI_START exceeds VSOFI_START_LOFF
 - VFBH-FBL exceeds VFBH_FBL_OL
- Analog dimming: This is controlled by the SET pin
- Digital dimming: This is controlled by the PWMI pin

SOFT_START and COMP capacitor values are chosen to see the impact of SOFT_START in the start-up until the circuit is reaching steady state. If the COMP ramp is faster than the SOFT_START ramp and exceeds SOFT_START by more than 0.7 V, then the COMP ramp will be limited by SOFT_START.

RFB is set to 150 mOhm in order to have 1 A at the output. SET pin is decreased from 1.4 V (100% analog dimming) to 0.8 V (50% analog dimming).

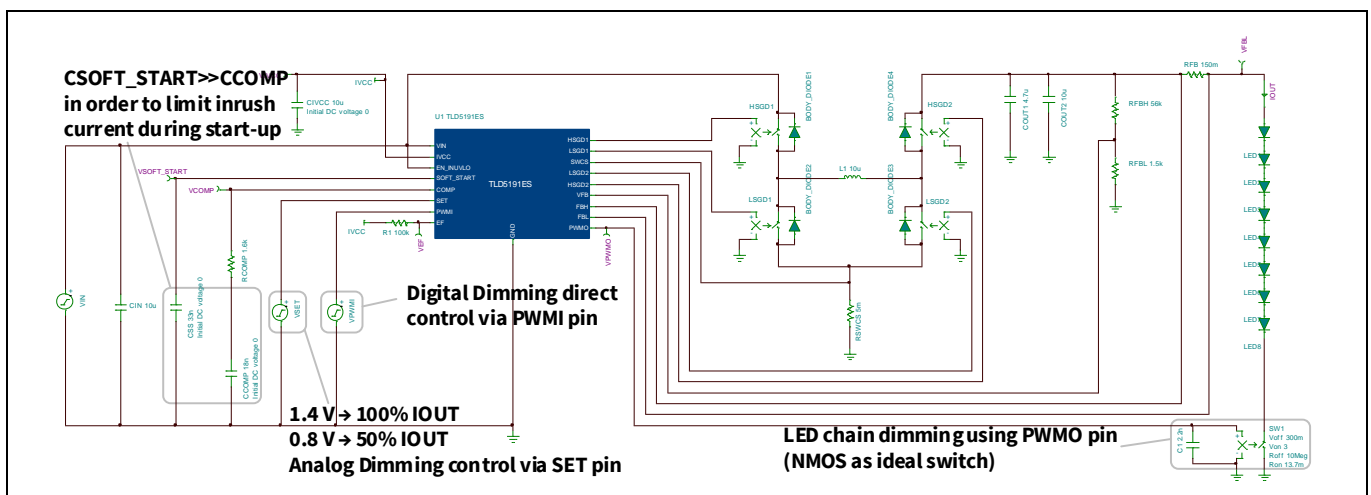


Figure 3 Test setup for soft start, analog and digital dimming [click to open](#)

Model performance

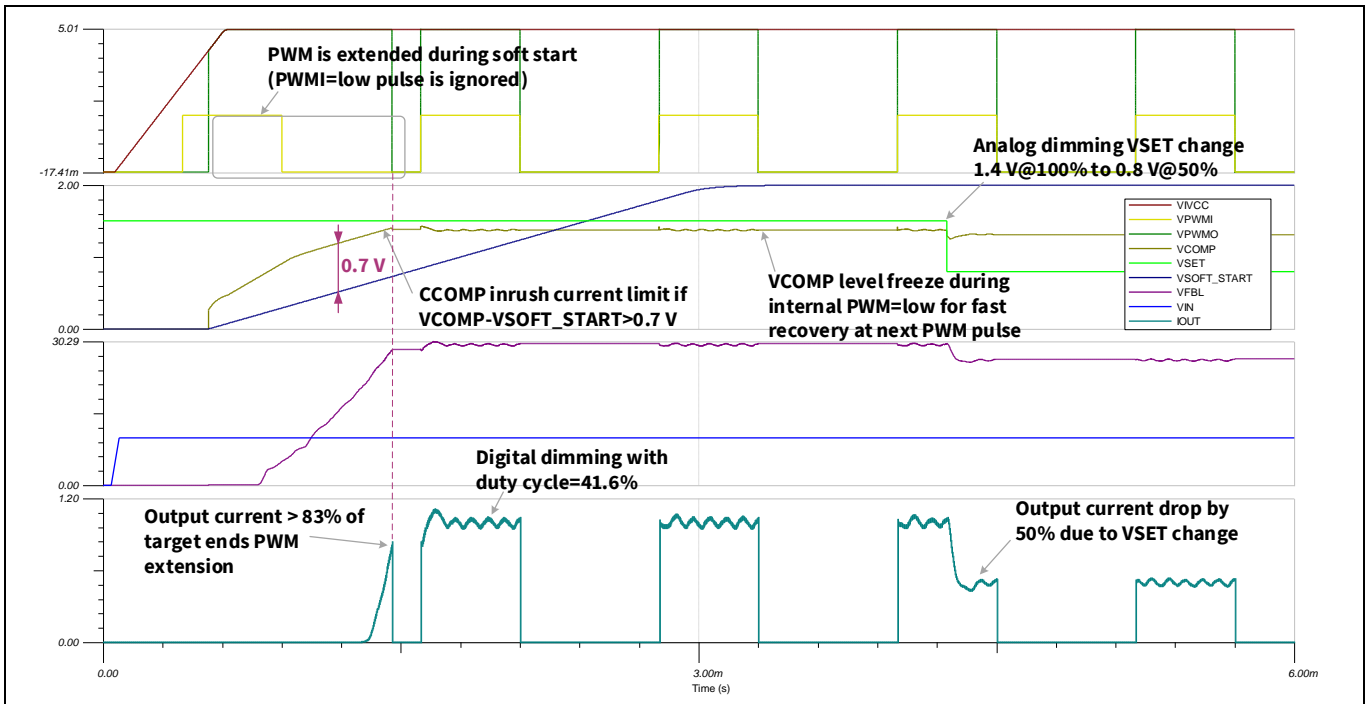


Figure 4 Simulation results

3.3 PWM engine – transient

This test bench shows digital dimming via the internal PWM engine feature.

During the rising edge of SOFT_START, the internal PWM signal is extended until one of the two following conditions is reached:

- VSFT_START exceeds VSFT_START_LOFF
- VFBH-FBL exceeds VFBH_FBL_OL

Depending on voltage level at the PWMI pin, the output current is dimmed accordingly with a certain duty cycle (digital dimming).

A PWMI low pulse is applied for more than 25 ms to show the restart of the device with a soft start routine.

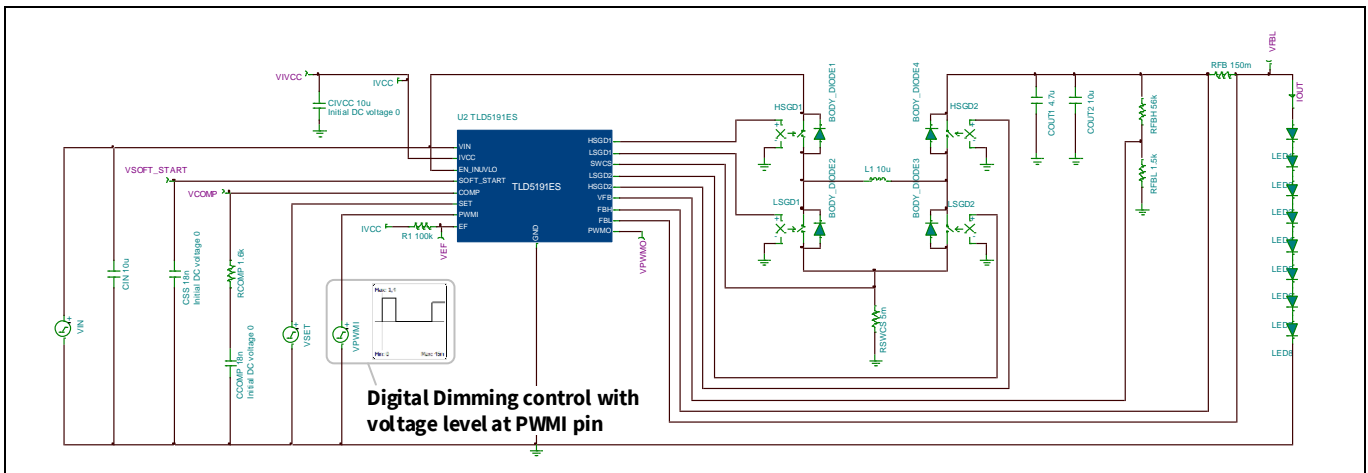


Figure 5 Test setup for PWM engine [click to open](#)

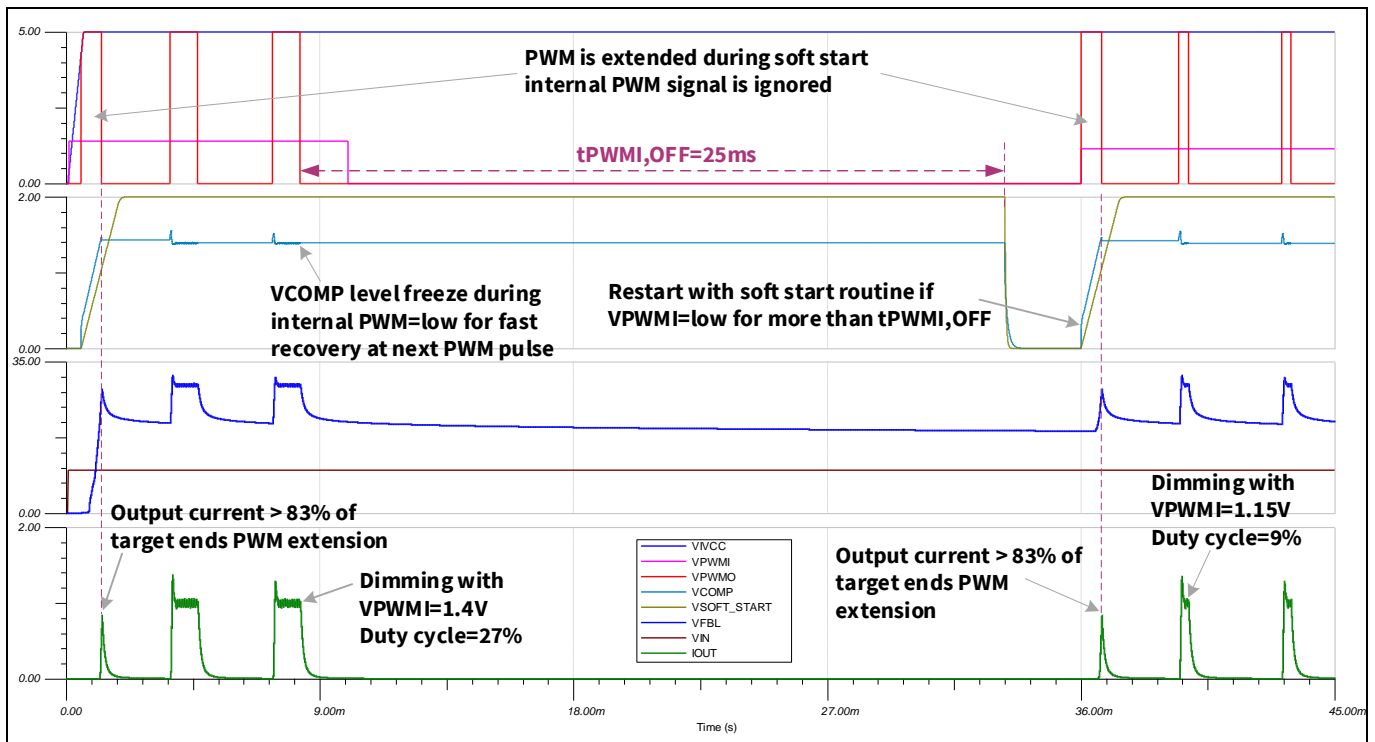


Figure 6 Simulation results

3.4 Slow switch – transient

When the load changes (for example, because the number of LEDs is suddenly decreased), the voltage at the output capacitor creates a current spike, which can damage the LEDs.

The setup shows a slow switching technique, which prevents the appearance of the current spike by controlled discharge of the output voltage to a value closer to the equivalent voltage drop of the new number of LEDs. A load bypass event is applied at 2 ms causing the output voltage to decrease, and based on the turn-on timing of the PMOS, 2 out of 5 LEDs are shorted.

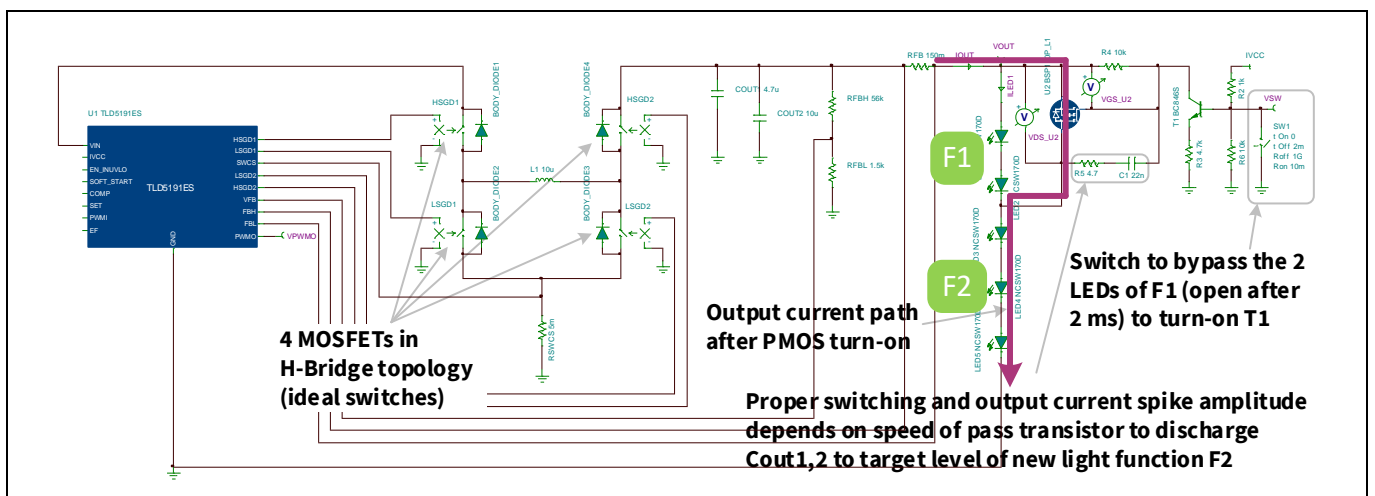


Figure 7 Test setup for slow switch [click to open](#)

Model performance

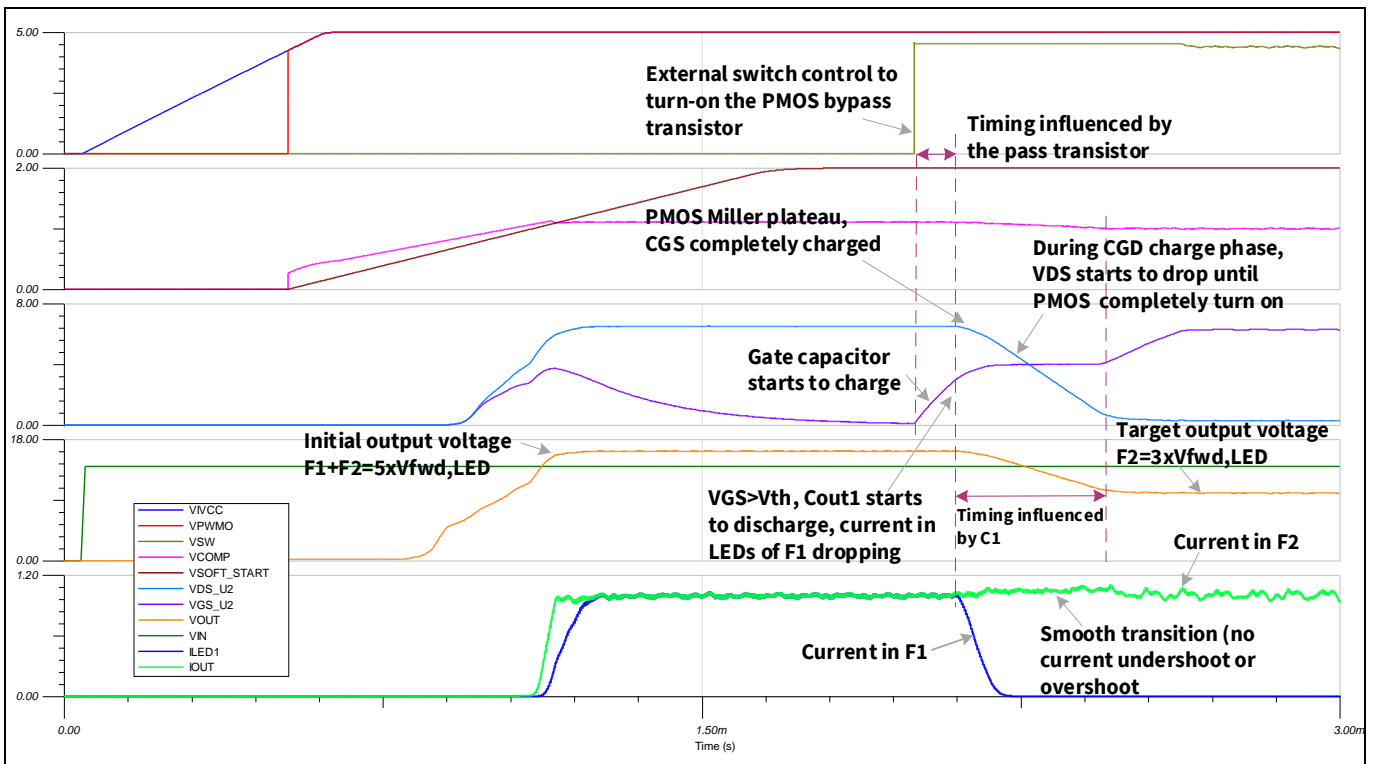


Figure 8 Simulation results

3.5 Short circuit to ground – transient

This test bench shows the short circuit to ground detection and protection.

The fault is applied at 2.5 ms and released at 15 ms. During this time interval, the device will initiate the retry strategy using the SOFT_START pin.

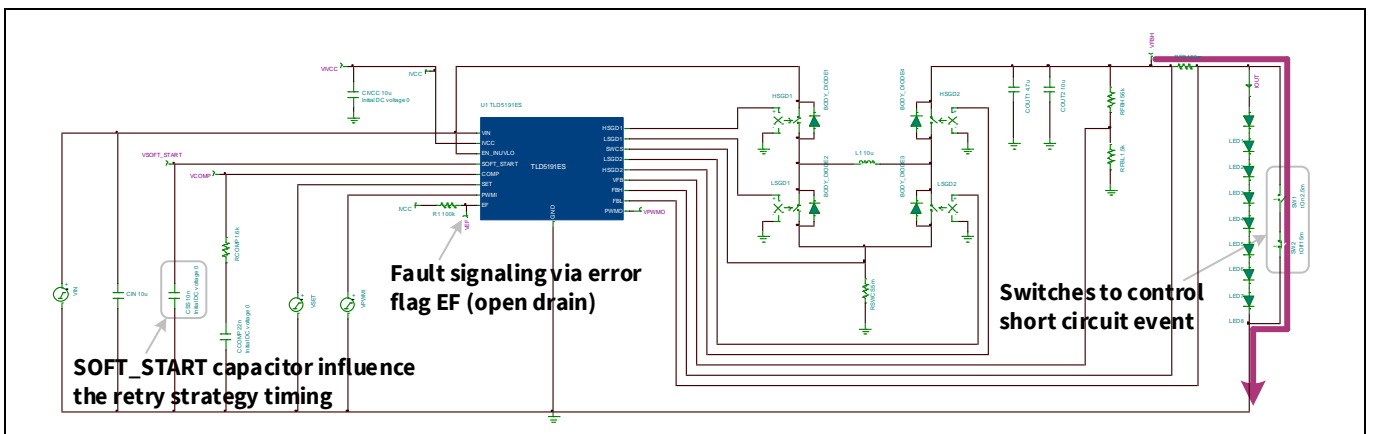


Figure 9 Test setup for short circuit [click to open](#)

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LITIX™ Power TLD5191ES

Model performance

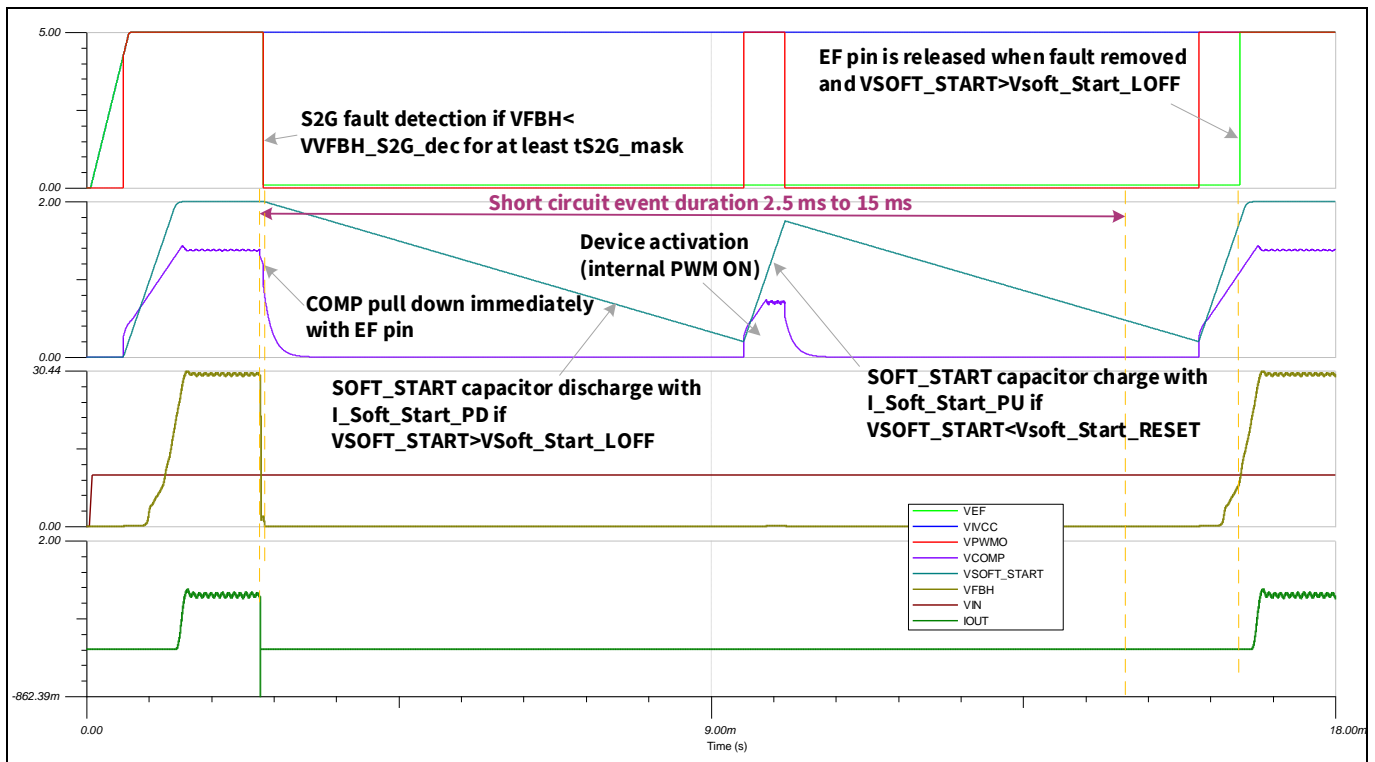


Figure 10 Simulation results

4 List of references

[1] Product datasheet: Infineon-TLD5191ES-DataSheet-v01_00-EN.pdf, Rev.1.00, 2022-02-18

Revision history

5 Revision history

Document version	Date of release	Description of changes
Rev.1.00	30.06.2022	Initial version created

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