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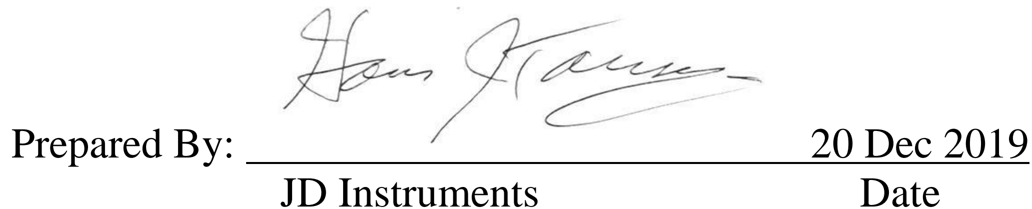
TID-RLAT Test Report for Cypress 16Mb SRAMs (CYRS1061)

Fab Lot:
L9903000, Wafer #2

Date: 20 Dec 2019 Revision: A

Purchase Order:
Cypress Semiconductor Corporation 4700013426



Prepared By: ________________ 20 Dec 2019
JD Instruments Date

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Executive Summary

Radiation Lot Acceptance Testing (RLAT) for Total Ionizing Dose (TID) was performed on 16Mb SRAMs (CYRS1061), fab (diffusion) lot L9903000, wafer #2. All lots passed RLAT analysis to 250K rad(Si).

A companion report has been prepared in which 2 of these part types were irradiated to 450K rad(Si) to demonstrate radiation capability level. Even at this much higher dose all parameters stayed well within specified limits.

Parts were provided in 54 pin ceramic SOIC packages.

Irradiation and testing was performed in accordance with MIL-STD 883 Method 1019.8 Condition A. Radiation induced changes were evaluated using KTL statistics with Probability of Survival (Ps) of 99% and Confidence Level of 90%.

“ON-SITE RLAT Tests” were performed before and immediately after the parts were exposed to radiation. These consisted of functional tests as well as DC parametric measurements on device pins in their normal mode of operation. All parameters monitored on-site stayed well within spec sheet limits up to the maximum exposure of 250K rad(Si)

“PRODUCTION RLAT Tests” were performed pre- and post-irradiation at the Cypress Semiconductor facility in San Jose, CA. After irradiation and on-site testing the parts were transported back to the Cypress facility using the TM1019 dry ice procedure.

All devices passed the full suite of AC, parametric and functional tests performed on the production tester.

Testing was performed by Mr. Jake Tausch of JD Instruments and monitored by Mr. Helmut Puchner of Cypress Semiconductor.

1.0 PART DESCRIPTION

Total Ionizing Dose (TID) Testing was performed by JD Instruments on one lot of16Mb SRAMs (CYRS1061). A total of 12 devices were irradiated for this testing and two devices were used as control/reference. All parts were serialized by the manufacturer.

These devices have the architecture shown in Figure 1.

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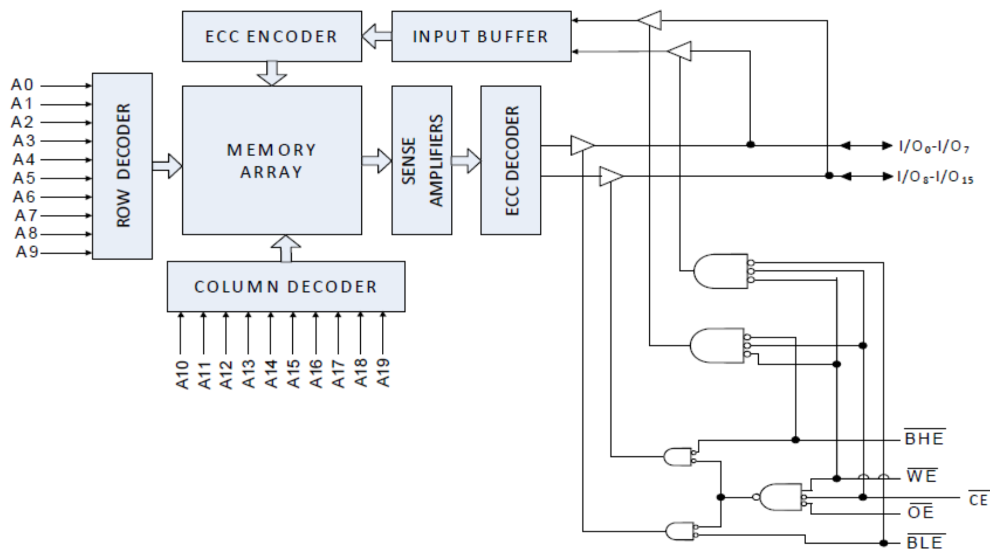

Figure 1. Functional Diagram for CYRS1061 16Mb SRAMs

2.0 TEST DESCRIPTION

Devices were provided in 54 pin SOIC packages. These were inserted into sockets for bias and test. A picture of a part mounted in a test socket is shown in Figure 2.

Figure 2. 54 Pin SOIC Device Mounted in Test Socket

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Special boards were used to provide bias to these parts during irradiations. Figure 3 shows one of the bias boards. Note that these boards were designed to accommodate the 54 pin ceramic version of these parts and also the 48 pin plastic version. The 4 sockets shown at the top of the picture were used during TID irradiations for the ceramic parts.

Figure 3. TID Bias Board

A small portion of the circuit schematic for the bias board is shown in Fig. 4 to detail the static bias conditions. Note that all parts are held in a standby state with half of the address pins and half of the I/O pins grounded and the other pins tied high.

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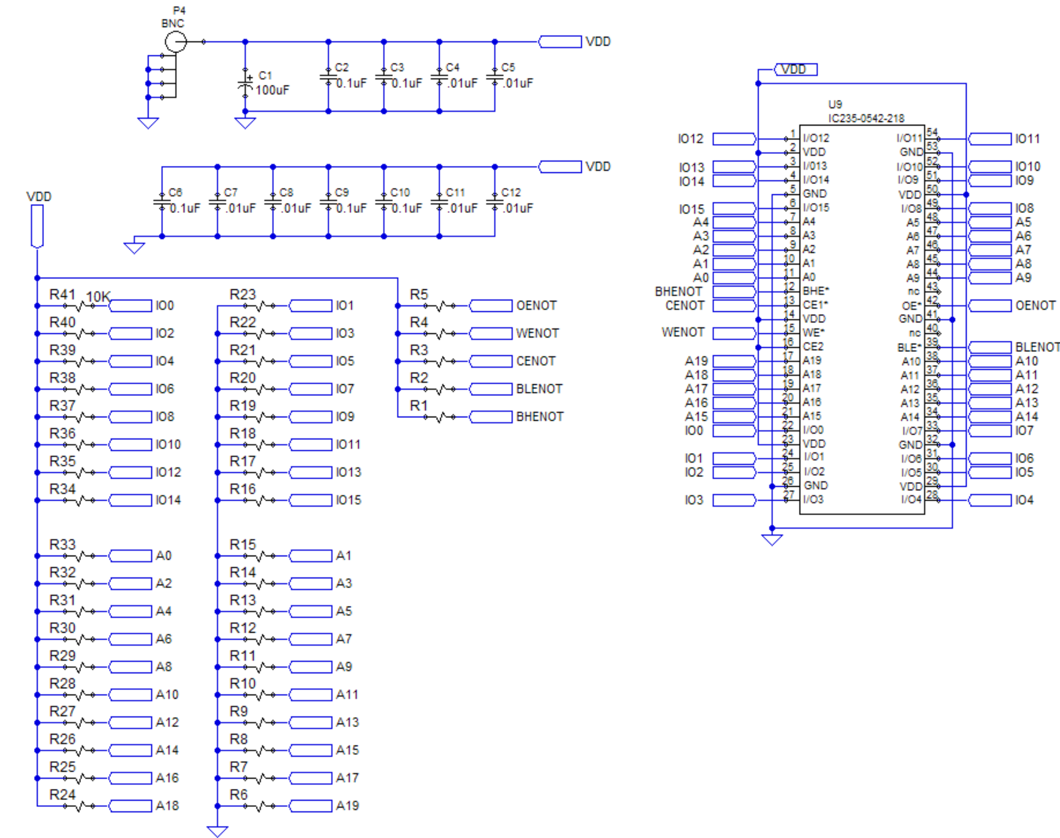

Fig. 4. Partial Circuit Schematic of Bias Board Showing Static Bias Conditions

These devices can be operated over a wide range of supply voltages between 2.3V and 5.5V. Irradiations were performed with devices biased to their maximum supply voltages (Vdd = 5.5V). Later testing was performed with devices biased to their lowest nominal operating voltage (Vdd =3.3V). This was considered the worst case combination of bias conditions since more radiation damage will be induced at a higher bias and AC performance (e.g. race conditions) are worse at lower biases.

RLAT testing was divided into 2 sets of tests: tests performed on-site at the radiation facility (ON-SITE RLAT TESTS) and tests performed remotely at the Cypress Semiconductor production facility (PRODUCTION RLAT TESTS).

After being irradiated parts were removed from the bias boards and ON-SITE RLAT TESTS were performed using a JD Instruments Algorithmic Test Vector (ATV) system. After all radiation exposures and on-site tests were completed the parts were packed in dry ice and transported to the main Cypress Semiconductor facility for PRODUCTION RLAT TESTS.

2.1 DOSIMETRY

Dosimetry was provided by AFRL personnel using a NIST traceable ion chamber. Dose rates for these tests were 54 rad(Si)/sec.

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2.2 ON-SITE RLAT TESTS

Before start of testing and after radiation exposure DUT functionality was verified using a MarchX test pattern. Standby current (I_{SB1} and I_{SB2} conditions) were measured with the parts loaded with both a logical checkerboard and logical checkerboard-NOT pattern. A list of parameters measured is shown in Fig. 5. These parameters were measured at room temperature using the nominal Vdd for these parts which is 3.3V.

Parameter		Test Conditions	Limit
Functionality		MarchX	Pass
Isb1 (CB)		Logical Checkerboard	<30mA
Isb2 (CB*)		Logical Checkerboard-Not	<30mA
Voh		Ioh = -4mA	>2.4V
Vol		Ioh = 8mA	<0.4V
Vih		MarchX, vary Vih to find passing level	>2V
Vil		MarchX, vary Vil to find passing level	<0.8V
Iix		Vin = 1/2Vdd	1uA
Ioz		Output Disabled, V=1/2Vdd	1uA
Icc		F = 25MHz	<80mA
Taa		Address to Data Valid	<10nS
Tace	(Tce)	CE* low to Data Valid	<10nS
Tdoe	(Toe)	OE* low to Data Valid	<5nS
Thzoe	(Tohz)	OE* high to high Z	<5nS
		Data setup to Write End for Both	
TSD-CE*	(Tds)	Write Cycle #1 (CE* controlled)	<5nS
TSD-WE*	(TdsCE)	Write Cycle #2 (WE* controlled)	<5nS

Names in Parens are the ATV test library names.

Fig. 5. Test Parameters and Limits

On-Site testing was performed using an Algorithmic Test Vector (ATV) system from JD Instruments as shown in figure 6. This is a portable system containing many of the features found in larger main-frame test systems. For this application it is particularly useful in that it collects data in both primitive error logs and also records summary results in spreadsheet form, simplifying on-site understanding of results as the test proceeds.

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Figure 6. ATV Test System used for SEE Testing

The part “travelers” that documented irradiation and test times is shown in Appendix A.

2.3 PRODUCTION RLAT TESTS

The full suite of production tests were performed on these devices both pre- and post-irradiation. Results of these tests are shown in Appendix B to this report.

3.0 LOT ACCEPTANCE TECHNIQUE

Parameters were measured and recorded in an excel format spread sheet. The measured values at each radiation step were analyzed using the Radiation Lot Acceptance Test (RLAT) “variables method” (see MIL-HDBK-814, Appendix Section 50, especially Table IXB).

In the RLAT variables method the average (Avg) and standard deviation (Std) of each parameter are calculated for the group of parts being irradiated. A value is then calculated and compared to the part limits using this average and standard deviation along with a one sided tolerance factor, KTL.

For parameters where the limit is higher than measured values the lot is acceptable if

$$Avg + KTL * Std < Limit \qquad \text{(eq. 1)}$$

For parameters where the limit is lower than measured values the lot is acceptable if

$$Avg - KTL * Std > Limit \qquad \text{(eq. 2)}$$

Values for KTL vary depending on sample size, Probability of Survival (Ps) and confidence level. For this test, with a radiation sample size of 12, Ps of 0.99 and a confidence level of 0.9, the value for KTL was 3.372 (MIL-HDBK-814, Table IXB).

Figure 7 shows test results for one of the parameters that changed slightly with radiation. This is a plot of Vil which is the input voltage which will affect the part as a valid logic low input. Vil was determined by

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repeatedly performing a MarchX test over a small memory space (1024 addresses) while varying the logic low level in a bisectional search. Vil was the maximum voltage at which the MarchX test was performed with no errors.

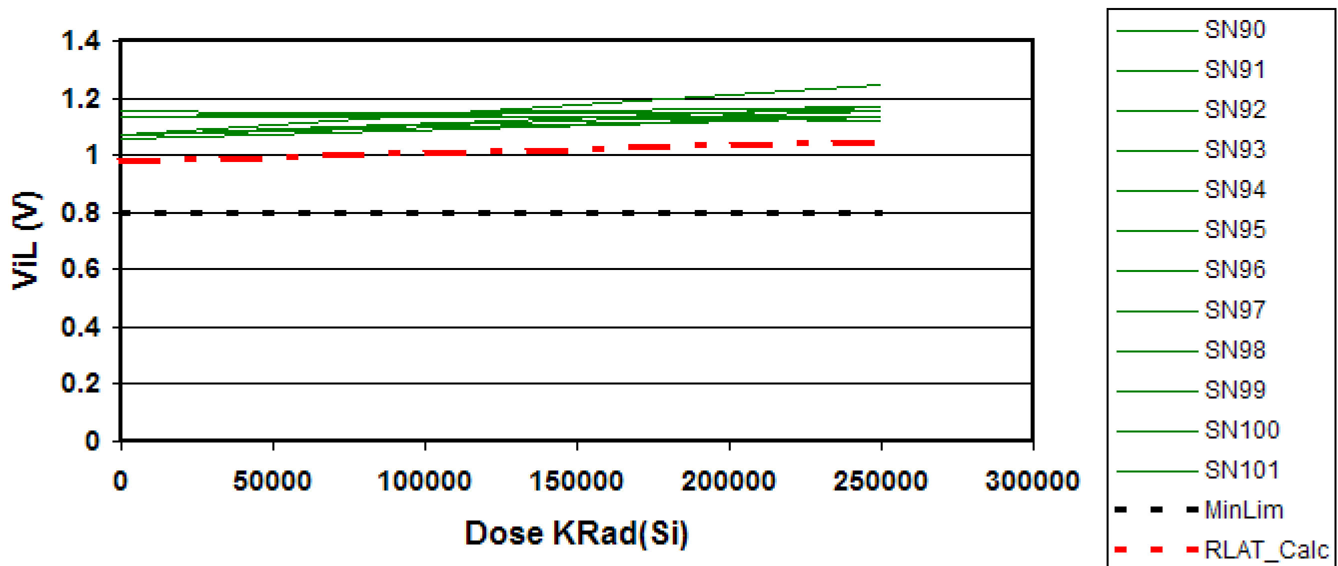

Figure 7. Idd Continuous READ – CheckerBoard

In this plot first note that the limit is plotted as a dashed, bold BLACK line and is 0.8V in this case. Measured values for each DUT are plotted using solid green lines. The RLAT value calculated from all measurements is plotted as a dashed, bold red line.

The plot shows that there was some variation in Vil across the 12 irradiated parts resulting in the RLAT value being distinctly outside the group of measured parameters. There was almost no change in these measurements after the radiation dose of 250K rad(Si). No part nor the RLAT calculation exceeded the limit.

4.0 ON-SITE RLAT Analysis Results

No memory bits on any device ever failed during this testing and are therefore not discussed further. Results of the other parameters are presented below.

4.1 Idd (F = 25MHz)

Power supply current was measured while performing a continuous write to the DUT. The results for Idd WR are shown in Figure 8

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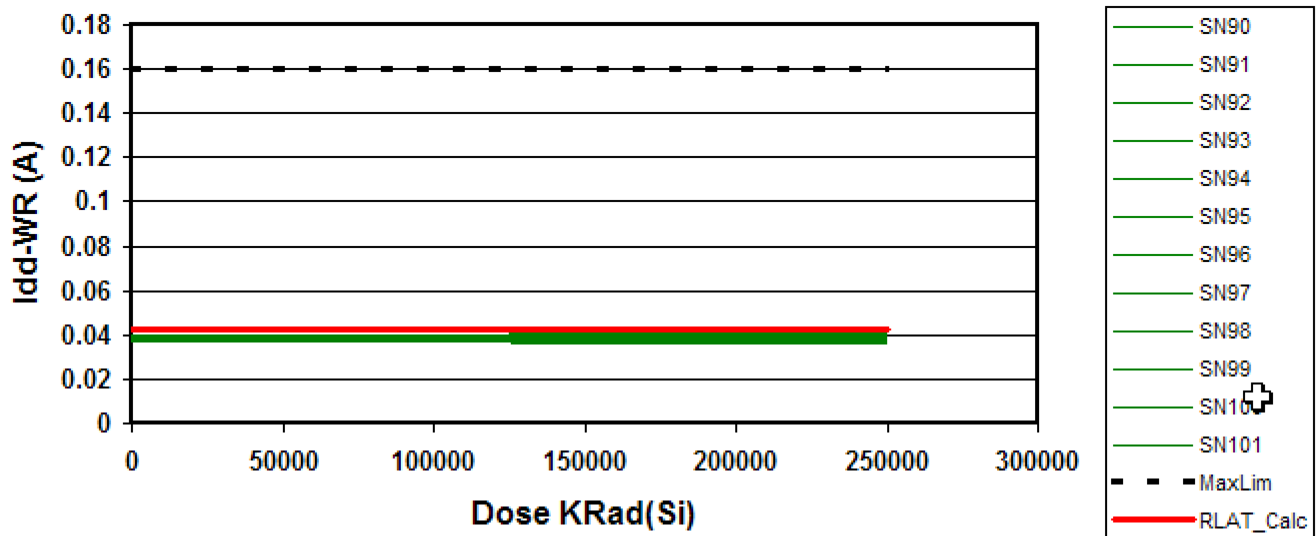

Fig. 8. Idd Continuous WRITE

Idd measured while performing continuous writes did not change appreciably after parts were irradiated to 250K rad(Si). Measurements from all parts were very similar resulting in a calculated RLAT value very close to DUT measurements.

4.2 Isb2 (Standby Current, Condition 2)

Standby currents were measured with parts in standby conditions 1 and 2. Figs. 9 and 10 show these currents for all parts. There was no change in these parameters when parts were irradiated to 250K rad(Si).

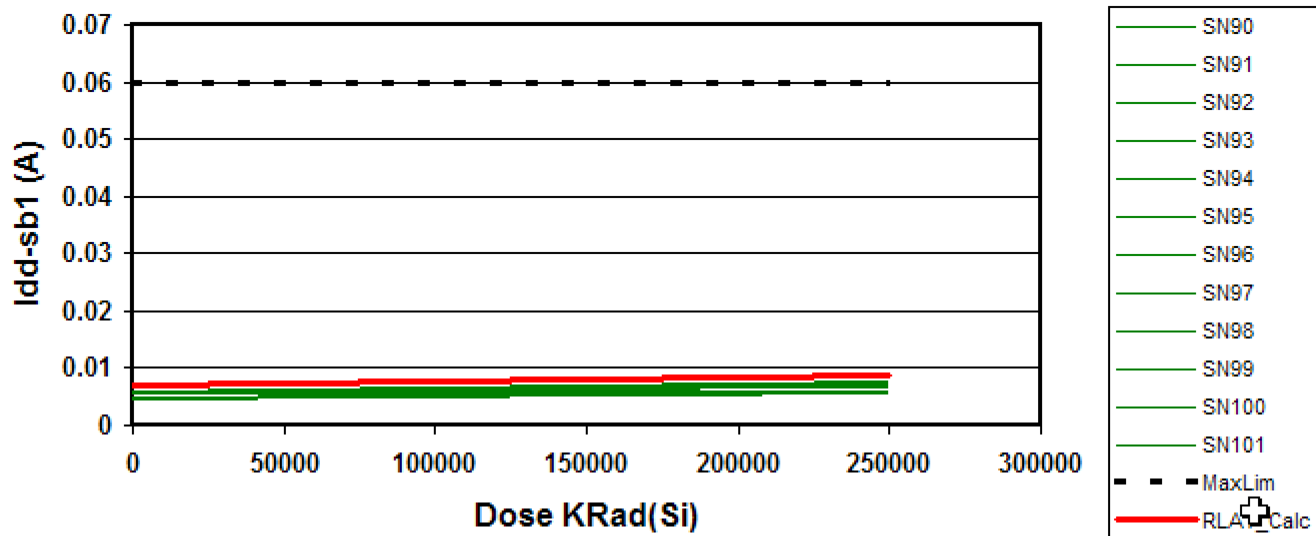

Fig. 9. Isb Condition 1

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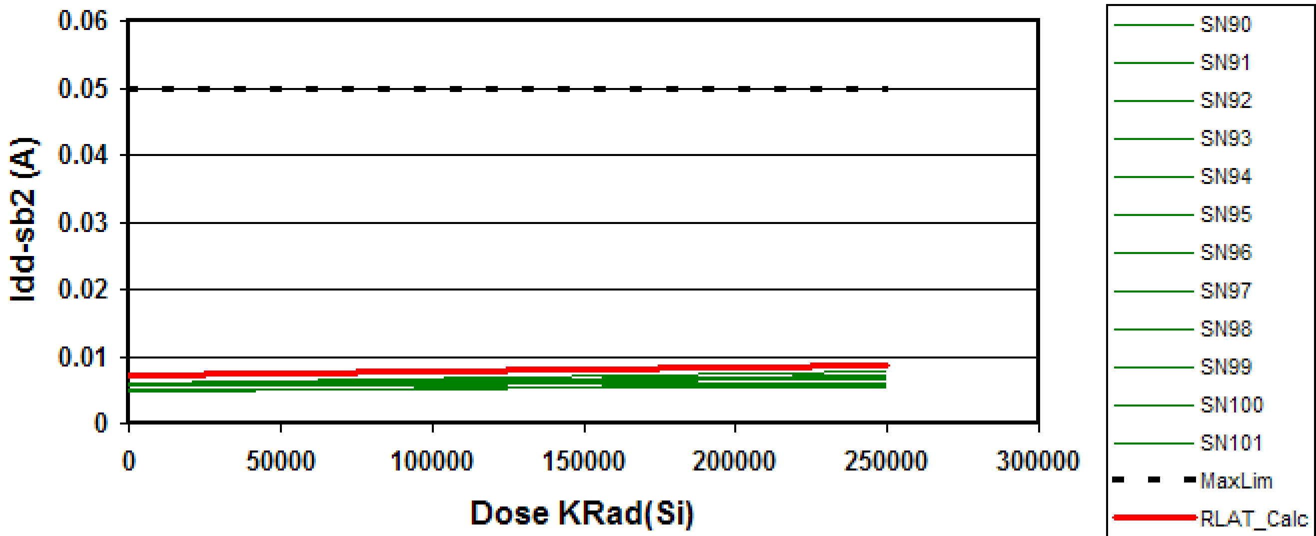

Fig. 10. Isb Condition 2

4.3 Vih and ViL

As mentioned earlier, Vih and Vil are measured by varying input logic levels in a bisectional search to determine the minimum Vih and maximum Vil where the DUT will correctly pass a MarchX test. Figure 11 shows measurements and RLAT analysis for Vih. Figure 12 shows measurements and RLAT analysis for Vil. There was no significant change in these parameters with increasing radiation and the lot passes RLAT analysis for both parameters.

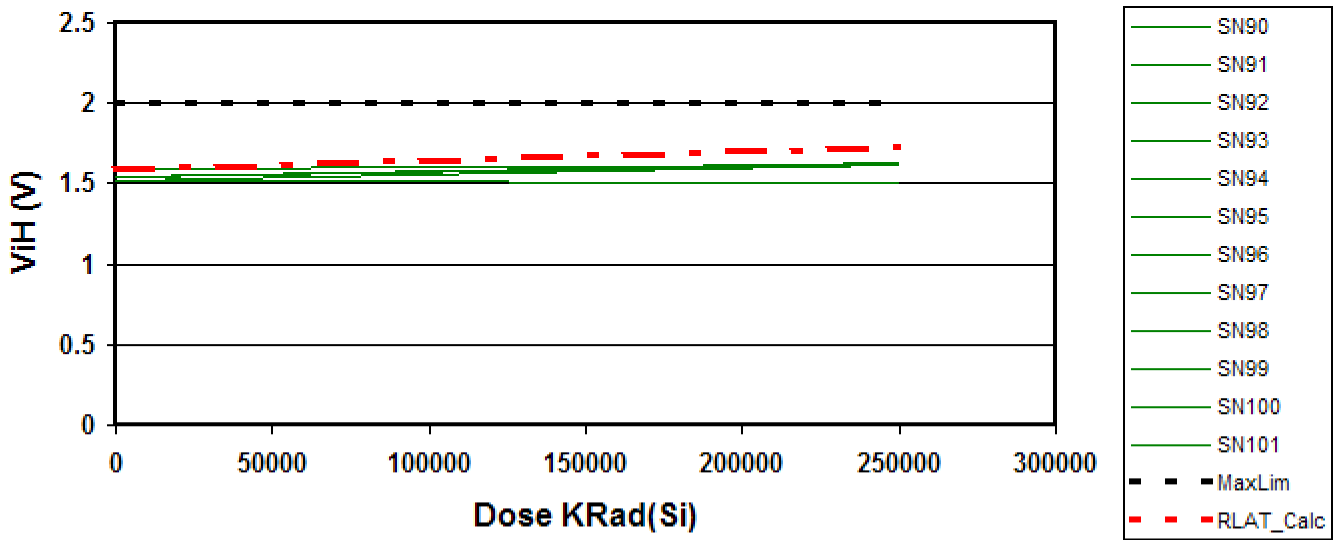

Figure 11. RLAT Results for Vih

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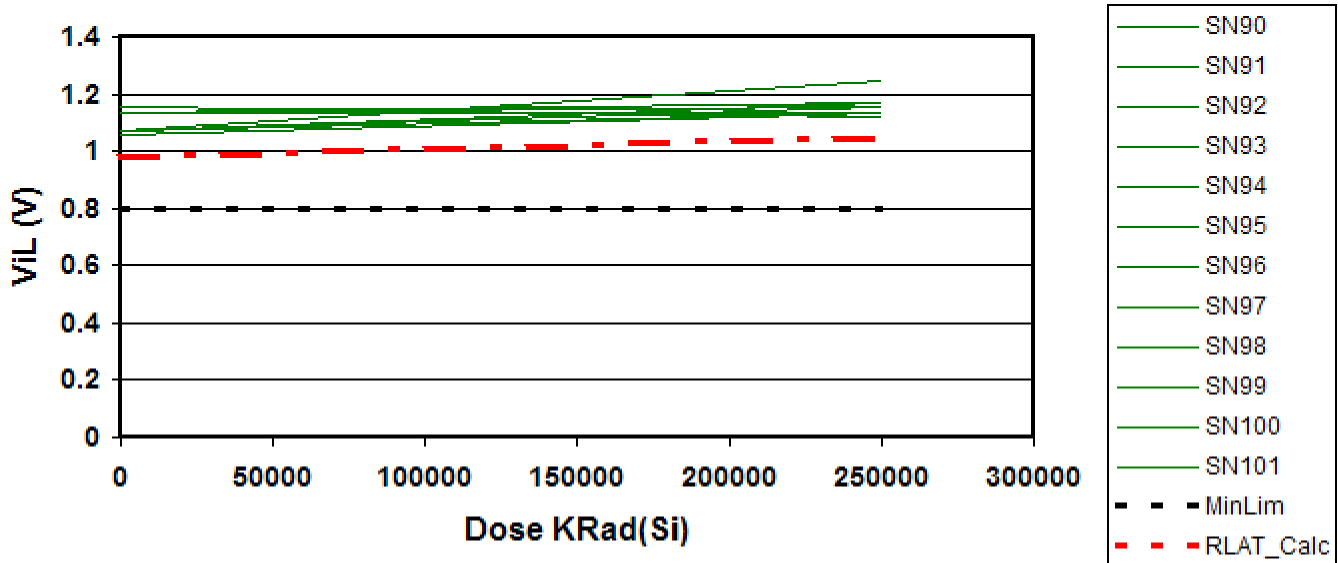

Figure 12. RLAT Results for ViL

4.4 Voh and Vol

Voh and Vol was measured on these parts by programming one memory address to all 1's or all 0's and then reading that address with a timing diagram such that the outputs would remain on. All 16 outputs were then measured and the worst case measurement was used as the parameter for that DUT. Voh was measured with a load current of 4mA and Vol with a load current of 8mA. Figure 13 shows the results for Voh and figure 14 for Vol. There was no detectable change in Voh with increasing radiation and a small "improvement" in Vol. This lot passes RLAT analysis for both parameters.

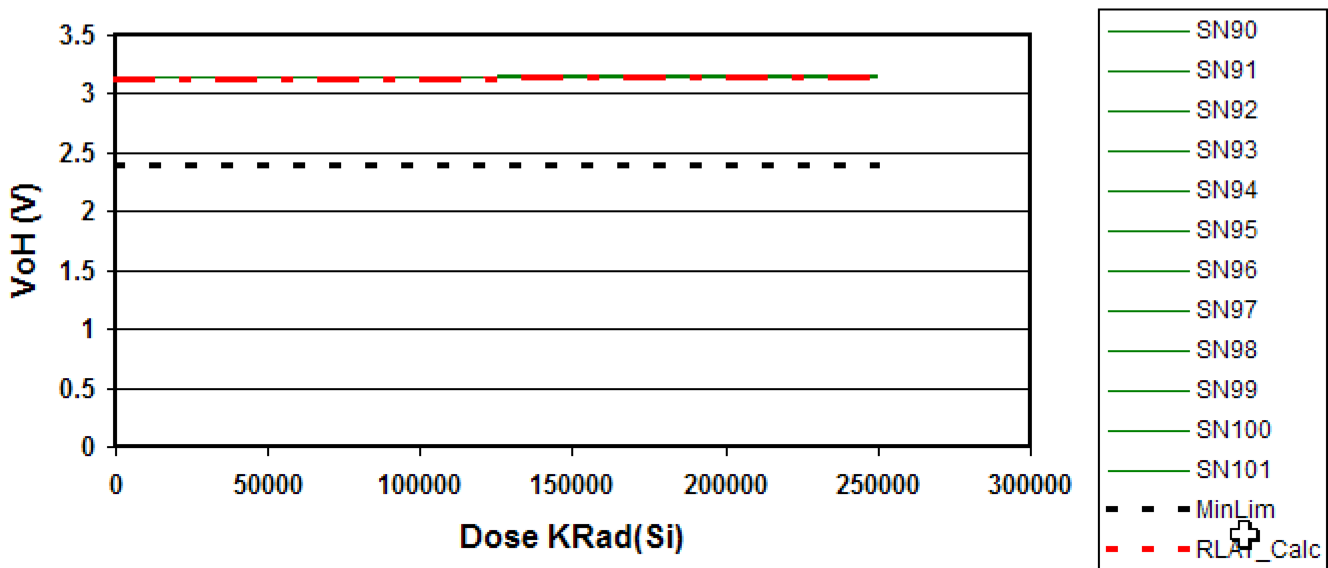

Figure 13. RLAT Results for Voh (4mA Load Current)

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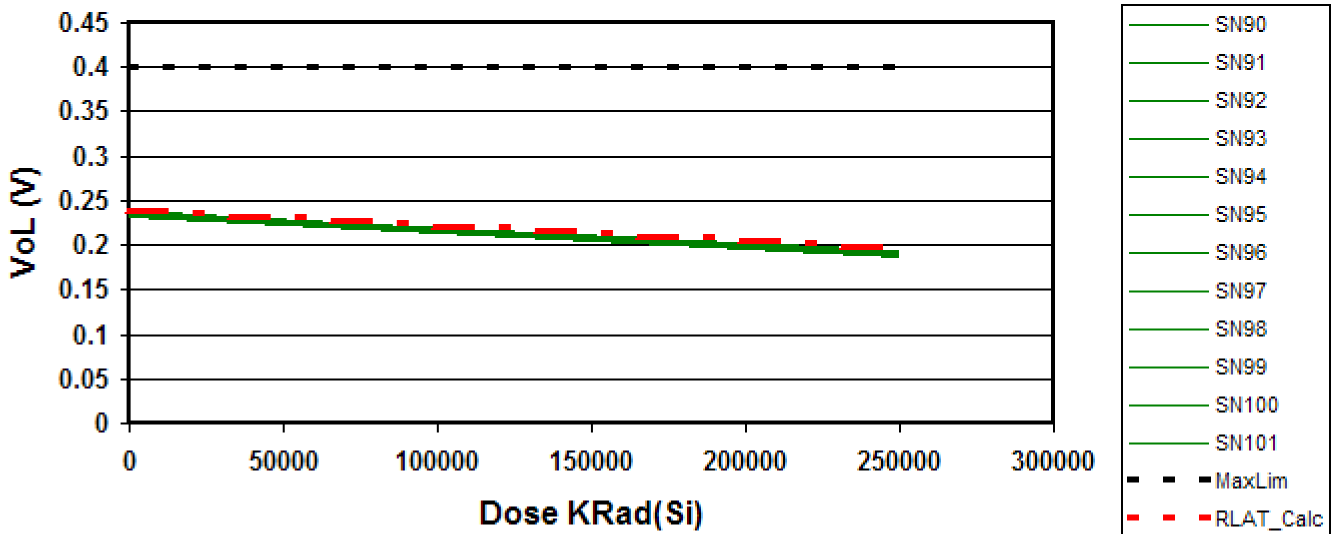

Figure 14. RLAT Results for Vol (8mA Load Current)

4.5 Iih and IiL

Iih and Iil are the input leakage currents when the inputs are biased to a logic high and logic low. Both have a limit of 5uA. Iih results are shown in figure 15. Iil results are shown in figure 16. Both parameters easily pass RLAT analysis for all lots.

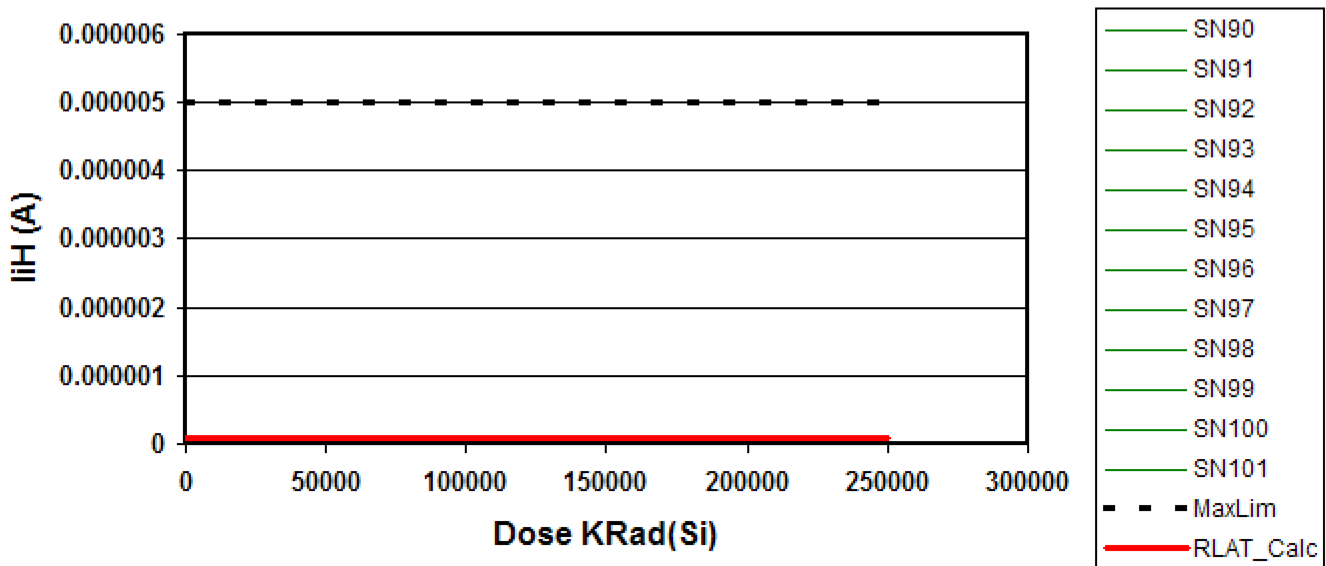

Figure 15. RLAT Results for Iih

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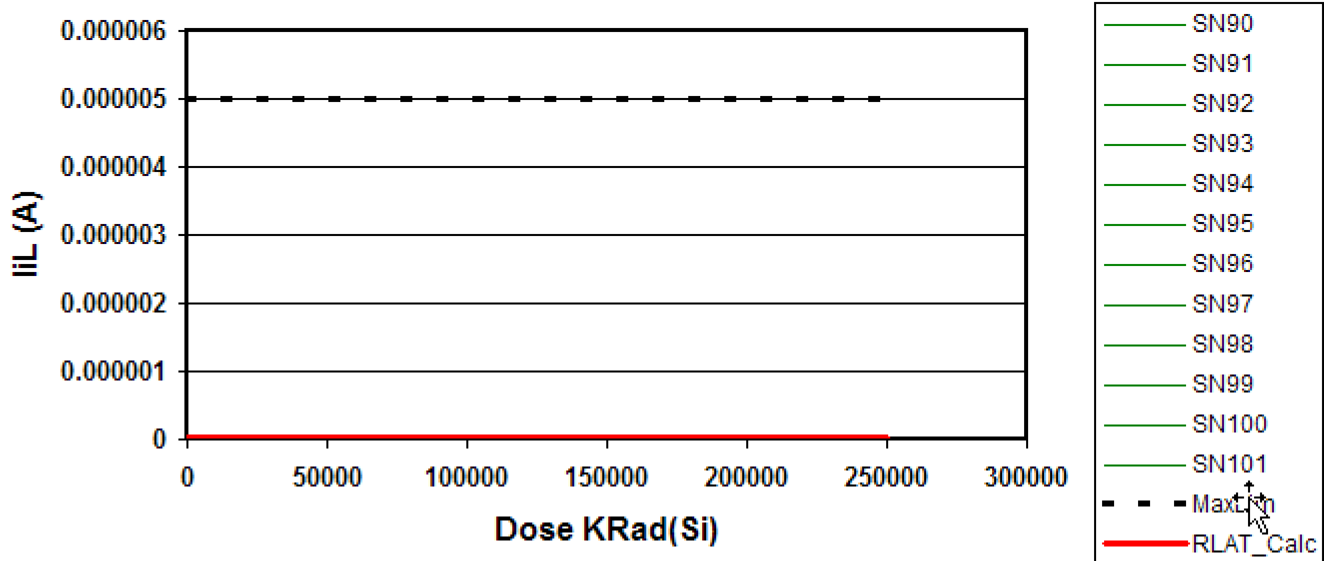

Figure 16. RLAT Results for IiL

4.6 Iozh and IozL

Iozh and Iozl are the output leakage currents when devices are tri-stated and voltages equal to logic high and logic low are applied to the outputs. Limits are 5uA for both parameters. Iozh measurements are shown in figures 17. Iozl measurements are shown in figure 18. Both parameters easily pass RLAT analysis for this lot.

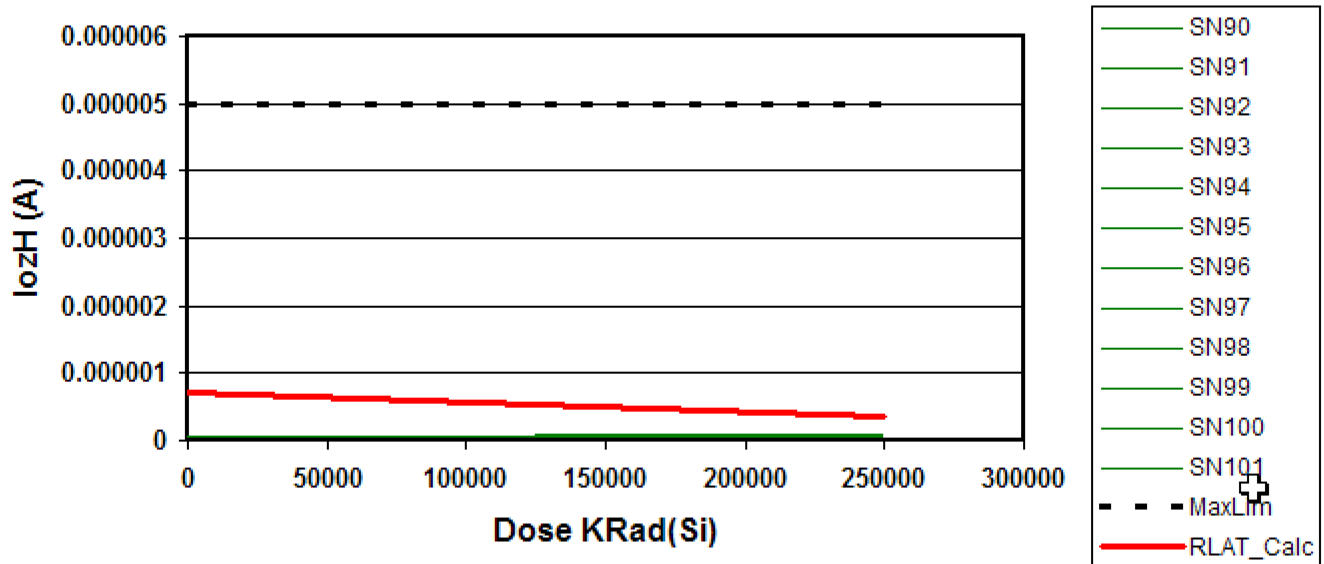

Figure 17. RLAT Results for Iozh

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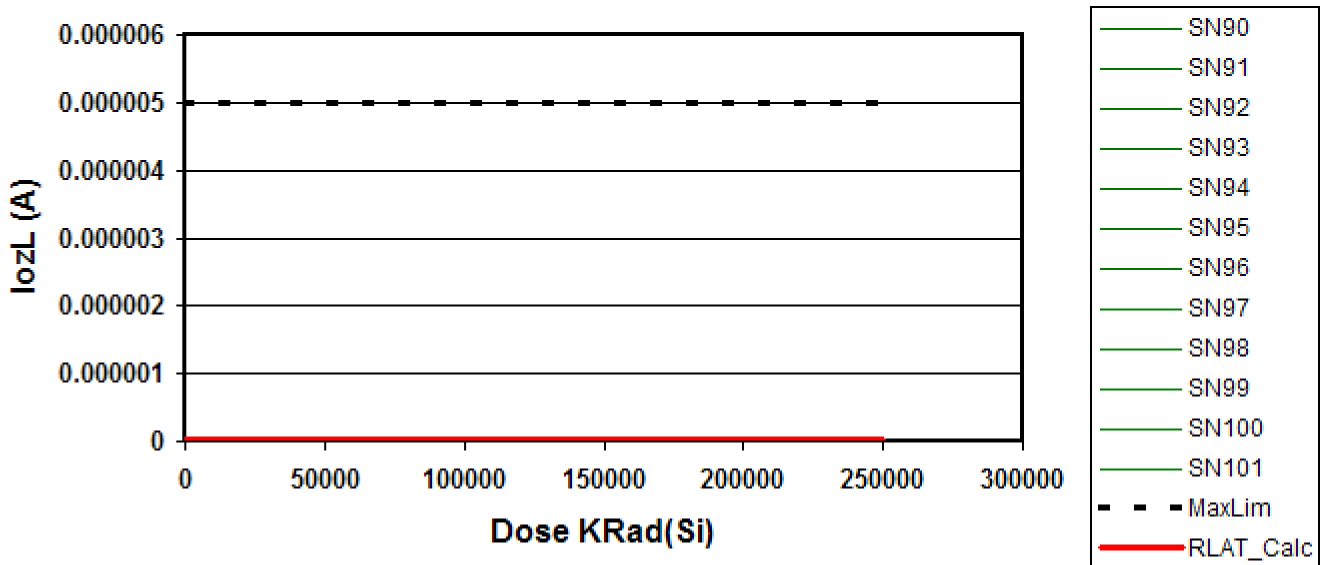

Figure 18. RLAT Results for IozL

4.7 Tace

Tace is the time between when CE* goes low and output data is valid. This parameter was measured by repeatedly performing a MarchX test while varying the delay between when the CE* signal was applied to a DUT and when a compare strobe was used to measure output values. The compare strobes were varied in steps of ~1nS so the results are somewhat “granular”. Measurements of this parameter are shown in figure 19.

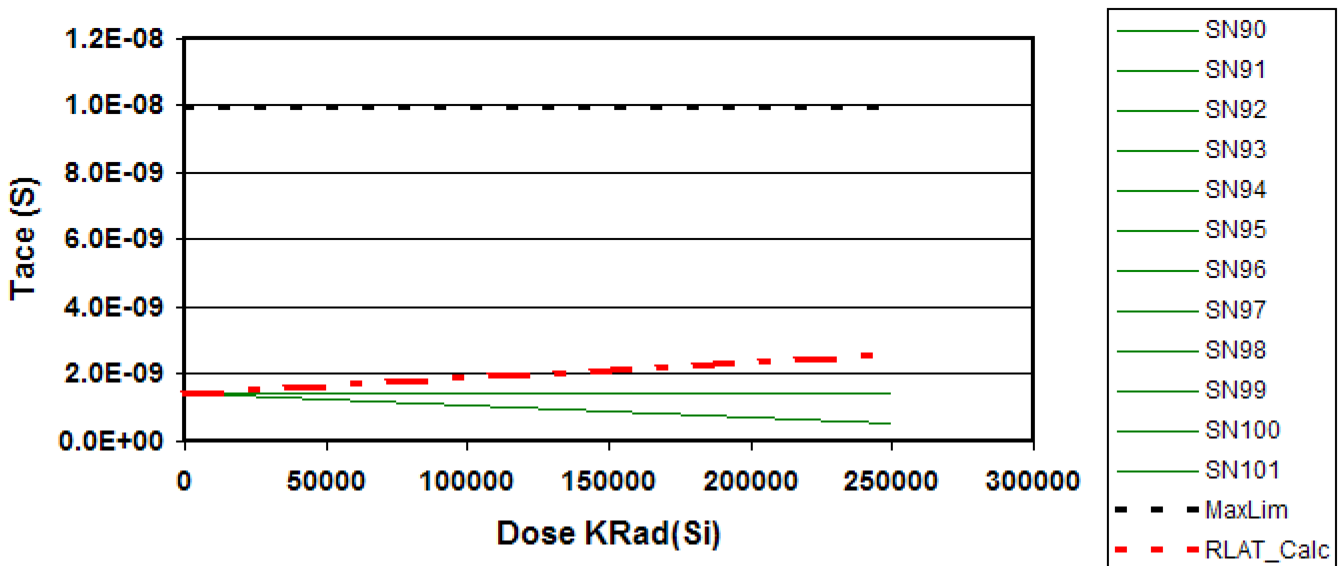

Figure 19. RLAT Results for Tace

The limit for this parameter is 10nS. All measurements and the RLAT calculation were all well below this limit.

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4.8 Tdoe

Tdoe is the time between when OE* goes low and output data is valid. This parameter was measured by repeatedly performing a MarchX test while varying the delay between when the OE* signal was applied to a DUT and when a compare strobe was used to measure output values. Measurements of this parameter are shown in figure 20.

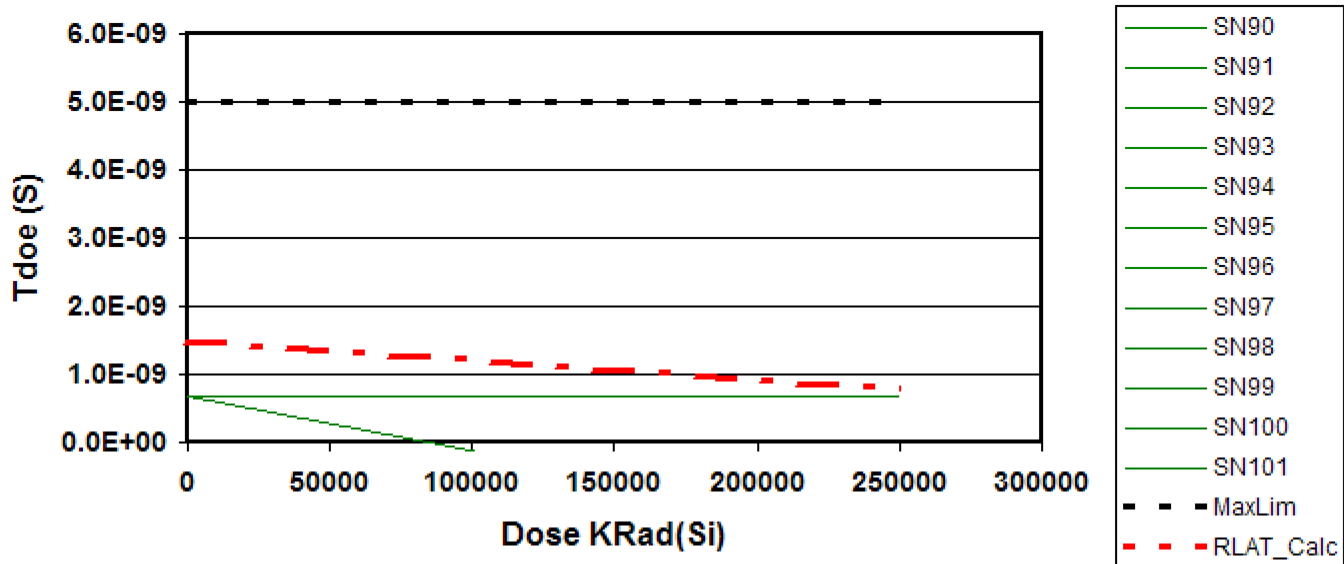

Figure 20. RLAT Results for Tdoe

The limit for this parameter is 5nS. All measurements and the RLAT calculation were all below this limit.

4.9 Taa

Taa is the time between when the address input changes and output data is valid. This parameter was measured by repeatedly performing a MarchX test while varying the delay between when the OE* signal was applied to a DUT and when a compare strobe was used to measure output values. Measurements of this parameter are shown in figure 21.

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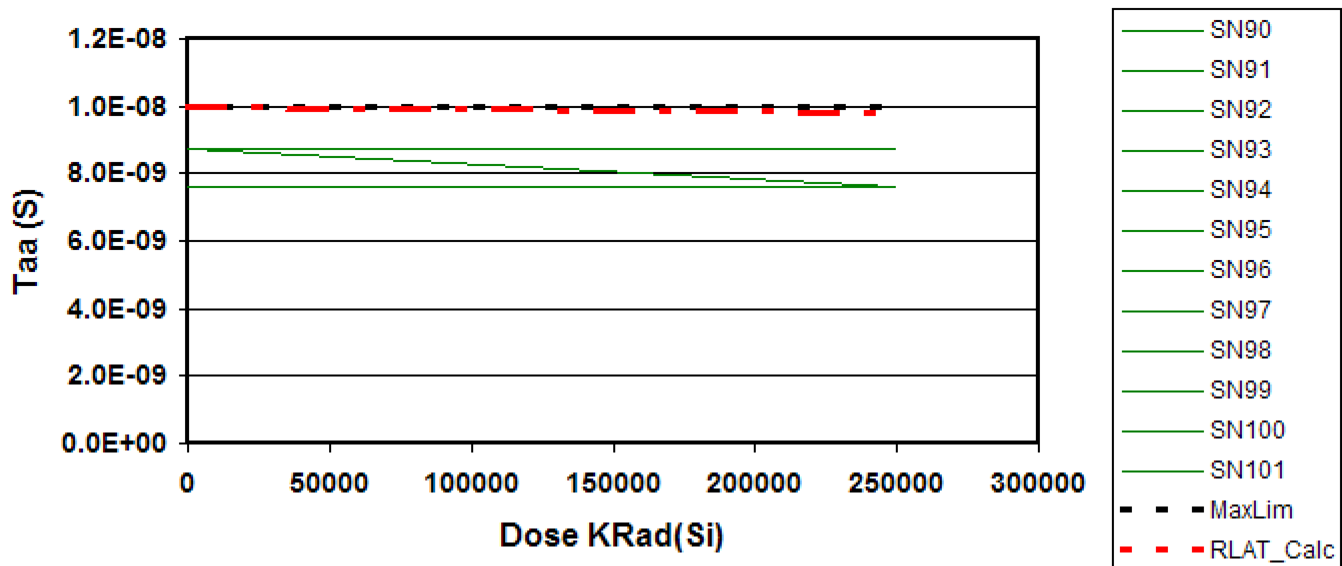

Figure 21. RLAT Results for Taa

The RLAT calculation for this parameter was close to the limit of 10nS but this was most likely due to the granular nature of the measurements. As can be seen from the plot there was no change in this parameter with radiation and measurements for all parts fell into 1 of 2 readings. If a finer grained time step had been used then distribution of this parameter would probably been tighter and this would have resulted in a better behaved RLAT calculation. Nonetheless the RLAT calculation was below the 10nS limit after 250K rad(Si).

4.10 Thzoe

Thzoe is the time between when OE* goes high and output data is no longer valid. This parameter was measured by repeatedly performing a MarchX test while varying the delay between when the OE* signal was pulsed high to a DUT and when a compare strobe was used to measure output values. Measurements of this parameter are shown in figure 22.

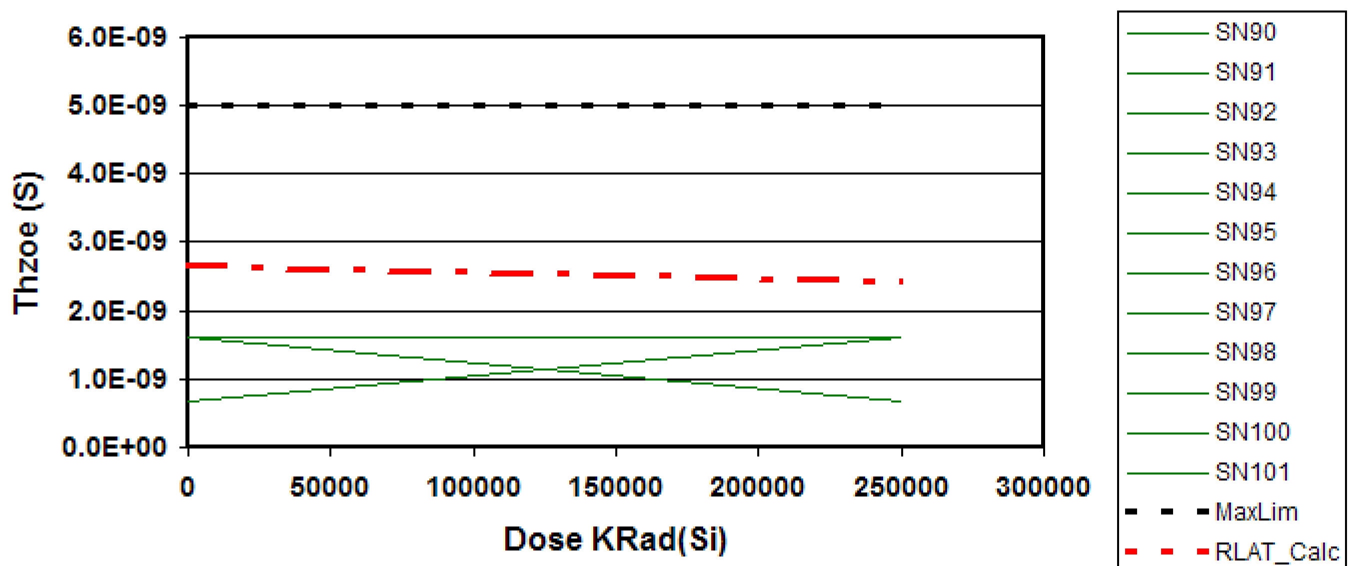

Figure 22. RLAT Results for Thzoe

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The limit for this parameter is 5nS. All measurements and the RLAT calculation were all well below this limit.

4.11 TSD-CE*

TSD-CE* is the data setup time before OE* goes high at the end of a write cycle. This parameter was measured by repeatedly performing a MarchX test while varying the delay between when a data input pattern is applied to a DUT and the OE* signal was pulsed high. Measurements of this parameter are shown in figure 23.

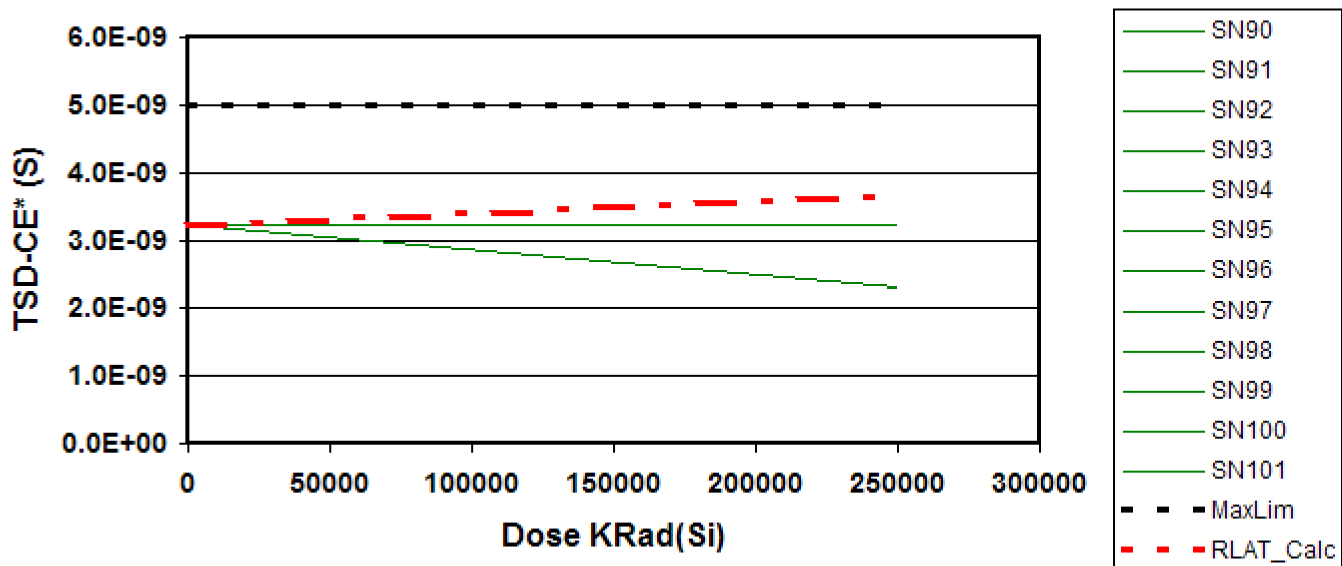

Figure 23. RLAT Results for TSD-CE*

The limit for this parameter is 5nS. All measurements and the RLAT calculation were well below this limit.

4.12 TSD-WE*

TSD-WE* is the data setup time before WE* goes high at the end of a write cycle. This parameter was measured by repeatedly performing a MarchX test while varying the delay between when a data input pattern is applied to a DUT and the WE* signal was pulsed high. Measurements of this parameter are shown in figure 24.

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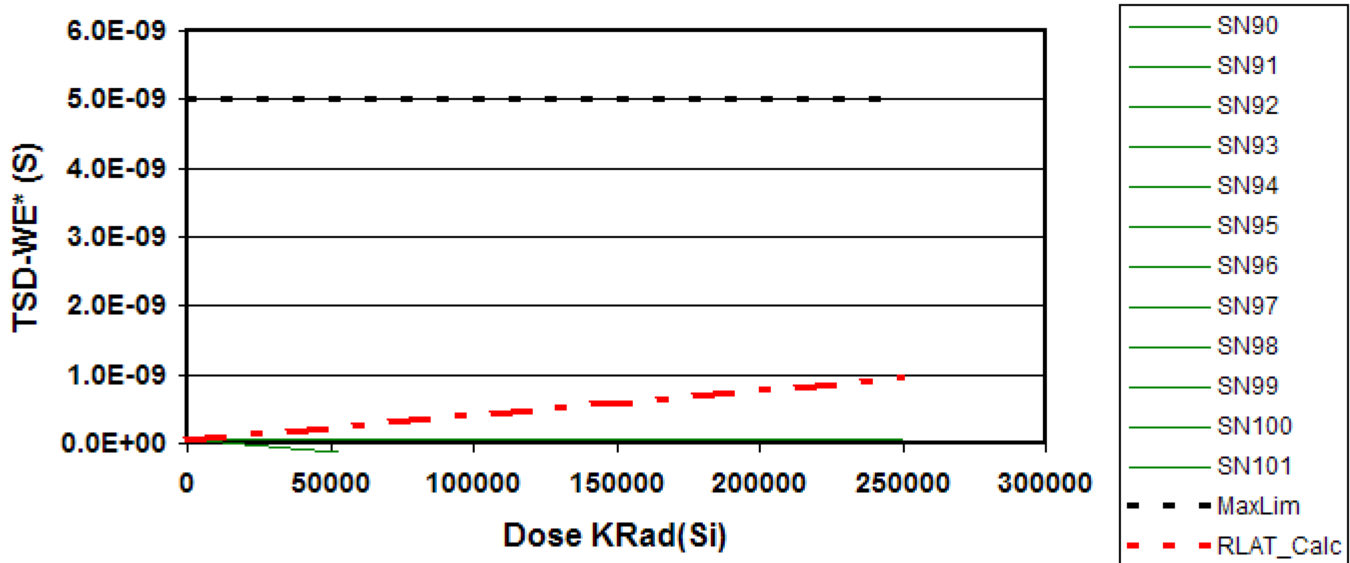

Figure 24. RLAT Results for TSD-WE*

The limit for this parameter is 5nS. All measurements and the RLAT calculation were well below this limit.

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6.0 Conclusions

CYRS1061 devices from fab lot L9903000, wafer #2 passed RLAT analysis to 250K rad(Si) on all parameters listed in the data sheet after the application of 99/90 KTL statistics.

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Appendix A. Part Traveler

JDI Rad Test Part Traveller - Dry Ice Shipment Option

Customer:	Cypress Semiconductor
Part Type:	CYRS1061G 16Mb SRAM
Test Type:	TID
P.O.:	4700013426

							TID Test					Remote Facility				
								Time				Unpack			Finish Test	
DUT	Lot	Wafer	SN	Alternate Marking	Received Date	PreRad Char	Date	Start Test	Last Test	Package	Temperature	Date	Time	Temperature	Date	Time
1	9903000	2	090		3-Dec-19	4-Dec-19	12/17/2019	12:25	12:28	12:46	-78.8	12/18/2019	9:53	-60	12/18/2019	9:57
2	9903000	2	091		3-Dec-19	4-Dec-19	12/17/2019	12:29	12:31	12:46	-78.8	12/18/2019	9:58	-60	12/18/2019	10:00
3	9903000	2	092		3-Dec-19	4-Dec-19	12/17/2019	12:41	12:43	12:46	-78.8	12/18/2019	10:01	-60	12/18/2019	10:03
4	9903000	2	093		3-Dec-19	4-Dec-19	12/17/2019	12:44	12:46	12:46	-78.8	12/18/2019	10:04	-60	12/18/2019	10:07
5	9903000	2	094		3-Dec-19	4-Dec-19	12/17/2019	12:33	12:37	13:07	-78.2	12/18/2019	10:08	-60	12/18/2019	10:08
6	9903000	2	095		3-Dec-19	4-Dec-19	12/17/2019	12:50	12:52	13:07	-78.2	12/18/2019	10:09	-60	12/18/2019	10:12
7	9903000	2	096		3-Dec-19	4-Dec-19	12/17/2019	12:53	12:59	13:07	-78.2	12/18/2019	10:13	-60	12/18/2019	10:15
8	9903000	2	097		3-Dec-19	4-Dec-19	12/17/2019	13:00	13:06	13:07	-78.2	12/18/2019	10:16	-60	12/18/2019	10:17
9	9903000	2	098		3-Dec-19	4-Dec-19	12/17/2019	14:36	14:38	14:50	-72.6	12/18/2019	10:18	-60	12/18/2019	10:19
10	9903000	2	099		3-Dec-19	4-Dec-19	12/17/2019	14:39	14:41	14:50	-72.6	12/18/2019	10:20	-60	12/18/2019	10:21
11	9903000	2	100		3-Dec-19	4-Dec-19	12/17/2019	14:42	14:45	14:50	-72.6	12/18/2019	10:22	-60	12/18/2019	10:23
12	9903000	2	101		3-Dec-19	4-Dec-19	12/17/2019	14:46	14:50	14:50	-72.6	12/18/2019	10:24	-60	12/18/2019	10:25
13	9903000	2	102	(Ref 1)	3-Dec-19	4-Dec-19	12/17/2019									
14	9903000	2	103	(Ref2)	3-Dec-19	4-Dec-19	12/17/2019									

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Appendix B. Production RLAT Tests

	SN 90	SN 91	SN 92	SN 93	SN 94	SN 95	SN 96	SN 97	SN 98	SN 99	SN 100	SN 101	RLAT_CALC	Limit	Pass/Fail
Voh 3.0V	2.867	2.8618	2.86	2.8661	2.8653	2.8652	2.8625	2.8575	2.8627	2.8624	2.8629	2.8597	2.853	>2.4	Pass
Vol, 3.0V	0.204	0.204	0.203	0.203	0.193	0.202	0.205	0.219	0.203	0.202	0.207	0.208	0.225	<0.4	Pass
Voh, 3.6V	3.4672	3.4605	3.4579	3.4663	3.4661	3.4664	3.4617	3.4578	3.4622	3.4617	3.462	3.4584	3.451	>2.4	Pass
Vol, 3.6V	0.190	0.191	0.190	0.190	0.187	0.189	0.192	0.192	0.190	0.189	0.193	0.194	0.197	<0.4	Pass
ILK_IH,3.0V	8.4E-08	9.0E-08	8.8E-08	8.4E-08	9.0E-08	8.4E-08	8.7E-08	8.8E-08	7.7E-08	9.6E-08	9.3E-08	8.0E-08	1.0E-07	< 1.0E-06	Pass
ILK_IH,3.6V	8.4E-08	9.4E-08	9.0E-08	9.2E-08	8.0E-08	7.8E-08	8.4E-08	8.5E-08	8.9E-08	8.7E-08	9.0E-08	8.4E-08	1.0E-07	< 1.0E-06	Pass
ILK_IL,3.0V	1.8E-08	2.5E-08	2.2E-08	2.5E-08	1.7E-08	1.5E-08	2.0E-08	1.4E-08	1.4E-08	1.5E-08	2.0E-08	1.5E-08	3.2E-08	< 1.0E-06	Pass
ILK_IL,3.6V	1.4E-08	1.9E-08	1.1E-08	1.0E-08	1.1E-08	1.6E-08	2.6E-08	2.4E-08	2.0E-08	1.4E-08	1.9E-08	1.3E-08	3.4E-08	< 1.0E-06	Pass
IOLK_IH,3.0V	8.7E-08	8.3E-08	8.6E-08	9.5E-08	8.4E-08	8.8E-08	9.1E-08	9.0E-08	9.1E-08	8.4E-08	8.8E-08	9.1E-08	1.0E-07	< 1.0E-06	Pass
IOLK_IH,3.6V	9.1E-08	8.3E-08	8.4E-08	9.5E-08	9.6E-08	9.8E-08	8.7E-08	8.9E-08	9.3E-08	9.3E-08	9.5E-08	1.0E-07	1.1E-07	< 1.0E-06	Pass
IOLK_IL,3.0V	1.4E-08	1.7E-08	1.4E-08	2.2E-08	1.8E-08	1.9E-08	1.4E-08	2.1E-08	2.8E-08	2.4E-08	1.7E-08	1.2E-08	3.4E-08	< 1.0E-06	Pass
IOLK_IL,3.6V	1.4E-08	1.3E-08	2.2E-08	2.1E-08	1.4E-08	1.7E-08	1.4E-08	1.7E-08	1.5E-08	6.3E-09	1.4E-08	1.7E-08	2.9E-08	< 1.0E-06	Pass
ICC,3.6V	0.0894	0.0944	0.0924	0.0950	0.0917	0.0937	0.0954	0.0900	0.0959	0.0924	0.0898	0.0904	0.1004	<0.175	Pass
ISB1,3.6V	0.0070	0.0069	0.0057	0.0063	0.0060	0.0070	0.0062	0.0069	0.0059	0.0071	0.0067	0.0066	0.0082	<0.035	Pass
ISB2,3.6V	0.0063	0.0063	0.0052	0.0056	0.0053	0.0063	0.0054	0.0062	0.0053	0.0064	0.0062	0.0061	0.0076	<0.035	Pass
ICCDR,2V	0.0056	0.0054	0.0043	0.0048	0.0045	0.0056	0.0046	0.0055	0.0044	0.0056	0.0052	0.0052	0.0068	<0.025	Pass

Pre-Rad

	SN 90	SN 91	SN 92	SN 93	SN 94	SN 95	SN 96	SN 97	SN 98	SN 99	SN 100	SN 101	RLAT_CALC	Limit	Pass/Fail
Voh 3.0V	2.8659	2.8603	2.8585	2.8641	2.8643	2.8632	2.8589	2.862	2.8614	2.8617	2.8611	2.8569	2.853	>2.4	Pass
Vol, 3.0V	0.205	0.204	0.204	0.203	0.199	0.204	0.203	0.204	0.203	0.202	0.208	0.209	0.212	<0.4	Pass
Voh, 3.6V	3.4655	3.458	3.4548	3.4628	3.4638	3.4617	3.4576	3.4594	3.4585	3.4584	3.4574	3.4539	3.447	>2.4	Pass
Vol, 3.6V	0.190	0.191	0.190	0.189	0.186	0.188	0.189	0.191	0.188	0.188	0.192	0.193	0.195	<0.4	Pass
ILK_IH,3.0V	1.1E-07	8.9E-08	9.2E-08	1.0E-07	9.0E-08	9.4E-08	1.0E-07	9.9E-08	8.9E-08	8.8E-08	8.4E-08	9.4E-08	1.2E-07	< 1.0E-06	Pass
ILK_IH,3.6V	8.0E-08	8.7E-08	8.7E-08	9.9E-08	8.4E-08	8.7E-08	8.7E-08	9.2E-08	8.3E-08	9.4E-08	8.9E-08	8.7E-08	1.1E-07	< 1.0E-06	Pass
ILK_IL,3.0V	1.0E-08	1.8E-08	3.2E-08	1.8E-08	2.2E-08	1.7E-08	1.1E-08	2.3E-08	1.5E-08	1.8E-08	1.1E-08	1.8E-08	3.8E-08	< 1.0E-06	Pass
ILK_IL,3.6V	2.3E-08	1.3E-08	1.5E-08	1.4E-08	2.2E-08	2.2E-08	2.4E-08	2.1E-08	1.9E-08	1.2E-08	1.9E-08	1.2E-08	3.3E-08	< 1.0E-06	Pass
IOLK_IH,3.0V	8.5E-08	8.3E-08	9.2E-08	9.1E-08	8.8E-08	9.5E-08	9.5E-08	9.3E-08	3.8E-07	8.3E-08	8.3E-08	8.3E-08	4.0E-07	< 1.0E-06	Pass
IOLK_IH,3.6V	8.6E-08	8.7E-08	9.7E-08	9.3E-08	8.1E-08	9.3E-08	8.5E-08	8.8E-08	2.9E-07	9.3E-08	9.3E-08	9.0E-08	3.1E-07	< 1.0E-06	Pass
IOLK_IL,3.0V	1.4E-08	1.2E-08	1.7E-08	1.8E-08	1.2E-08	1.6E-08	1.2E-08	1.3E-08	2.0E-08	2.2E-08	1.6E-08	1.7E-08	2.7E-08	< 1.0E-06	Pass
IOLK_IL,3.6V	1.1E-08	2.8E-08	2.0E-08	1.5E-08	1.8E-08	1.2E-08	1.2E-08	1.8E-08	3.1E-08	2.3E-08	1.5E-08	1.8E-08	4.0E-08	< 1.0E-06	Pass
ICC,3.6V	0.0794	0.0810	0.0794	0.0833	0.0809	0.0822	0.0843	0.0794	0.0878	0.0812	0.0797	0.0786	0.0903	<0.175	Pass
ISB1,3.6V	0.0065	0.0067	0.0057	0.0060	0.0060	0.0072	0.0059	0.0062	0.0058	0.0072	0.0065	0.0061	0.0081	<0.035	Pass
ISB2,3.6V	0.0061	0.0063	0.0053	0.0054	0.0054	0.0067	0.0054	0.0057	0.0054	0.0067	0.0062	0.0058	0.0076	<0.035	Pass
ICCDR,2V	0.0053	0.0055	0.0046	0.0046	0.0046	0.0059	0.0046	0.0049	0.0046	0.0059	0.0054	0.0050	0.0069	<0.025	Pass

Post-Rad

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