TDM22545D OptiMOS™

Dual Phase 120A Power Stage Module with Integrated Inductor

Features

- Integrated dual converters including two smart power stages, two inductors, and decoupling capacitors
- Infineon's latest smart power stages utilize OptiMOS™-6 MOSFETs
- 4x 0402 25-V, X7R, 0.22- µF input capacitors included
- 2x 0603 25-V, X7S, 2.2- µF input capacitors included
- 4x 0201 10-V, X7R, 0.1- µF Vcc decoupling capacitors included
- 2x 0201 10-V, X7R, 0.1- µF bootstrap capacitors included
- 2x 0201 0 Ohm bootstrap resistors included
- Output DC current capability of 70 A per phase (Thermally managed)
- Output peak current capability of 120 A per phase
- Input voltage (VIN) range of 4.25 V to 16 V
- On-chip MOSFET Current sensing and reporting at 5 µA/A.
- 8mV / °C temperature analog output
- VCC supply of 4.25 V to 5.5 V
- Output voltage range from 0.225 V up to 3 V at VIN = 12 V
- Operation up to 2 MHz
- VCC under voltage lockout (UVLO)
- Bootstrap under-voltage protection
- Auto-replenishment on bootstrap capacitors
- Over temperature protection and thermal shutdown
- Cycle-by-cycle over current Protection (OCP) and flag
- Control MOSFET short (HSS) detection and flag
- Compatible with 3.3 V tri-state PWM Input
- Body-Braking™ load transient support
- DEEP SLEEP mode for power saving via EN= low (32 µA typ per phase)
- Lead free RoHS compliant package
- Small LGA package in 10 mm (length) x 9 mm (width) x 5 mm (height)

Potential applications

- Artificial Intelligence accelerators chips
- CPU Power
- FPGA Power
- Telcom/datacenter

Product validation

Qualified for industrial applications according to JESD47 and IPC9701

Description

- High frequency, compact DC-DC converters
- Voltage Regulators for CPUs, GPUs, FPGAs and DDR memory arrays
- Server, communication and artificial intelligence systems.

The TDM22545D dual OptiMOS™ Power Module co-packages two smart power stages, two power inductors, and decoupling capacitors to implement two independent synchronous buck converters into a small 10mm x 9mm x 5mm package. The package is optimized for PCB layout, heat transfer, driver/MOSFET control timing, and minimal switch node ringing. The smart power stage pairs optimized gate drivers and MOSFETs to enable higher efficiency at lower output voltages required by cutting edge CPU, GPU, FPGA and DDR memory designs.

The improved MOSFET current-mirror current-output sensing achieves superior current sense accuracy versus best-in-class controller-based Inductor DCR sense as well as MOSFET Rdson current sense methods.

Protections include IC temperature reporting and over temperature protection feature (OTP with thermal shutdown), cycle-by-cycle over current protection (OCP), control MOSFET short detection (HSS - High side short detection), and VCC under-voltage protection. The OptiMOS™ Power Module power stage also features "refreshing" of bootstrap capacitor to prevent the bootstrap capacitor from over-discharging.

Inductors are optimized for switching frequencies between 600 kHz to 1.2 MHz, which enables high performance transient response while maintaining industry leading efficiency.

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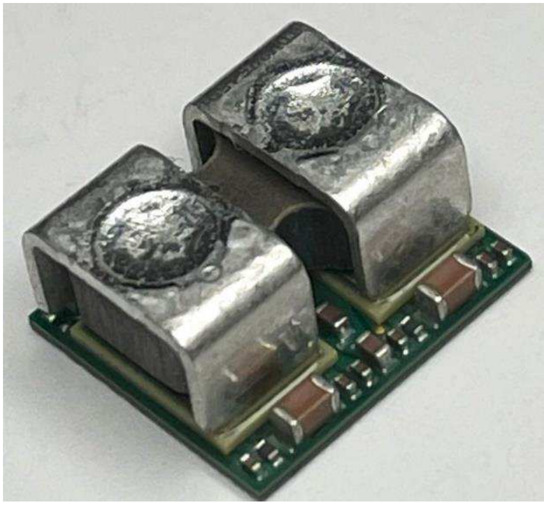
1 Ordering information

Table 1 Ordering Information

Part Number	Temp Range	Package	Orderable Part Number
TDM22545D	0 to 125°C	LG-MLGA-72-1 10 mm x 9 mm x 5 mm	TDM22545DXUMA1



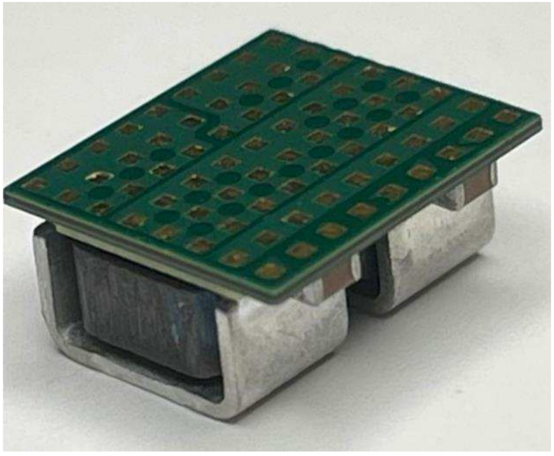


Figure 1 Picture of the Product, Top and Bottom Side

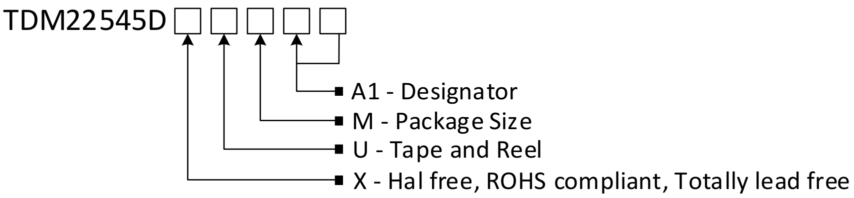


Figure 2 Part Number Configuration

2 Functional block diagram

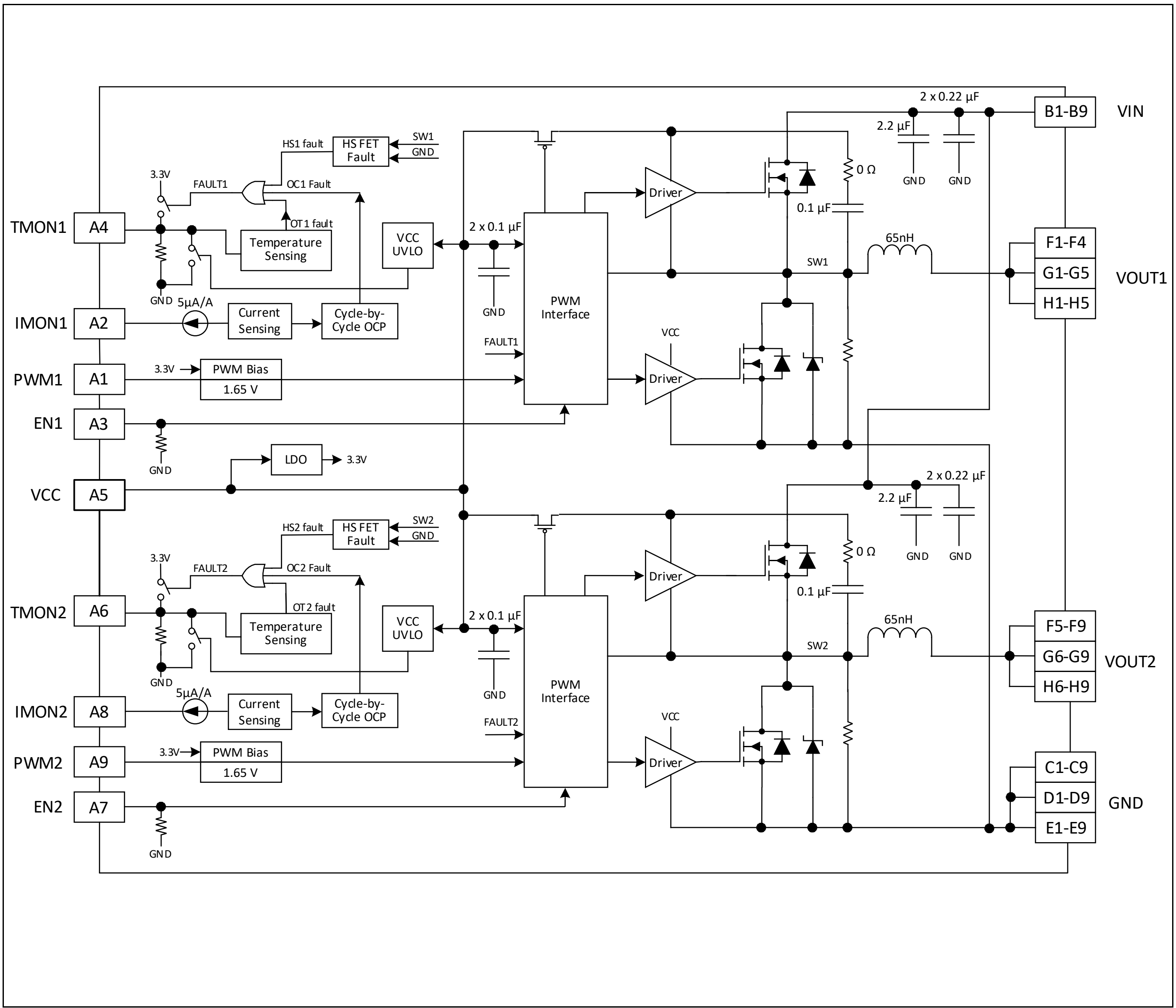


Figure 3 TD22545D Block diagram

3 Pin descriptions

3.1 Pinout

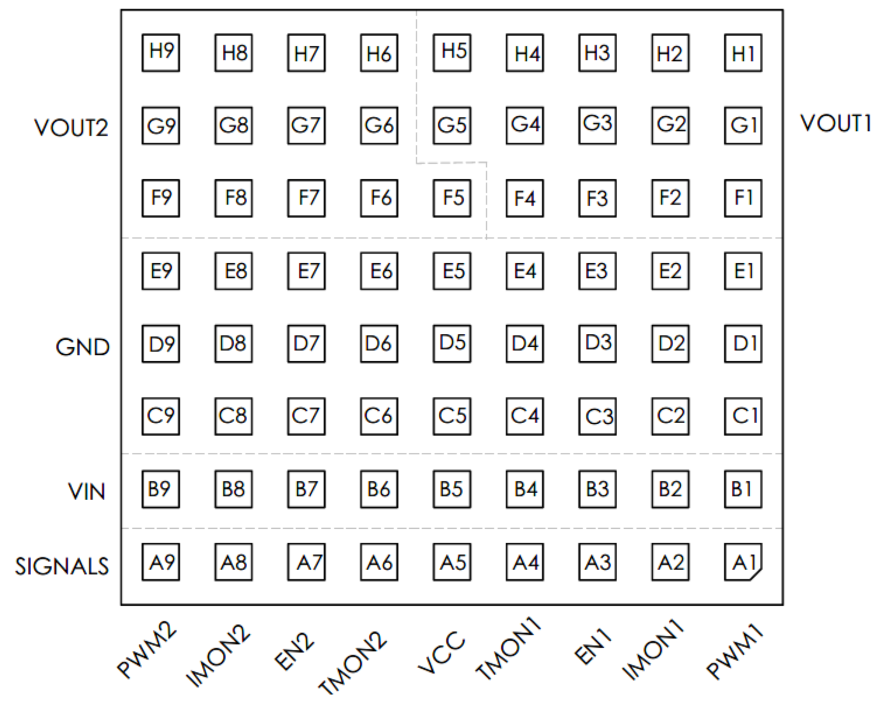


Figure 4 Pinout, Numbering and Name of Pins (transparent top view)

Note:

I = Input, O = Output,

Table 2 Pin Descriptions

Pin No.	Name	Pin Type	Buffer Type	Function
A1	PWM1	I	+3.3 V logic	3.3 V logic level PWM input of Phase 1. PWM input: "High" turns control MOSFET on; "Tri-state" turns both MOSFETs off; "Low" turns the synchronous MOSFET on.
A2	IMON1	O	Analog	Sensed current output signal of Phase 1 through external resistor. Voltage across that resistor represents current information.
A3	EN1	I	+3.3 V logic	Enable control of Phase 1. Pulling EN high enables the driver; pulling EN low disables the driver and enters ultra-low quiescent current mode. Floating this pin is not recommended, however a pull-down is embedded to keep the driver off if the pin is floating. This pin is VCC tolerant.

Pin No.	Name	Pin Type	Buffer Type	Function
A4	TMON1	O	Analog	Temperature monitoring of Phase 1. The voltage at this pin is defined by the equation, 8mV * (Celsius Temperature) + 0.6 V. This pin will be pulled up to 3.3 V under severe over-temperature, over-current, high-side MOSFET short, or bootstrap under-voltage condition.
A6	TMON2	O	Analog	Temperature monitoring of Phase 2. The voltage at this pin is defined by the equation, 8mV * (Celsius Temperature) + 0.6 V. This pin will be pulled up to 3.3 V under severe over-temperature, over-current, high-side MOSFET short, or bootstrap under-voltage condition.
A7	EN2	I	+3.3 V logic	Enable control of Phase 2. Pulling EN high enables the driver; pulling EN low disables the driver and enters ultra-low quiescent current mode. Floating this pin is not recommended, however a pull-down is embedded to keep the driver off if the pin is floating. This pin is VCC tolerant.
A8	IMON2	O	Analog	Sensed current output signal of Phase 2 through external resistor. Voltage across that resistor represents current information. This pin is also used for advanced fault reporting to identify the type of fault and faulty phase
A9	PWM2	I	+3.3 V logic	3.3 V logic level PWM input of Phase 2. PWM input: “High” turns control MOSFET on; “Tri-state” turns both MOSFETs off; “Low” turns the synchronous MOSFET on.
F1-F4, G1-G5, H1-H5	VOUT1	O	Analog	Output pins of the converter phase 1.
F5-F9, G6-G9, H6-H9	VOUT2	O	Analog	Output pins of the converter phase 2.
A5	VCC	POWER	–	Supply voltage for control logic and drivers. Four 0201 10-V 0.1-uF VCC decoupling capacitors included. VCC should be connected to +5 V power supply.
B1-B9	VIN	POWER	–	4.25 V to 16 V high current input voltage connection of Phase 1 and Phase 2. Four 0402 25-V 0.22-uF and two 0603 25-V 2.2uF input decoupling capacitors included.
C1-C9, D1-D9, E1-E9	PGND	GND	–	Power ground. They are also the power ground of the synchronous MOSFETs.

4 Absolute maximum ratings

Note: $T_A = 25°C$

Table 3 Absolute maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of the PWM input	f_{SW}	0.3	–	2	MHz	
Maximum average load current per phase	I_{OUT1}, I_{OUT2}	–	–	70	A	Thermally managed
Maximum peak load current per phase	I_{OUT_PEAK1}, I_{OUT_PEAK2}	–	–	120	A	
Input voltage	V_{IN}	-0.3	–	25	V	Pin VIN
Logic and supply voltage	V_{CC}	-0.3	–	6.5	V	Pin VCC
Output voltage	V_{OUT}	-0.3	–	6.5	V	Pins VOUT1 and VOUT2
EN voltage	V_{EN1}, V_{EN2}	-0.3	–	6.5	V	Pins EN1 and EN2
PWM voltage	V_{PWM1}, V_{PWM2}	-0.3	–	4.0	V	Pins PWM1 and PWM2
TMON voltage	V_{TMON1}, V_{TMON2}	-0.3	–	3.6	V	Pins TMON1 and TMON2
IMON voltage	V_{IMON1}, V_{IMON2}	-0.3	–	3.6	V	Pins IMON1 and IMON2
Junction temperature	T_{Jmax}	-40	–	150	°C	–
Storage temperature	T_{STG}	-40	–	150	°C	–

Note:

All rated voltages are relative to voltages on the AGND and PGND pins unless otherwise specified.

Attention: ***Stresses above those listed in Table 3 "Absolute Maximum Ratings" may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings for extended periods may adversely affect the operation and reliability of the device.***

5 Thermal Characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance-Junction to PCB (pin D9)	θ_{JC_PCB}	–	1.0	–	K/W	–
Thermal resistance-Junction to top of package	θ_{JC_Top}	–	2.5	–		–

6 Recommended Operating Conditions

Table 5 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input voltage	V_{IN}	4.25	–	16	V	–
Logic supply and MOSFET driver voltage	V_{CC}	4.25	–	5.5		–
Frequency of the PWM1 and PWM2	f_{SW}	300	–	2000	kHz	-
EN1 and EN2 voltage	V_{EN}	–	–	5.5	V	Pins EN1 and EN2
PWM1 and PWM2 voltage	V_{PWM}	–	–	3.6	V	Pins PWM1 and PWM2
Current Sense reference voltage	V_{IMON_CM}	1.1	–	1.9	V	Pins IMON1 and IMON2
Ambient temperature	T_{AMB}	0	–	+85	°C	–
Junction temperature	T_{jOP}	0	–	+125	°C	–

7 Electrical Characteristics

Note: $V_{CC} = 5\ V$, $T_J = 25$

Table 6 Voltage Supply, Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO, VCC rising	V_{UVLO_R}	3.9	4.05	4.2	V	Note 2
UVLO, VCC faling	V_{UVLO_F}	3.7	3.85	4.0		Note 2
Driver current	I_{VCC}	–	80	–	mA	EN1 = EN2 = H, f_{SW} = 800 kHz, D=15%
		–	72	–	µA	No switching, EN1 = EN2 = L
VIN Current	I_{VIN}	–	–	10	µA	No switching, EN1 = EN2 = L Note 2
VIN Current	I_{VIN}	–	200	280	mA	EN1=L, EN2 = H or EN1=H, EN2 = L, f_{SW} = 800 kHz, D=15%
VIN Current	I_{VIN}	–	400	550	mA	EN1=H, EN2=H, f_{SW} = 800 kHz, D=15%

Table 7 Current Sense

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
IMON1, IMON2	IMON Voltage range	V_{IMON}	0.8	–	2.35	V	DC + AC components. Note 1
	Current sense gain	A_{cs}	–	5	–	µA/A	Note 2
	IMON Gain resistor range	R_{IMON}	–	1	–	kΩ	Resistor to be connected between IMON and GND. For 5mV/A, recommended 1kΩ R_{IMON}
	Leakage Current	I_{Leak}	-2	0	2	µA	I_{OUT} = 0A, V_{IMON}=1.2V, PWM in tri-state.
	Accuracy at T_J = -5 to 125°C V_{CC} = 5 V ± 10 %		-3.0	–	3.0	%	For 25A < I_{OUT} < I_{OCP_TH}. Note 1
			-0.5	–	0.5	A	For -25A < I_{OUT} < 25A. Note 1

Table 8 Temperature Sense and Fault Communication

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TMON1, TMON2	Temperature Sense Slope	$A_{TMPGAIN}$	7.84	8.0	8.16	mV/°C	25°C ≤ T_J ≤ 125°C. Note 2
	Temperature Sense Offset Voltage	$V_{TMPOFFSET}$	784	800	816	mV	T_J = 25°C, 0.6 V + 8 mV/°C * T_J. Note 2
	TMON / FAULT Source Current	$I_{TMONSRC}$	400	500	650	µA	TMON / FAULT pulled low. Note 2
	TMON / FAULT Sink Current	$I_{TMONSNK}$	26	32	40	µA	TMON / FAULT pulled high. Note 2
	Fault mode Active High	$V_{TFLTHIGH}$	2.6	3.3	3.6	V	$I_{TMON/FAULT}$ = 5 mA and under Over-Temperature, Over-Current, bootstrap undervoltage or HSS Fault. Note 2
	TMON / FAULT Low	$V_{TFLTLOW}$	–	–	0.17	V	No Fault, $V_{CC} < V_{UVLO1\_R}$. Note 2
	TMON / FAULT pull down resistance	R_{PULLDN_TMON}	125	150	200	kΩ	No Fault, $V_{CC} < V_{UVLO1\_R}$. Note 2

Table 9 Other Logic Functions, Inputs/Outputs and Thresholds

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
EN1, EN2	Enable Power-on Delay	$t_{EN\_ondelay}$	5	17	25	µs	PWM=0. Measured from EN rising edge to V_{GL}> 1 V. Note 2
	Enable Power-off Delay	$t_{EN\_offdelay}$	0.1	-	1	µs	PWM=0. Measured from EN falling edge to V_{GL} < 4 V. Note 2
	Internal Pull-down Resistance	R_{PULLDN_EN}	220	280	350	kΩ	When EN is floating. Note 2
	Input High Voltage	V_{EN_H}	2.0	–	–	V	
	Input Low Voltage	V_{EN_L}	–	–	0.95	V	
PWM1, PWM2	PWM Input High Threshold	V_{IH}	2.4	–	–	V	PWM Low or Tri-state to High.
	PWM Input Low Threshold	V_{IL}	–	–	0.8	V	PWM High or Tri-state to Low.
	PWM Hysteresis	I_{PWM_HYS}	1	40	120	mV	Active to Tri-state or Tri-state to Active. Note 2
	PWM Input Tri-State Floating Voltage	V_{PWM_TRI}	1.4	1.6	1.8	V	PWM Input Floating. Note 2
	Tri-state Window	V_{PWM_S}	1.2	–	2.0	V	Note 2

	PWM Input Equivalent Pull-up Resistance	R_{PWM_PU}	12	20	28	kΩ	Note 2
	PWM Input Equivalent Pull-down Resistance	R_{PWM_PD}	42	50	65	kΩ	Note 2

Table 10 Protection

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
OTP	Over Temp Rising Threshold	T_{RISE}	–	140	–	°C	TMON/FAULT pulled up high. Note 2
	Over Temp Falling Threshold	T_{FALL}	–	128	–	°C	TMON/FAULT released. Note 2
HSS FAULT	TMON/FAULT Delay	T_{HSS_DEL}	–	150	–	ns	After V_{HSS_TH} is detected, and TMON/FAULT is pulled high. Note 2
OCP	Over-Current Threshold	I_{OCP_TH}	107	120	133	A	Note 2
	Over-Current Delay	T_{OCP_DEL}	10	–	–	Cycle	PWM High-Low Cycles to TMON/FAULT is pulled high. Note 2

Note:

1. Guaranteed by design but not tested in production.
2. Guaranteed by design and tested prior module assembly.

8 Typical efficiency and Power Loss curves

8.1 Fsw = 600kHz, Vout = 0.8V

PVin = 6.75V, 12.0V and 13.5V Io = 0A - 80A, fsw= 600 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of TDM22545D, the inductor losses, the losses of the input and output capacitors, and PCB trace losses.

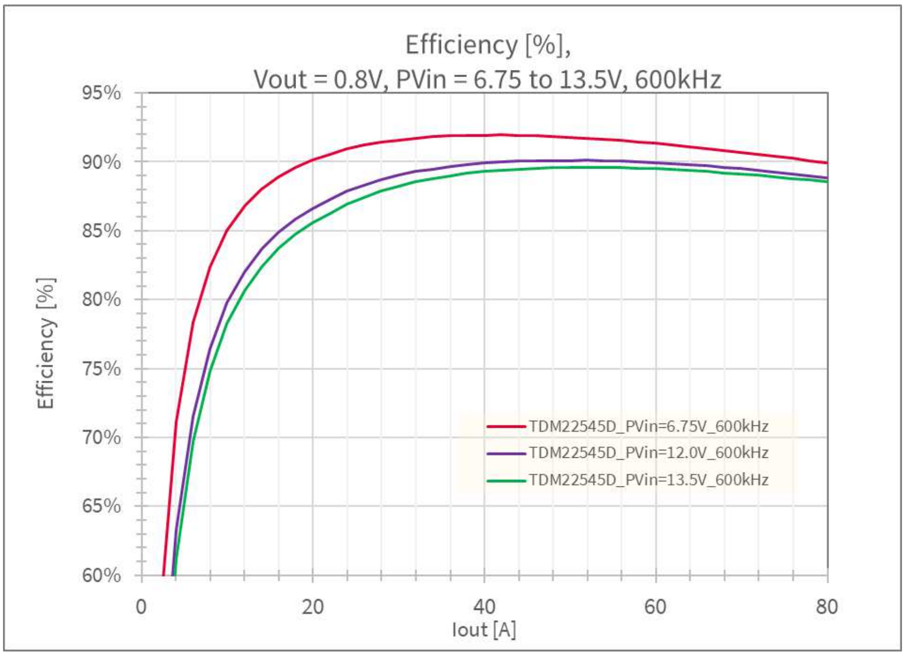


Figure 5 TDM22545D, PVin = 6.75V, 12.0V and 13.5V.

8.2 Fsw = 800kHz, Vout = 0.8V

PVin = 4.50V to 16.0V Io = 0A - 80A, fsw= 800 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of TDM22545D, the inductor losses, the losses of the input and output capacitors, and PCB trace losses.

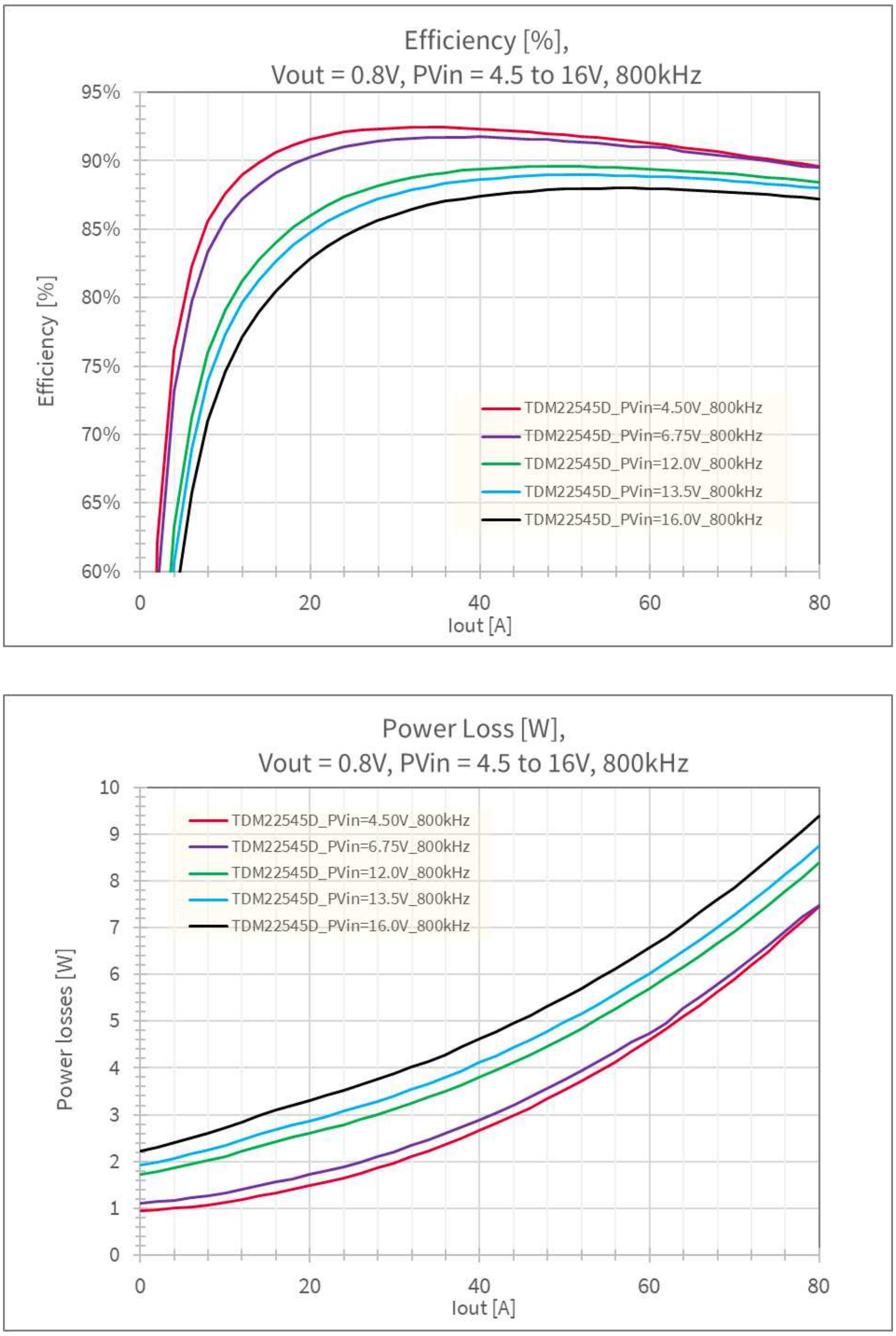


Figure 6 TDM22545D, PVin = 4.50V, 6.75V, 12.0V, 13.5V and 16.0V.

8.3 Fsw = 1000kHz, Vout = 0.8V

PVin = 6.75V, 12.0V and 13.5V Io = 0A - 80A, fsw= 1000 kHz, Room Temperature, No Air Flow. Note that the efficiency and power loss curves include the losses of TDM22545D, the inductor losses, the losses of the input and output capacitors, and PCB trace losses.

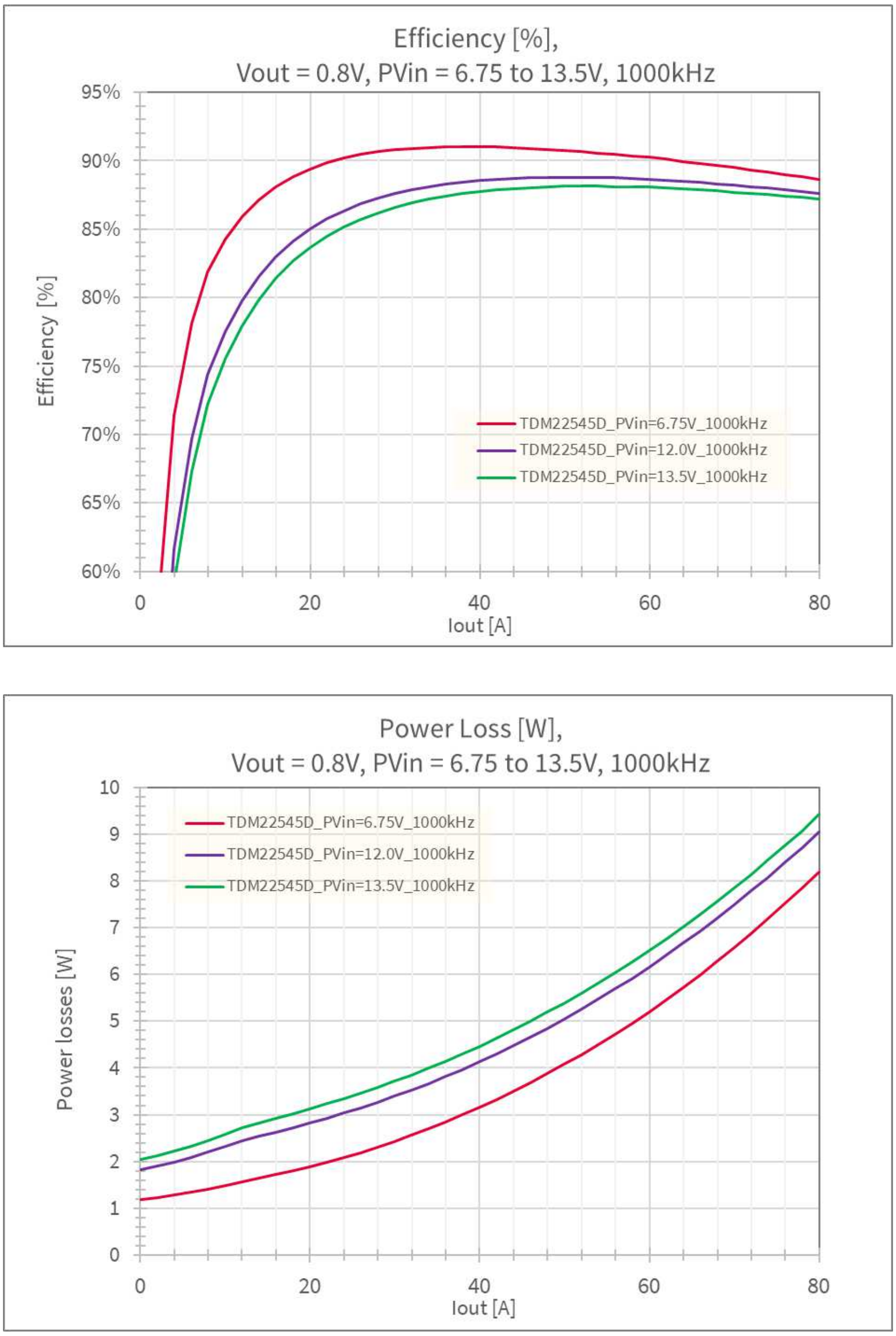


Figure 7 TDM22545D, PVin = 6.75V, 12.0V and 13.5V.

9 Vout Regulation

9.1 Fsw = 600kHz, Vout = 0.8V

PVin = 6.75V, 12.0V and 13.5V Io = 0A - 80A, fsw= 600 kHz, Room Temperature, No Air Flow.

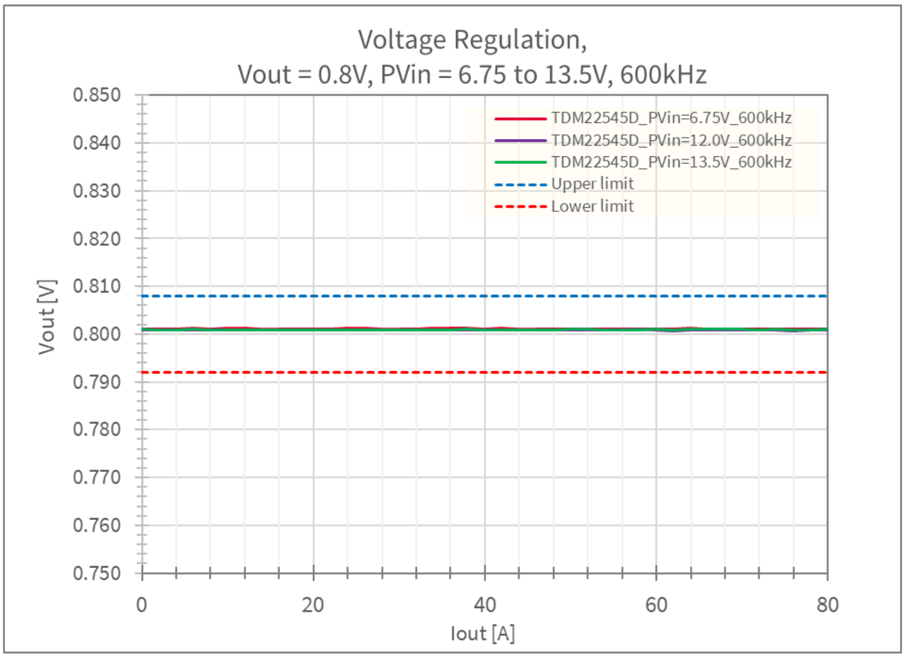


Figure 8 TDM22545D, PVin = 6.75V, 12.0V and 13.5V.

9.2 Fsw = 800kHz, Vout = 0.8V

PVin = 4.50V to 16.0V Io = 0 A - 80 A, fsw= 800 kHz, Room Temperature, No Air Flow.

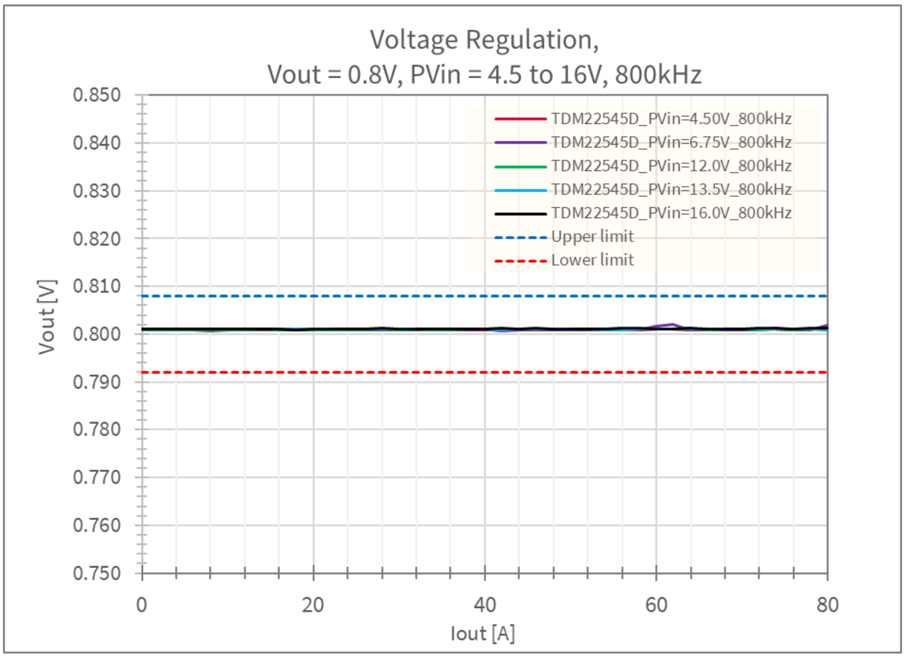


Figure 9 TDM22545D, PVin = 4.50V, 6.75V, 12.0V, 13.5V and 16.0V.

9.3 Fsw = 1000kHz, Vout = 0.8V

PVin = 6.75V, 12.0V and 13.5V Io = 0 A - 80 A, fsw= 1000 kHz, Room Temperature, No Air Flow.

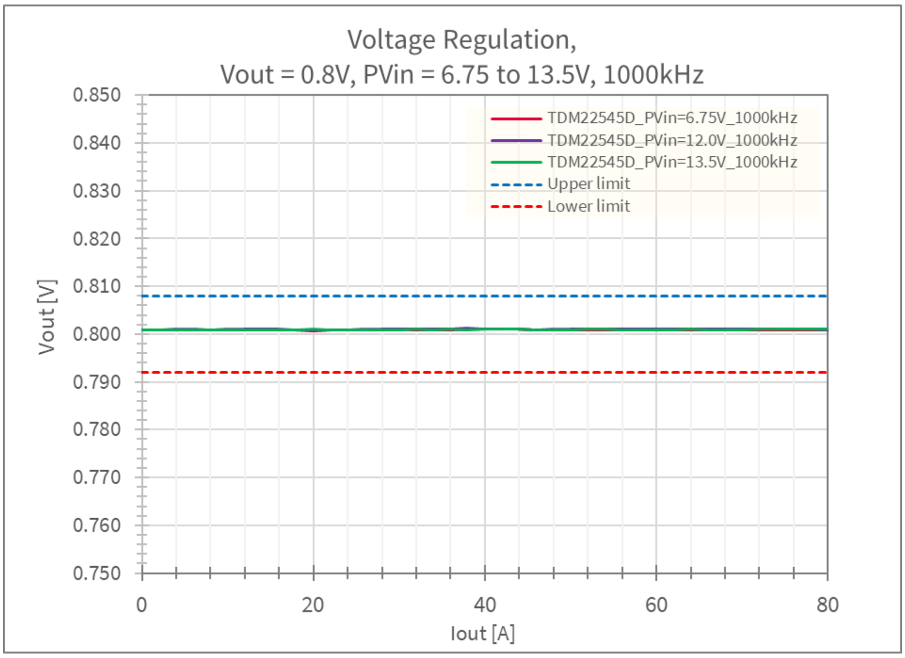


Figure 10 TDM22545D, PVin = 6.75V, 12.0V and 13.5V.

10 Thermal De-rating curves

Measurement is done on Evaluation board of EVAL_TDM22545D. PCB is an 8-layer board with 2.0-ounce Copper per layer (Top, Bottom, and inner layers), FR4 material, size 4.75”x4.95”.

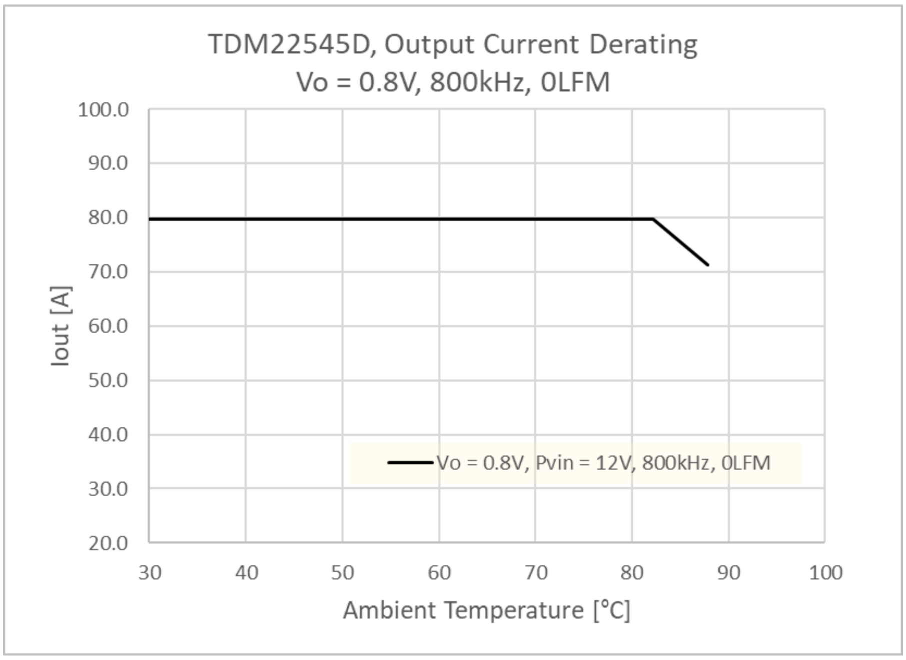


Figure 11 Thermal de-rating curves, 0 LFM. Heat sink: 3.56"L x 3.56"W x 1.14"H

11 Theory of operation

11.1 Description

The TDM22545D contains an improved high speed MOSFET driver optimized to drive a pair of co-packaged high-side and low-side OptiMOS MOSFETs at frequency up to 2 MHz. DC-DC controllers using traditional current sense methods like DCR sensing and Rdson sensing typically have limitations. DCR current sensing is sensitive to temperature changes of the inductor and needs temperature compensation either implemented externally using a thermo-couple or inside the power stage. RDSon current sensing, on the other hand, is not dependent on the inductor but there is a temperature co-efficient associated with the MOSFET RDSon. Besides, it is difficult to implement RDSon current sensing for high-side MOSFET which is therefore replaced by emulated current while the low-side current is sensed across the MOSFET. With the advanced current-mirror sensing in TDM22545D, all these limitations are eliminated while achieving superior accuracy. Current on both high-side as well as low-side MOSFET is mirrored on a sense MOSFET which is a part of the main MOSFET device, and hence comes with an inherent temperature compensation without the need for an additional circuitry. Real current-sensing on both MOSFET ensures that the system is always monitoring the real output current and can immediately react to any critical events like load step or over-current fault.

The TDM22545D reports accurate temperature with the gain of 8 mV / °C, which helps the system to actively monitor the temperature in real time. Temperature outputs from multiple power stages can be connected together to report the highest temperature to Infineon's digital PWM controller.

The TDM22545D PWM input is compatible with industry standard 3.3V PWM input with tri-state. The TDM22545D can enable Body-Braking mode by responding to PWM tri-state signals sent from the controller, quickly disabling both MOSFETs in the power stage in order to enhance transient performance or provide a high impedance output.

The TDM22545D supports diode emulation mode through the PWM tri-state signal. Controlled by Infineon's digital PWM controller, the PWM tri-state signal will force the low-side FET to be off when the inductor current is about to go negative. The light-load efficiency then can be increased by preventing conduction loss caused by negative inductor current.

The TDM22545D also supports deep-sleep power saving mode. When in deep-sleep mode, the driver will disable most of the function circuitry to greatly reduce power consumption.

The TDM22545D features a full-range of protection, including VCC/VDRV Under-Voltage-Lockout (UVLO), thermal shutdown against an internal over-temperature condition, phase fault detection of a shorted high-side MOSFET, and cycle-by-cycle over-current protection due to an overload condition or saturated output inductor.

The TDM22545D also features internal protection circuitry to automatically replenish the voltage across the bootstrap capacitor. It avoids the gradual depletion of capacitor energy when the power stage sits in tri-state for a long period of time.

11.2 Sleep Modes

When EN is pulled low, the power stage enters deep-sleep mode. The gate driver circuitry will be turned off immediately and most of the logic circuitry will be shut down to reduce the bias current to less than 32 µA. The IMON output will be shorted to IMONREF in deep sleep mode.

When EN toggles from low to high, the power stage will be active and able to accept PWM signals after a delay of 17 µs.

11.3 Current Sensing and Reporting

The TDM22545D features a very accurate current mirror architecture on both high-side as well as low-side MOSFET, thus reporting the real time current information. The current information is reported using the IMON pin. The reported current is in the form of current output with the gain of 5µA /A from the IMON pin. In order to convert this into voltage, a 1KΩ, 0.1% resistor is recommended at the IMON pin and placed close to the PWM controller. The other side of this resistor (not connected to the IMON pin of TDM22545D) can be optionally connected to the IMONREF pin but is not a requirement. A differential connection from the sense resistor connected at the IMON pin is connected to the PWM controller to report the power stage current information to the controller. The converted voltage signal at the controller side has an effective gain of 5mV/A i.e. for every 1 A load, the controller will read 5mV from the power stage. The current-output differential signal from the power stage provides excellent noise immunity to the reported current information.

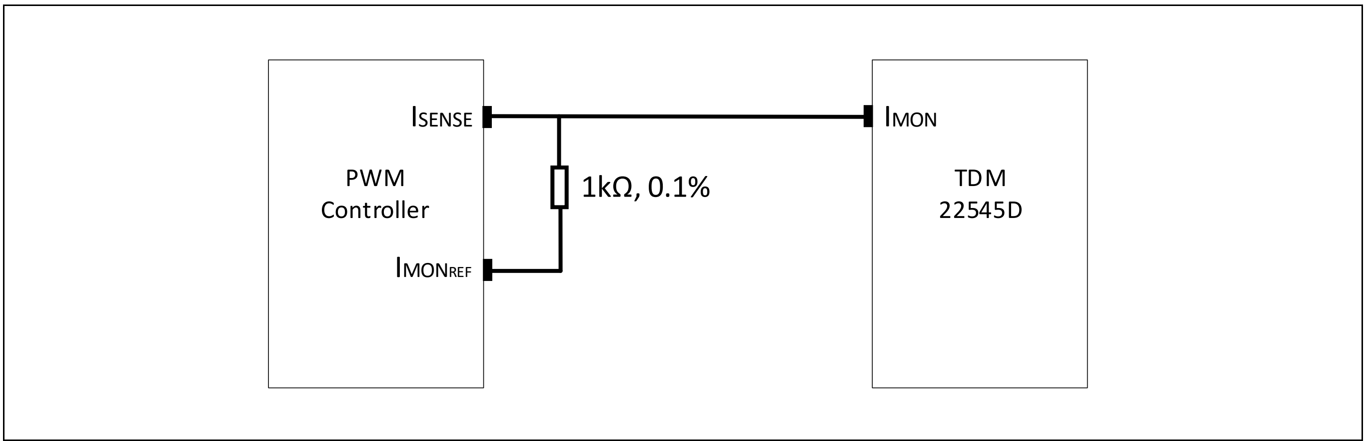


Figure 12 IMON connection to PWM Controller

11.4 Advanced Fault Reporting

TDM22545D uses TMON / FAULT pin for reporting all types of faults detected. Since typical multiphase applications connect the TMON / FAULT signal from all the phases in a particular loop into a wired OR connection, the system cannot distinguish the faulty phase and the type of fault occurred. This is resolved by using advanced fault reporting in TDM22545D which uses a combination of TMON / FAULT and IMON signals to identify the fault. Since the IMON is separately connected from each phase to the controller, it provides phase-specific information in the event of a fault. Appropriate IMON response to each fault is explained in the corresponding fault sub-sections further. A summary of fault reporting and fault reporting timing diagram is given in the Table 11 at the end of Section 12.

11.5 VDRV Undervoltage Lock-out (UVLO)

TDM22545D features a VDRV under voltage lock-out fault circuitry that monitors the VDRV voltage actively. As shown in Figure 13, this is a non-catastrophic fault, and the TMON/FAULT pin is pulled low with a weak pull down as long as the VDRV voltage is below the UVLO threshold. If the power stage has not started up, the power stage PWM pin is also pulled down to 0V with a weak pull down. This can be monitored by the PWM controller as a signal from the power stage indicating that it is not ready yet for power up. As soon as VDRV voltage is above the UVLO threshold, the PWM pin is at tri state instead of 0V, this indicating the controller that it is OK to send the PWM signals. At the same time, TDM22545D shorts IMON and IMONREF thus identifying itself to the controller that it is in UVLO condition.

Once the powerstage is in normal operation, if then it encounters a VDRV UVLO condition, the power stage stops switching, and both TMON and IMON pins are pulled down to 0V. If there are multiple phases connected in the same loop, the TMON pin voltage, being connected to other power stage TMON pins, will continue reporting the highest power stage temperature. But the controller can still detect IMON pin voltage to be 0V (IMON –IMONREF = -IMONREF, as seen by the controller), and thus identify this faulty phase. Since TMON pin is not pulled high, but continues reporting the temperature, this can be distinguished from a BOOT UVLO condition as shown in Figure 13.

11.6 Temperature Reporting and Over-temperature protection

An internal temperature-sense circuit monitors the temperature of the TDM22545D. The sensed temperature is reported at the TMON/FAULT pin with a linear voltage slope of 8mV/°C and a 0.6V offset at 0°C, as shown in equation (1).

$$V_{TMON/FAULT}(V) = 0.6V + 0.008V/°C x T_j(°C) \quad (1)$$

The TMON/FAULT pin also serves as a FAULT pin that is pulled to 3.3V in case of any catastrophic faults and is pulled down to 0V in case of any non-catastrophic faults. When there is no fault, it continues reporting temperature as long as the VCC supply is connected to a voltage in the recommended operating range. For a junction temperature below -25C, the TMON voltage is clamped to 0.4V to avoid false triggering of VDRV under-voltage.
Once the temperature rises above the OTP rising threshold (140 °C), the TMON/FAULT output will be pulled high immediately and the driver turns off the high side and low side MOSFETs. TDM22545D stops responding to the PWM from controller and stops switching. The TMON/FAULT will remain high until temperature falls below the falling threshold (128 °C). As soon as TMON is pulled high during OTP, controller drives the PWM to tri-state. After PWM tri-state, IMON is internally shorted to 0.8V, thus identifying the faulty phase and occurrence of OTP to the system. The system can then respond accordingly.

11.7 Over Current Protection and Flag

This feature protects the power stage from self-destruction from repetitive high current events such as saturated inductors due to poor component selection or by incorrectly optimized control loops. These high current events could eventually lead to a shorted high-side MOSFET failure.

With cycle-by-cycle self-preservation, the current is monitored every cycle. If the over-current threshold (default 120 A) has been exceeded, the PWM high pulse will be truncated so that the inductor current is allowed to relax. When TDM22545D detects 10 consecutive PWM cycle over-current events without 3 consecutive good events(no over-current), the TMON/FAULT pin is flagged high to indicate the controller of the fault. As soon as TMON is pulled high during OCP, controller drives the PWM to tri-state. After PWM tri-state, IMON is internally shorted to 2.2V, thus identifying the faulty phase.

11.8 Bootstrap Capacitor Under-Voltage

TDM22545D features a bootstrap capacitor under voltage circuitry that detects a missing bootstrap capacitor before powering up or a damaged bootstrap capacitor during normal operation. When TDM22545D detects 10 consecutive PWM cycles of bootstrap capacitor under voltage, the TMON/FAULT pin will be pulled high to report a catastrophic fault to the PWM controller. As soon as TMON is pulled high during OCP, controller drives the PWM to tri-state. After PWM tri-state, IMON is internally shorted to 0V, thus identifying the faulty phase. Counter is reset after three consecutive PWM cycles without bootstrap under voltage condition.

11.9 High Side Short (HSS) Protection

TDM22545D features a High-Side short detection circuitry that detects a high side MOSFET short condition. As soon as the TDM22545D detects the HSS fault, TMON/FAULT pin and IMON pin will be pulled high to report a catastrophic high-side short fault to the controller. The power stage continues responding to the PWM from controller. As a response to the HSS fault, the controller may decide to issue a PWM low signal so that the low side FET also turns on to self-destruct the powerstage.

Table 11 Advanced Fault Reporting and Identification

Fault Severity Level	Type of Fault	Power stage PWM Response	Power stage IMON Response	Powerstage TMON Response
Non-Catastrophic	VDRV UVLO (power-up)	Weak pull down to 0V (PWM pin voltage can be driven by controller, no switching on powerstage)	= 0V	Weak pull down to 0V (or V_{TMON} from other power stages in same loop)
	VDRV UVLO (normal operation)	Weak pull down to 0V (PWM pin voltage can be driven by controller, no switching on powerstage)	= 0V	Weak pull down to 0V (or V_{TMON} from other power stages in same loop)
Catastrophic	OTP	Power stage stops responding to PWM pulse (latched)	= 0.8V (Latched – after PWM tri-state)	= 3.3V (Latched) (Temperature reporting after PWM tri-state)
	OCP (10 events without 3 consecutive good cycles)	Power stage stops responding to PWM pulses(latched)	=2.2V (Latched - after PWM tri-state)	= 3.3V (Latched) (Temperature reporting after PWM tri-state)
	HSS	Power stage continues responding to PWM signal from controller.	= 3.3V (Latched)	= 3.3V (Latched)
	BOOT UVLO (10 events without 3 consecutive good cycles)	Power stage stops responding to PWM pulses (Latched)	= 0V (Latched - after PWM tri-state)	= 3.3V (Latched) (Temperature reporting after PWM tri-state)

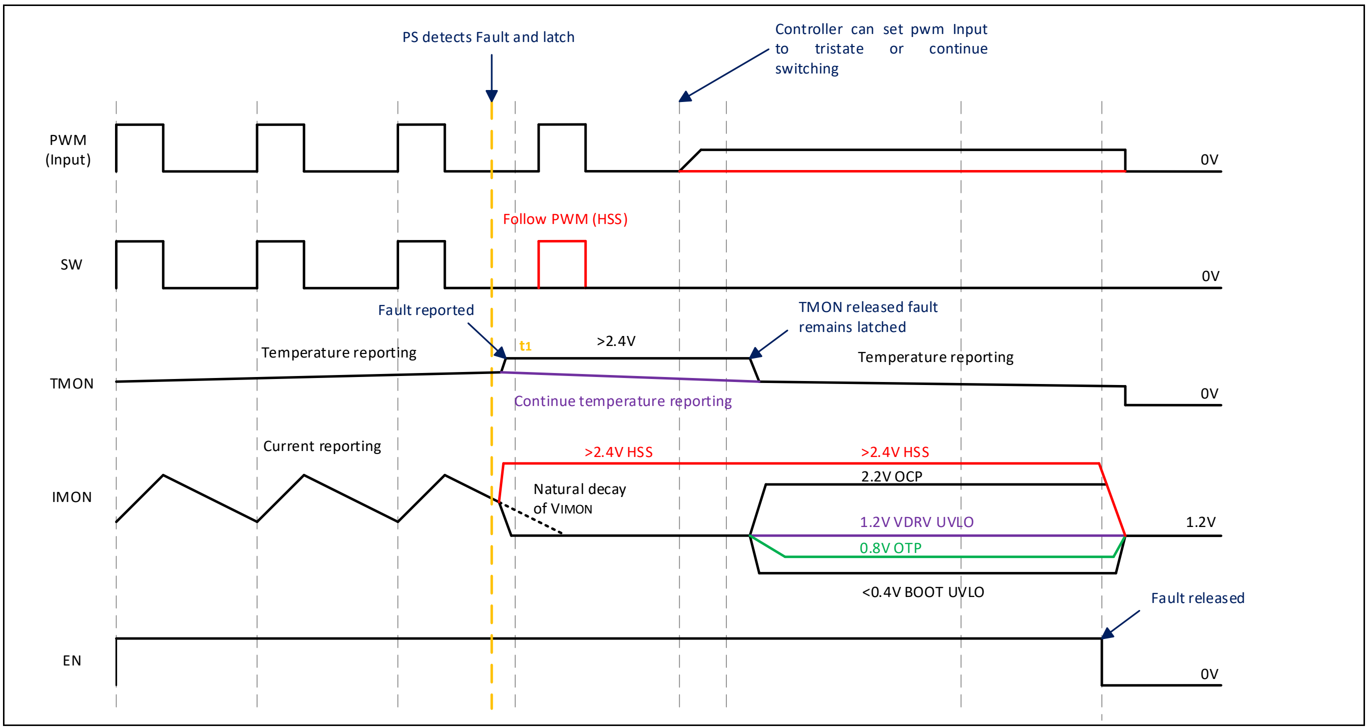


Figure 13 **Advanced Fault Reporting Timing Diagram**

12 Typical application diagram

12.1 Block Diagram for Dual Phase 120A Power Stage Module

PVin = 12.0 V, Vo = 0.8 V, Io = 0A – 80A, fsw = 800 kHz.

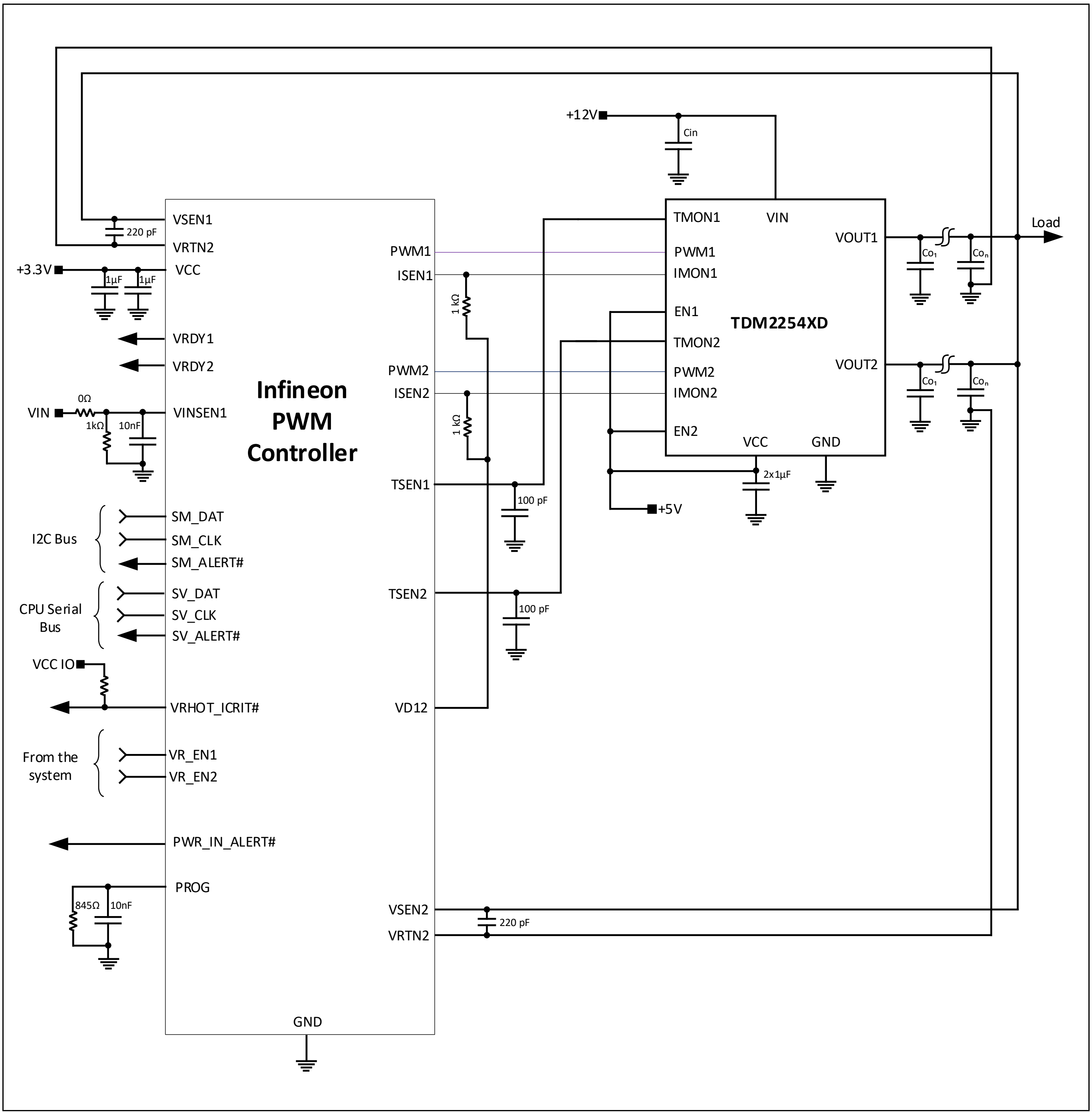


Figure 14 120A Dual Phase Power Stage Module typical application

12.2 Typical Operating Waveforms

Dual Phase Power Module Evaluation Board. PVin = 12.0 V, Vo = 0.8 V, Io = 0 – 80 A, fsw = 800 kHz, Room Temperature, no airflow

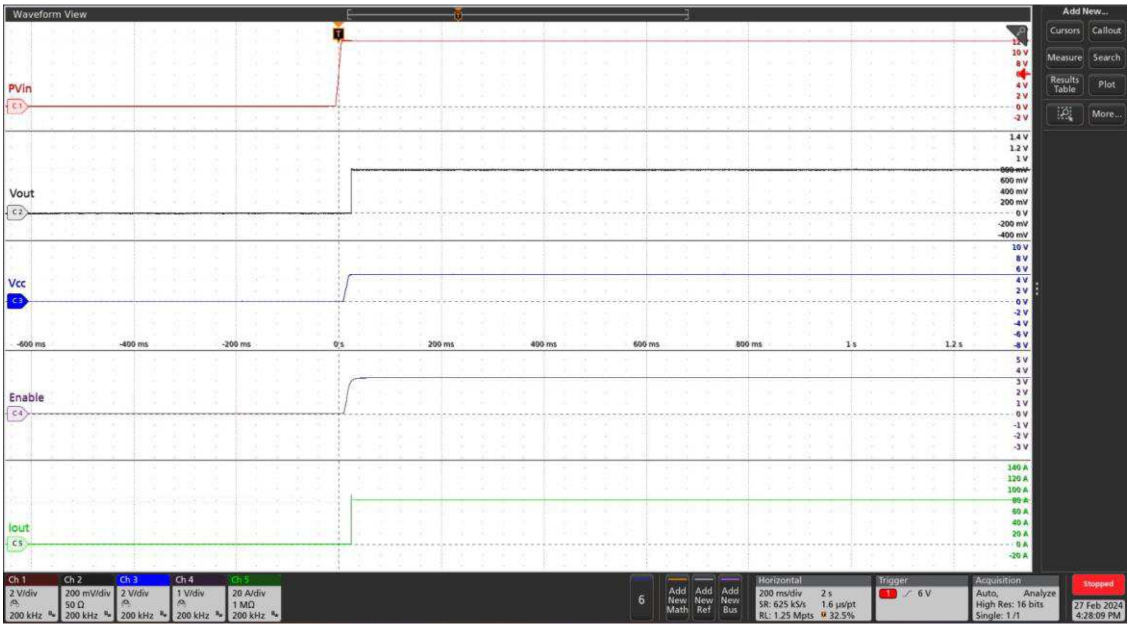


Figure 15 Start up at 80 A Load, (Ch1: PVin, Ch2: Vou, Ch3:Vcc ,Ch4:En, Ch5:Iout)

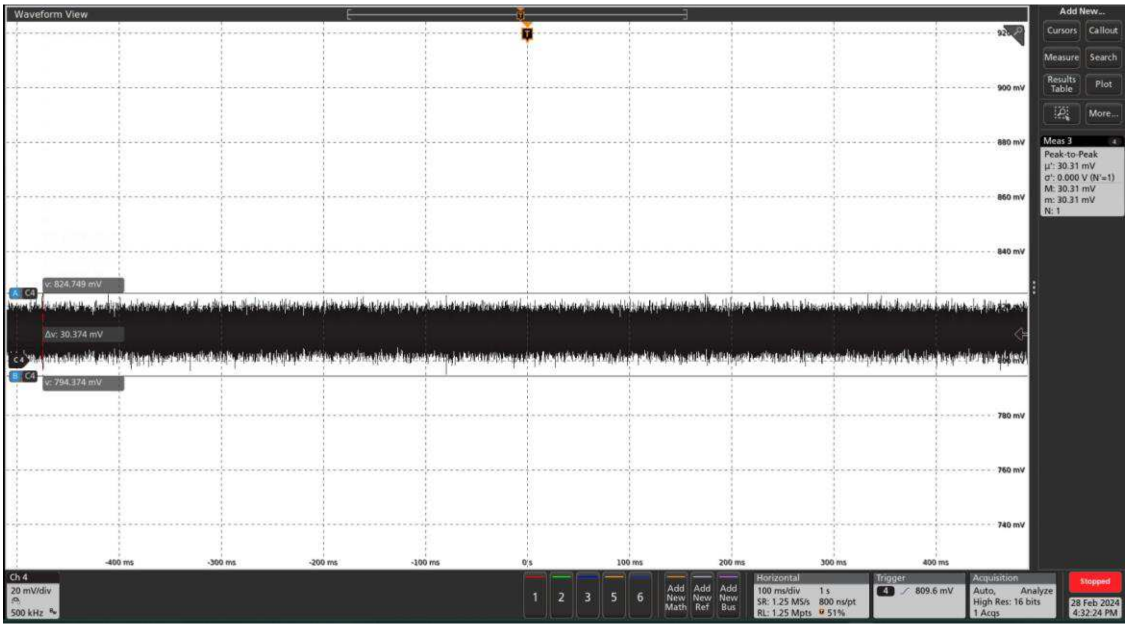


Figure 16 Vo ripple at 80 A Load, fsw = 800 kHz, (Ch4: Vo). Cout=6x10µF, 2x22µF, 1x470µF per Phase.

12.1 Block Diagram for Power Stage Module in 12+0 Phase Configuration

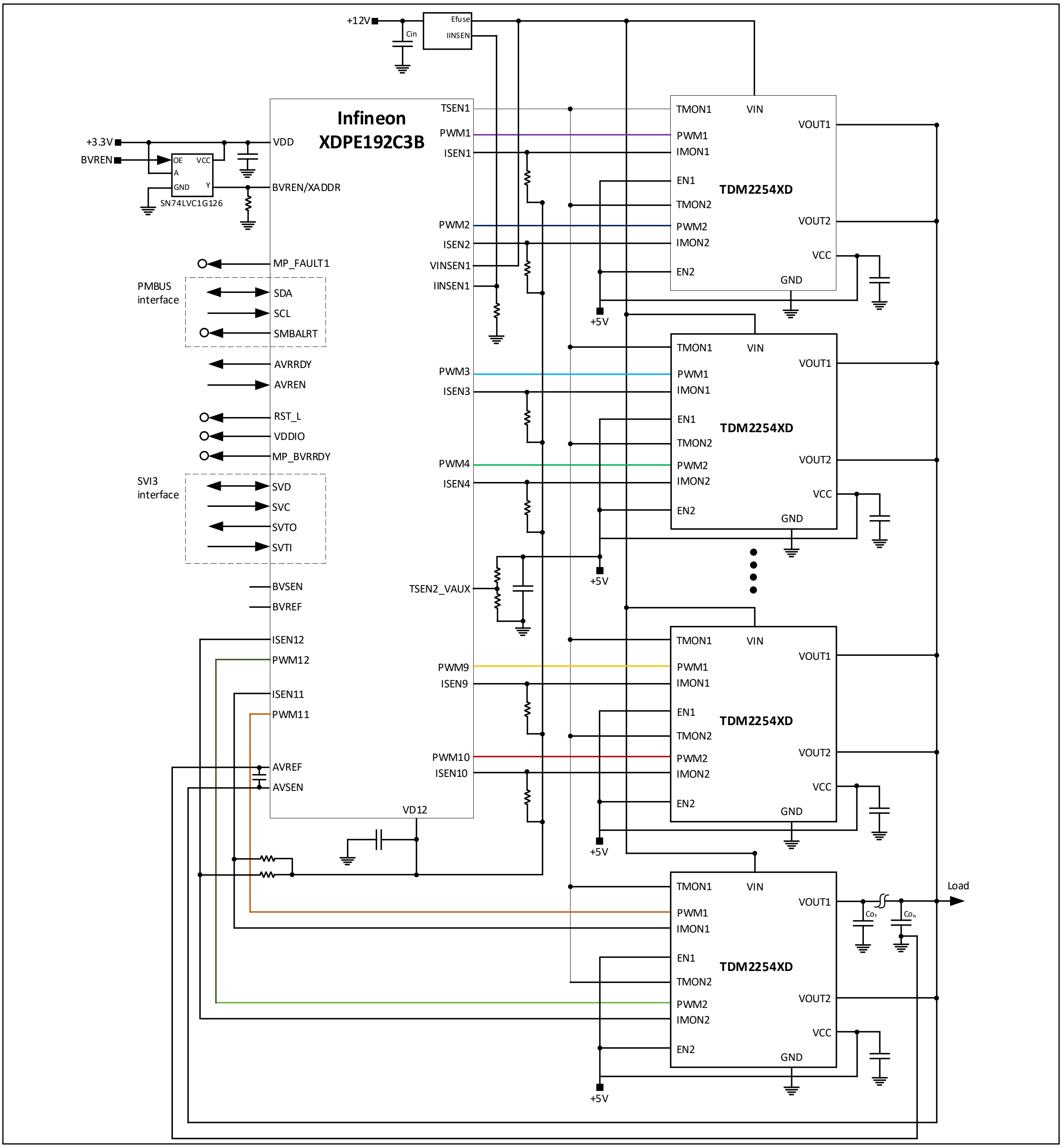


Figure 17 Single Loop VR using XDPE192C3B and TDM22545D Power Stage Module in 12+0 phase configuration

13 Layout Recommendations

In Progress.

Following figures illustrate the PCB layout design of the TDM2254XD Dual Phase 120A Power Stage Module Evaluation Board, FR4 material, 8 layers, 4.75 x 4.95in.

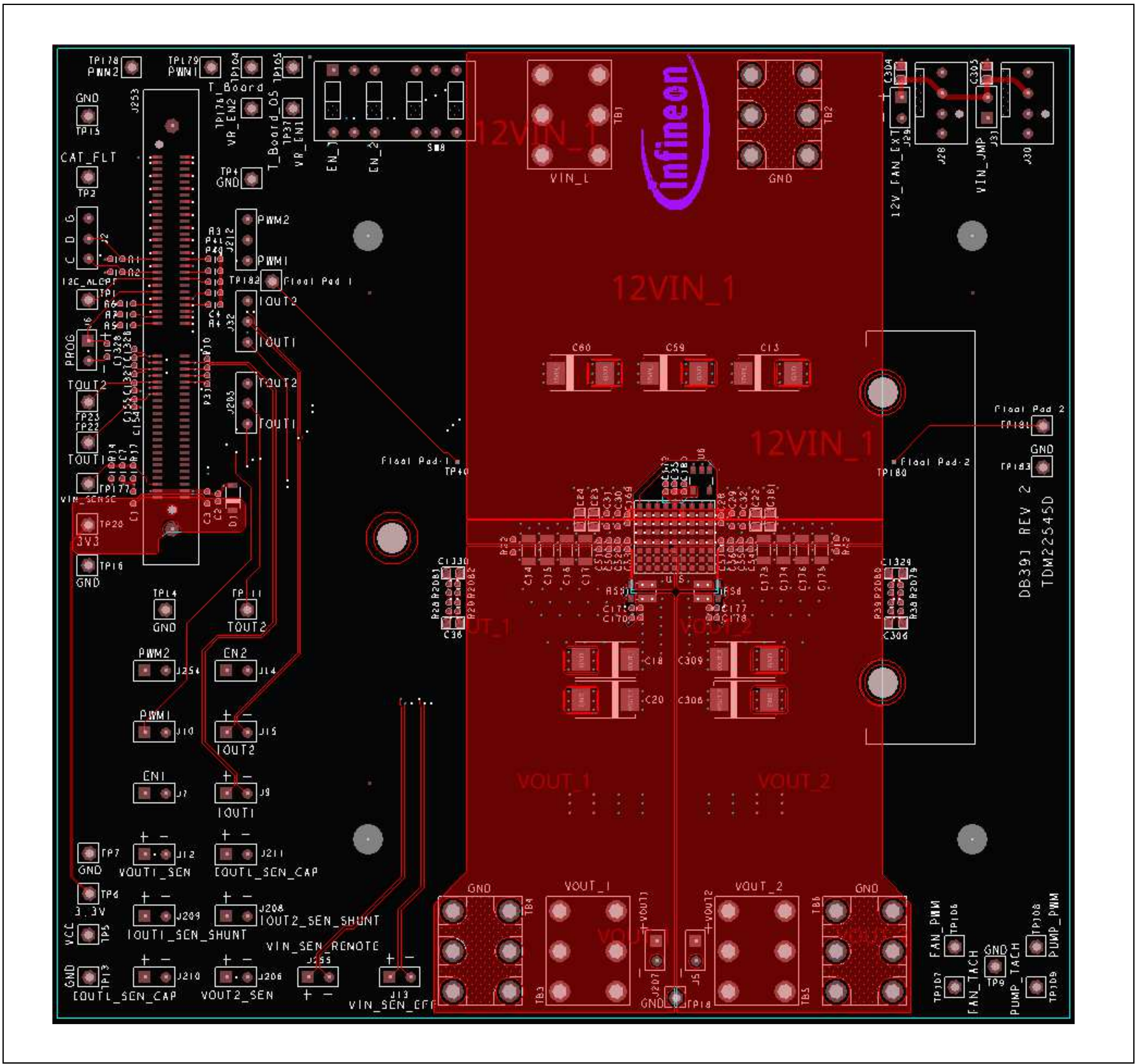


Figure 18 TDM2254XD Demo Board – Top Layer (Layer 1)

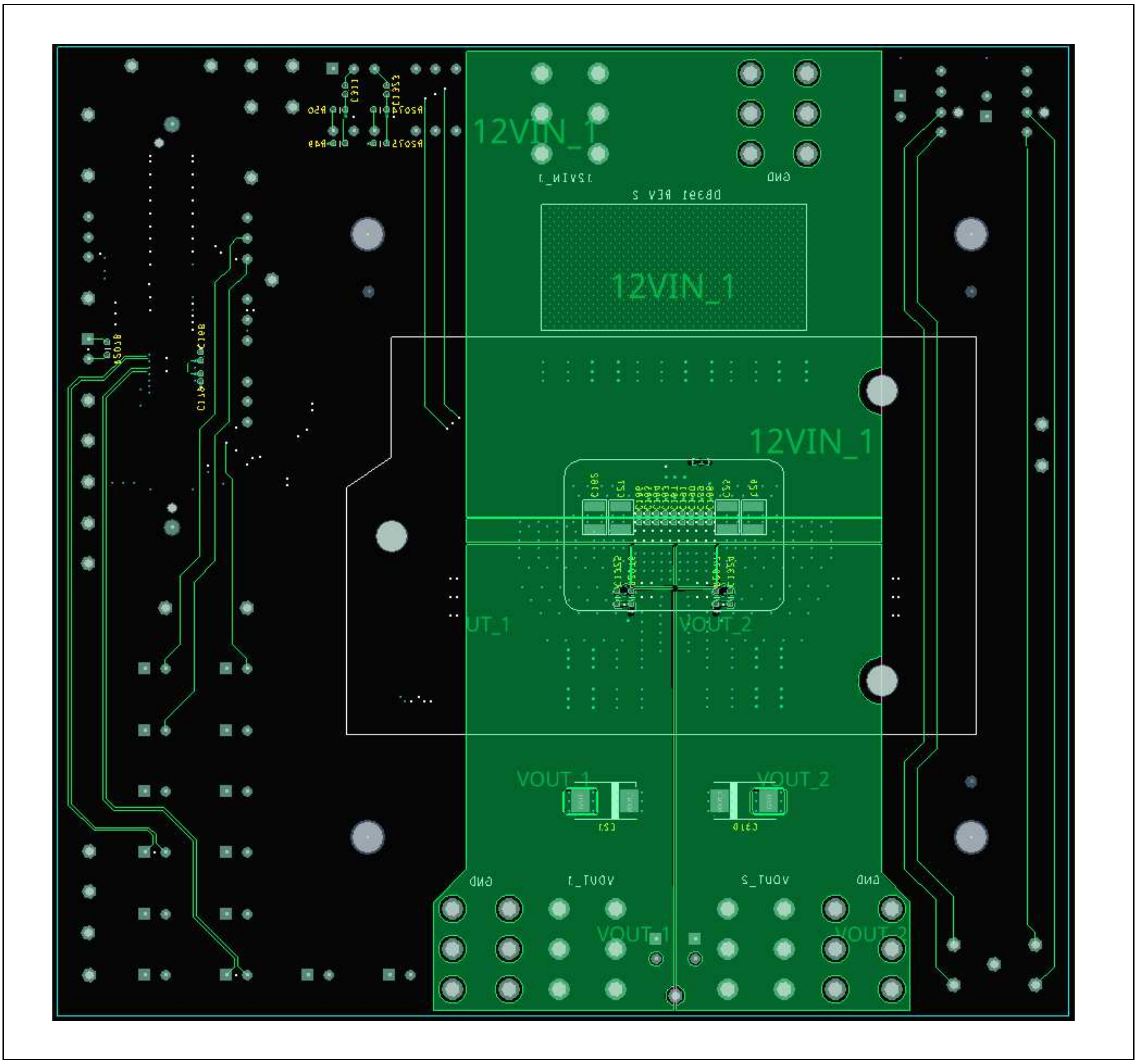


Figure 19 **TDM2254XD Demo Board – Bottom (Layer 8)**

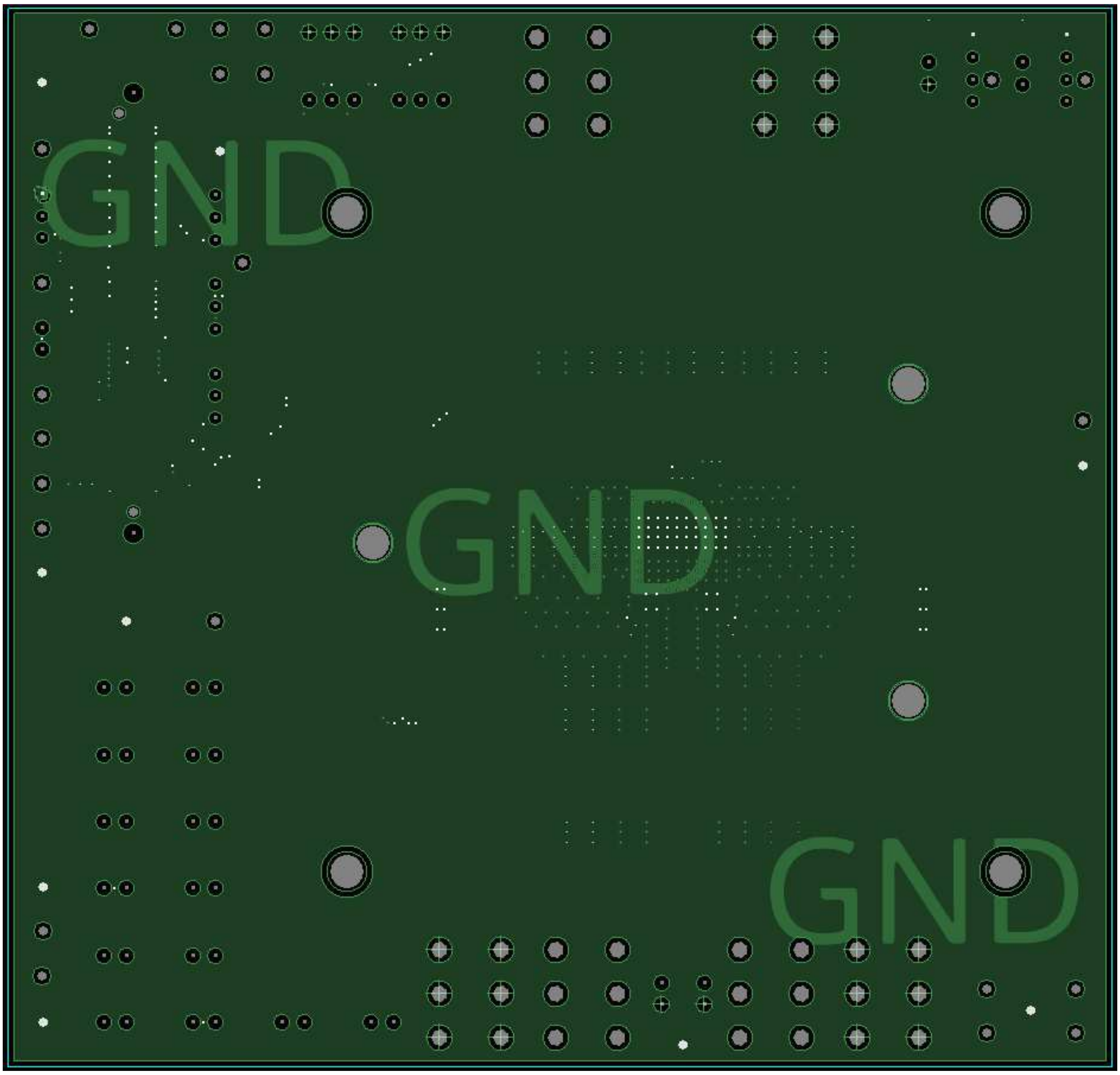


Figure 20 TDM2254XD Demo Board – Ground 1 (Layer 2)

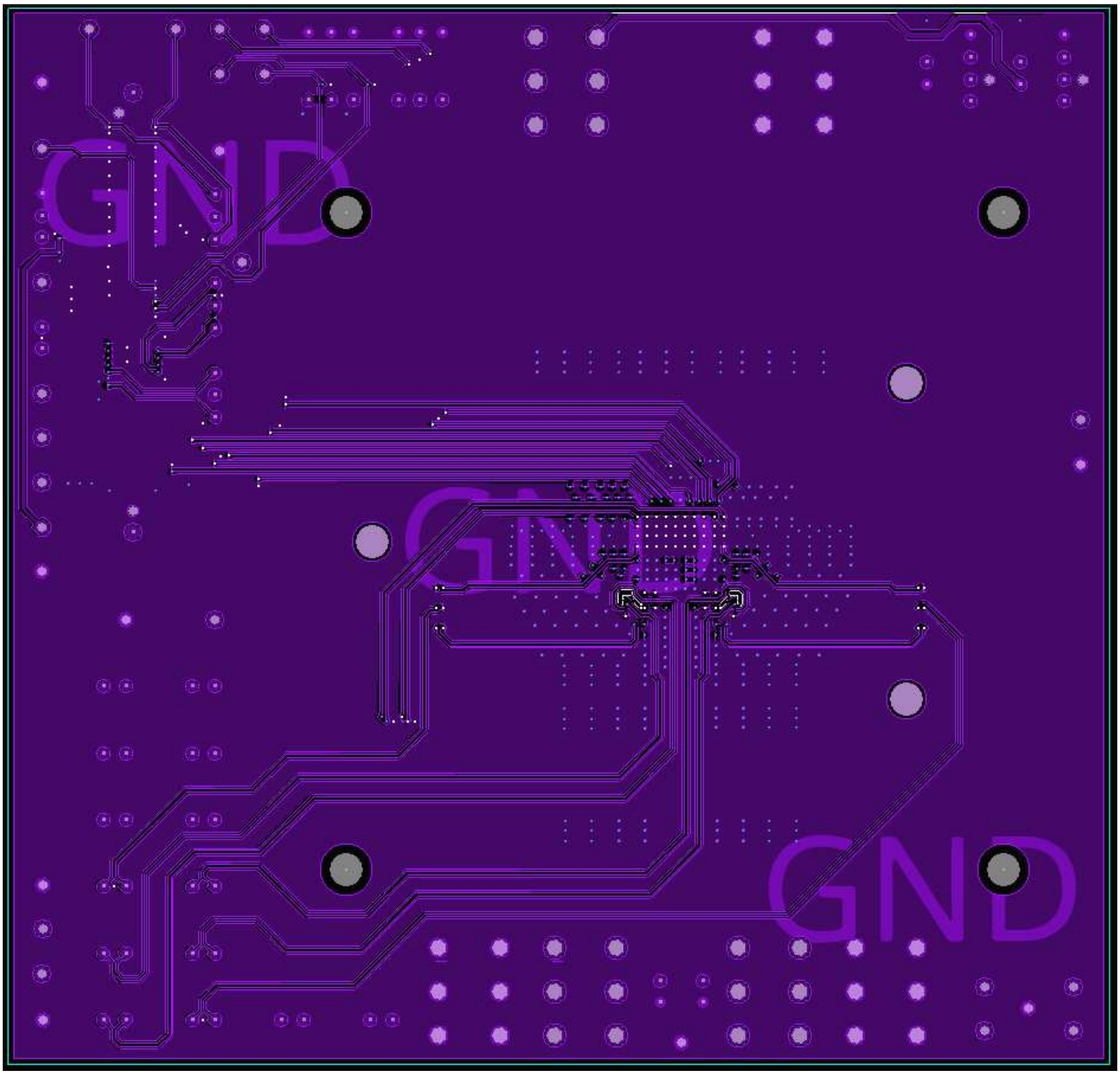


Figure 21 TDM2254XD Demo Board – Signal 1 (Layer 3)

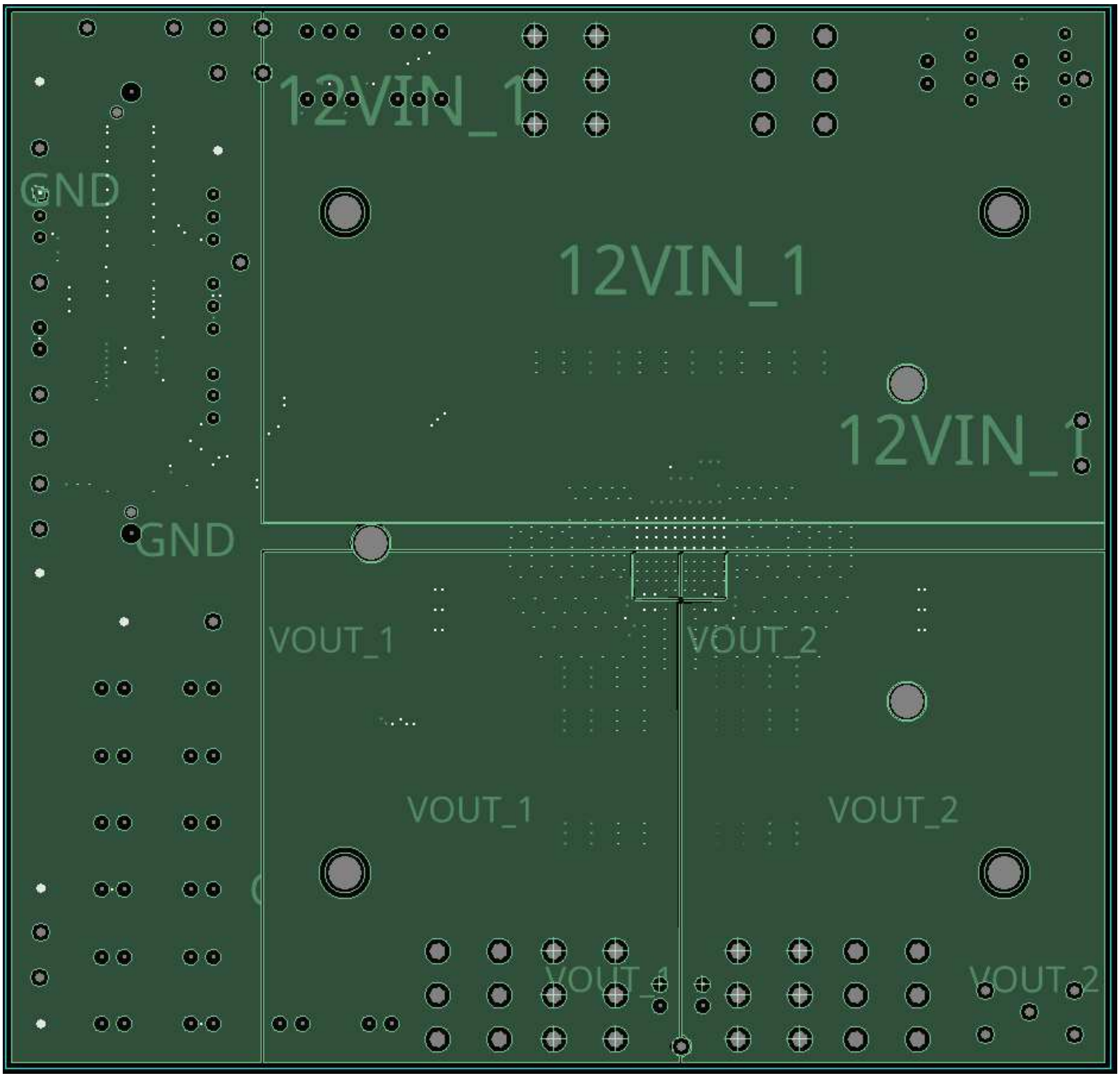


Figure 22 TDM2254XD Demo Board – Power 1 (Layer 4)

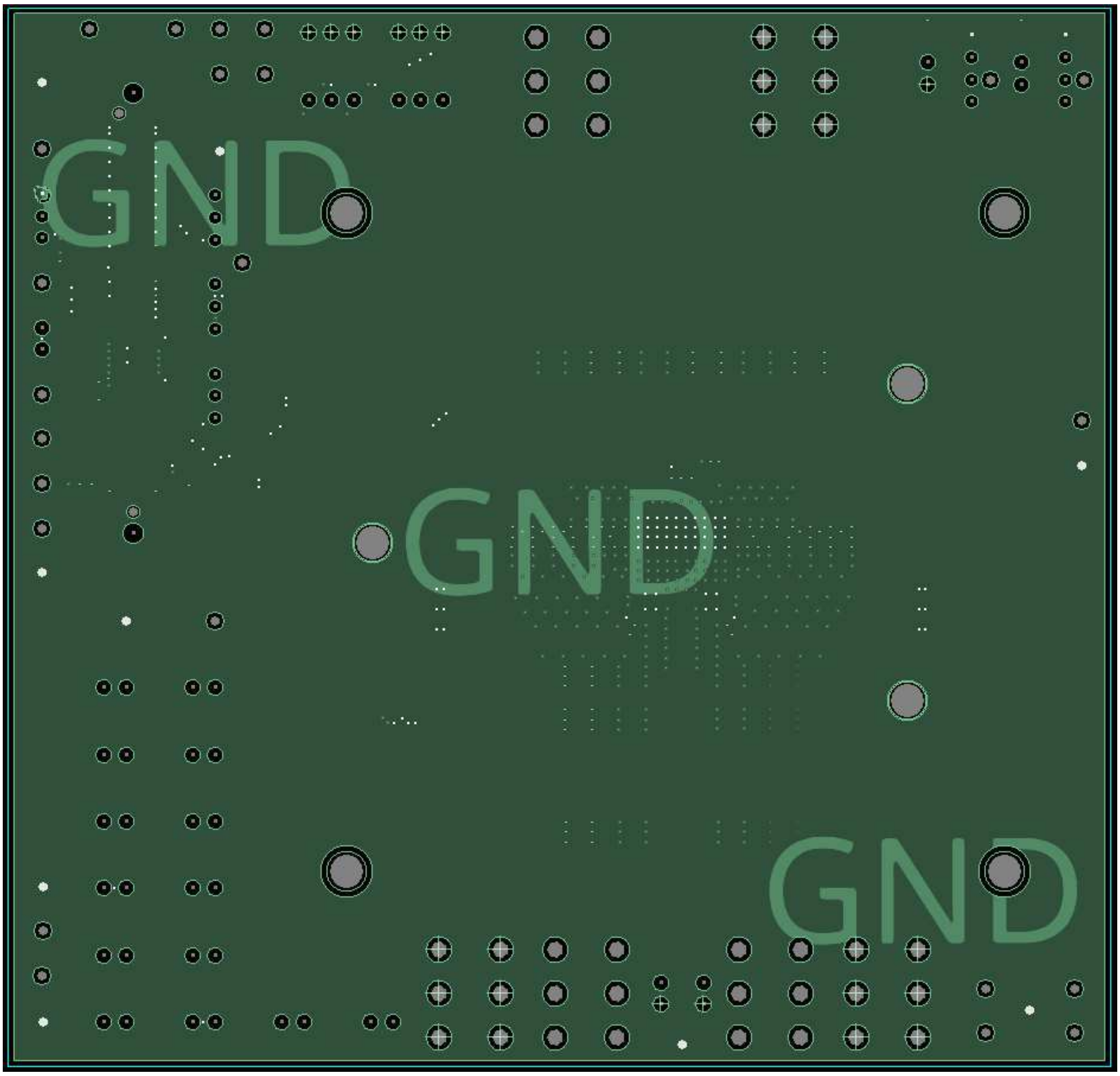


Figure 23 **TDM2254XD Demo Board – Power 2 (Layer 5)**

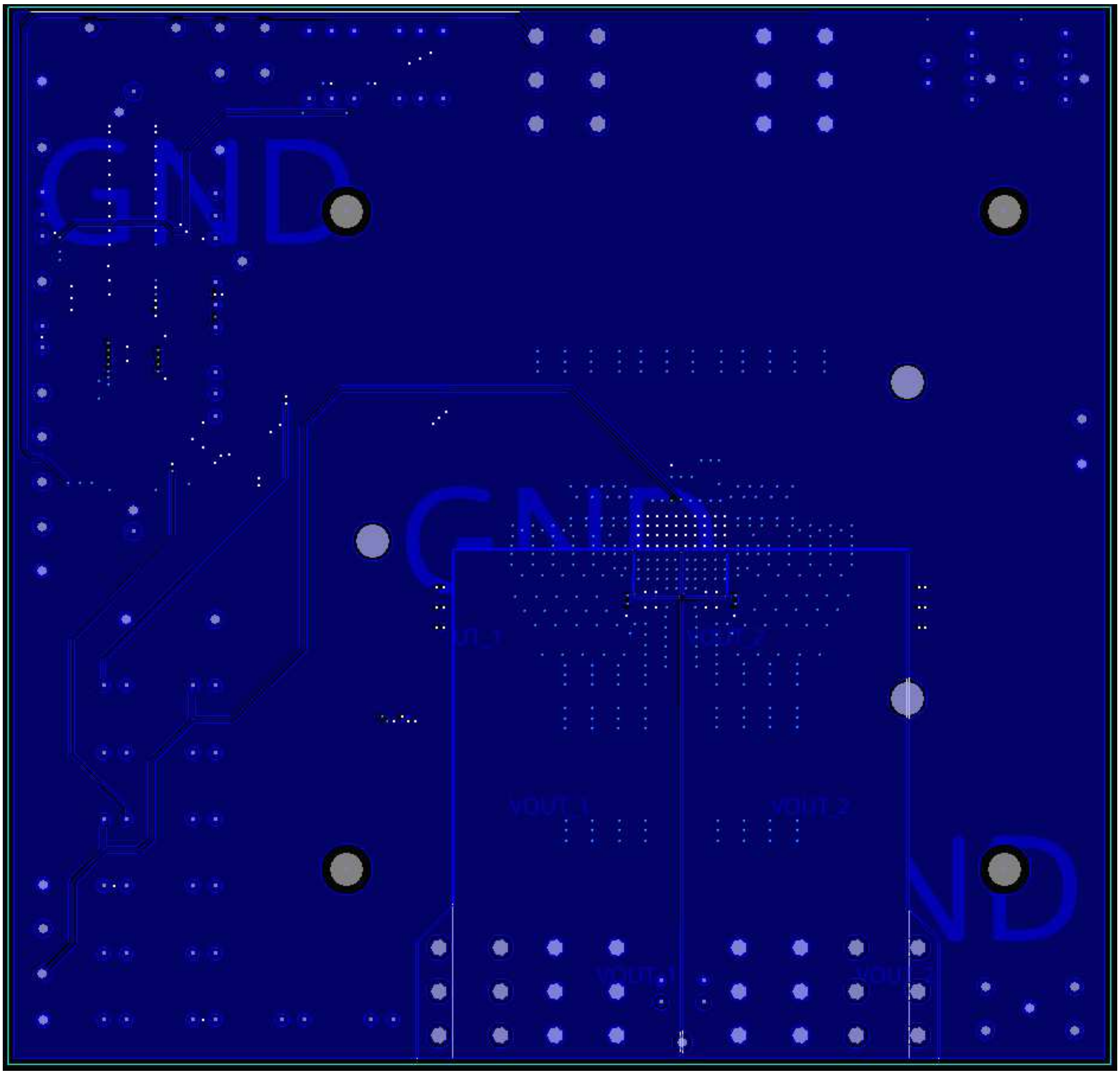


Figure 24 TDM2254XD Demo Board –Signal 2 (Layer 6)

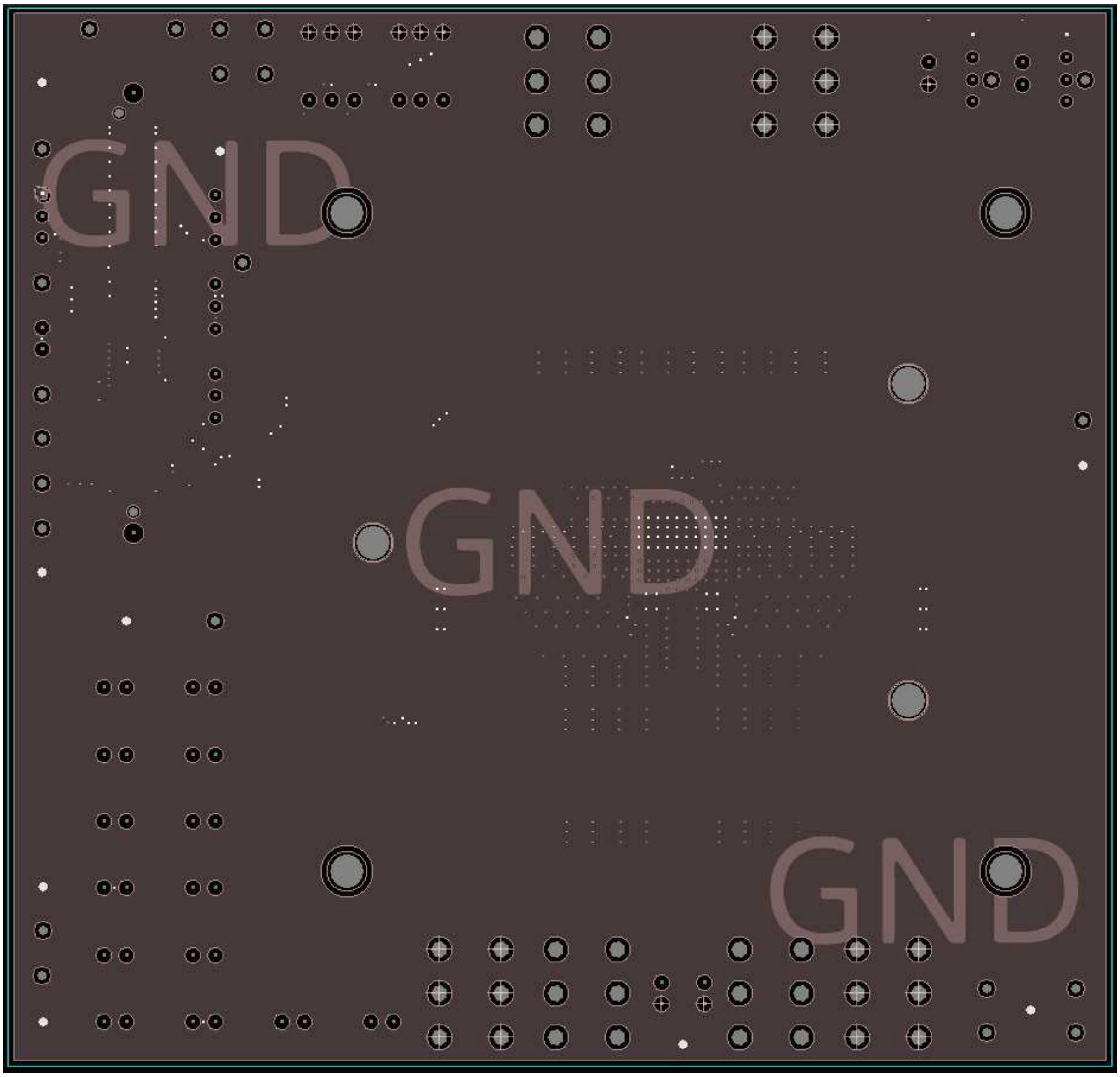


Figure 25 **TDM2254XD Demo Board – Ground 2 (Layer 7)**

14 Solder Mask

Figure 26 Solder mask (all dimensions in mm)

15 Stencil Design

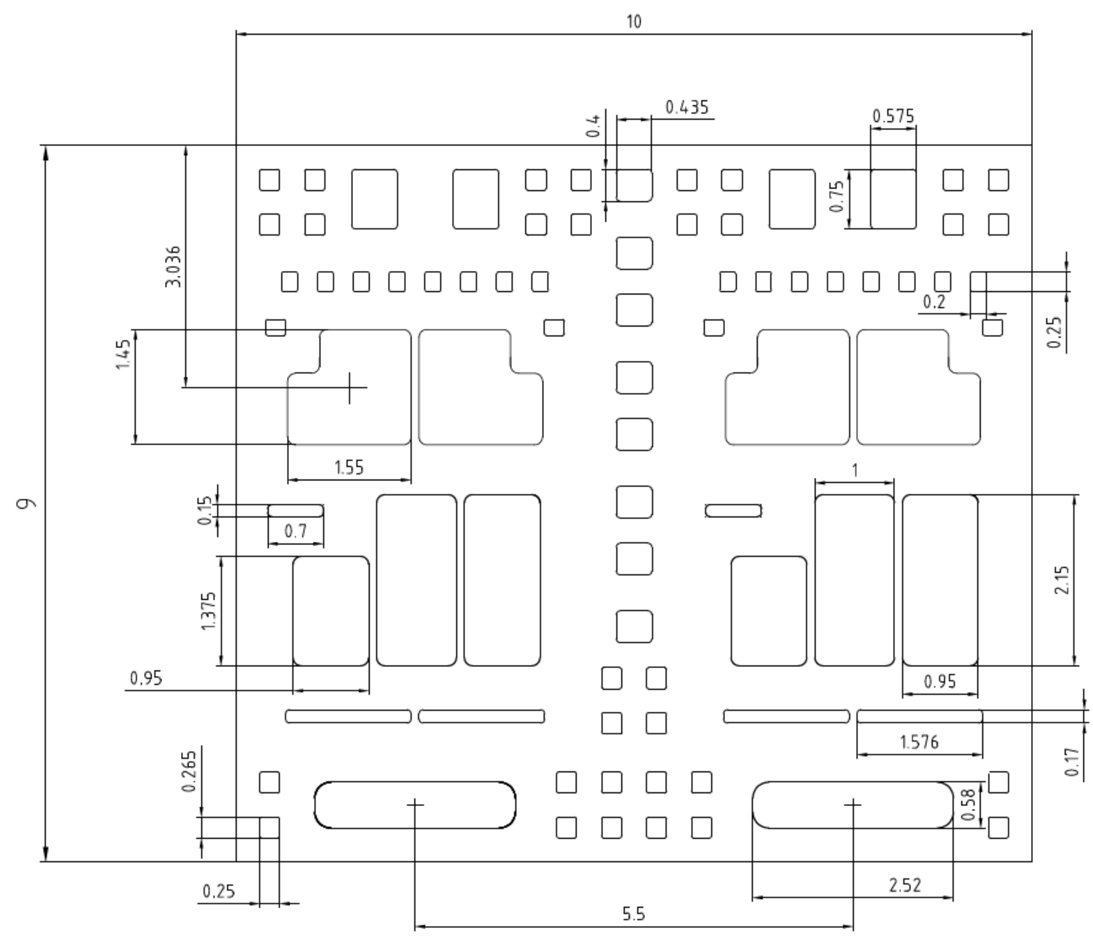


Figure 27 Stencil pad size and spacing (all dimensions in mm)

16 Package

This section includes marking, mechanical and packaging information for TDM22545D.

16.1 Marking Information

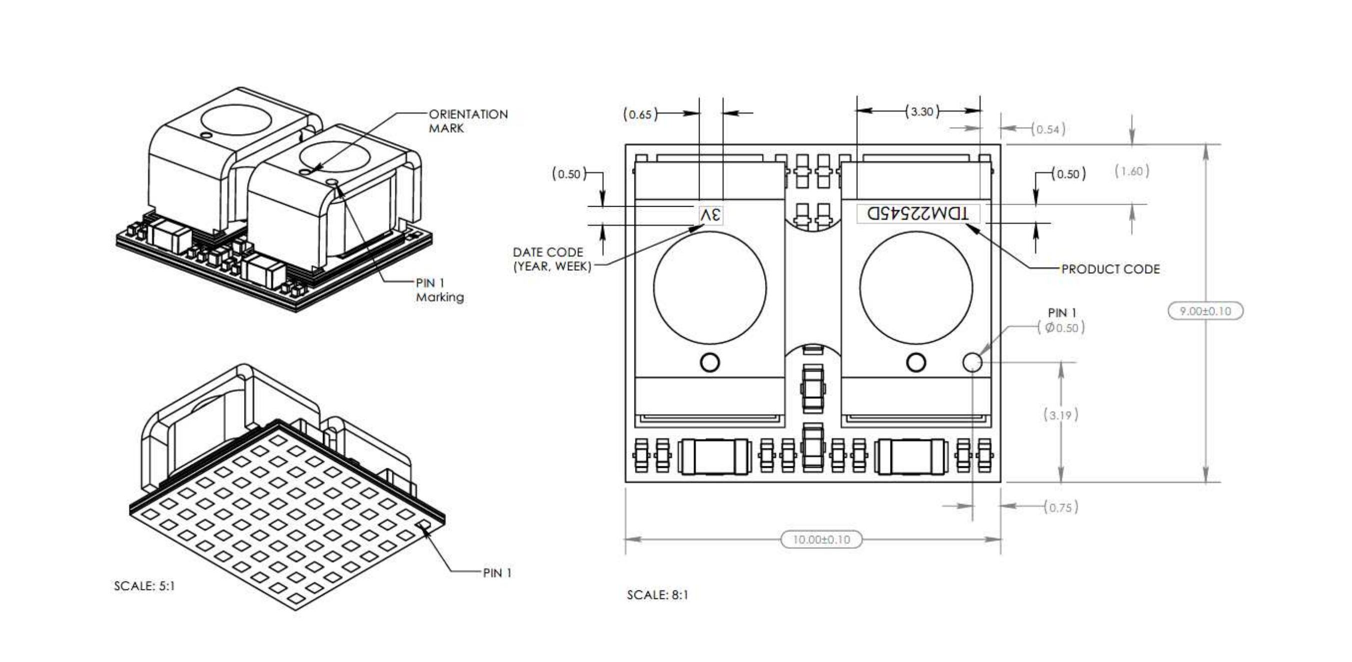


Figure 28 Package Marking

16.2 Dimensions

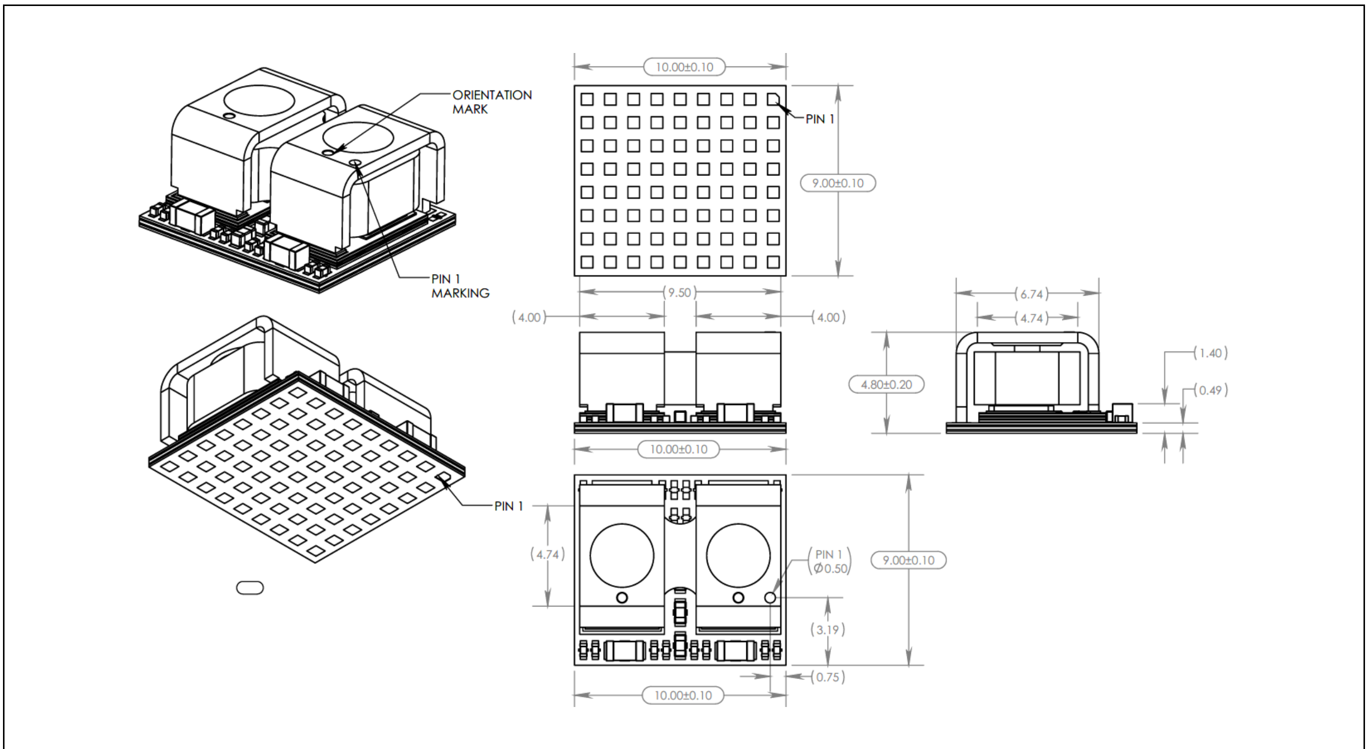


Figure 29 Package Dimensions (all dimensions in mm)

16.3 Tape and Reel Information

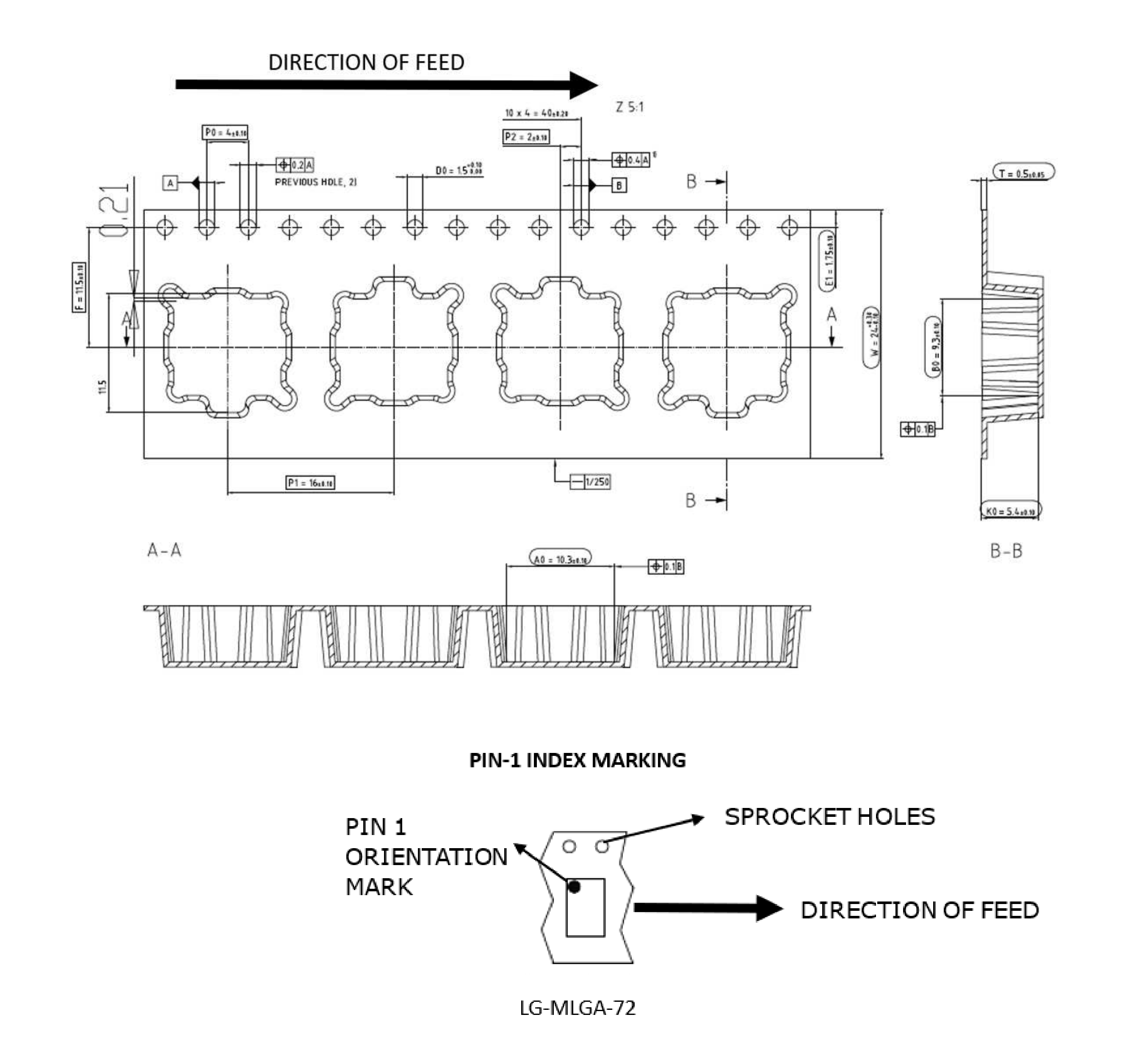


Figure 30 Tape and reel details

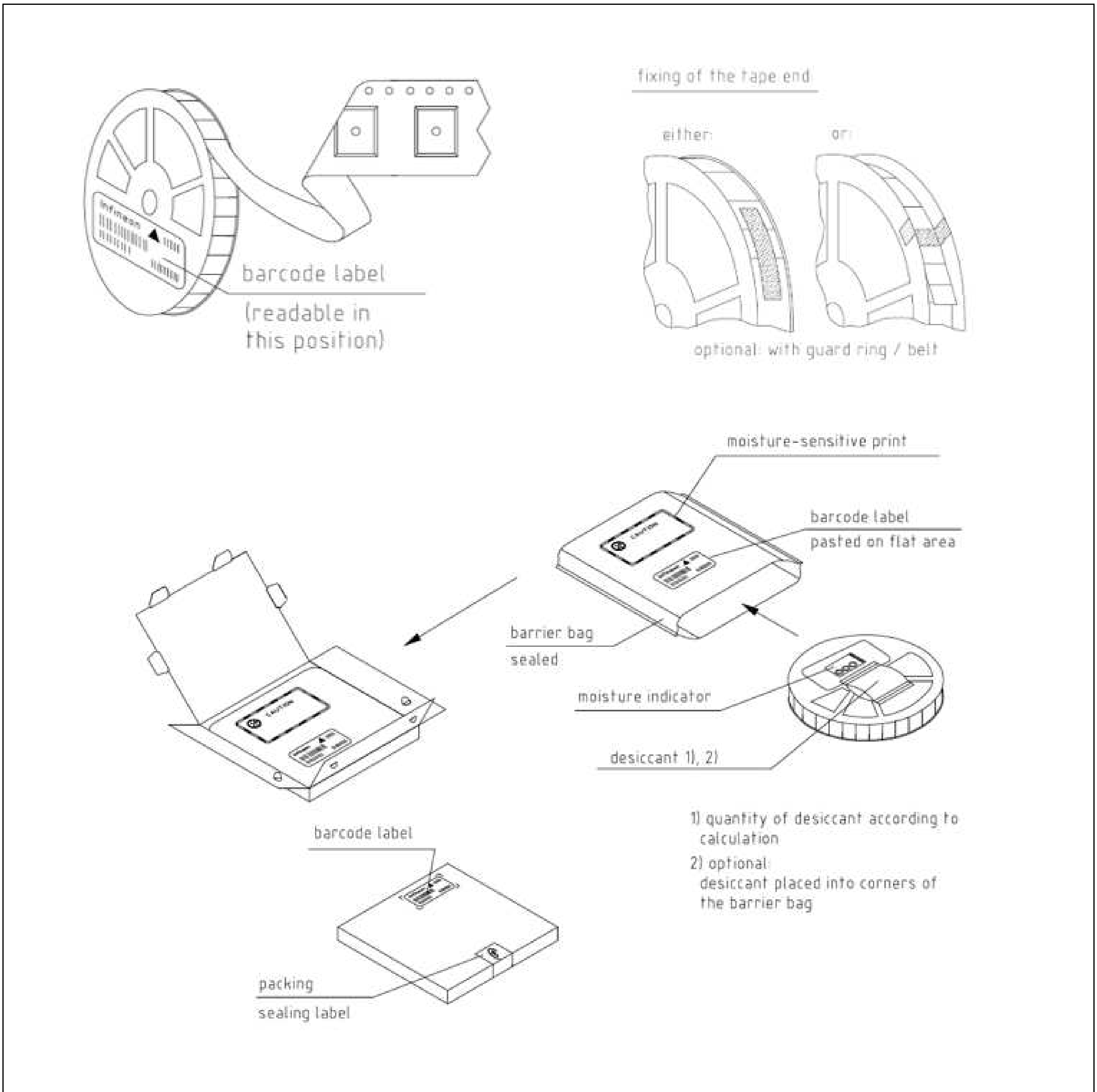


Figure 31 Tape and reel packaging

Table 12 TDM22545D LGA72 - Packaging information

Material	Surface Resistance	Reel Diameter (mm)	Reel Width (mm)	Reel Capacity	Reel Weight	Tape Width (mm)	Pocket Pitch (mm)	Pocket Depth (mm)
ANTISTATIC POLYSTYRENE (PS)	$10^2 \leq R < 10^{11}\ \Omega$	330	24	500	1260g/FULL REEL	24	16	5.4

17 Environmental Qualifications

Qualification Level		**Industrial**	
Moisture Sensitivity		9x10x5mm LG-MLGA-72-1 Package	JEDEC Level 3 @ 260 °C
ESD	[HBM] Human Body Model	ANSI/ESDA/JEDEC JS-001, Class 2 (2000V to <4000V)	
	[CDM] Charged Device Model	ANSI/ESDA/JEDEC JS-002, Class C3 (≥1000)	
RoHS Compliant		Yes	

18 Evaluation Boards and Support Documentation

Table 13 TD2254XD Evaluation Boards and User Guides

Evaluation board	Specifications	Website Address
EVAL_TDM2254XD_0.8Vout	12 V±10%, 0.8 V, 120 A	---

Table 14 TD22545D Package Information

Device	Package Type	Website Address
TDM22545D	LG-MLGA-72-1 Package, 9x10x5mm	---

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Document reference

Revision History

TDM22545D

Revision: 2024-03-21, Rev. 1.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2023-03-20	Release of preliminary version
1.1	2024-03-21	DS format, data and parameters updated.

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