SmartLEWIS™ RX+

TDA5240/35/25

Schematic, Layout and Configuration Recommendations

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
V1.2, 2013-11-14	
---	“Layout recommendations for TDA5240 family_v1.1” got additional items and recommendations on schematic, configuration and communication were added.

Table of Contents

Introduction

General information:
All items below are valid for all products of the SmartLEWIS RX+ family (TDA5240, TDA5235 and TDA5225), unless explicitly noted.

1 Schematic Recommendations (S.)

1) **First starting point** on a schematic for the TDA5240 family (=TDA5240/35/25) should be the evaluation board shown in the data sheet. Additional hints and advice are given below.

2) In 5V supply mode the **VDD5V** pin shall get a slew rate limitation. In some constellation the slew rate for **P_ON** pin shall be limited as well. Further details are described in our FAQ list item 8.

3) We recommend to use **supply blocking capacitor** values as noted in the datasheet and in FAQ item 8.

   The reason for using and recommending 100nF decoupling capacitor on the output of those 3 regulators (as noted in the datasheet) are the following:

   a) Each regulator needs a certain capacitor value on the output for a stable operation (no oscillation). Depending on the used capacitor value the regulator shows a certain phase margin (avoiding oscillation). The larger the phase margin the larger the margin which ensures that no oscillation appears (stability).

   b) 100nF is a good choice to filter-out (attenuate) lower frequency disturbances on the one hand and shows usually a not too big inductance (see also self-resonance) to attenuate higher frequency disturbances or interferers on the other hand.

   c) Furthermore 100nF is usually relative cheap.

4) Our **FAQ list** (downloadable from our product homepage) contains many other helpful information, so please refer to this document as well (e.g. information on how to handle unused I/O pins).

5) Undesired noise at the input pins of the **SPI bus** (NCS, SCK and SDI) of this high sensitivity radio can reduce the receiver's sensitivity. Therefore an RC low-pass filter on these lines from application controller to TDA5240/35/25 is recommended. Keep in mind to set the corner frequency of this low-pass filter about 10-times higher than the maximum occurring SPI rate (intended signal is almost not affected, but higher frequent noise is filtered-out).

6) Keep in mind that TDA5235 **SDO** output is in tristate mode, when SDO is not active => using a pull-up resistor close to the application controller input pin is a good idea here for avoiding floating inputs on the application controller.

7) The **output pins** (PPx and SDO) are in tristate during power-down. Thus, a pull-up or pull-down resistor may be required for PPx output pins used in the application.

8) **P_ON** pin shall be connected to an output pin of the application controller in order to providing an opportunity to reset the receiver chip (see also FAQ list item 18). Tristate mode of this output pin of the application controller would lead to a floating input of P_ON pin. This shall be avoided by applying either a pull-up or a pull-down resistor of about 100kOhm.

9) **RSSI** pin (pin26) shall not see less than 100kOhm and not more than 20pF load (see datasheet reference section).

10) **Crystal** should be placed close to TDA5240/35/25. The connection lines between crystal, crystal load capacitors and TDA5240/35/25 XTAL pins shall form a small active area on the PCB (see picture below in the “Layout Recommendations” section). This gives better EMC behavior.

11) The application shall use **NINT** signal on PP2 (pin12) of TDA5240/35, because PP2 already contains the NINT signal after a reset. Therefore a power-up reset (see datasheet section 2.4.9.2; e.g. after a brown-out reset) can be detected by the application controller as well, when PP2 uses NINT signal.

12) **PP3 output** (pin 25) is located close to the LNA input, therefore PP3 shall contain a relatively quiet signal only (like LOW, HIGH or RX_RUN). Other signals are not recommended on PP3 pin.

13) We cannot judge on the **RF matching network**, because this needs to be measured and fine-tuned at the customer anyway.

2 Layout Recommendations (L.)

1) **First starting point** on a layout for the TDA5240 family (=TDA5240/35/25) should be the evaluation board shown in the data sheet. Deletion of the components, which are not required in the specific *Customer Application,* will lead to a more compact layout:

   - e.g. 2nd IF filter
   - If analog RSSI is not needed, then also the copper track on the PCB should be removed
   - Depending on the supply mode, some components and connections can be removed
   - Crystal and load capacitors can be shifted closer in order to have a smaller exposed area to interfering EMI sources
   - Avoid loops covering large surfaces, as these may “collect” a large amount of induced (interferer) voltage , if exposed to an external EM field

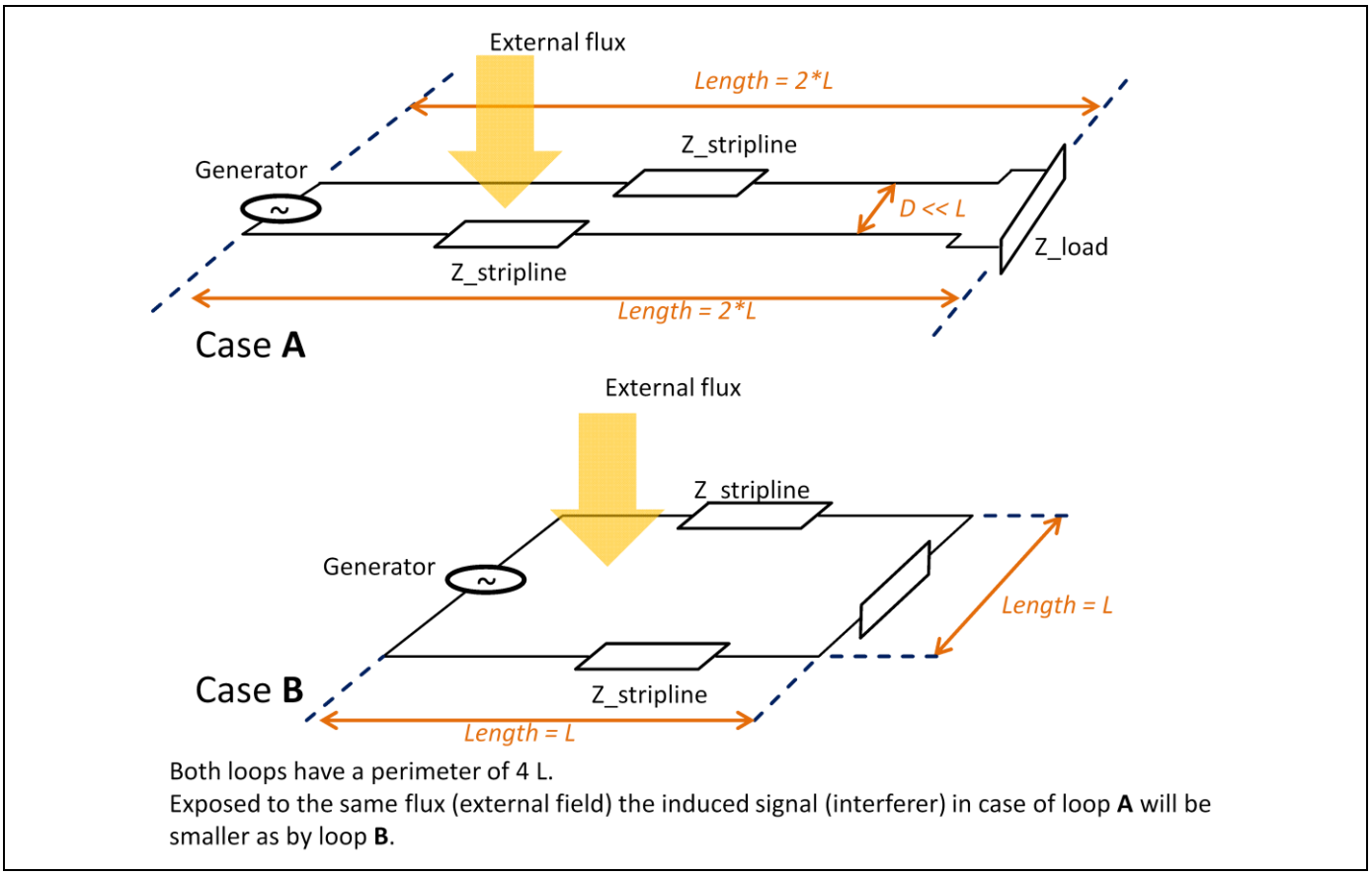

Figure 1 Avoiding loops covering large surface

2) The application **PCB** shall have at least 2 **layers**:

   - Top layer (layer 1) mainly for signal routing
   - The layer below top layer (layer2) shall mainly be used as ground plane. Other layers below layer 2 (e.g. layer 3, 4) can be used, if necessary.

3) **Supply decoupling capacitors** should be placed as close as possible to the chip on top layer. For those capacitors models with low ESR value should be chosen.

4) **Differential input matching** is performing better by rejection of common-mode injected EMI as single-ended

   - Best solution: differential SAW filter ➔ attenuates the common-mode interference (GND noise) and most of out-of-band signals

5) PCB layout hints for **minimum EMI cross-coupling**:

   Potential On-PCB EMI Source Examples:
   - TDA5240/35/25 Crystal oscillator
   - TDA5240/35/25 CLKOUT, if routed out via PPx
   - TDA5240/35/25 VDDD Pins and tracks on PCB
   - on-board µController/CLK generators and their supply lines
   - SPI clock and data lines
   - on-board LIN transceiver
   - on-board high power drivers
   - other RF emitting components on the PCB …

   EMI-aware PCB design attenuating the cross-coupling between the EMI sources:
   - take special care about the pins:
     - LNA_INN, LNA_INP, GNDRF
   - shielding using multilayer PCB and RF shielding
   - star-point topology for supply routing
   - good isolation between XOSC, PPx, SPI, other toggling lines and input RF structures
   - good isolation between digital supply (VDDD) and input signal lines and matching components
   - large distance between the sensitive RF application part (TDA5240/35/25 and its external components, like crystal, RF matching, CER filter, supply lines, I/O lines) and the EMI source

6) Digital supply lines and cross-coupled digital EMI show very short duration current and voltage surges, glitches and spikes generating **high-frequency spectrum** up to GHz range at $\mathbf{f_{EMI}}$ = $\mathbf{N*f_{SRC}}$

   For achieving the best sensitivity results the following has to be kept in mind. Every digital system generates certain frequencies (fSRC, e.g. the crystal frequency or a microcontroller clock) and harmonics (N * fSRC) of it, which can act as interferer (EMI source) and therefore sensitivity can be reduced. For more details see data sheet in section 3.

7) **GNDRF** (pin 24) and **GNDA** (pin 3) shall be connected low-ohmic to the solid RF-ground plane below TDA5240/35/25 chip (=Reference-GND) on top layer of the PCB. Additionally vias to ground plane layer (e.g. on layer 2) shall be placed.

8) Ground side of blocking caps of **VDDD** (pin 7) and **VDDD1V5** (pin 8) shall be connected to **GNDD** (pin 9) on top layer, forming a low-ohmic connection. So that the digital blocks have a good ground connection in the digital domain. GNDD (pin 9) shall be connected to the separate ground plane layer by a via in order to get a separation between digital ground and analog/RF ground.

9) Information: In case these low-ohmic connections would not be implemented, then exchange currents could flow between the grounds. This can cause self-made interference, which shall be avoided. All this is well known to every RF engineer.

10) Do not connect the “GND-pin” of the blocking capacitors of the digital supply (**VDDD** and **VDDD1V5**) directly with the “GND-pin” of the blocking capacitor of the 5V supply (**VDD5V**), but connect the “GND-pin” of the blocking capacitor of VDD5V directly to the GND-plane below the IC (GNDRF and GNDA).

11) Do not place **other noise generating units/devices** (e.g. containing strong charge pumps, which can generate harmonics on TDA5240/35/25 receive frequencies or LO or image frequencies) on the same supply net. Also do not place such noise generating units close to the highly sensitive radio receiver.

12) Please note that these are **“general” recommendations** (assuming ideal models/circumstances), but usually several compromises and trade-offs have to be found and accepted, so that sometimes certain circumstances, not ideal layout or GND concept, … can cause a different behavior, so that certain changes or measures (layout change, GND concept change …) which should actually improve the performance – as representing a better approach to an ideal layout or GND concept or … - can even degrade the performance or a certain performance parameter.

13) In case **analog RSSI** (pin 26) is not required in the application, then no test point connection shall be placed to RSSI pin (so that this copper line cannot act as antenna => see also FAQ item 16).

14) As a good practice in any RF design, **shielding** around sensitive nodes can improve the EMC performance of the application. So shielding over the complete chip area or sensitive nodes like crystal oscillator is recommended.

15) We cannot give detailed recommendations on the **RF matching** (LNA_INN (pin22)) and matching of a SAW-filter, as this is strongly dependent on the layout, board thickness, board material and even on the “layout” and other parameters of the passive components. Therefore this needs to be measured finally by the user. However, a few general hints are given in the following items:

    1. Connection from matching network to LNA input shall be rather short.

    2. RF matching shall not be spread over a large and long area, but shall be made rather compact.

    Do not place interfering signal lines close to the RF matching or crystal oscillator circuit, as these undesired signal frequencies might be coupled into the high-sensitivity radio receiver.

3 Recommendations on Chip Configuration / SPI Communication (C.)

1) TDA5240/35/25 registers are either pure Write registers or pure Read registers, but no combined Write/Read registers (see also FAQ list item 17). After an **SPI write** command sequence we recommend to readout the SPIAT and SPIDT registers and compare these values with the address and data byte of the previous SPI communication sequence (details shown in datasheet section 2.5.5).

2) After an **SPI burst write** command sequence we recommend to readout the SPICHKSUM register and compare this value with the calculated SPI checksum of the previous SPI communication sequence (details shown at the end of datasheet section 2.5.5).

3) Blocks of increasing adjacent register addresses (e.g. register x, x+1, x+2, x+3) need to be grouped by the user and can be sent within one **SPI burst write** command. In case of a gap in the register addresses a new block needs to be generated. Each of these blocks needs its own Burst-Write command, because Burst Write does NOT skip register address gaps.

4) One general comment on µC-software implementation regarding **NCS**. NCS line shall be set to low only in case of SPI communication. So keep NCS line high when no SPI communication takes place.

5) Registers shall **not be downloaded to TDA5240/35/25** when the chip is operated in RMS (Run Mode Slave) or SPM (Self Polling Mode).

   In case TDA5240/35/25 is operated in **SPM**, then the chip needs to be set into SLEEP mode before changing a registers. The same can be applied, when the chip is operated in **RMS**. Alternatively, in case TDA5240/35/25 is operated in RMS, then the chip can be set into Hold mode before changing registers.

6) Any **SPI communication during reset** of TDA5240/35/25 needs to be avoided, because depending on timing between reset-finished and SPI communication a different SPI command/address could be understood by the chip. And this needs to be avoided.

7) The transparent mode receiver TDA5225 has only a very weak wake-up criterion - RSSI. Usage of this **weak wake-up criterion RSSI** is not really recommended, because it's located very early in the signal chain and false alarms may be the undesired consequence. TDA5225 shall be used in Slave mode (RMS or SLEEP mode), where the activation/deactivation of reception of TDA5225 is done via SPI commands sent by the external application controller.

8) One important step for the application is to **center the receive frequency** by XTAL trimming. More details can be taken from FAQ list item 5.

9) When **AFC (Automatic Frequency Control)** is activated, then even noise can pull the receivers center frequency (before a real signal is transmitted). This "AFC drift" needs to be taken into account especially when the chip is in **RMS** (always receiving). So in this case the AFCLIMT (AFC offset saturation limit) shall be set to a rather low value (not more than 42.8kHz).

   In **SPM** this effect is not critical, because in case a transmit telegram is sent, the receiver's SPM ON- and OFF-times need to be set in a way that the receiver will see a transmit signal during ON-time and AFC can follow this transmitted signal. No "AFC drift" takes place before a real signal is transmitted. However, we recommend to use no larger AFCLIMT than 64.3kHz in SPM. In SPM it will be wise to activate the feature "Enable Restart at Channel Change in Self Polling Mode" (Explorer wizard page 10).

10) Keep in mind that the **filter settings** inside TDA5240/35/25 (BPF, PDF) need to be selected depending on:

    1. Modulation spectrum
    2. Transmitter tolerances (mainly crystal tolerances)
    3. Receiver tolerances (mainly crystal tolerances)
    4. Tolerances of BPF (band pass filter inside receiver chip) regarding center frequency and bandwidth (see datasheet reference item G3.1 and G3.3/G3.4)

    Info: The typical and the minimum analog bandwidth (BWana) for each BPF setting can be taken from our AFC Application note "AN_TDA5225_35_40_Sensitivity_improvement_usingAFC_V1.x.pdf", which is downloadable from our product homepage.

11) Keep in mind that **SigRec** thresholds (Signal detector, noise detector and SIGDETLO thresholds) of TDA5240/35 are depending on chip settings, filter settings and frontend matching. So these thresholds need to be set by the customer for the final application module using our Application Note "AN_TDA5240_35_Signal_Noise_Detector_Threshold_Settings_v1.xxxx.pdf" (downloadable from our product homepage).

    SigRec thresholds can be determined very easily when using TDA5240/35 Explorer ➔ "Explore" tab ➔ "Power Readout Statistics" tab together with SIB-Interface and IFX TDA5240/35 3.3V evaluation board. Even a 3.3V customer application can be evaluated by connecting to header X6 of the IFX evaluation board, when:

    a) cutting the P_ON line between header X6 and P_ON pin of the chip mounted on the IFX evaluation board

    b) and connecting P_ON pin of the chip mounted on the IFX evaluation board to GND (in order to set this chip in powerdown mode, so that no response from this chip can interfere the desired communication to the chip on the customer application board).

    In case of a 5V customer application, the above described evaluation of SigRec thresholds is possible, when using a levelshifter in-between (Note: SIB is working in 3.3V domain). See also FAQ list item 19.

12) In case very accurate RSSI values are required in the application (see datasheet reference items G2.7 – G2.10), then our Application Note on **RSSI Trimming** ("AN_TDA5240_Family_CalculationSheet_201xxxxx__RSSItrimming_v1.x.pdf", downloadable from our product homepage) will be very helpful.

13) When using **Self Polling Mode (SPM)**, some timer values (ON-time, OFF-time, WULOT) inside TDA5240/35 need to be set. For this purpose our XLS-based Application Note "AN_TDA5240_35__SP_Timings_general_xxxxx.xls" (downloadable from our product homepage) can be used.

    In case Signal Recognition is used as WU criterion (Level criterion or UFFB) in TDA5240/35, use a value of **8** in entry field "**SigRec on time in 1/16 Bits**" in Explorer wizard page 9 for all activated RF channels.

14) In Self Polling Mode (SPM) some activity on the RX_RUN signal is observable according to the selected ON- and OFF times. This RX_RUN activity can be evaluated by the application controller as some kind of **“health” signal** of the receiver chip. Keep in mind: After successful wake-up (receiver changes from SPM to RMSP – Run Mode Self Polling), the RX_RUN signal stays in a static state until the receiver returns to SPM again (e.g. after a TOTIM event or a detected EOM – see state diagram “Run Mode Self Polling” in the datasheet).

15) **Unused PPx signals** in the application shall be set to a quiet state like “LOW”. It’s OK to use these selected signals during evaluation and for debugging, but in the final application they should be set to “LOW”.

16) In case **FIFO mode** (POFM … Packet Oriented FIFO Mode) is used, then CH_DATA shall only be used as debug output.

17) In case **CH_DATA** output gets processed by the application controller (and FIFO data is not used in the application), then the “External Data Processing” mode “Chip Data (RX Mode: TMCDS)” shall be used (see Explorer wizard page 1). See also Errata sheet item 7 for additional settings required in this receive mode.

18) Our **FAQ list** and the **Errata Sheet** (both downloadable from our product homepage) contain additional helpful information, so please refer to these documents as well.

19) **Performance testing** of the configuration on the application module shall be done according our “RF Design Verification Guideline” or “Customer Application Verification Tests” documents.

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