TDA38740/25 OptiMOS iPOL

40/25A Single-voltage Synchronous Buck Regulator with PMBus

Quality Requirement Category: Industrial

Features

- Single 4.5 V to 17 V application or Wide Input Voltage Range from 3.0 V to 17 V with external Vcc
- Output Voltage Range: 0.25 V to 5.12 V based on Output Feedback resistor divider network
- Enhanced Fast COT Engine Stable with Ceramic output Capacitors without External Compensation
- Optional Forced Continuous Conduction Mode and Diode Emulation for Enhanced Light Load Efficiency
- Pin programmable Output Voltage, Switching Frequency/mode selection with 16 unique selectable settings
- Programmable Switching Frequency from 400 kHz to 2 MHz in steps of 200 kHz, excluding 1600 kHz
- Monotonic Start-Up with Selectable Soft-Start Time through PMBus commands & Pre-Bias Start-Up
- Thermally Compensated Internal Over Current Protection with Eight Selectable Settings
- Enable input with Voltage Monitoring Capability & Power Good Output
- PMBus system interface for reporting of Temperature, Voltage, Current, & Power telemetry
- Single image Multiple Time Programming (MTP) for the USER section
- Digitally programmable load-line without any external components
- Operating temp: -40 °C < Tj < 125 °C
- Small Size: 5 mm x 6 mm PQFN
- Lead-free, Halogen-free and RoHS2 Compliant with Exemption 7a

Applications

- Server Applications
- Storage Applications
- Telecom & Datacom Applications
- Distributed Point of Load Power Architectures

Description

The TDA38740/725 is an easy-to-use, fully integrated and highly efficient dc-dc regulator. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode make TDA38740/725 a small footprint solution, providing high-efficiency power delivery. Furthermore, it uses a fast Constant On-Time (COT) control scheme, which simplifies the design efforts and achieves fast transient response.

TDA38740/725 is a versatile regulator, operating with wide input and output voltage ranges, offering programmable switching frequency from 400 kHz to 2 MHz in steps of 200KHz excluding 1600KHz, and providing eight unique selectable current limits. It features a programmable dc loadline, which provides an additional tool to manage the transient response.

It also features important protection functions, such as thermally compensated current limit, over voltage and under voltage protection, and thermal shutdown to give required system level security in the event of fault conditions. The device configuration can be easily defined using Infineon's XDP Designer GUI and is stored in the

on-chip memory. The controller requires the fewest possible external components and results in a simplified Bill of Materials (BOM).

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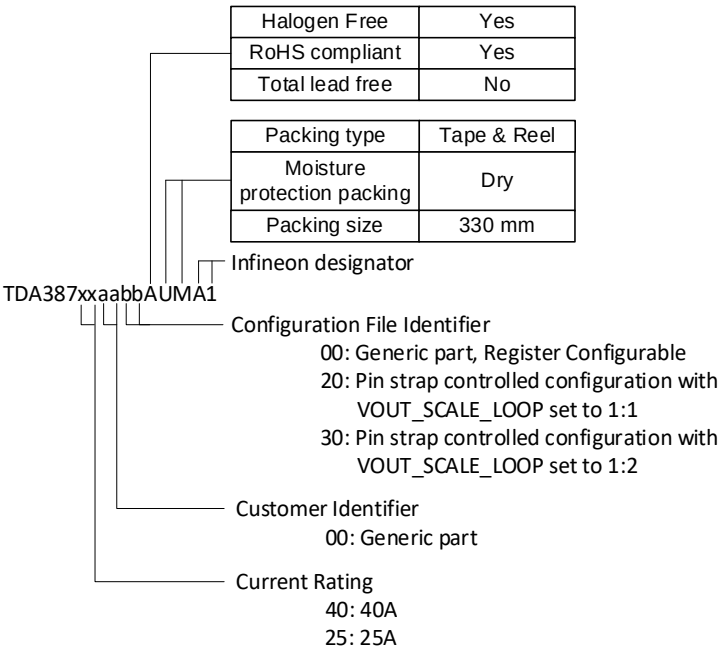
1 Ordering Information

Table 1 Ordering Information

Sales Part Number	Package Type	Standard Pack Form and Qty		Orderable Part Number	Part type
TDA38740-aabb	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA387400000AUMA1	40A Generic Part–PMBus controlled configuration
	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA387400020AUMA1	40Amp Generic Part – Pin strap controlled configuration with VOUT_SCALE_LOOP set to 1:1
	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA387400030AUMA1	40Amp Generic Part – Pin strap controlled configuration with with VOUT_SCALE_LOOP set to 1:2
	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA38740aabbAUMA1	40A Custom part
TDA38725-aabb	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA387250000AUMA1	25A Generic Part-PMBus controlled configuration
	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA387250020AUMA1	25Amp Generic Part – Pin strap controlled configuration with VOUT_SCALE_LOOP set to 1:1
	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA387250030AUMA1	25Amp Generic Part – Pin strap controlled configuration with VOUT_SCALE_LOOP set to 1:2
	QFN 5 mm x 6 mm	Tape and Reel	5000	TDA38725aabbAUMA1	25A Custom part



Ordering Information

Orderable Part Number Description

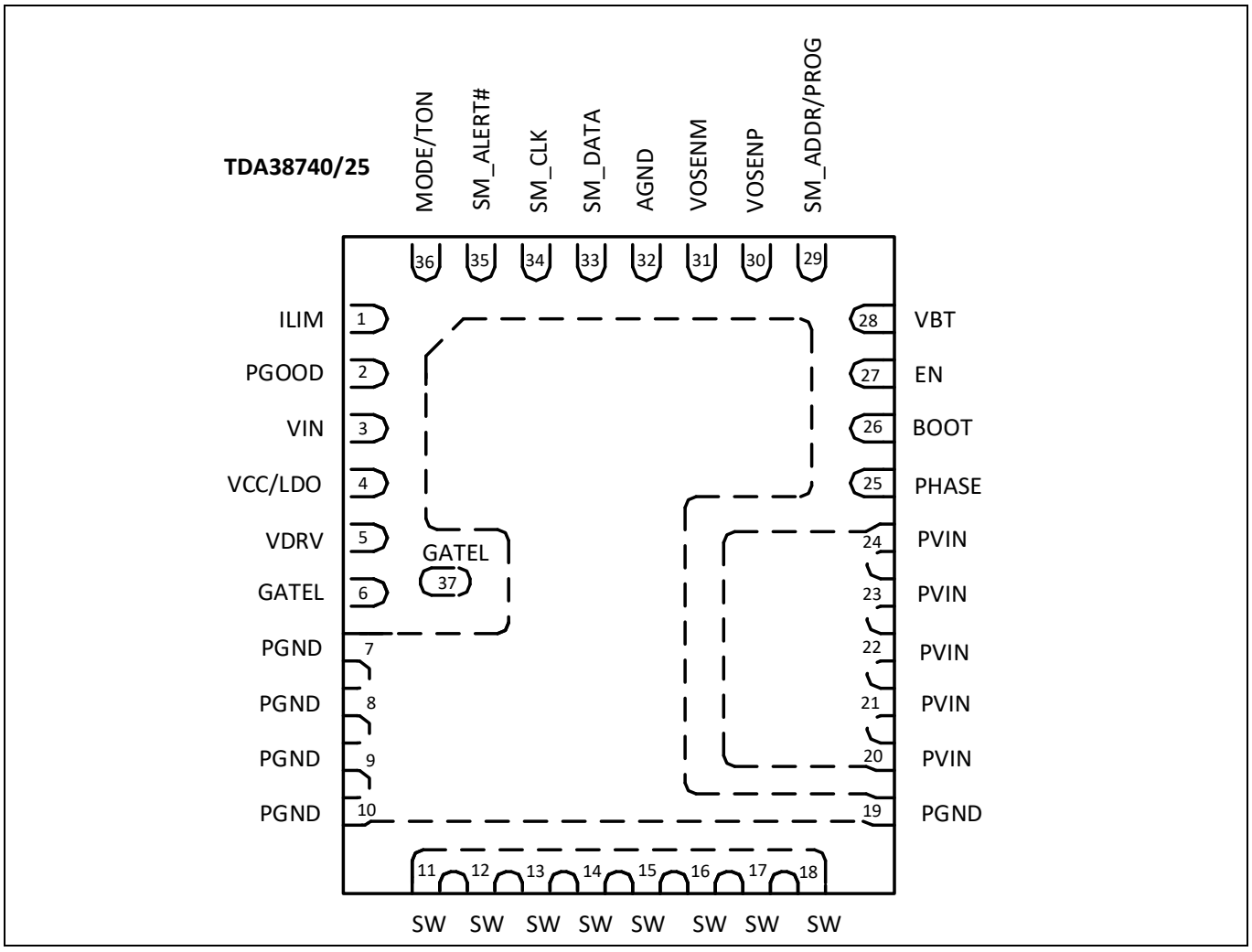


Figure 1 Package Top View

2 Functional Block Diagram

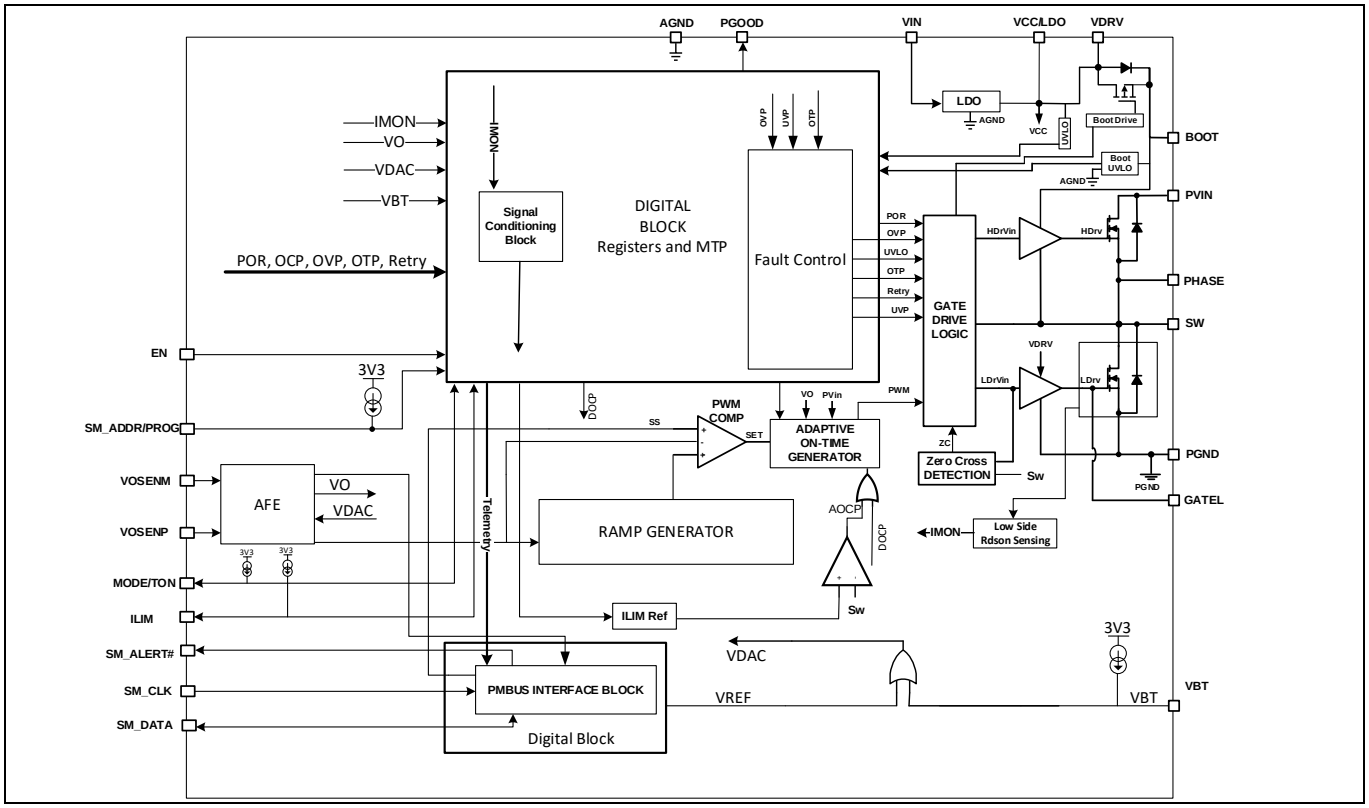


Figure 2 Block Diagram

3 Typical Application Diagram

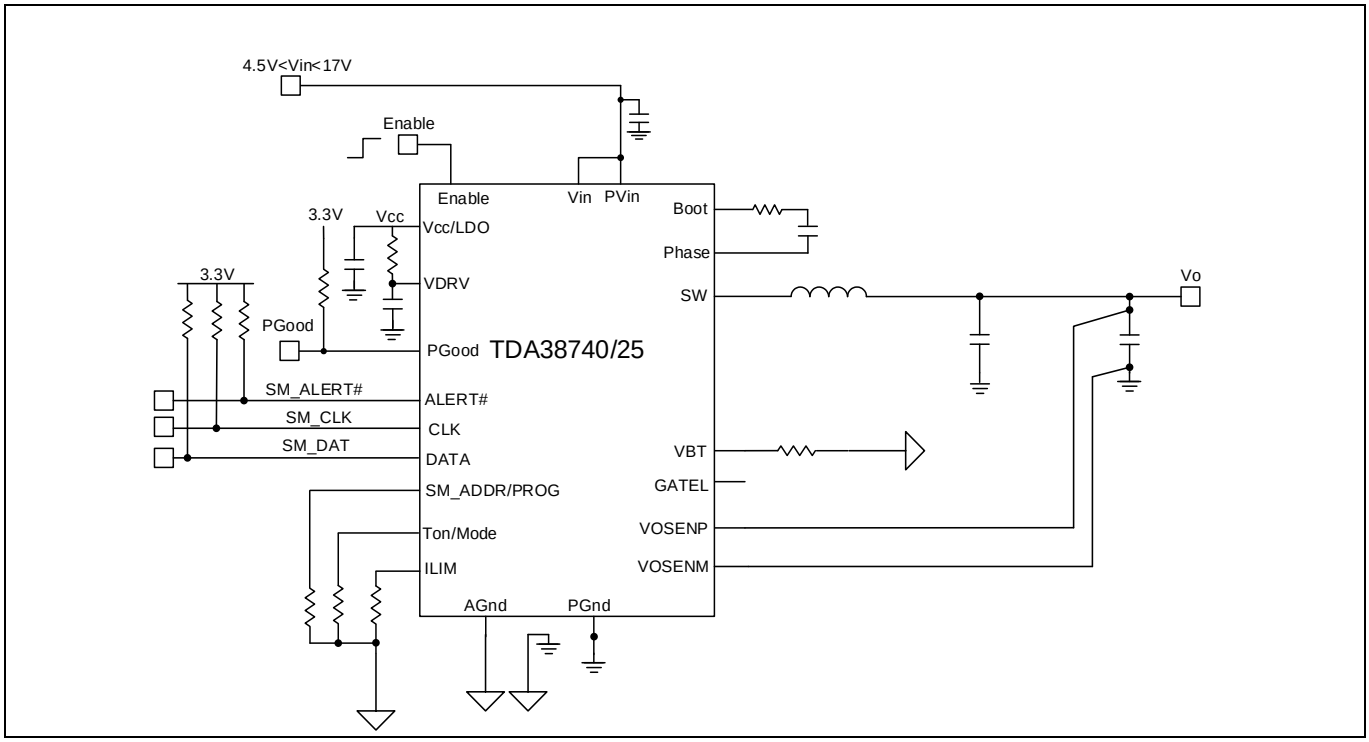


Figure 3 TDA38740/725 application circuit for Vout< 2.5 V

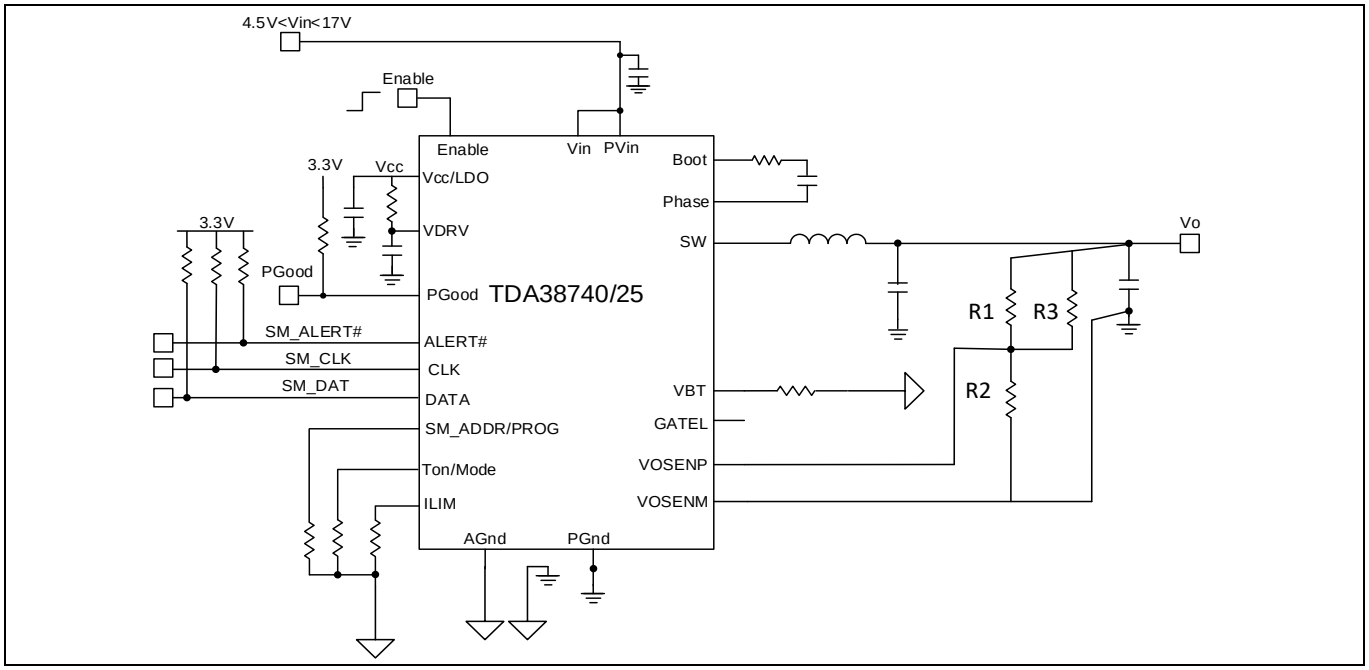


Figure 4 TDA38740/725 application circuit for Vout> 2.5 V

4 Pin Descriptions

Note: A- Analog; D- Digital; [I]- INPUT; [O]- OUTPUT; [B]- BI-DIRECTIONAL; [P]- POWER

Table 2 Pin Descriptions

Pin#	Pin Name	Pin Type	Pin Description
1	ILIM	A[I]	Connect a resistor to ground to set Over Current Protection (OCP) limit. Eight user selectable OCP limits are available.
2	PGood	D[O]	Power Good status output pin is open drain. Connect a pull up resistor from this pin to an external bias voltage.
3	VIN	A[I]	Input voltage for an Internal LDO. A 4.7 uF capacitor should be connected between this pin and PGND. If an external supply is connected to the Vcc/LDO pin, this pin should be shorted to the Vcc/LDO pin and a 2.2 uF ceramic capacitor can be shared with Vin and Vcc/LDO.
4	Vcc/LDO	A[P]	Input bias for an external Vcc voltage /Output of the internal LDO. A 2.2 uF ceramic capacitor is recommended to use between Vcc/LDO, VDRV and the Power ground (PGND). An optional decoupling capacitor can be placed between Vcc/LDO and AGND. Connect to external supply when internal LDO not being used.
5	VDRV	A[P]	VDRV should be shorted to the Vcc/LDO pin on the PCB. A 2.2 uF ceramic capacitor is recommended to use between VDRV, Vcc/LDO and the Power ground (PGND). Connect to external supply when internal LDO not being used.
6, 37	GATEL	A [O]	Gate of Low-side FET. The signal on this pin should be used for test purposes only and should not have external components connected to it.
7, 8, 9, 10, 19	PGND	-	Power Ground. Should be connected to the system's power ground plane. PGND and AGND are internally connected via the lead frame.
11, 12, 13, 14, 15, 16, 17, 18	SW	A [O]	Switch Node. Connect these pins to an output inductor.
20, 21, 22, 23, 24	PVin	A [P]	Input supply for the power stage.
25	Phase	A [O]	Source of High-side FET. Connect a bootstrap capacitor between this pin and the Boot pin. A high temperature (X7R) 0.1 uF or greater value ceramic capacitor is recommended.
26	Boot	A [I]	Supply voltage for the high side driver. Connect this pin to the Phase pin of the regulator through a bootstrap capacitor.
27	EN	A [I]	Enable pin to turn the IC on and off.
28	VBT	A[I]	A resistor from this pin to ground defines the default boot voltage that the part will boot up in.
29	SM_ADDR/PROG	D[I]	PMBus Slave Address and PROG pin. A resistor to ground on this pin points to one of the sixteen unique PMBus slave devices which needs to be addressed on the board. The same address also defines the specific configuration from a multi image configuration file (supports 13 images max) that will be loaded from the OTP during power-up.

Pin Descriptions

Pin#	Pin Name	Pin Type	Pin Description
30	VOSENP	A [I]	Output voltage feedback pin. Connect this pin to the output of the regulator to regulate the output voltage.
31	VOSENM	A [I]	The pin provides the return path for the remote voltage sensing. It is used as a reference for the Analog Front End (AFE)
32	AGND	-	Signal ground for the internal circuitry. AGND should be connected to PGND on the PCB.
33	SM_DATA	D [B]	Serial data line I/O. PMBus bi-directional serial data line.
34	SM_CLK	D [I]	Serial Clock Line Input. PMBus serial clock input. The interface is rated to max of 1 MHz
35	SM_ALERT#	D [O]	SMB Active low alert line
36	MODE/TON	D [I]	Multi-function pin. This pin can be used to select one of eight switching frequencies, and FCCM or DEM mode by connecting a resistor from this pin to ground.

5 Absolute Maximum Ratings

Stresses higher than those mentioned in Table 3 below may result in permanent damage to the device. These are the absolute stress ratings only and the operation of the device is not recommended or implied at these or any other condition's in excess of those given in the recommended operating ratings in Table 5. Exposure of values over and above the recommended ratings for extended periods may adversely affect the operation and reliability of the device.

Table 3 Absolute Maximum Ratings

Description	Symbol	Values			Unit	Note/ Test Conditions
		Min	Typ	Max		
Power Input voltage	V_{PVIN}	-0.3	-	25	V	Note 1, PVIN Pin
LDO Input voltage	V_{IN}	-0.3	-	25	V	Note 1, VIN Pin
Enable voltage	V_{EN}	-0.3	-	25	V	EN Pin
PVIN-PHASE voltage	V_{PVin} -V_{PHASE}	-5 V for 5 ns, -0.3 V dc	-	34 V for 1 ns, 25 V dc	V	PVIN-PHASE pin
PVin-Switch Node voltage	V_{PVin} -V_{SW}	-5 V for 5 ns, -0.3 V dc	-	34 V for 1 ns, 25 V dc	V	VIN-PHASE pin
PVIN-Switch Node voltage	V_{PVIN} -V_{SW}	-5 V for 5 ns, -0.3 V dc	-	34 V for 1 ns, 25 V dc	V	PVIN- SW Pin
Internal Driver voltage	V_{DRV}	-0.3	-	6	V	Note 1, VCC/VDRV Pin
Gate Low Pin voltage	V_{GATEL}	-0.3	-	6	V	GateL Pin
BOOT voltage	V_{BOOT}	-0.3 V for 5 ns, -0.3 V dc	-	29 V dc	V	BOOT Pin
	V_{BOOT} - V_{PHASE}	-0.3	-	7 V for 5 ns, 6 V dc	V	BOOT – PHASE Pin
Switch Node voltage	V_{SW}	-7 V for 5 ns, -0.3 V dc	-	34 V for 1 ns, 25 V dc	V	Switch Node Pin
Phase Node voltage	V_{PHASE}	-7 V for 5 ns, -0.3 V dc	-	34 V for 1 ns, 25 V dc	V	Phase Pin
Address/PROG voltage	$V_{SM_ADDR/PROG}$	-0.3	-	3.6	V	Note 1, SM_ADDR/PROG Pin
Output Positive Sense voltage	V_{VOSENP}	-1.5 V for 5 ns, -0.3 V dc	-	3.6	V	Note 1, VOSENP Pin
Output Negative Sense voltage w.r.t AGND	V_{VOSENM}	-0.3	-	0.3	V	Note 1, VOSENM Pin
Voltage Regulator Power Good	V_{PGOOD}	-0.3	-	3.6	V	Note 1, PGOOD Pin
ILIM Voltage	V_{ILIM}	-0.3	-	3.6	V	Note 1, ILIM Pin
MODE/TON voltage	$V_{MODE/TON}$	-0.3	-	3.6	V	Note 1, MODE/TON Pin
VBT voltage	V_{VBT}	-0.3	-	3.6	V	Note 1, VBT voltage pin
Power GND w.r.t Analog GND voltage	V_{PGND}- V_{AGND}	-1.5 V for 5 ns, -0.3 V dc	-	1.5 V for 5 ns, 0.3 V dc	V	PGND – AGND Pin
SM CLK voltage	V_{SM_CLK}	-0.3	-	3.6	V	SM_CLK Pin

Absolute Maximum Ratings

Description	Symbol	Values			Unit	Note/ Test Conditions
		Min	Typ	Max		
SM Data voltage	V_{SM_DAT}	-0.3	-	3.6	V	SM_DAT Pin
SM Alert voltage	$V_{SM_ALERT\#}$	-0.3	-	3.6	V	SM_ALERT# Pin
Juntion Temperature	T_{Jmax}	-40	-	150	°C	-
Storage Temperature	$T_{STORAGE}$	-55	-	150	°C	-

Note:

1. PGND and AGND pins are connected together.

Attention: Stresses beyond these listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied.

6 Thermal Characteristics

Table 4 Thermal Characteristics

Description	Symbol	Values	**Test Conditions**
Junction to Ambient Thermal Resistance	θ_{JA}	19 °C/W	Note 2
Junction to PCB Thermal Resistance	$\theta_{JC\text{-}PCB}$	1.1 °C/W	Note 3
Junction to Case Top Termal Resistance	θ_{JC}	24 °C/W	

Note:

2. *Thermal resistance is measured with components mounted on a standard EVAL_TDA38740_1.2Vout demo board in free air*
3. *Thermal resistance is based on the board temperature near pin 22*

7 Electrical Specifications

Table 5 Recommended Operating Conditions for Reliable Operation

Description	Min	Max	Unit	Note
PVin Voltage Range with External Vcc	3	17	V	Note 4, Note 5
PVin Voltage Range with Internal LDO	4.5	17	V	Note 5 , Note 6 & Note 10
Vcc Supply Voltage Range	4.5	5.5	V	Note 4 , Note 7
Output Voltage Range	0.25	5.12	V	Note 8
Continuous Output Current Range for TDA38740		40	A	Note 9
Continuous Output Current Range for TDA38725		25	A	Note 9
Switching Frequency (excluding 1600 kHz)	400	2000	kHz	Note 10
Operating Junction Temperature	-40	125	°C	

Note:

4. *VCC/VDRV pin is connected to an external bias voltage when Pvin is less than 4.5 V*
5. *A common practice is to have 20% margin on the maximum SW node voltage in the design. For applications requiring PVin equal to or above 14 V, a small resistor in series with the Boot pin should be used to ensure the maximum SW node spike voltage does not exceed absolute maximum specs. Alternatively, a snubber can be used at SW node to reduce the SW node spike.*
6. *PV_{in} with internal LDO is used. For single-rail applications with the internal LDO and PV_{in} = 4.5 V-5.4 V, the internal LDO may enter dropout mode. AOCP limits can be reduced due to the lower VCC voltage.*
7. *The TDA38740/725 is designed to function with VCC down to 4.5 V. However, electrical specifications such as AOCP limits may be degraded.*
8. *The maximum output voltage is limited by the minimum off-time. For output voltages above 2.56 V an external feedback resistor divider is needed.*
9. *Refer to Section 15.1 for maximum output current rating at different ambient temperature and OCP threshold tolerance*
10. *The maximum LDO output current must be limited within 50 mA for operations requiring the full operating temperature range of -40 °C ≤ T_J ≤ 125 °C. Thermal De-rating may be needed at an elevated ambient temperature to ensure the junction temperature remains within the recommended operating range.*

7.1 Electrical Characteristics

Unless otherwise specified, these specifications apply over, 4.5 V ≤ Vin = PVin ≤ 17 V, in 0 °C < T_J < 125 °C. Typical values are specified at Ta = 25 °C.

Table 6 Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Stage						
Top Switch	$R_{ds(on)_Top}$	VBoot – Vsw= 5.0 V, Io = 35 A, Tj =25 °C	-	2.9	-	mΩ
Bottom Switch	$R_{ds(on)_Bot}$	Vcc = 5.0, Io= 35 A, Tj =25 °C	-	1.00	-	mΩ
Bootstrap Diode Forward Voltage		I(Boot) = 25 mA	-	780	950	mV
SW Leakage Current	I_{SW}	SW = 0 V, EN = 0 V	-	-	175	µA
		SW = 0 V, EN = high, No Switching	-	-	175	µA
Dead Band Time	T_{db}	SW Node rising edge, 40 A, Internal LDO, T_j=25 °C, Note 11	-	10	-	ns
		SW Node falling edge, 40 A , Internal LDO, T_j=25 °C, Note 11	-	10	-	ns
Supply Voltage	**PVin, Vin and External VCC**					
PVin range (using external VCC = 5V)			-	3-17	-	V
Vin Range (using internal LDO)		Fsw = 600 kHz	-	4.5 -17	-	V
		Fsw = 2000 kHz	-	4.5 –17	-	V
External VCC			4.5	5	5.5	V
Supply Current	**Iin**					
PVin Supply Current (standby)(External Vcc)	$I_{in\ (Standby)}$	EN = Low, No Switching, Note 14	-	2	-	mA
PVin Supply Current (dynamic)(External Vcc)	$I_{in\ (Dyn)}$	EN = High, Fs = 800kHz, Vin=PVin=12 V, Vout =1.1 V, Note 14	-	15	-	mA
PVin Supply Current (standby)(Internal Vcc)	$I_{in\ (Standby)}$	EN = Low, No Switching, Note 14	-	12	-	mA
PVin Supply Current (dynamic)(Internal Vcc)	$I_{in\ (Dyn)}$	EN = High, Fs = 800kHz, Vin=PVin=12 V, Vout =1.1 V, Note 14	-	48	-	mA
Remote Voltage Sense Inputs	**VOSENP, VOSENM**					
VOSENP Input Current		VOSENP = 3.6 V	-	-	230	µA
		VOSENP = -0.3 V	-85	-	-	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VOSENM Input Current		VOSENM = 0.3 V	-155	-	-	µA
		VOSENM = -0.3 V	-200	-	-	µA
Differential Input Voltage Range			-	-	2.56	V
VOSENM Input CM Voltage			-	±300	-	mV
MODE/TON						
Output Current			-	104	-	µA
VBT/ILIM/SM_ADDR						
Output Current			-	15	-	µA
Open-Drain Outputs-20mA Drive	**SM_CLK, SM_DAT, SM_ALERT#**					
Output Low Voltage		I = 20 mA	-	-	0.4	V
On Resistance		I = 20 mA	-	7	-	Ω
Tri-State Leakage		0 – 3.6 V	-5	-	5	µA
On-Time Timer						
Frequency Range (programmable)		Excluding 1600 kHz and in steps of 200 kHz	400	--	2000	KHz
Minimum On-Time		Tj=25°C, PVin=12 V, Vo=0 V, Note 11	-	25	-	ns
Minimum Off-Time	Toff(Min)	Tj=25°C, VFB=0 V, Note 11	-	150	-	ns
System Set Point Accuracy						
0.25 V ≤ Vout ≤ 0.445 V		-40 °C ≤ T_J ≤ 125°C Typ = 3σ, Note 11 & 12	-	±10	-	mV
0.45 V ≤ Vout ≤ 0.995 V			-	±8	-	mV
1.0 V ≤ Vout ≤ 2.52 V			-	±1	-	%
VCC LDO Output	**Vcc**					
Vcc Output Voltage	Vcc	5.5 V ≤ PVin ≤ 17 V, when Icc =50 mA, Cload = 2.2 uF, Tj=25°C	4.7	5.0	5.3	V
VCC Dropout	Vcc_drop	PVin = 4.5 V, Icc=50 mA, Cload=2.2uF, Tj=25°C	-	650	-	mV
Under Voltage Lockout						
Vcc_Good Start Threshold	VCC_UVLO_Start	Vcc Rising Trip Level	3.8	4.0	4.2	V
Vcc_Good Stop Threshold	VCC_UVLO_Stop	Vcc Falling Trip Level	3.6	3.8	4.0	
Enable-Start-Threshold	Enable_UVLO_Start	Ramping up	0.61	0.65	0.69	V
Enable-Stop-Threshold	Enable_UVLO_Stop	Ramping down	0.51	0.55	0.59	
Boot Rising Threshold	BOOT_UVLO_Rising	Boot-Phase Ramping up, Note 11	3.7	3.85	4.0	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Boot Falling Threshold	BOOT_UVLO_Falling	Boot-Phase Ramping down, Note 11	3.5	3.65	3.8	
Over Current Limit						
TDA38740 Current Limit Threshold (Valley Current)	I_{oc}	Tj = 25 °C, Vcc =5.0 V,	-	10	-	A
			-	15	-	
			-	20	-	
			-	25	-	
			-	30	-	
			-	40	-	
			-	50	-	
			-	60	-	
TDA38725 Current Limit Threshold (Valley Current)	I_{oc}	Tj = 25 °C, Vcc =5.0 V,	-	10	-	A
			-	15	-	
			-	20	-	
			-	25	-	
			-	25	-	
			-	25	-	
			-	25	-	
			-	25	-	
Current Limit Threshold Accuracy		See Note 11		±20		%
Over Voltage Protection						
Fixed OVP Threshold (Programmable)	OVP_Vth	In VOUT_SCALE_LOOP 1:1 mode, 8 Discrete Options	-	0.8	-	V
			-	1.0	-	
			-	1.2	-	
			-	1.35	-	
			-	1.5	-	
			-	1.8	-	
			-	2.2	-	
			-	2.85	-	
		In VOUT_SCALE_LOOP 1:2 mode, 8 Discrete Options. Note 11 & 13	-	1.6	-	V
			-	2.0	-	
			-	2.4	-	
			-	2.7	-	
			-	3.0	-	
			-	3.6	-	
			-	4.4	-	
			-	5.7	-	
Output Fixed OVP Threshold Accuracy		See note 11		±5		%
Relative OVP Threshold (programmable)		Relative to Vout in steps of 50 mV in VOUT_SCALE_LOOP 1:1 mode, Note 14	50	-	400	mV

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		Relative to Vout in steps of 50 mV in VOUT_SCALE_LOOP 1:2 mode, Note 13 and 14	100	-	800	mV
Output Relative OVP Threshold Accuracy		VOUT_SCALE_LOOP 1:1 mode, Note 14	-	±100	-	mV
		VOUT_SCALE_LOOP 1:2 mode, Note 13 & 14	-	±200	-	mV
Under Voltage Protection						
UVP Trip Threshold	UVP_Vth	Relative to Vout in steps of 50 mV in VOUT_SCALE_LOOP 1:1 mode, Note 13	50	-	400	mV
		Relative to Vout in steps of 50 mV in VOUT_SCALE_LOOP 1:2 mode, Note 13 and 14	100	-	800	mV
Output Relative UVP Threshold Accuracy		VOUT_SCALE_LOOP 1:1 mode, Note 13	-	±100	-	mV
		VOUT_SCALE_LOOP 1:2 mode, Note 13 & 14	-	±200	-	mV
IMON Reporting Accuracy						
IMON Accuracy	Imon	Vin = 12 V, Vout = 1.2 V, Iout = 40 A, Note 11	-	±6	-	%
Power Good	**Pgood**					
Pgood Sink Current	I_{PG}	V_{PG} = 0.5 V, Rpull-up = 500 Ω to 3.3 V	-	5	6	mA
Pgood Open Drain Leakage Current		V_{PG} = 3.6 V	-5	-	5	µA
Pgood Low Voltage	V_{PG_L}	Vin = Vcc = 5 V, I = 20 mA	-	-	0.1	V
Pgood Low Voltage	V_{PG_H}	Vin = Vcc = 0 V, Rpull-up = 4.7 kΩ to 3.3 V, Note 11	-	-	0.7	V
Thermal Shutdown						
Thermal Shutdown		Note 11	-	140	-	°C
Hysteresis		Note 11	-	20	-	
PMBus Reporting			-		-	
Bus Speed		Normal	-	100	-	kHz
		Fast	-	400	-	kHz

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		High-Speed	-	1000	-	kHz
Output Voltage Resolution		See Note 14 & 15	-	0.625, 0.977, 1.953, 3.906	-	mV
Output Voltage Filter Rate			-	8	-	kHz
Output Voltage Update Rate			-	379	-	kHz
Highest Reported Vout		VOUT_SCALE_LOOP =1:1	-	-	2.56	V
		VOUT_SCALE_LOOP =1:2	-	-	5.12	V
Vout Reporting Accuracy		-40 °C - 125 °C (Tj), 4.5 V < Vcc < 5.5 V, 0.25 ≤ Vout ≤ 0.5; VOUT_SCALE_LOOP in 1:1 mode	-2	-	2	%
		-40 °C - 125 °C (Tj), 4.5 V < Vcc < 5.5 V, 0.5<Vout ≤ 2.52; VOUT_SCALE_LOOP in 1:1 mode	-1	-	1	%
Iout Resolution			-	0.0625	-	A
Iout Filter Rate			-	8	-	kHz
Iout Update Rate			-	379	-	kHz
Iout Digital Monitoring Range			-	-	64	A
Iout Accuracy (PMBus)		0 °C-125 °C, 4.5 V<Vcc<5.5 V 10 A ≤ Iout ≤ 40 A 0.25 V ≤ Vout ≤ 2.52 V	-	±6	-	%
Temperature Resolution			-	1	-	°C
Temperature Filter Rate			-	4	-	kHz
Temperature Update Rate			-	189	-	kHz
Temperature Monitoring Range			-40	-	125	°C
Temperature Reporting Accuracy		Note 11	-	±1	-	°C
PMBus Interface Timing Specifications SM_DAT, SM_CLK						
Input Low Voltage (V_{IL})			-	-	0.8	V
Input High Voltage (V_{IL})			1.35	-	-	V
Output Low Voltage (V_{OL})			-	-	0.4	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data and Clock pulldown resistance			5	-	13	Ω
SMALERT# pulldown resistance			5	-	20	Ω
Input Leakage			-1	-	1	µA
Pin Capacitance		See Note 11	-	-	4	pF

Note: .

11. *Guaranteed by design and not tested in production*
12. *Cold temperature performance is guaranteed via correlation using statistical quality control. Not tested in production*
13. *FOVP, ROVP and RUVP threshold accuracies for VOUT_SCALE_LOOP 1:2 are based on the use of an output divider as specified in section 13.3*
14. *Guaranteed by Bench Characterization at Room Temperature and not tested in production*
15. *Actual output voltage resolution is limited by internal DAC*

8 Pin Strap Resistors Application Information

The TDA38740/25 devices allow pin-strapping functionality to boot up the part with output voltage, current limit, switching frequency, FCCM/DEM mode and address offset parameters to a value determined by pin strap resistors.The pin functionality can be enabled by writing '0' to the registers ilim_docp_override_pin(0x5E[0]), ilim_aocp_override_pin(0x5E[1]), lcf_zero_override_pin(0x5E[2]), vboot_override_pin(0x5E[3]), ton_override_pin(0x5E[4]), fccm_override_pin(0x5E[5]), fovp_override_pin(0x5E[6]), rovp_override_pin(0x5E[7]). The pinstrapping functionality is disabled on TDA38740/725-0000 parts and these parameters are set by PMBus commands. The TDA38740/725-0000 parts have VOUT_COMMAND set to 0V and there will not be any output until the output is set to desired value. The pinstrapping functionality is enabled on TDA38740-0020 and TDA38740-0030 parts. Refer to Section 1 for custom part number information for Pin configurable and Register configurable parts.

The tables and descriptions below detail different parameters that can be set using pin strap resistor.

Table 7 MODE/TON Table

Bin	MODE/TON (kΩ)	Freq (kHz)	MODE
0	SHORT	600	FCCM
1	2.49	1000	
2	3.24	1400	
3	4.02	2000	
4	4.87	1200	DEM
5	5.76	1400	
6	6.81	1800	
7	7.87	2000	
8	9.09	400	
9	10.5	600	
10	12.1	800	
11	14	1000	
12	15.8	400	FCCM
13	17.8	1800	
14	20	1200	
15	FLOAT	800	

When operating in the pin strap resistor mode the switching frequency and the operating mode can be set by connecting a resistor from the MODE/TON pin to GND as per the table above. Switching frequency can be selected from 400 kHz to 2000 kHz in steps of 200 kHz except for 1600 kHz. Mode can be selected to operate the part in Forced Continous Conduction Mode (FCCM) mode or Diode Emulation Mode (DEM).

Table 8 TDA38740/725 Boot Up Voltage and OVP Limits Table for VOUT_SCALE_LOOP 1:1

VBT (kΩ)	BOOT-Up Voltage (V)	Relative OVP/UVP (mV)	Fixed OVP (V)
SHORT	0.4	150	0.8
5.62	0.5	150	1
9.53	0.6	150	1
14	0.7	150	1.2
21	0.8	200	1.2
30.1	0.90	200	1.2
36.5	1	200	1.35
43.2	1.05	200	1.35
51.1	1.1	200	1.35
61.9	1.2	200	1.5
75	1.25	250	1.8
88.7	1.35	250	1.8
105	1.5	300	2.2
127	1.65	300	2.2
147	1.8	300	2.2
FLOAT	2.5	300	2.85

Table 9 Boot Up Voltage and OVP Limits Table for VOUT_SCALE_LOOP 1:2

VBT (kΩ)	BOOT-Up Voltage (V)	Relative OVP/UVP (mV)	Fixed OVP (V)
SHORT	0.8	200	1.6
5.62	1.0	200	1.6
9.53	1.2	200	1.6
14	1.4	300	2.0
21	1.6	300	2.4
30.1	1.8	300	2.4
36.5	2.0	300	2.7
43.2	2.1	300	2.7
51.1	2.2	300	2.7
61.9	2.4	300	3.0
75	2.5	300	3.0
88.7	2.7	300	3.6
105	3.0	300	3.6
127	3.3	300	4.4
147	3.6	300	4.4
FLOAT	5.0	300	5.7

When operating in the pin strap resistor mode, the output voltage can be selected by connecting a resistor from the VBT pin to GND per the table above.

When setting the output voltage using VOUT_COMMAND, the VOUT_SCALE_LOOP of 1:1 should be used for obtaining outputs in the range of 0.25 V to 2.56 V. For obtaining output voltages between 2.56 V and 5.12 V, the VOUT_SCALE_LOOP of 1:2 should be used. When operating in VOUT_SCALE_LOOP 1:1 mode the full output voltage should be fed back to the VOSENP pin as shown in Figure 3. When operating in VOUT_SCALE_LOOP 1:2 mode, half of the output voltage is fed back to the VOSENP Pin by using a resistor divider as shown in Figure 4. The VBT pin

can be used to set the output voltages in the range of 0.4 V to 2.5 V in VOUT_SCALE_LOOP 1:1 and from 0.8 V to 5 V in VOUT_SCALE_LOOP 1:2.

Table 10 TDA38740 OCP and Loop Compensation Filer Zero selection

R_{ILIM}(kΩ)	Typical OCP(A)	Internal Loop-Compensation-Filter-Zero Register (LCF)	Default LCF zero capacitor value (pF), Note 16
SHORT	15	LCF 0	1
3.32	60	LCF 4	8
6.98	20	LCF 2	4
11	10	LCF 0	1
15.4	15	LCF 1	2
21	20	LCF 1	2
26.1	25	LCF 2	4
31.6	30	LCF 2	4
43.2	40	LCF 3	6
51.1	50	LCF 4	8
64.9	25	LCF 1	2
78.7	60	LCF 3	6
95.3	40	LCF 2	4
113	50	LCF 3	6
133	10	LCF 1	2
FLOAT	30	LCF 3	6

Table 11 TDA38725 OCP and Internal Phase margin Zero selection

R_{ILIM}(kΩ)	Typical OCP(A)	Internal Loop-Compensation-Filter-Zero Register (LCF)	Default LCF zero capacitor value (pF), Note 16
SHORT	15	LCF 0	1
3.32	15	LCF 4	8
6.98	20	LCF 2	4
11	10	LCF 0	1
15.4	15	LCF 1	2
21	20	LCF 1	2
26.1	25	LCF 2	4
31.6	10	LCF 2	4
43.2	15	LCF 3	6
51.1	20	LCF 4	8
64.9	25	LCF 1	2
78.7	10	LCF 3	6
95.3	15	LCF 2	4
113	20	LCF 3	6
133	10	LCF 1	2

R_{ILIM}(kΩ)	Typical OCP(A)	Internal Loop-Compensation-Filter-Zero Register (LCF)	Default LCF zero capacitor value (pF), Note 16
FLOAT	25	LCF 3	6

When operating in the pin strap resistor mode, the OCP limit can be selected by connecting a resistor from the ILIM pin to GND per the table above. Loop Compensation Filter (LCF) Zero selection is also available on ILIM pin, however it does not affect the OCP operation and is part of the control loop tuning. This capacitance is built in within the IC and can be selected between 1pF and 8pF by appropriate selection of the ILIM resistor. This provides some flexibility to set the Loop Compensation Filter Zero using ILIM pin strap resistors. However, default selection of the capacitance value is limited and does not allow selection of all 8 possible capacitance values from 1pF to 8pF. If the desired performance could not be achieved with default LCF zero values available through the ILIM pin, the capacitance value can be selected from 1pF to 8pF in increments of 1pF through the register loop_compensation_filter_zero_0, 0x64[14:12] through PMBus. Please refer to the App note AN_2204_PL12_2204_183614 for more details on this register.

Table 12 SM_ADDR/PROG Pin with the consecutive images starting from Config 0 at location 0

Resistor to GND (kΩ)	SM_ADDR function: Offset selection from the base address	PROG function: Config selection (For single -image Config)	PROG pin: Config selection (For Multi-image Config)	Programmability for single and multi-image config file
SHORT	0	Most recently programmed CONFIG	CONFIG0	Please refer to section 13.2 for single image and multi-image programming details
5.62	1		CONFIG1	
9.53	2		CONFIG2	
14	3		CONFIG3	
21	4		CONFIG4	
30.1	5		Not supported	
36.5	6			
43.2	7			
51.1	8			
61.9	9			
75	10			
88.7	11			
105	12			
127	13			
147	14			
FLOAT	15			

A resistor to ground on this pin sets a fixed slave address offset for both I2C and PMBus interface. Apart from this it selects a configuration from the 5 possible config files of a multi image config file in the OTP during power-up. As shown in Table 12 above, the SM_ADDR pin selects an offset based on the resistor connected to the SM_ADDR/PROG pin. The PROG functionality is used to select one of the 5 images of a multi-image config file to load from the OTP.

The pin programming limits the address offset adjust capability via the pin to a maximum of 4 as per the programming capability available to the customer. For single image applications, the most recently programmed CONFIG image will be loaded from the OTP irrespective of the pin programmed address offset. For multi-image application, the table above shows the CONFIG image that will be loaded from the OTP based on the pin

programmed address offset. For any application which needs more than 5 images or greater than 4h offset to the base address, please contact Infineon.

The address offset from the pin can be disabled by setting register i2c_disable_addr_offset(0x42[6]) to 1. In this mode the effective address is determined by the register value in i2c_device_addr(0x40[6:0]) and pmb_device_addr(0x40[6:0]). This is helpful when address offset need to be 0x5 or higher which is otherwise not possible with multi-image config application when i2c_disable_addr_offset(0x42[6]) is set to 0.

For more information on programming single and multi-image config file, please refer to Section 13.2.

Note:

16. *The default LCF value can be changed using Registers 0x64[14:12], 0x62[2:0], 0x62[6:4], 0x62[10:8], 0x62[14:12] for LCF 0, LCF 1, LCF 2, LCF 3, LCF 4 respectively*

9 Typical Efficiency and Power Loss Curves

9.1 $PV_{in} = V_{in} = 12$ V, Vout = 1.2V, $F_{sw} = 600$kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid lines indicate efficiency and dashed lines show power loss at 600 kHz.

Table 13 Inductors for $PV_{in}=V_{in}=12$ V, $F_s = 600$ kHz

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm)
1.2	150	L101247A-100L	0.125	10 x 6.4 x 12
3.3	470	L101158A-R47MHF	0.81	10 x 7 x 10

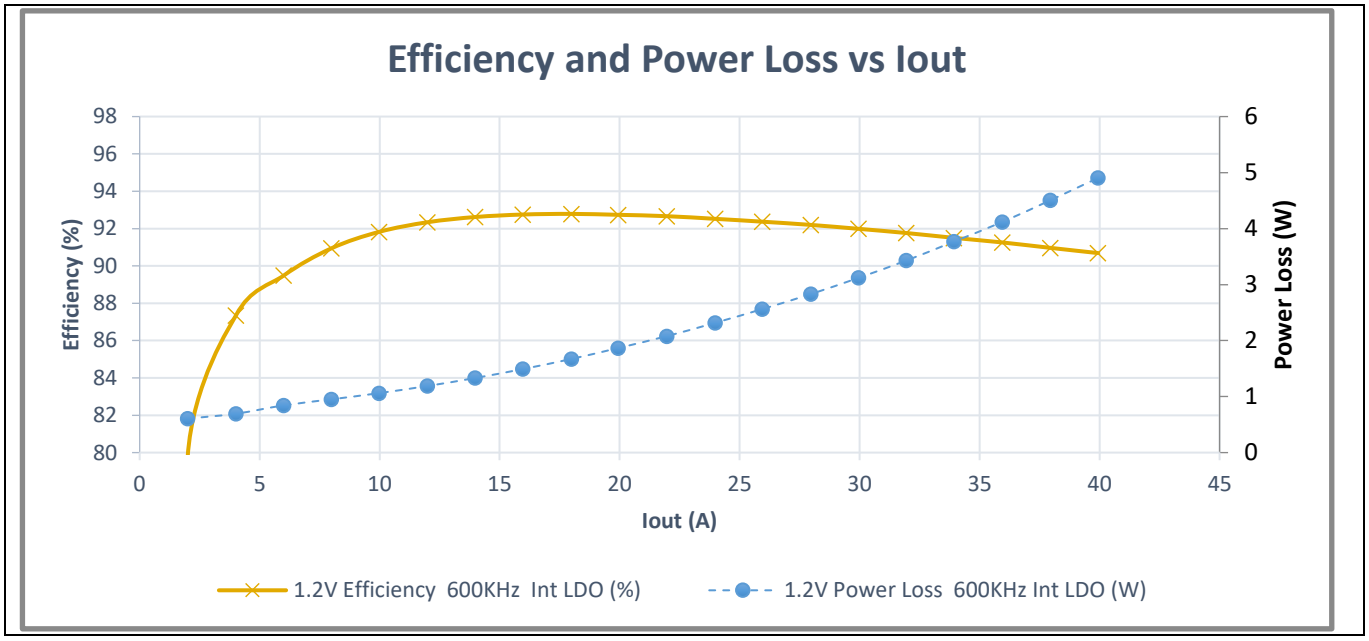


Figure 5 Typical efficiency and power loss curves, $PV_{in} = V_{in} = 12$ V, Vout = 1.2 V, $F_{sw} = 600$ kHz

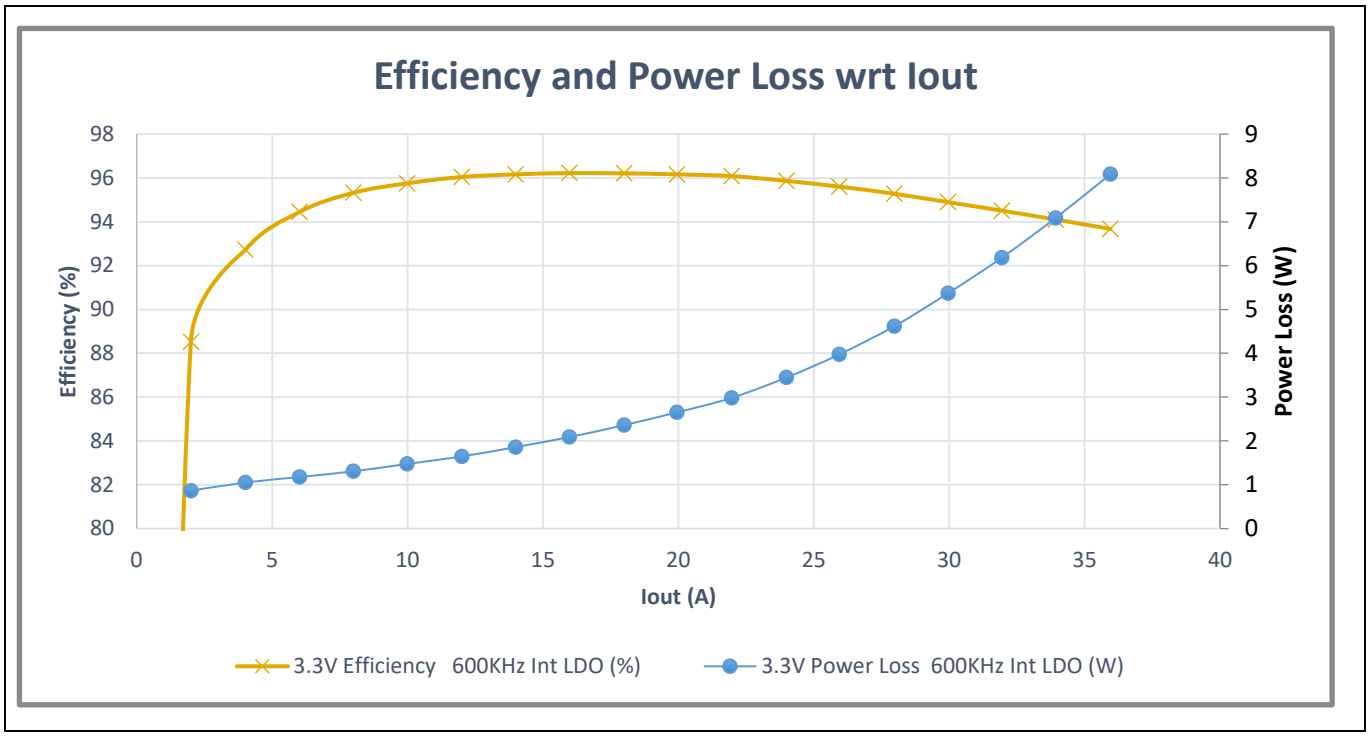


Figure 6 Typical efficiency and power loss curves, PV_{in} = V_{in} = 12 V, Vout = 3.3 V, F_{sw} = 600 kHz

9.2 PV_{in} = V_{in} = 12 V, F_{sw} = 800 kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid line indicate Efficiency and dashed lines are showing power loss at 800 kHz.

Table 14 Inductors for PV_{in}=V_{in}=12 V, F_{sw} = 800 kHz

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm^3)
1.2	150	L101247A-150L	0.125	10 x 6.4 x 12
3.3	470	L101158A-R47MHF	0.81	10 x 7 x 10

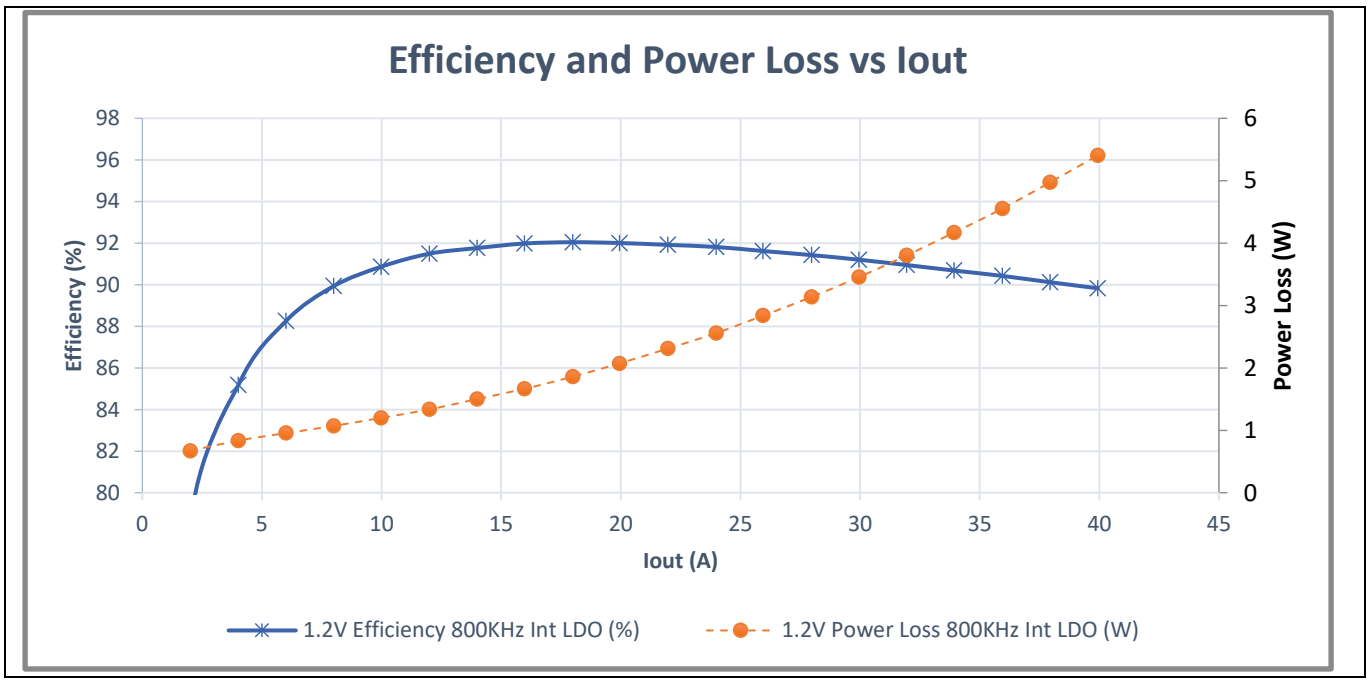


Figure 7 Typical efficiency and power loss curves, PV_{in} = V_{in} = 12 V, Vout = 1.2 V, F_{sw} = 800 kHz

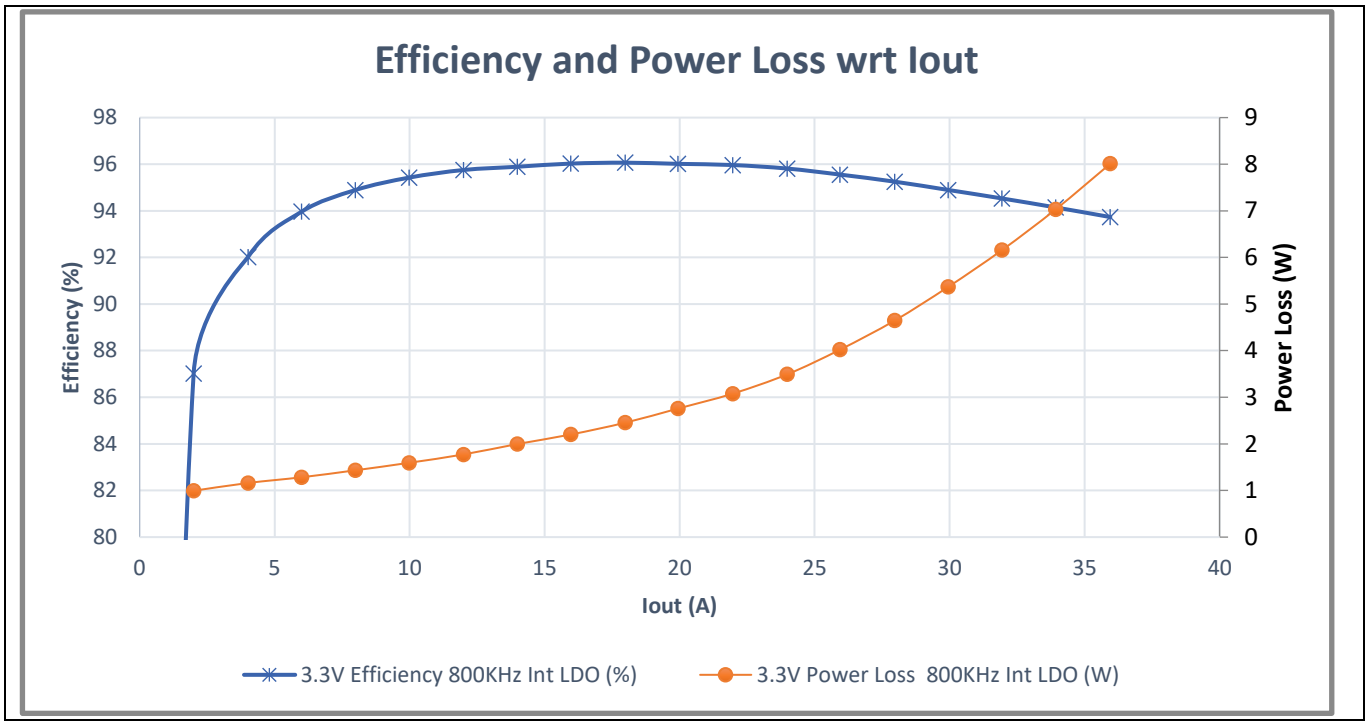


Figure 8 Typical efficiency and power loss curves, PV_{in} = V_{in} = 12 V, Vout = 3.3 V, F_{sw} = 800 kHz

9.3 PV_{in} = V_{in} = 12 V, F_{sw} = 1000 kHz

The test for efficiency was done at 0 LFM and the driver losses are included in the efficiency numbers. Solid lines indicate efficiency and dashed lines show power loss at 1000 kHz.

Table 15 Inductors for PV_{in}=V_{in}=12 V, F_{sw} = 1000 kHz

Vout (V)	Lout (nH)	P/N	DCR (mΩ)	Size (mm^3)
1.2	150	L101247A-150L	0.125	10 x 6.4 x 12
3.3	470	L101158A-R47MHF	0.81	10 x 7 x 10

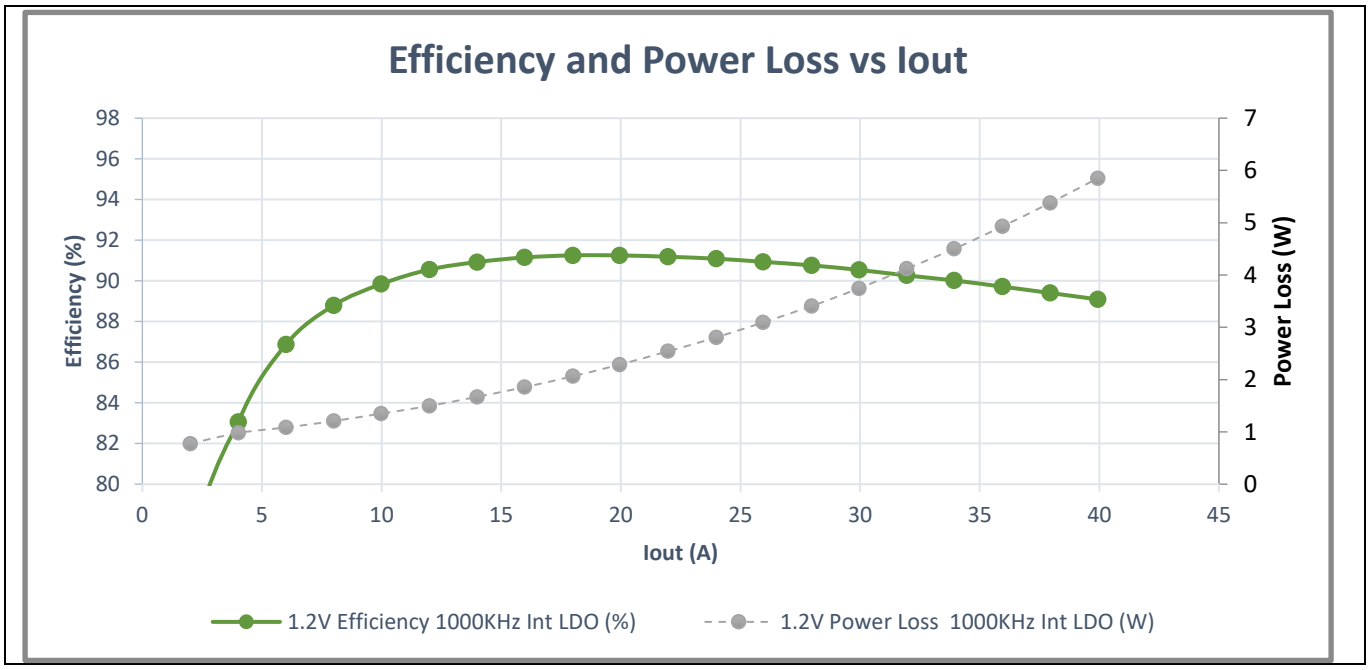


Figure 9 Typical efficiency and power loss curves, PV_{in} = V_{in} = 12 V, Vout =1.2 V, F_{sw} = 1000 kHz

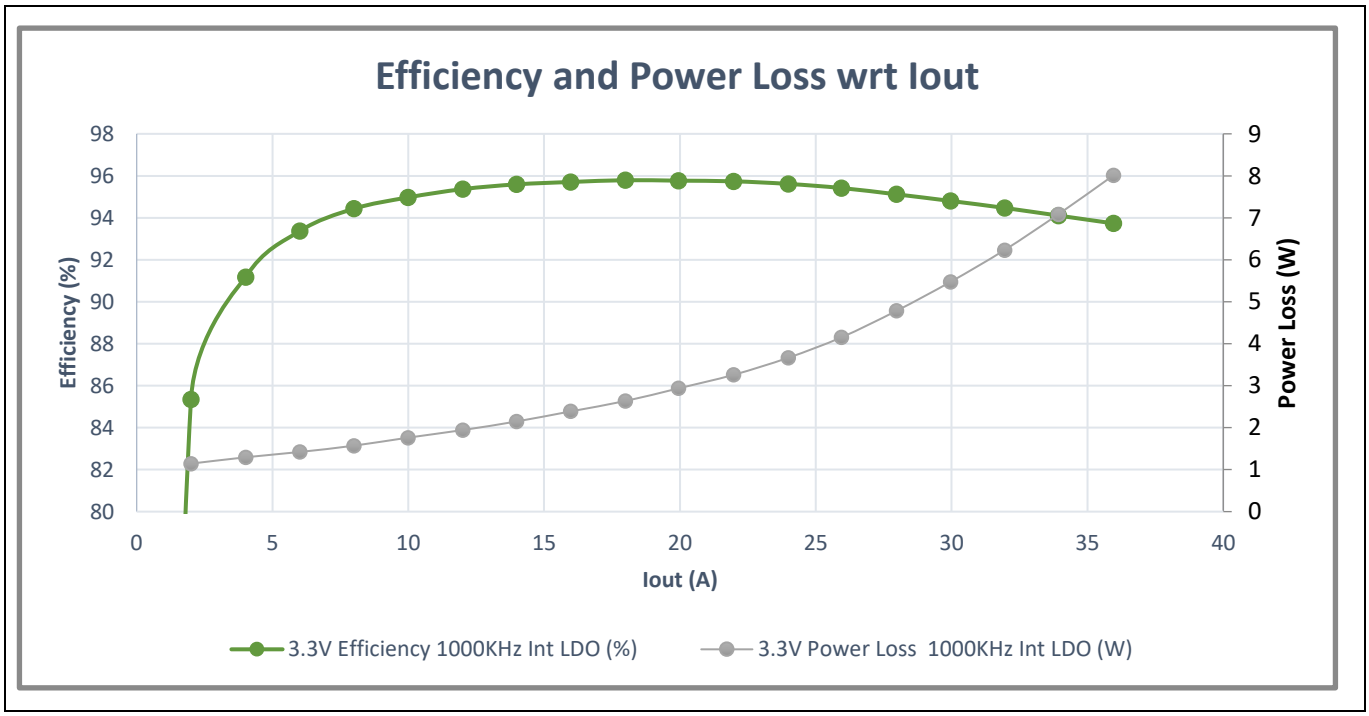


Figure 10 Typical efficiency and power loss curves, PV_{in} = V_{in} = 12 V, Vout =3.3 V, F_{sw} = 1000 kHz

10 Thermal De-rating curves

Measurement is done on Evaluation board DB356. The PCB is an 8-layer board with 2 oz Copper for top and bottom layers and 2 oz Copper for the inner layers, FR4 material, size 5.25”x4.1”.

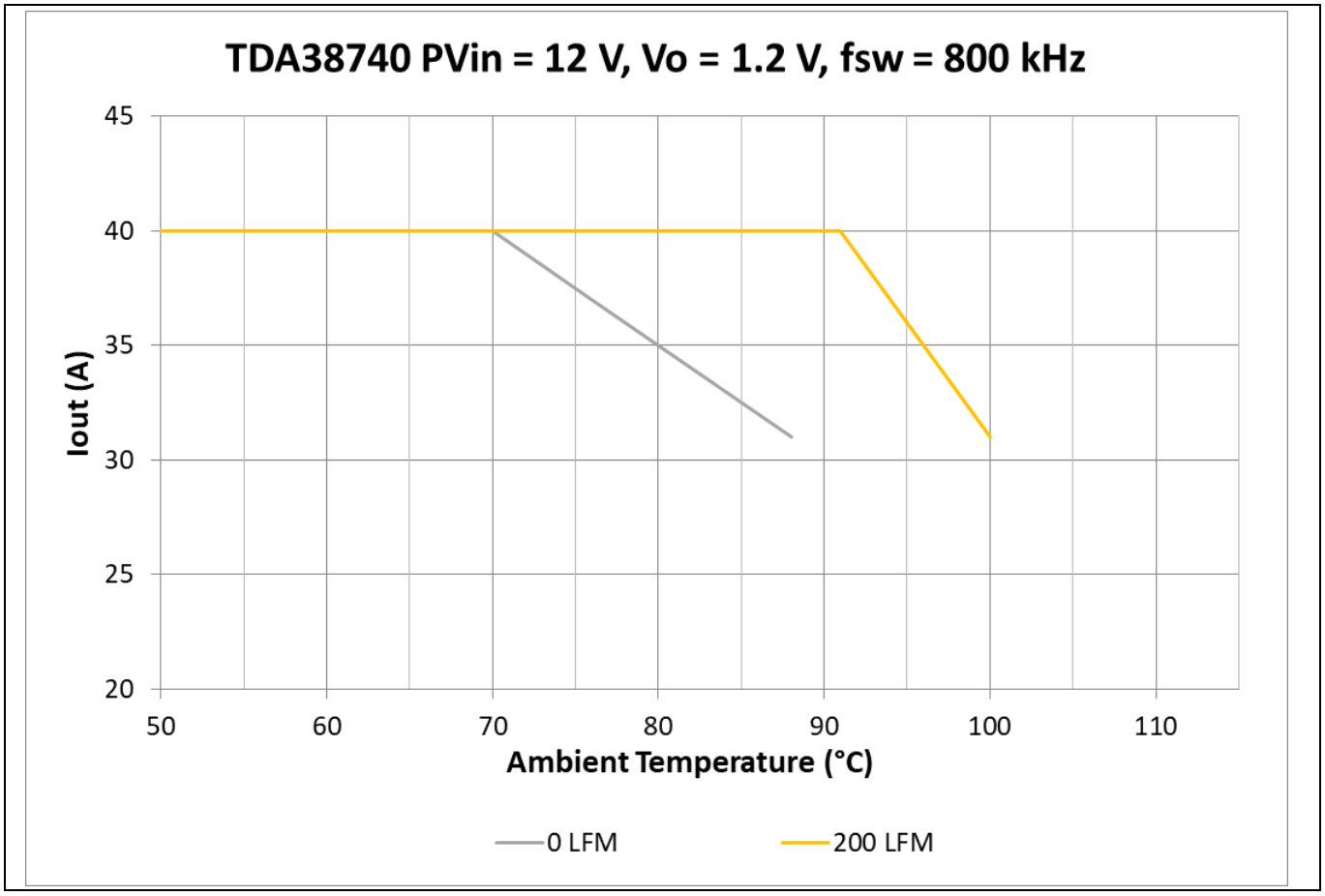


Figure 11 Thermal de-rating curves, PV_{in} = 12 V, Vout = 1.2 V, f_{sw} = 800 kHz, VCC = Internal LDO

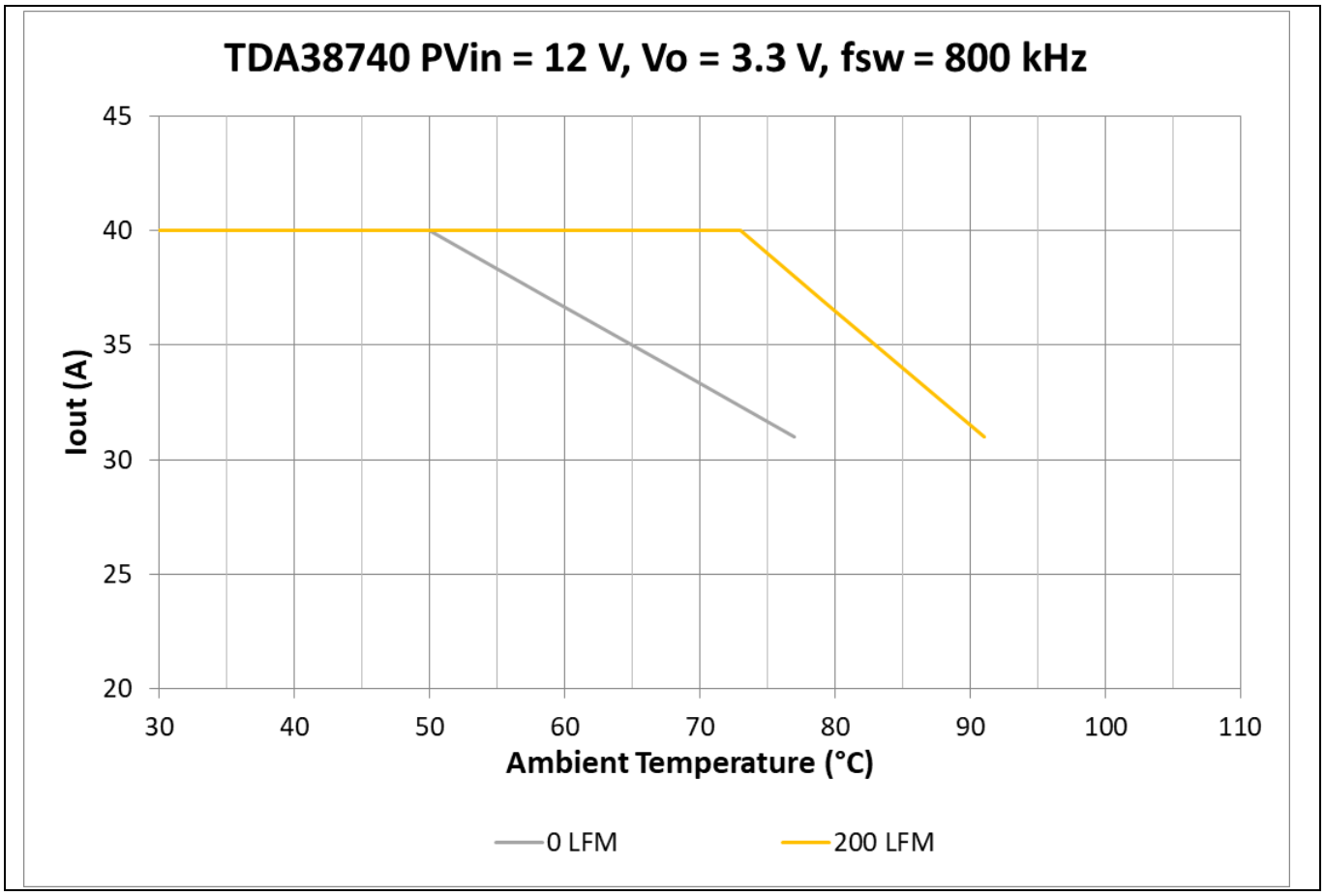


Figure 12 Thermal de-rating curves, PV_{in} = 12 V, Vout = 3.3 V, f_{sw} = 800 kHz, VCC = Internal LDO

11 $R_{DS(on)}$ of MOSFET Over Temperature

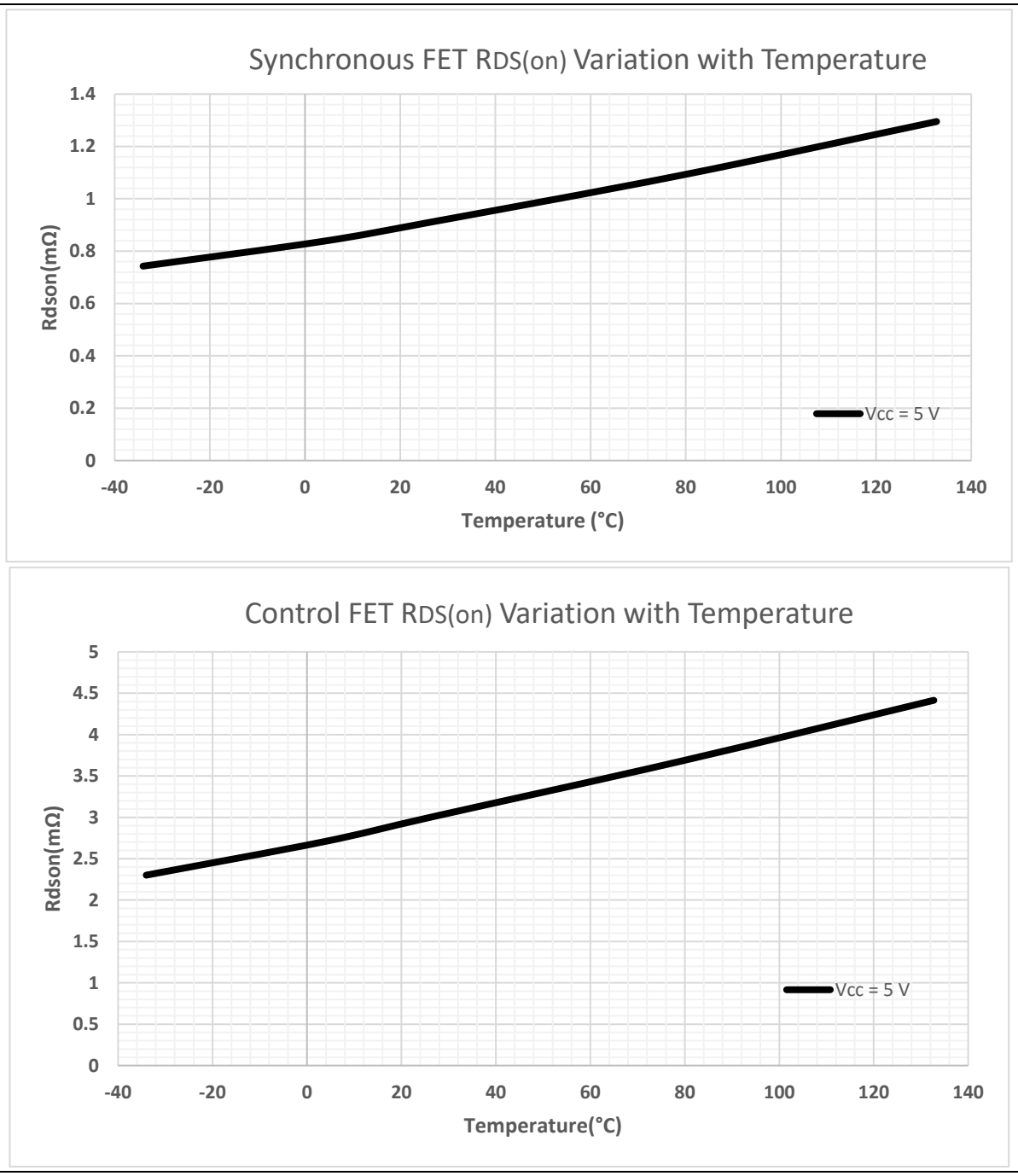


Figure 13 RDS(on) of MOSFETs over Junction Temperature

12 Typical operating characteristics (-40 °C ≤ T_j ≤ +125 °C)

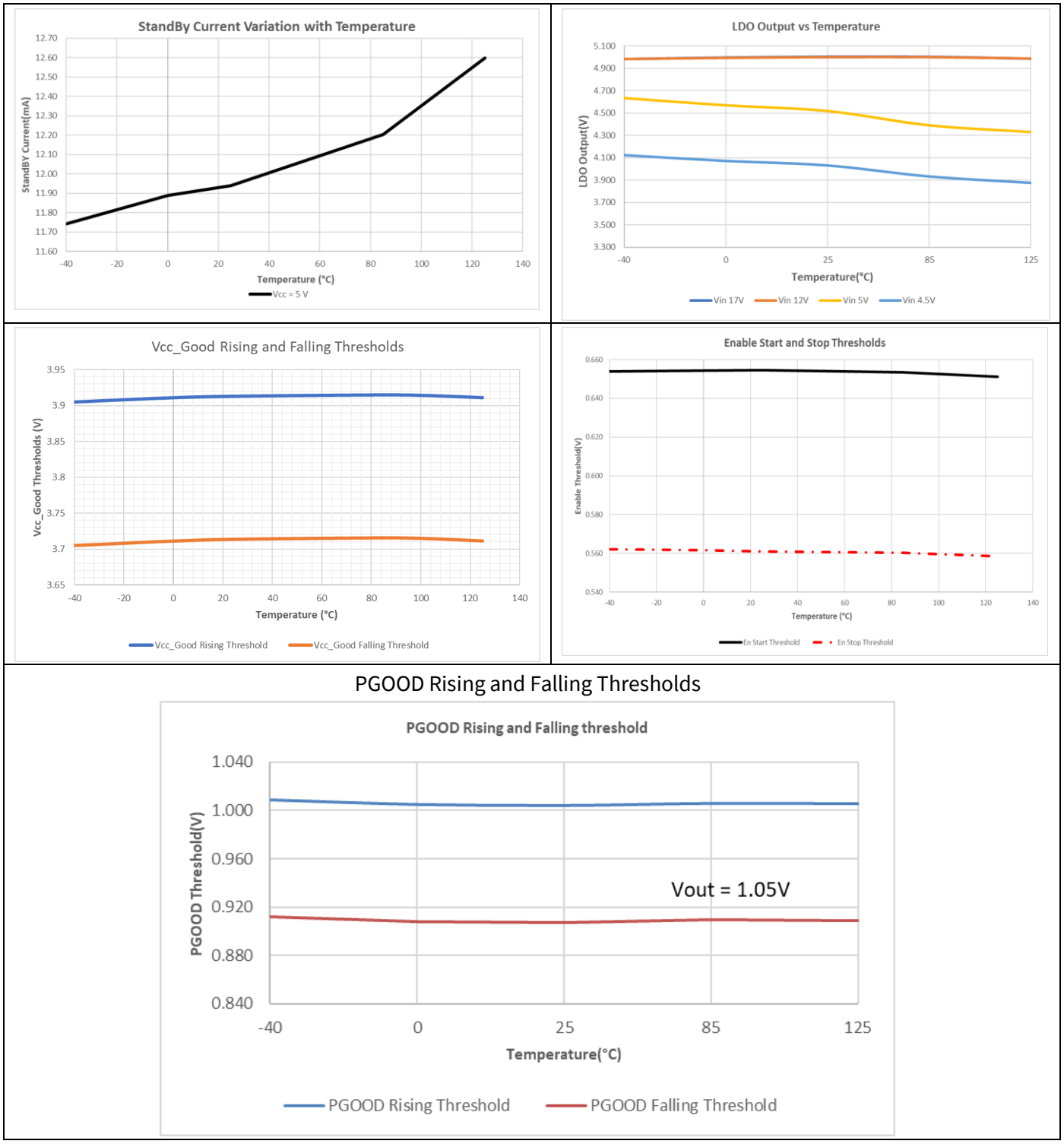


Figure 14 Typical operating characteristics (set 1 of 2)

Typical operating characteristics (-40 C ≤ Tj ≤ +125 C)

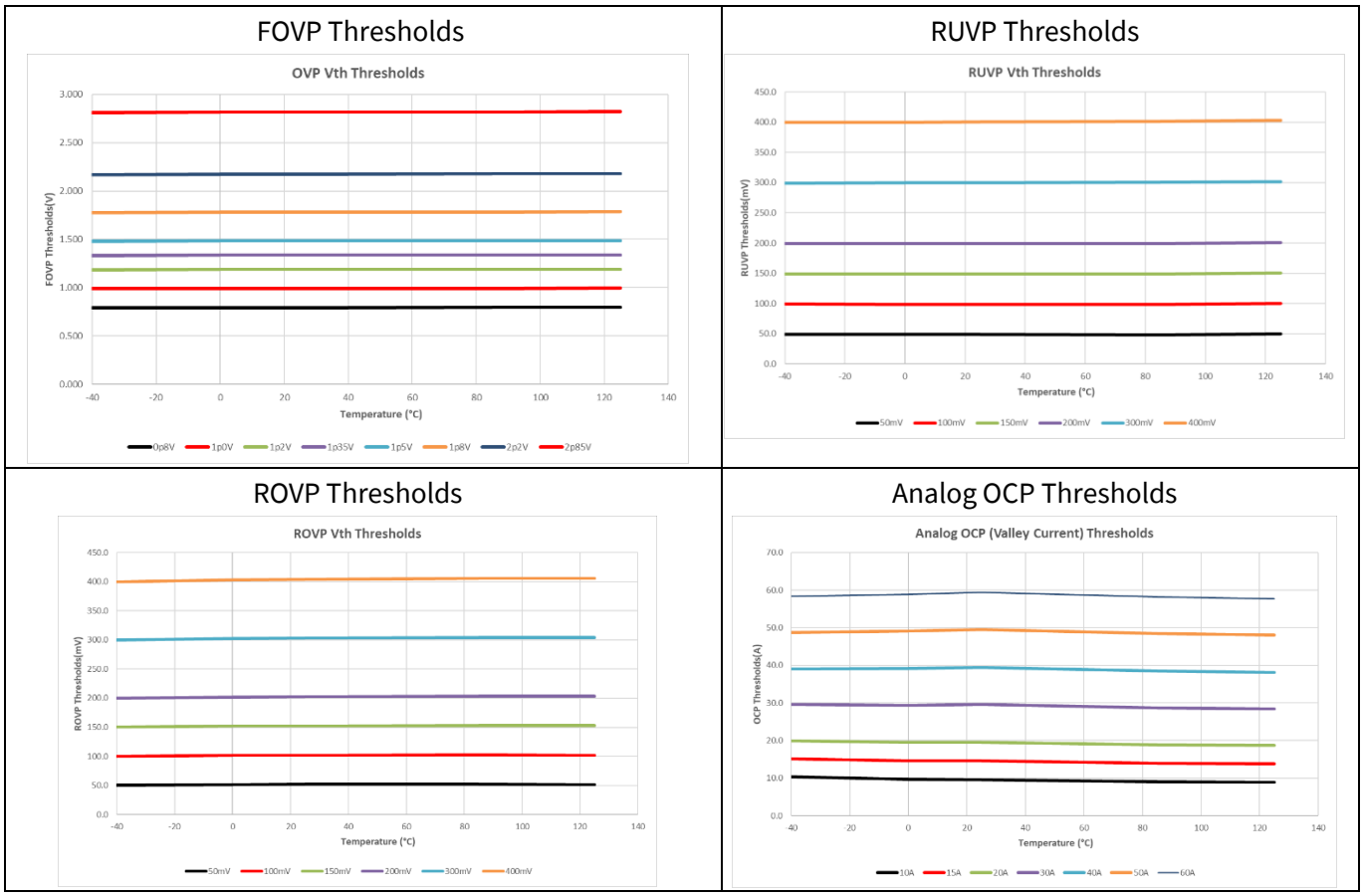


Figure 15 Typical operating characteristics (set 2 of 2)

13 General Description

The TDA38740/725 is an easy-to-use, fully integrated, and highly efficient dc-dc regulator optimized to convert a 12 V input supply to a voltage level required by high-performance microprocessors, DDR memory, housekeeping supplies, base stations, etc. The onboard PWM controller and OptiMOS™ FETs with integrated bootstrap diode makes TDA38740/725 a small footprint solution, providing highly efficient power delivery. A fast Constant On-Time (COT) control scheme simplifies design efforts and achieves fast control response. The device configuration can be easily defined using Infineon's XDP Designer GUI and is stored in the on-chip memory.

13.1 PMBUS Operating Mode

The TDA38740/725 can be used in PMBUS mode. In PMBUS mode, the output voltage is controlled by the PMBUS VOUT_COMMAND command. The VOUT_MODE resolution can be set to 0.625 mV/lsb, 0.977 mV/lsb, 1.953 mV/lsb, or 3.906 mV/lsb. The output DAC resolution is 1.25 mV/lsb. The resolution is user-programmable via a configuration file.

See Table 18 for a complete list of all supported PMBUS commands. Please refer to App Note AN_2203_PL12_2204_184108 for more details.

13.2 Multiple Time Programming Memory (MTP)

The multiple time programming memory (MTP) stores the device configuration. At power-up, MTP contents are transferred to operating registers for access during device operation. MTP allows customization during both design and high-volume manufacturing. MTP integrity is verified by Cyclic Redundancy Check (CRC) validation on each power up. The controller will not start up in the event of a CRC error.

The TDA38740/725 allows up to 5 unique configurations, to configure basic device parameters such as frequency, fault operation characteristics, and boot voltage. This represents a significant size and component saving compared to traditional analog methods. In addition, the TDA38740/725 also allows the loading of multi-image (up to 5 consecutive) configuration files and automatic selection of a unique file after power-up based on the resistor value at the SM-ADDR/PROG pin and the pointer (0x00[13:8]). There are registers available in the CNFG section of the register map which allow the user the capability to set the starting point for a multi-image (register 0x0000[13:8]) and the number of images as part of the multi-image config file (register 0x0000[3:0]).

TDA38740/725 can be programmed successfully for an application up to 16 times for a single image config file. This should be done during offline programming or by using an Infineon programming solution. Additionally, the TDA38740 also allows loading a maximum of 5 config files for the multi-image designs. For any application which needs multi-image configuration, Infineon will establish custom part numbers and program at an Infineon production facility. After soldering parts with a 5-image multi-image, it may be programmed two more times with a single image.

The user still has access to all the possible I2C slave addresses by setting the address through address registers. This requires the address offset capability of the SM_ADDR/PROG pin to be disabled by setting the bit 0x42[6] to 1. Thus, the base address register 0x40[14:8] for I2C and 0x40[6:0] for PMBus will represent the effective slave address for the device. In this case, the SM_ADDR/PROG effectively becomes just the PROG pin used for selecting the correct config file for an application. For example, for an effective 7-bit I2C address of 14h the register 0x40[14:8] should be set to 14h. The second method for choosing the effective slave address is using the base address in register 0x40 and adding the offset selected by the SM_ADDR/PROG pin. The pin configuration limits the offset capability available for an application, as shown in Table 12.

13.3 Voltage Sense

In applications that require high Vout set point accuracy with vout_scale_loop of 1:2 where a resistor divider is used to feedback the output voltage, a resistor R3 may be connected in parallel to R1 of the divider as shown in Figure 4. Value of resistor R3 is calcualted as follows:

$$\text{Rtop} = \frac{\text{Vo}-\text{Vfb}}{\left(\frac{\text{Vfb}}{\text{R2}}+\frac{\text{Vfb}}{13570}-\frac{1.2}{20000}\right)}$$

Where
Rtop= Effective value of R1 and R3 in parallel
Vo=Target Output Voltage
Vfb=Vo/2
R1, R2=499 Ohms (recommended)

$$\text{R3} = \frac{\text{R1xRtop}}{\text{R1}-\text{Rtop}}$$

For given feedback resistor values Vout is calculated as follows:

$$\text{Vout} = \text{Vfb}\left(1+\frac{\text{Rtop}}{\text{R2}}+\frac{\text{Rtop}}{13570}\right)-1.2\text{x}\frac{\text{Rtop}}{20000}$$

Suggested values of R1 anf R3 are as follows:

Target Vout (V)	R1 (Ohms)	R3 (kOhms)
2.5	499	39.2
3.3	499	26.7
5	499	20

13.4 I2C & PMBus Interface

An I2C or PMBus interface is used to communicate with the TDA38740/725. This two-wire serial interface consists of clock and data signals and operates as fast as 1 MHz. The bus provides read & write access to the internal registers for configuration and for monitoring of operating parameters. The bus is also used to program on-chip non-volatile memory (MTP) to store operating parameters.

To ensure operation with multiple devices on the bus, a base address for TDA38740/25 is programmed into the MTP. The unique slave address for the device is a combination of the base address in the device register plus the offset generated by the SM_ADDR/PROG pin (depending on the resistor value connected to the pin). Alternatively, this can be achieved by programming the effective I2C address into the base address register and disabling the SM_ADDR/PROG pin offset functionality via bit 0x42[6] in the USER section.

To protect customer configuration and information, the I2C and PMBus interface can be configured for either limited access or locked with a 16-bit software password. Limited access includes both write and read protection options. In addition, there is a telemetry-only mode which only allows reads from the telemetry registers.

Refer to the PMBus Command Codes in Table 18 for more information. One can access the non-PMBus registers (I2C register) via the MFR_REG_ACCESS(D0h) PMBus Command. Through the PMBus, it is possible to access configuration registers and the PMBus registers in the device. It has a 7-bit register to set the base PMBus address 0x40[6:0] of the device. Setting this address to zero disables the PMBus interface. All registers at this address are protected by the i2c_pmb_addr_lock register 0xD4[2]. Please refer to the App note AN_2204_PL12_2204_183614 for more information on the register map.

13.5 Infineon XDP Designer GUI

The Infineon XDP Designer GUI provides the designer with a comprehensive design environment that includes input settings, output settings, telemetry and PMBus interface. With these tools, a designer can monitor and set system configuration settings for fault thresholds and output behavior in real time. The XDP Designer GUI allows real-time design monitoring of key parameters such as output current and power, input current and power, efficiency, temperature, and faults. Figure 16 shows the GUI home screen with the available parameter windows.

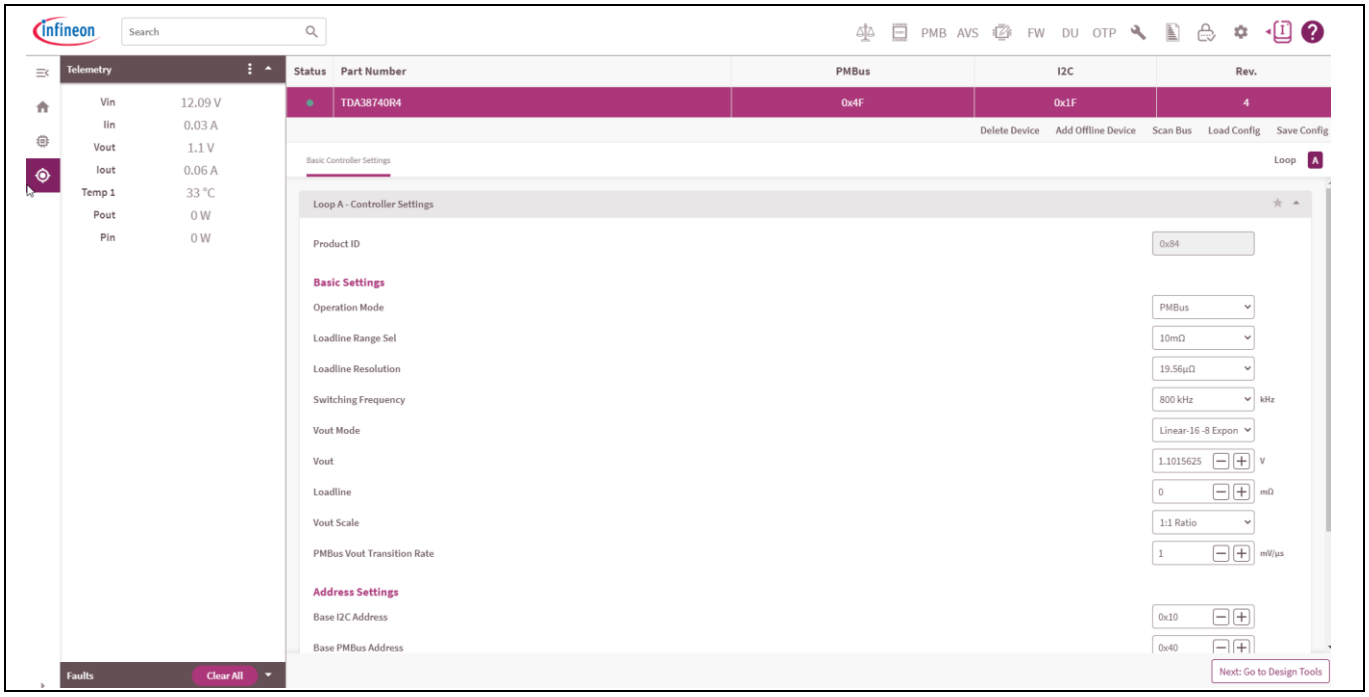


Figure 16 XDP Designer GUI home screen.

13.6 Programming

Once a design is complete, the XDP Designer GUI produces a complete configuration file. These configurations files can be saved and loaded. Infineon does not recommend loading a new config file and programming the device while the device is operating to produce an output voltage. Please refer to the programming guide AN_2204_PL12_2204_185449 for more details.

13.7 Real-time Monitoring

The TDA38740/725 can be accessed through the use of PMBus Command codes (described in Table 18) to read the real-time status of the power supply (dc-dc converter) including input and output voltages, input and output currents, input and output power and temperature.

14 Theory of Operation

14.1 Start up Configuration

TDA38740 operation is controlled by OTP configuration stored in NVM, then loaded into working registers during initialization.

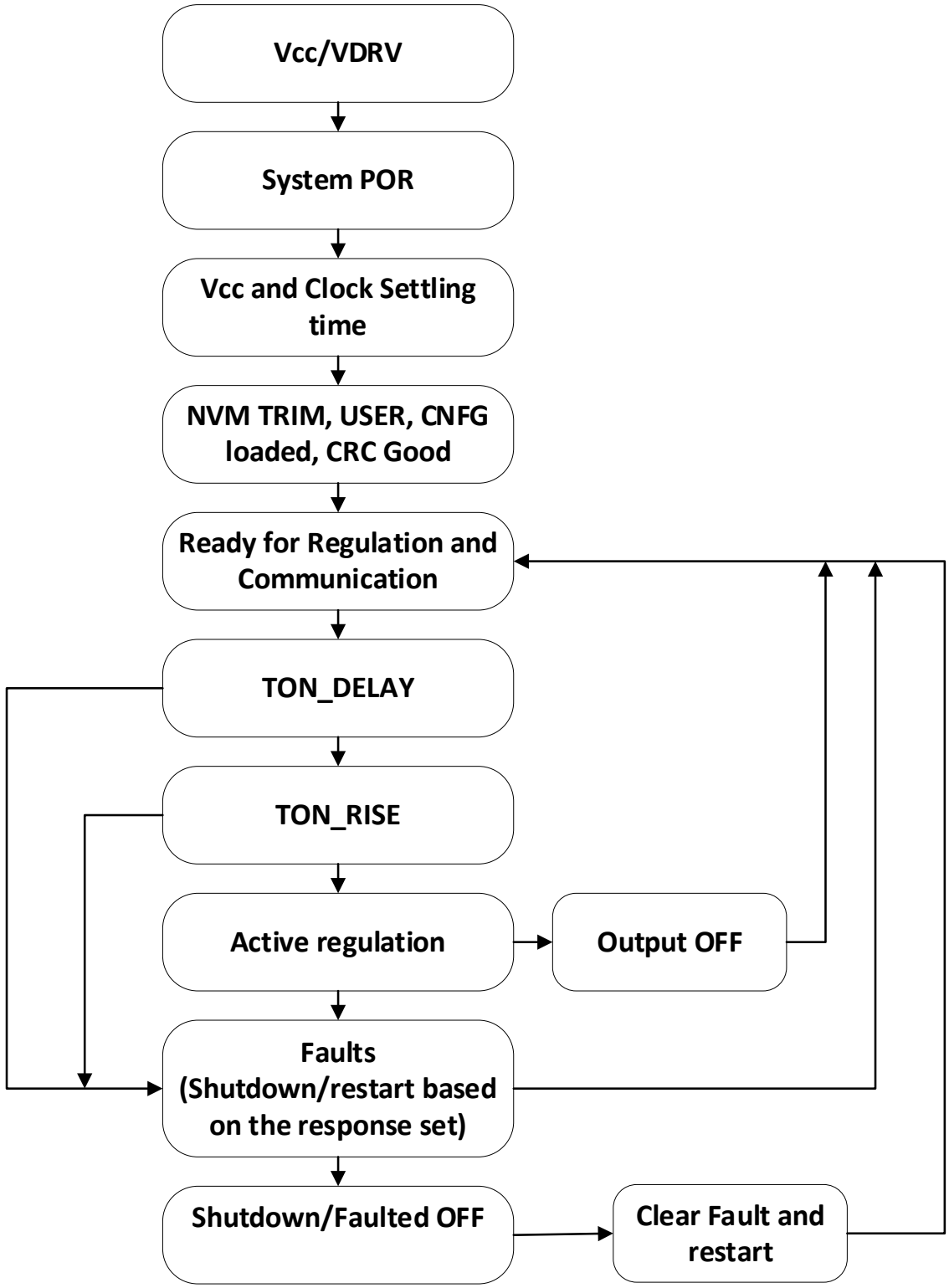


Figure 17 State Machine

14.1.1 Power On Reset and Configuration

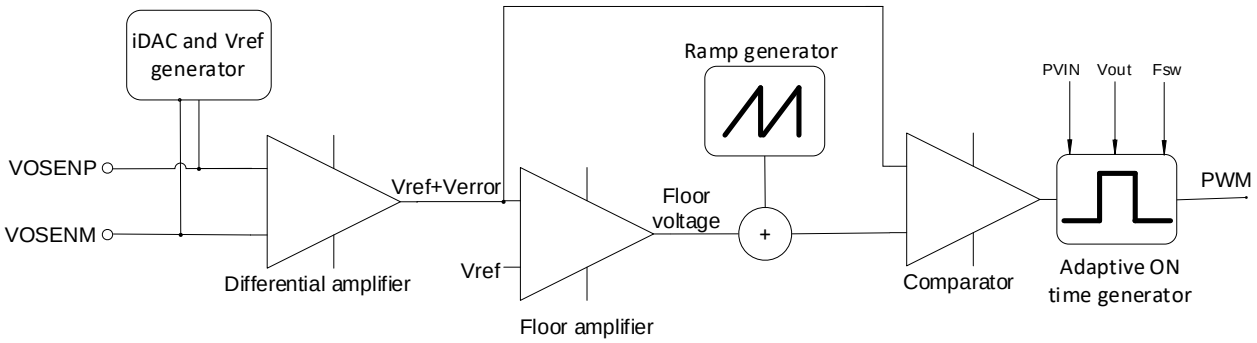
The on-chip regulator operates from the Vcc/VDRV and generates an internal +1.2 V voltage. TDA38740/25 operation is initialized by an internal threshold-based power-on reset circuit. To ensure no sensitive analog measurements is executed prior to Vcc/VDRV supply is settled, the controller provides a delay which extends the “System POR” state between power-on reset and entering the NVM Load state. This delay is used to ensure internal analog circuitry settles before making any precision measurements. After this, Trim and Config images are loaded from NVM to working registers. While waiting for the Trims to take effect, current sources are enabled at all pins that have external resistors (ILIM, SM_ADDR, VBT, TON/MODE). The resulting voltages are read through the low-speed ADC and latched. If Trim and Config CRC matches, User configuration is loaded from NVM to the working registers CRC check is carried out to validate the data in these registers. If the calculated CRC does not match the CRC stored in the NVM, CRC error is flagged and next sequences in ther start up are terminated. If there is a CRC match, the part continues with the start up sequence. The device starts switching once part is ready for regulation and communication and enable signal is pulled high. When the contents of the NVM are being loaded into the working registers the PWM outputs are held in high impedance (Hi-Z) state.

14.1.2 TON_DELAY and TON_RISE (Soft-start)

Once the startup conditions are satisfied, the controller will wait for a programmable period of time specified by TON_DELAY before ramping up the output voltage. Prior to entering the active regulation state, the controller performs a controlled, monotonic ramp of the voltage output based on time specified by TON_RISE. This acts as a Soft-Start and is performed by actively regulating the output voltage while digitally ramping up a reference voltage to its final target value.

14.1.3 Active Regulation

During active regulation, the output voltage is applied as a feedback voltage alongwith Vref to a differential amplifier. Vref is proporatinal to the set Vout. The error voltage produced by differential amplifier is added to the Vref and fed to a floor amplifier. The difference between this input and Vref is amplified by floor amplifier to generate a floor voltage. The floor amplifier helps improve the transient response and Vout accuracy. Floor voltage and the ramp signal are added together and applied to the comparator and compared against error voltage. The resultant output is fed to Adaptive ON time generator. This block generates PWM signal of pseudo constant frequency. The Adaptive ON Time generator turns the PWM ON for a fixed duration based on the PVIN, Vout and Fsw. The PWM OFF time is determined by the set Fsw and output load. The output is regulated at the set level until the output is commanded OFF, Fault occurs or POR is deasserted.



14.1.4 Shutdown

The shut-down state can be entered from either soft-start or active regulation states through user intervention such as Enable being pulled low or through a detected fault including OTP, OCP, UVP, OVP, VIN fault etc. The output may be set to shutdown after a delay specified by TOFF_DELAY and at a ramp down rate specified by

TOFF_FALL. Alternatively, the output may be shutdown as fast as possible by stopping the switching. The response to Enable being pulled low is determine by the settings in ON_OFF_CONFIG register. In the event of shutdown due to fault, the part will execute a fault response based on the fault response set in the configuration of the part.

14.2 Start up Sequence

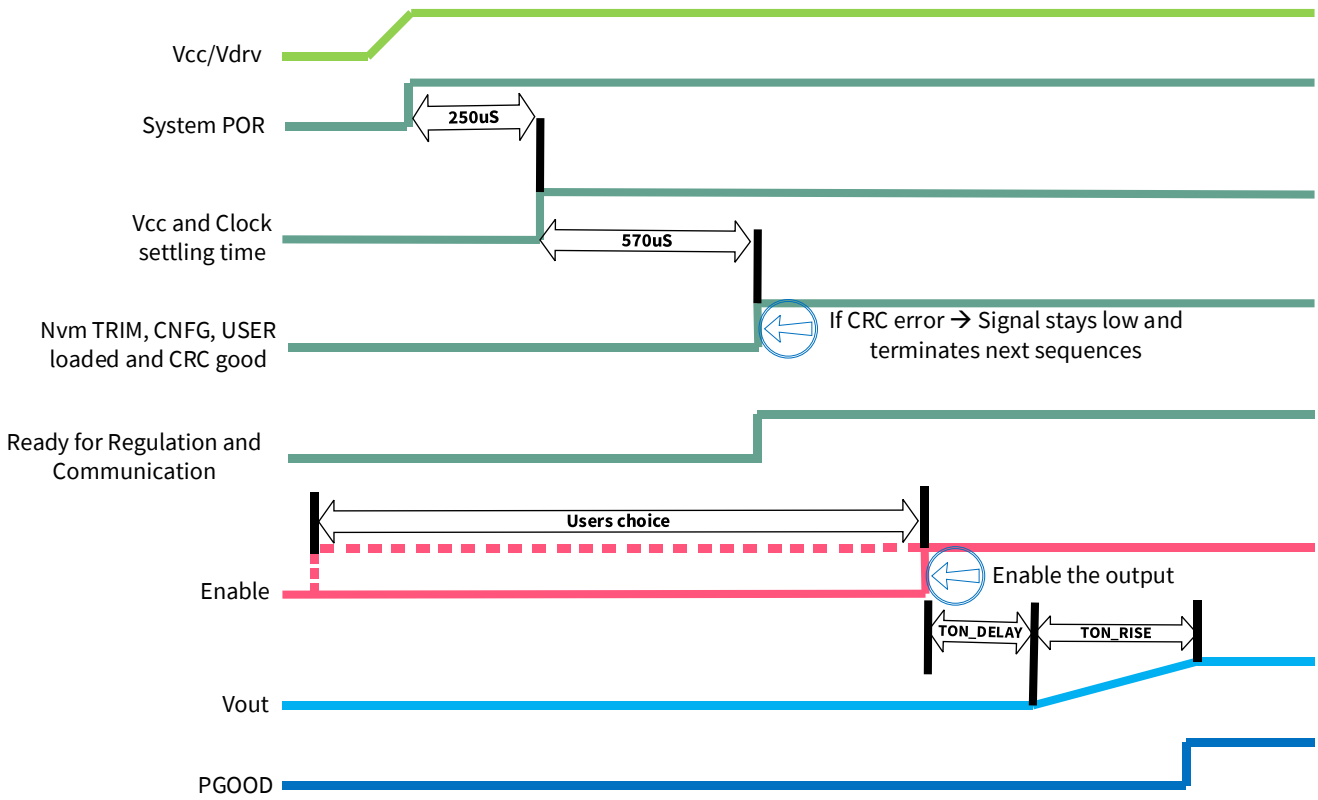


Figure 18 Start up Sequence

14.3 Pre-bias start-up

The TDA38740/725 is able to start up into a pre-charged output without causing oscillations and disturbances of the output voltage upto 0.5 V prebias level.

Prebias operation requirements are:

- The “power down analog circuit when the output is not enabled” feature should be disabled (set register 0x6C value to 0xF240)
- Based on whether Vcc is supplied externally or an internal LDO is used, the required power-up sequences are shown in Figure below.

For any application needs with prebias level > 0.5 V please contact Infineon.

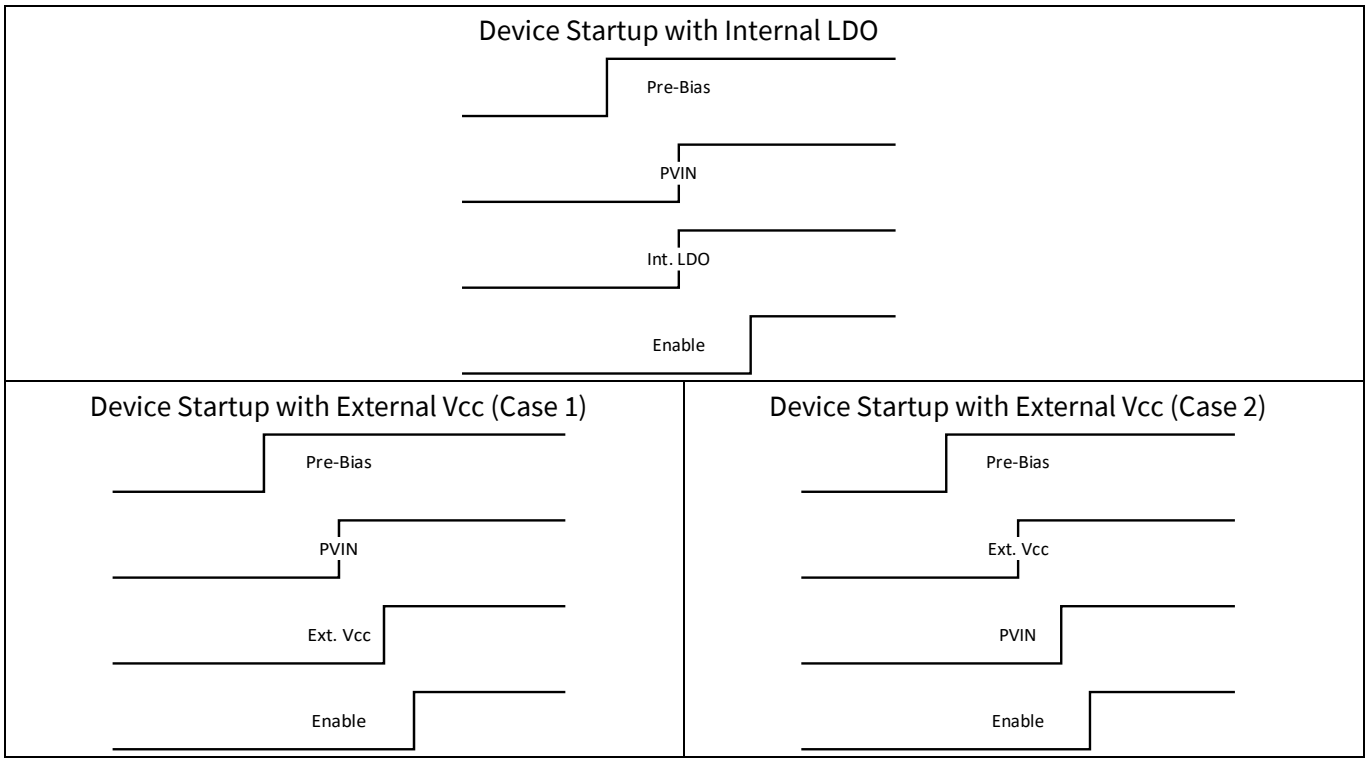


Figure 19 Device power-up sequence.

14.4 Internal Low-Droput (LDO) Regulator

The TDA38740/725 has an integrated low-dropout LDO regulator to provide the bias voltage for internal circuitry. VIN pin is the input for the LDO. When the VCC voltage rises above the VCC_UVLO_Start threshold and the EN voltage is above the Enable_UVLO_Start threshold, the soft-start sequence starts. When using the internal LDO for single rail operation, the VIN pin should be connected to the PVIN pin. To save power losses on the LDO, an external bias voltage can be used by connecting the VIN pin to the VCC/LDO pin. All generic part numbers listed in Table 1 have this LDO enabled. Figure 20 illustrates the possible configurations of VCC/LDO and PVIN pin.

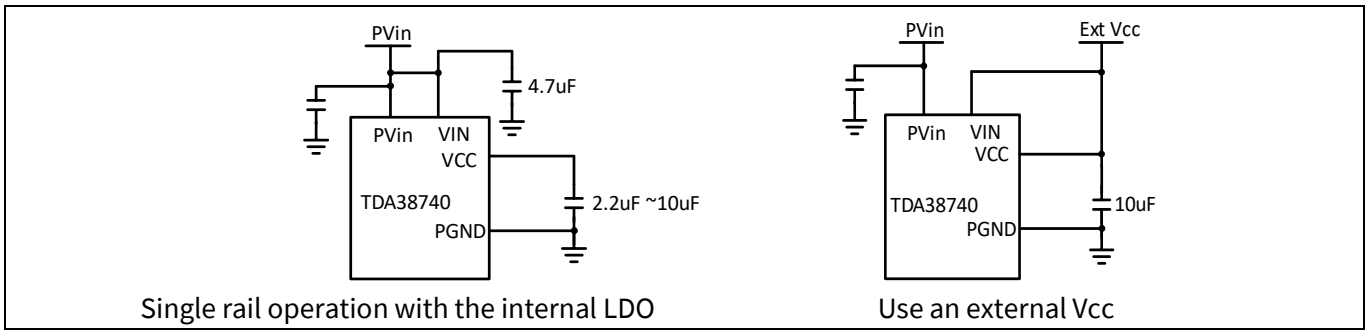


Figure 20 Configuration of using the internal LDO or an external VCC.

14.5 Fast Constant ON-Time Control

The TDA38740/725 features a proprietary Fast Constant On-Time (COT) Control, which can provide fast load transient response, good output regulation and minimize design effort. Fast COT control compares the output voltage, V_o, to a floor voltage combined with an internal ramp signal. When Vout drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares Vout with a reference voltage. Compared to traditional COT control, Fast COT control significantly improves Vout regulation.

14.6 EN (Enable) Pin

The EN pin controls the on/off state of the TDA38740/725. The soft-start sequence starts when the VCC/LDO voltage rises above the VCC_UVLO_Start threshold. The EN pin voltage needs to be toggled when the VCC voltage drops below VCC_UVLO_Stop and rises above the VCC_UVLO_Start threshold to start the soft-start sequence.

The EN pin can be configured in four ways. Three of them are as shown in Figure 21. Configuration one is an external logic signal. The second possible configuration derives the enable signal from the PVin voltage by a resistive divider, R_{EN1} and R_{EN2}. The third one is a direct connection of EN to the PVin pin. This is useful in space-constrained applications. The fourth configuration is controlled via PMBus register 0x204[7:0] using the PMBus lines. TDA38740/725 utilizes the PMBus ON_OFF_CONFIG command in combination with the OPERATION command, register 0x202[7:0], to control the enable digitally. Using this, a preference between hardware or software enable may be established. More information is available in the PMBUs app note AN_2203_PL12_2204_184108.

The EN pin should not be left floating. There is an internal pull down resistor of 1MΩ from EN to AGND pin. A pull-down resistor in the range of tens of kilohms is recommended.

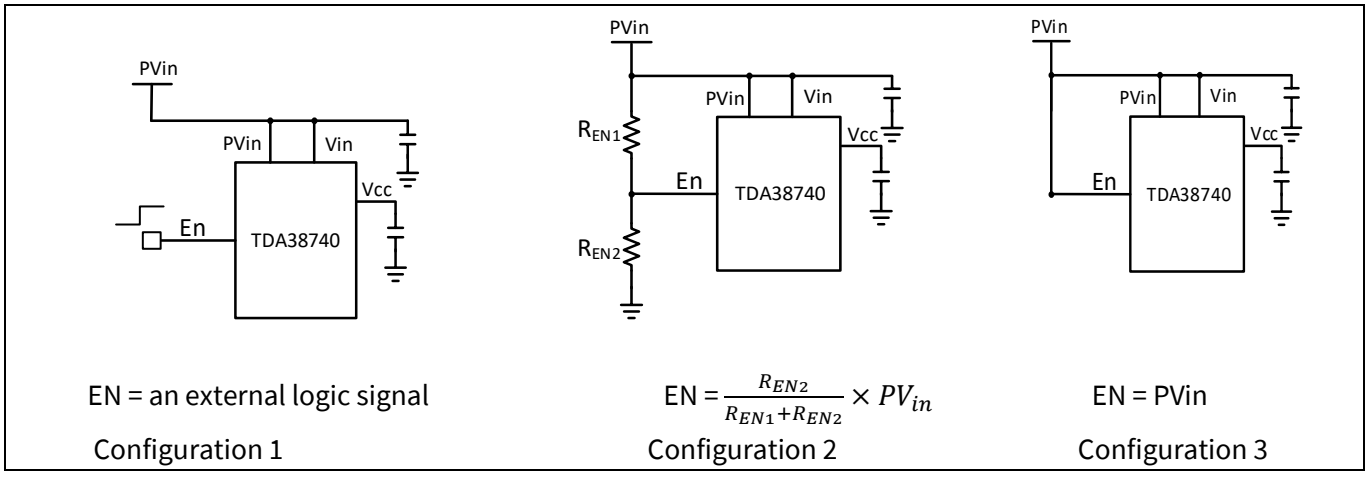


Figure 21 Enable Configurations

14.7 Switching Frequency and FCCM/DEM Operation

The TDA38740/725 offers two operation modes: Forced Continuous Conduction (FCCM) and Diode Emulation Mode (DEM). With FCCM, the TDA38740/725 always operates as a synchronous buck converter with a pseudo constant switching frequency and therefore achieves small output voltage ripple. In DEM, the synchronous FET is turned off when the inductor current is close to zero, which reduces the switching frequency and improves efficiency at light load. At heavy load, both FCCM and DEM operate in the same way. The operation mode can be selected by bit 0x5C [1] in the configuration register; value 1 for this bit programs the device to operate in FCCM mode and 0 for DEM. It should be noted that the selection of the operation mode cannot be changed on the fly. To load a new configuration, EN or VCC voltage must be cycled.

The TDA38740/725 offers eight programmable switching frequencies, f_{sw}, from 400 kHz to 2 MHz in steps of 200KHz excluding 1600 kHz, by editing the PMBus register, 0x266[15:0], using the PMBus lines. Alternatively, switching frequency and mode can be selected using eight resistor selectable options at Ton/Mode pin. The selected Ton/mode bin is loaded to the IC during the power-up and cannot be changed on the fly. To change the switching frequency and mode, users must cycle the EN signal or VCC voltage. To use the pin functionality, the ton_override_pin bit (0x5e [4]) and fccm_override_pin bit (0x5e [5]) should be set to 0. Based on the selected f_{sw}, the TDA38740/725 generates the corresponding on-time of the Control FET for a given PV_{in} and V_o, as shown by the formula below.

$$T_{on} = \frac{V_0}{PV_{in}} \times \frac{1}{f_{sw}}$$

Where f_{sw} is the desired switching frequency. During operation, the TDA38740/725 monitors PV_{in} and V_o, and can automatically adjust the on-time to maintain the pre-selected f_{sw}. With the increase of the load, the switching frequency can increase to compensate for the power losses. Therefore, the TDA38740/725 has a pseudo constant switching frequency.

Using the FREQUENCY_SWITCH PMBus command, the switching frequency may be programmed between 400 kHz and 2 MHz in steps of 200 kHz except 1600 kHz.

14.8 Soft Start

The soft-start functionality is based on the PMBus TON_RISE command. As shown in the waveform below, when the TON_RISE is set to 50 ms, the output voltage rises from zero to set value in 50 ms.

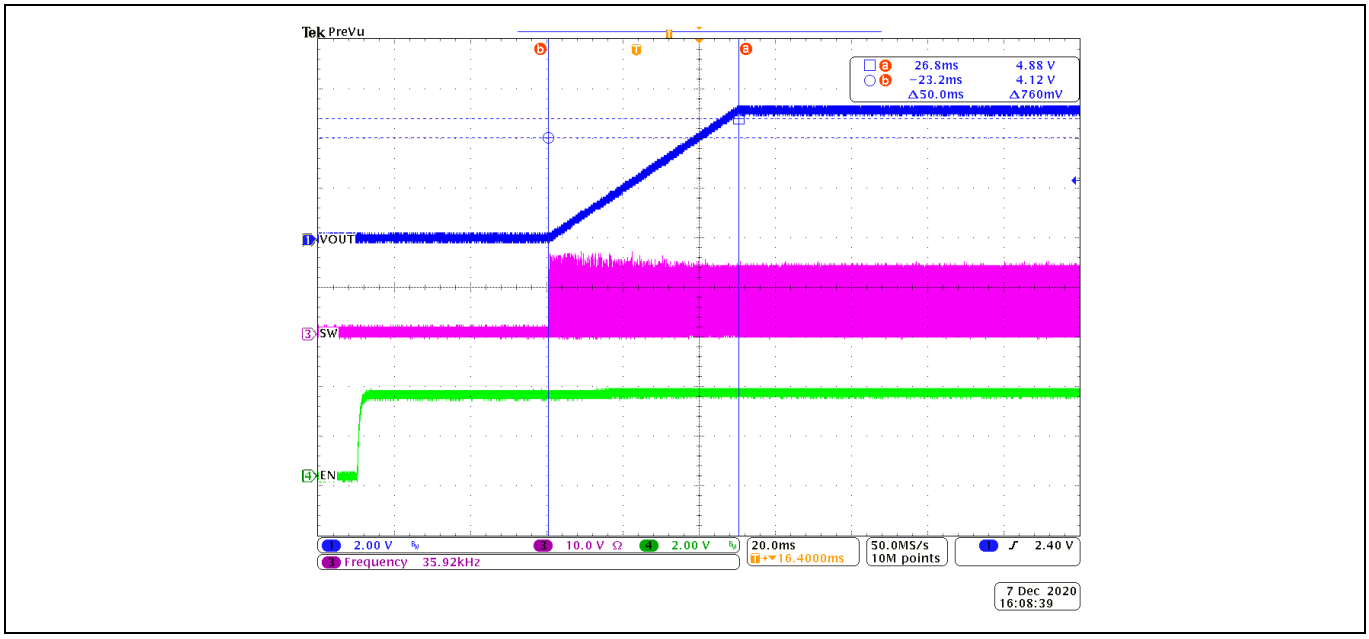


Figure 22 Vo=5V, Ch1=Vout, Ch3=Switching node, Ch4=Enable Signal

After the EN pin is enabled, the TON_DELAY command is executed before the TON_RISE command. Hence, the output will not begin to rise until the specified delay is completed. In the above example, the delay is also set to 50 ms.

14.9 Load-line

The TDA38740/725 offers a digital load line which can be set via configuration registers, without any need for external components. The load line can be programmed from 0 to 10 mΩ at a resolution of 19.53 µΩ using the VOUT_DROOP command 0x250[15:0]. The range and resolution of the VOUT_DROOP may be increased by using the bit loadline_range_sel 0x6a [6] to 0 to 50 mΩ at a resolution of 100 µΩ. In addition to this, the bandwidth of the digital load line is also programmable from 30 kHz to 500 kHz in steps of 30 kHz by using 4 bits of register 0x6a [3:0].

14.10 Output Voltage Differential Sensing

The TDA38740/725 VOSENP and VOSENM pins are connected across the output capacitors near the load to provide true differential remote voltage sensing with high common-mode rejection. Fast COT control compares the output voltage to a floor voltage combined with an internal ramp signal. When Vout drops below that signal, a PWM signal is initiated to turn on the high-side FET for a fixed on-time. The floor voltage is generated from an internal compensated error amplifier, which compares the Vout with a reference voltage. As shown in Figure 23, the output sense pins VOSENP and VOSENM are connected across the output capacitors.

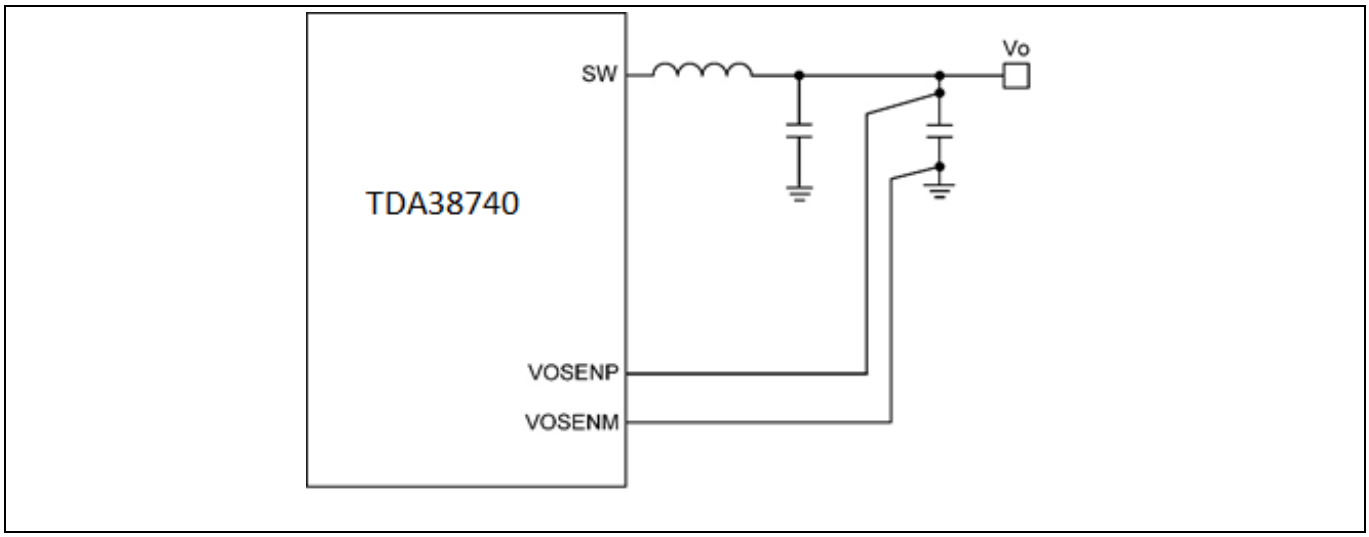


Figure 23 Output voltage sensing connections

14.11 Output Current Sensing

Current sensing for both telemetry and over-current protection is done by sensing the voltage across the sync FET $R_{DS(on)}$. This method increases the converter's efficiency, reduces cost by eliminating a current sense resistor and minimizes any sensitivity to layout-related noise issues. A novel scheme allows the reconstruction of the inductor current from the voltage sensed across the Sync FET $R_{DS(on)}$.

15 Faults and Protections

15.1 Over Current Protection (OCP)

The TDA38740/725 has two types of OCP protection: Analog OCP (AOCP) and Digital OCP (DOCP). The AOCP current limit is based on inductor valley current, whereas the DOCP is based on average current information. AOCP is a fast fault response, and should be set to a value that prevents failure of the device.

A novel scheme allows reconstruction of the inductor current from the voltage sensed across the Sync FET $R_{DS(on)}$. It should be noted here that it is this reconstructed average inductor current that is digitized by the ADC and used for output current reporting and for DOCP operation.

The AOCP fault protection circuit also uses the voltage sensed across the $R_{DS(on)}$ of the Synchronous MOSFET; however, the protection mechanism relies on a fast comparator to compare the sensed signal to the over-current threshold and does not depend on the ADC or reported current. Hence AOCP has a fast fault response. The current limit scheme uses an internal temperature-compensated current source that has the same temperature coefficient as the $R_{DS(on)}$ of the Synchronous MOSFET. As a result, the over-current trip threshold remains almost constant over temperature.

The TDA38740/725 AOCP level can be set either by pin strap resistor on ILIM pin or via three bits in the register map (aocp_thresh_sel [2:0]). The DOCP level can be set either by pin strap resistor on ILIM pin or) is available via the PMBus register IOUT_OC_FAULT_LIMIT, and the response is decided by IOUT_OC_FAULT_RESPONSE. Available responses are shutdown, latch off and retry. The indication of the fault is accessible in the STATUS_IOUT register with the PMBus.

AOCP shall be enabled during soft-start and normal operation including FCCM and DEM modes. When the AOCP threshold is crossed, the low side MOSFET will continue to stay on for the remaining cycle and the following high side pulse will be ignored to allow inductor relaxation (pulse skipping). If an AOCP condition is detected on the rising edge of a PWM pulse, the high side will still be blocked from turning on and the pulse will be skipped. The high-side will continue to be ignored if the current remains above the AOCP threshold. When current falls below the AOCP threshold, the following high-side pulse will be enabled. The Vout under AOCP is determined by the overload on the output and that determines if the PGOOD gets de-asserted or the UVP protection is triggered as a result of AOCP.

Current signal for the DOCP protection is passed through a 5.5KHz filter, before being compared with the IOUT_OC_FAULT_LIMIT threshold. Hence the response of the DOCP circuit is slower than AOCP due to the averaging of the current signal by the filter. The DOCP threshold operating point can be calibrated by IOUT_ CAL _GAIN and IOUT_ CAL _OFFSET. Because of the averaging of the current signal, DOCP is more accurate than AOCP. It is recommended to set AOCP higher than DOCP as AOCP may get triggered earlier than DOCP and may result in a drop-in output voltage when both AOCP and DOCP are set to same value. When the Digital OCP is triggered from the Analog OCP using docp_from_aocp register 0x60[3], a 10-count counter is implemented to count 10 AOCP events, then a signal is sent to the digital block to perform the programmed response. The counter is reset after 3 consecutive non-OCP events. The count occurs at the valley of the current. Note that COT switching frequency will decrease when skipping pulses. Figure 24 is an example AOCP response.

The TDA38740/725 also offers cycle-by-cycle AOCP response with a choice of eight selectable current limits, which are set by the resistance at ILIM pin. The selected OCP limit is loaded to the IC during the power-up and cannot be changed on the fly. To change the OCP limit, users must cycle the EN signal or Vcc voltage. Cycle-by-cycle OCP response allows the TDA38740/725 to fulfill a brief high current demand, such as a high inrush current during start-up. The output slew rate and the output capacitance will affect the AOCP during startup. At higher output voltages, a higher output slew rate or a higher output capacitance can falsely trigger AOCP at startup. The TON_RISE time should be increased or output capacitance should be reduced to avoid false triggering of AOCP.

The AOCP is activated when the EN voltage is above its threshold. During AOCP events, the valley of the inductor current is regulated around the AOCP limit. After the first switching cycle when the AOCP is detected, the valley of the inductor current can drop below the AOCP limit due to cycle skipping. However, as part begins to switch again after cycle skipping, the current will climb up again to AOCP level and it may take a few micro seconds to few hundreds of micro seconds to reach set AOCP level. It should be noted that AOCP events do not pull the PGOOD signal low unless the output voltage eventually drops below the PGOOD_OFF threshold or the Under-Voltage Protection (UVP) threshold.

The OCP limits are thermally compensated. The corresponding output dc current can be calculated as follows:

$$I_{out_OCP} = I_{LIM} + \frac{\Delta i_L}{2}$$

Where: I_{out_OCP} = Output dc current when AOCP is tripped. I_{LIM} = AOCP limit, which is the valley of inductor current. ΔiL = Peak-peak inductor ripple current.

To avoid inductor saturation during AOCP events, the following criterion is recommended for the inductor saturation current rating.

$$I_{sat} \geq I_{LIM_max} + \Delta i_L$$

Where: I_{sat} is the inductor saturation current and I_{LIM_max} is the maximum spec of the AOCP limit.

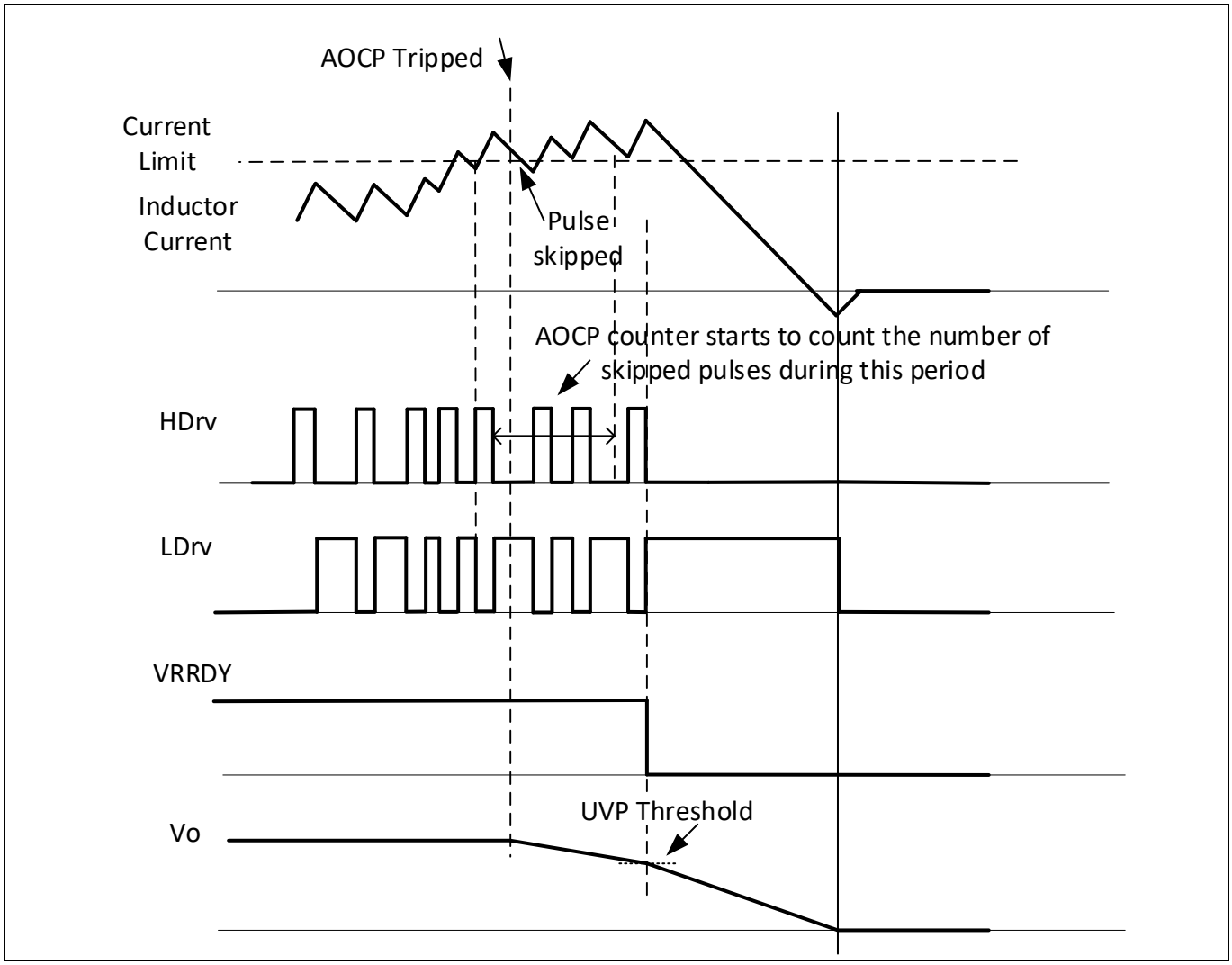


Figure 24 AOCP response timing diagram.

15.2 Output Under Voltage Protection (UVP)

The TDA38740/725 UVP response is a relative limit configurable from 50 mV to 400 mV in steps of 50 mV using the register bits relative_uvp_thresh[2:0] in configuration register 0x5e. The limit is programmed by the VOUT_UV_FAULT_LIMIT PMBus command, and the response is programmed via the VOUT_UV_FAULT_RESPONSE command. Possible responses are ignore, shutdown, and retry indefinitely.

When using the VBT pin to set the output voltage, the VOUT_COMMAND value should be the same as the VBT pinstrap setting to avoid improper UVP triggering.

When the UVP fault is triggered, a flag is raised and low-side FET is turned ON to drag down the output. The Vout setting is changed to 0V with a slew rate of 30mV/uS to drag the output to 0V as soon as possible. After that both MOSFETs are tri-stated until the flag is cleared using the PMBus CLEAR_FAULTS command. The part is started again by either cycling the Vcc voltage or the EN signal to the part.

If the response is set to retry, a user defined timer (1 ms to 8 ms in steps of 1 ms) is started as soon as the UVP fault is triggered and the output is tri-stated. At the end of the timer, the output is checked against a fixed level of 250 mV. If the output is below this voltage, the start-up sequence is initiated. Otherwise, the timer is reset and the output tri-state continues (both MOSFET's are tri-stated).

There are options for UVP protection to be lifted during voltage transitions (Vboot, Vout transition up and/or down) using the register bits blank_uv_sel[1:0] in configuration register 0x60. The options for this register are outlined in Table 16.

Table 16 Optional UVP blanking via register blank_uv_sel (0x60[11:10]).

sel	Description
3	blank UV faults during Vout transition up or down (including Vboot)
2	blank UV faults during Vout transition up (including Vboot)
1	blank UV faults during Vboot
0	no UV fault blanking

15.3 Over Voltage Protection (OVP)

The OVP response is divided into two parts: Fixed OVP (FOVP) and Relative OVP (ROVP). The Fixed OVP is typically used for start-up, all Vout transitions, and when EN is low. ROVP covers all other situations during operation. Figure 25 depicts an example of when FOVP and ROVP are utilized.

When using the VBT pin to set the output voltage, the VOUT_COMMAND value should be the same as the VBT pinstrap setting to avoid improper ROVP triggering.

The FOVP has 8 distinct levels (0.8 V, 1 V, 1.2 V, 1.35 V, 1.5 V, 1.8 V, 2.2 V, and 2.85 V in VOUT_SCALE_LOOP 1:1 and the levels are doubled in VOUT_SCALE_LOOP 1:2. FOVP is programmable via the register fixed_ovp_thresh [2:0] in configuration register 0x60. The response to an OVP event is programmed via the VOUT_OV_FAULT_RESPONSE command. OVP can have four responses: ignore, shutdown, and retry n (maximum of 6) times after n (defined by PMBus) msecs before latching and retry forever. The threshold for ROVP is relative to the programmed output voltage, and can be set from 50 mV to 400 mV in steps of 50 mV. The OVP fault can also be blanked by using the bits [13:12] of register 0x60 in common regmap space. Please refer to Table 17 for more details. The threshold for ROVP is relative to the programmed output voltage, and can be set from 50 mV to 400 mV in steps of 50 mV using the I2C register relative_ovp_thresh [2:0] (0x5e [14:12]). The PMBUs set ROVP using the VOUT_OV_FAULT_LIMIT command could be overridden by using the relative_ovp_thresh_en (0x5e [15]) bit.

Table 17 Optional OVP blanking via blank_ov_sel(0x60[13:12])

sel	Description
3	blank OV faults during DVID up or down (including Vboot)
2	blank OV faults during DVID up (including Vboot)
1	blank OV faults during Vboot
0	no OV fault blanking

When the output triggers an FOVP event, the OVP flag is set, the low side switch is turned ON and the high side switch is turned OFF. The low side switch is turned ON until the output voltage is dragged down to the set FOVP threshold. The output voltage then decreases to zero with its natural decay.

When the output triggers an ROVP event, the Vout set point is moved to 0 V at a controlled slew rate of 30mV/us and the OVP flag is set. Next, the low side switch is turned ON and the high side is turned off. This allows the output to discharge until the Vout set point reaches zero or Vout catches up with the VID set point. At this point the low side and high side switches turn ON and OFF as required to maintain the output at the VID set point. How fast the output voltage discharges during this event is determined by the output voltage, output capacitance and output inductor. This determines if the output voltage is indeed discharged to zero by the end of the controlled Vout ramp down. At the end of the ramp, if the output is not already at zero, the output voltage will discharge to zero with its natural decay.

Please refer to the relative OVP and UVP thresholds table under register 5E[10:8] of the register map app note AN_2204_PL12_2204_183614 for more information on how to set these thresholds for VOUT_SCALE_LOOP 1:1 and VOUT_SCALE_LOOP 1:2.

The picture below shows and example of how ROVP and RUVP work during DVID changes in conjuction with blank settings mentioned above. In this example, the ROVP is blanked during the DVID down and Vboot.

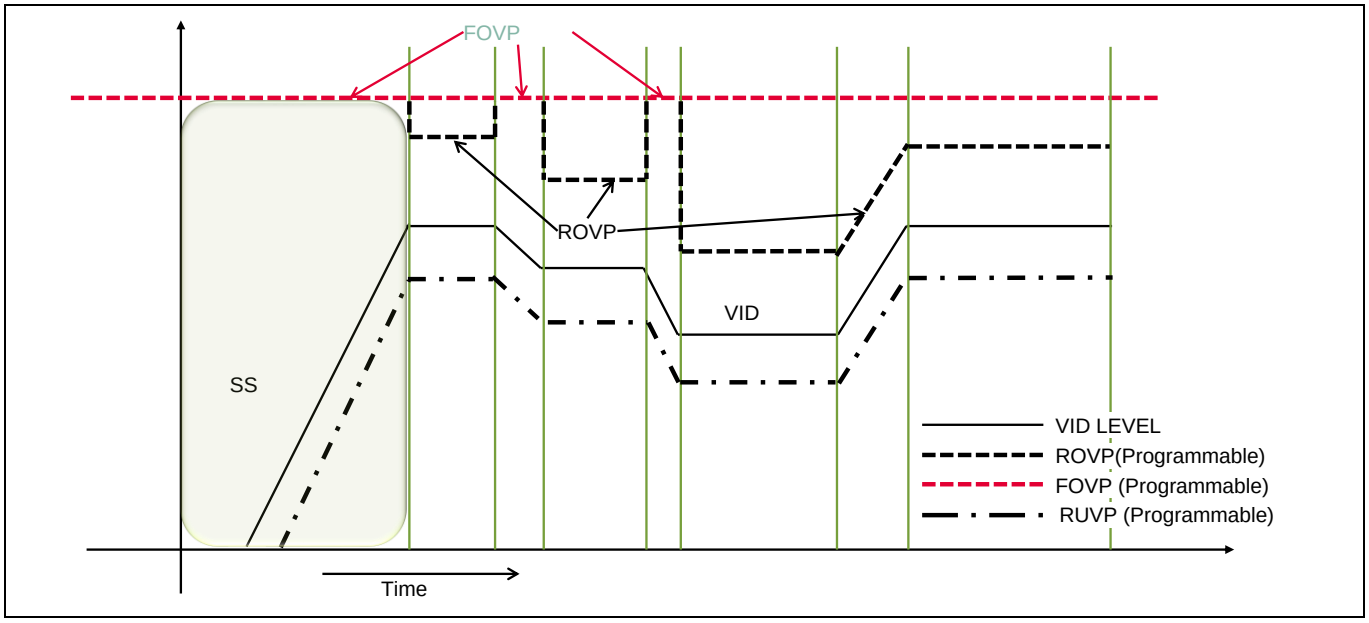


Figure 25 OVP example diagram. Note the situations in which FOVP takes over from ROVP.

15.4 Over Temperature Protection (OTP)

The temperature is measured by a thermal sensor in the controller die. Temperature protection is programmable via the OT_FAULT_LIMIT, OT_WARN_LIMIT, and OT_FAULT_RESPONSE PMBus registers. The TDA38740/725 supports three responses: ignore, shutdown, and retry indefinitely. The fault is non-latching.

An OTP event is triggered when the device temperature reaches the OT_FAULT_LIMIT. The switching output is tri-stated and the output discharges, while the controller stays biased with the internal LDO on. With the output switched off, the device cools until reaching the OTP_WARN_LIMIT, and if set to retry, the device will hiccup with the potential for pre-biased startup.

15.5 Boot Under Voltage Lockout (UVLO)

The voltage from the BOOT pin to the PHASE pin is monitored on the TDA38740/725. If the boot UVLO lower threshold violation is detected within the PWM cycle, the event is counted and a fault is asserted after 10 violations. After 3 consecutive cycles without a BOOT UVLO event (above the lower threshold during the PWM cycle), the counter resets. To clear the fault, the Vcc voltage or the EN signal has to be cycled. The boot UVLO fault is in the fail_code_sticky register.

15.6 Minimum On - Time and Minimum Off - Time

The minimum on-time refers to the shortest time for the control MOSFET to be reliably turned on. The minimum off-time refers to the minimum time duration in which the synchronous FET stays on before a new PWM pulse is generated. The minimum off-time is needed for TDA38740/725 to charge the bootstrap capacitor, and to sense the current of the synchronous MOSFET for OCP.

For applications requiring a small duty cycle, it is important that the selected switching frequency result in an on-time larger than the maximum specification of the minimum on-time in Section 7. Otherwise, the resulting switching frequency may be lower than the desired target. The following formula can be used to check for the minimum on-time requirement:

$$\frac{V_0}{k f_{sw} \times V_{in}} > \max\ spec\ of\ T_{on(\min)}$$

Where f_{sw} is the desired switching frequency. *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure design margin.

For applications requiring a high duty cycle, it is important to make sure a proper switching frequency is selected so that the resulting off-time is longer than the maximum specification of the minimum off-time in Section 7 which can be calculated as shown below.

$$\frac{V_{in} - V_0}{k f_{sw} \times V_{in}} > \max\ spec\ of\ T_{off(\min)}$$

Where f_{sw} is the desired switching frequency. *k* is the variation of the switching frequency. As a rule of thumb, select *k* = 1.25 to ensure the design margin.

The resulting maximum duty cycle is therefore determined by the selected on-time and minimum off-time.

$$D_{max} = \frac{T_{on}}{T_{on} + T_{off(\min)}}$$

15.7 High-Side Short (HSS) Detection

The TDA38740/725 offers high-side FET short detection. The phase pin is monitored when the low-side FET is active. HSS monitoring happens both at start-up and during normal operation. In an HSS event, if the HSS threshold is reached, the PGOOD pin is de-asserted. Once the HSS threshold is reached, the low-side FET is turned on and switching stops. There is no current reporting during this time. The fault is sticky and only clears when either the VCC voltage or the EN signal is cycled.

16 Faults Communication

TDA38740/725 supports the the following FAULTs via telemetry: OCP, OVP, UVP and OTP.

16.1 PMBUS Slave Addressing

The TDA38740/725 supports PMBus communication through the use of exclusive addressing. By using a 7-bit address, the user can configure the device to any one of 127 different PMBus addresses. Once the address of the TDA38740/725 is set, it can be locked to protect it from being overwritten. Optionally, a resistor can be tied to the SM_ADDR/PROG pin to generate an offset, as shown in Figure 26 .

Setting a base 7-bit PMBus address of 40h with a resistor offset of +15 sets the 7-bit PMBus address to 4Fh.

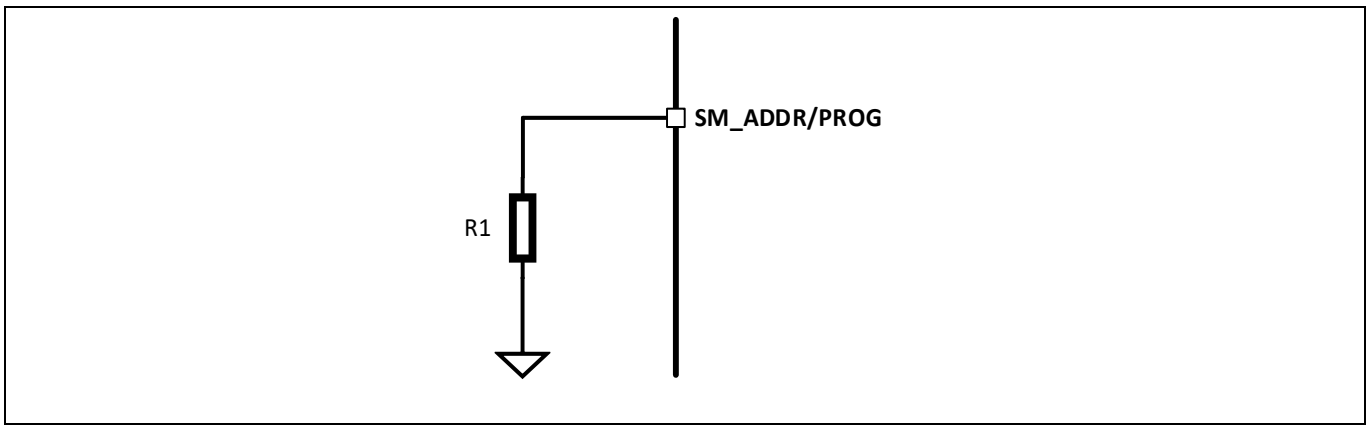


Figure 26 SM-ADDR/PROG Pin Components

16.2 Real-Time Telemetry

TDA38740/725 provides real-time accurate measurement of input voltage, output voltage, output current, temperature, output power, and input power over the PMBus interface. The output voltage is calculated based on the output voltage setting and the result is reported through the PMBus.

16.3 SMBUS/PMBUS PROTOCOLS

To access TDA38740 and TDA38725 configuration and monitoring registers, four different protocols are required:

- the SMBus Read/Write Byte/Word protocol with/without PEC (for status and monitoring)
- the SMBus Send Byte protocol with/without PEC (for CLEAR_FAULTS only)
- the SMBus Block Read protocol for accessing Model and Revision information
- the SMBus Process call (for accessing Configuration Registers)

In addition, the TDA38740/725 supports:

- Alert Response Address (ARA)
- Bus timeout
- Group command for writing to many VRs with one command

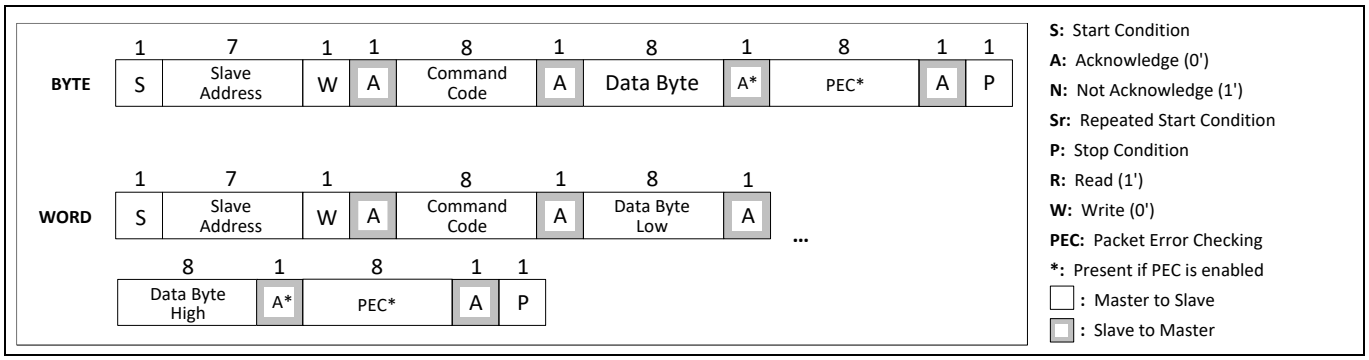


Figure 27 SMBus Write Byte/Word

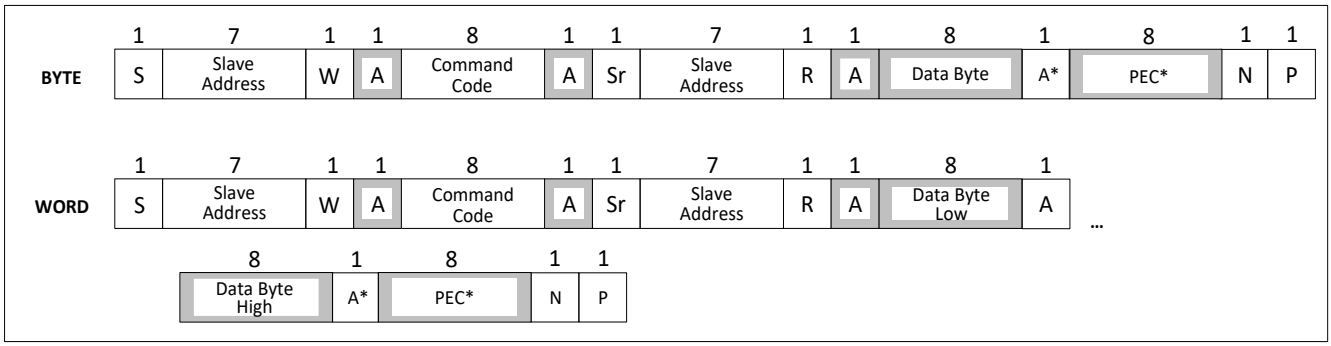


Figure 28 SMBus Read Byte/Word

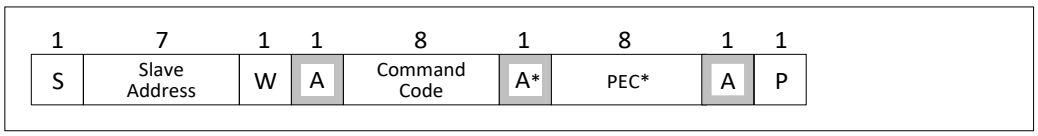


Figure 29 SMBus Send Byte

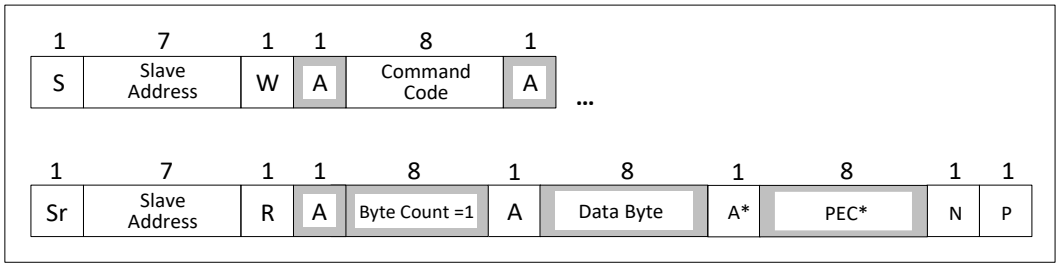


Figure 30 SMBus Block Read with Byte Count=1

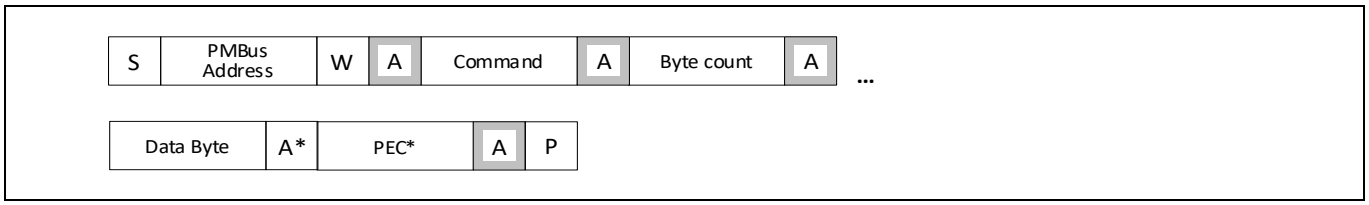


Figure 31 SMBus Block Write with Byte Count =1

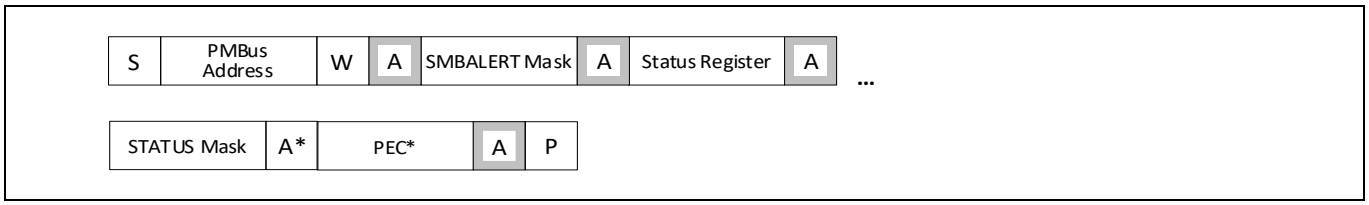


Figure 32 SMBALERT_MASK write

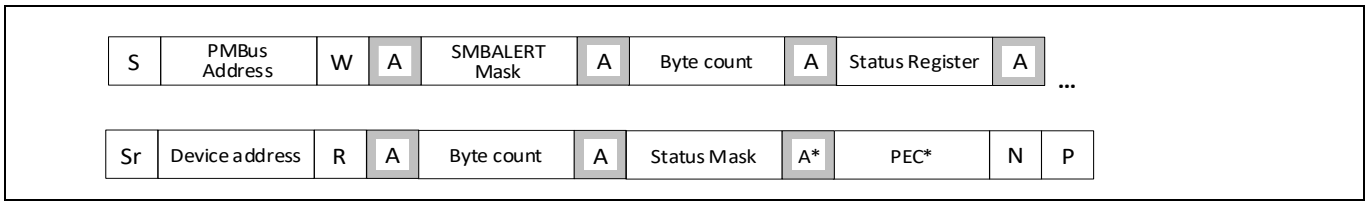


Figure 33 SMBALERT_MASK read

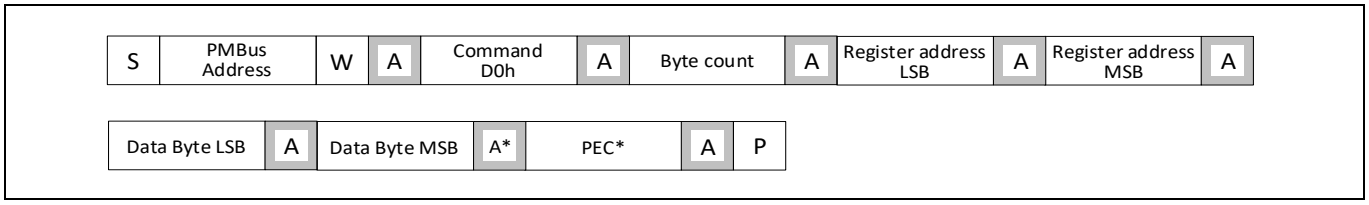


Figure 34 MFR specific command to Write an MFR Register

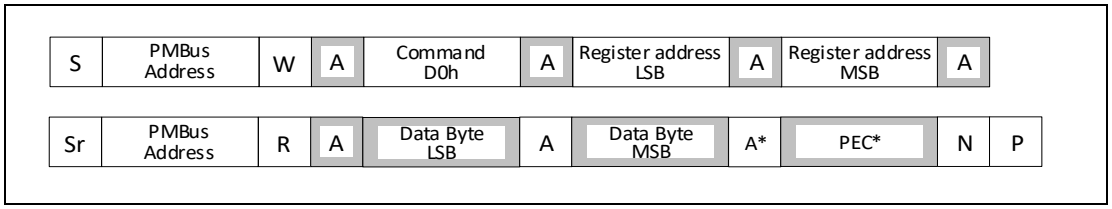


Figure 35 SMBus Custom Process Call to Read an MFR Register

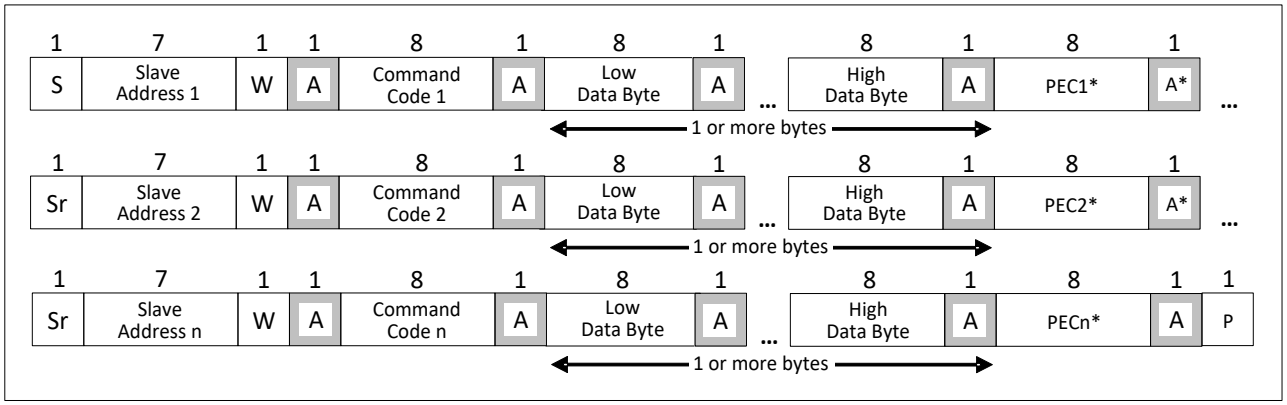


Figure 36 Group Command

Table 18 PMBus Commands Supported

Register Address	COMMAND	PMBus PROTOCOL	PMBus COMMAND CODE	DESCRIPTION
0x200	PAGE	Read/Write Byte	00h	Allows access of each loop via paging.
0x202	OPERATION	Read/Write Byte	01h	Enables or disables the output, controls soft off, voltage command source, and margin fault respose.
0x204	ON_OFF_CONFIG	Read/Write Byte	02h	Configures the combination of CONTROL pin and OPERATION commands needed to turn the unit on and off.
0x206	CLEAR FAULTS	Send Byte	03h	Clears contents of Fault registers
0x20A	PAGE_PLUS_WRITE	Write Block	05h	Set the PAGE within a device, send a command, and send the data for the command in one packet.
0x20C	PAGE_PLUS_READ	Block Write/Read Process Call	06h	Set the PAGE within a device, send a command, and read the returned data by the command in one packet
0x220	WRITE_PROTECT	Read/Write Byte	10h	Protects from overwriting the configuration files and modes accidentally
0x224	RESTORE_DEFAULT_ALL	Send Byte	12h	Instructs the device to reload the contents of NVM default store memory to operating memory
0x22C	RESTORE_USER_ALL	Send Byte	16h	Instructs the device to reload the contents of NVM user store memory to operating memory
0x232	CAPABILITY	Read Byte	19h	Returns 11010000 to indicate Packet Error Checking is supported. Maximum bus speed is 1 MHz
0x236	SMBALERT_MASK	Write word, Block Write/ Block Read Process Call	1Bh	Set to prevent warning or fault conditions from asserting the SMBALERT# signal. Write command code for STATUS register to be masked in the low byte, the bit to be masked in the High byte.
0x240	VOUT_MODE	Read/Write Byte	20h	Sets the format for VOUT related commands. Linear mode, -8, -9, -10, -11 and -12 exponents supported.
0x242	VOUT_COMMAND	Read/Write Word	21h	Sets the voltage to which the device should set the output. Format and resolution determined by VOUT_MODE.

0x248	VOUT_MAX	Read/Write Word	24h	Sets an upper limit on the output voltage the unit can command. Format and resolution according to VOUT_MODE.
0x24A	VOUT_MARGIN_HIGH	Read/Write Word	25h	Sets the margin high voltage when commanded by OPERATION. Must be in format determined by VOUT_MODE.
0x24C	VOUT_MARGIN_LOW	Read/Write Word	26h	Sets the margin low voltage when commanded by OPERATION. Format and resolution according to VOUT_MODE.
0x24E	VOUT_TRANSITION_RATE	Read/Write Word	27h	Sets the rate at which the output changes voltage during regulation. Resolution is exponant -3.
0x250	VOUT_DROOP	Read/Write Word	28h	Allows the user to set the load-line value in resolution of 5/256 or 25/256 mΩ.
0x252	VOUT_SCALE_LOOP	Read/Write Word	29h	Used to account for any external attenuation network on VOUT sense feedback and provide correct VOUT reporting.
0x256	VOUT_MIN	Read/Write Word	2Bh	Sets a lower limit on the commanded output voltage. Format and resolution according to VOUT_MODE
0x266	FREQUENCY_SWITCH	Read/Write Word	33h	Sets the switching frequency. Resolution is exponent 1
0x26A	VIN_ON	Read/Write Word	35h	Sets the value of the input voltage at which the unit should begin power conversion. Resolution is exponant -1.
0x26C	VIN_OFF	Read/Write Word	36h	Sets the value of the input voltage at which the unit, once operation has started, should stop power conversion. Resolution is exponant -1.
0x270	IOUT_CAL_GAIN	Read/Write Word	38h	Used to calibrate the output current's gain. Resolution is exponant -7.
0x272	IOUT_CAL_OFFSET	Read/Write Word	39h	Used to null out any offsets in the output current sensing circuitry. Resolution is exponant -4.
0x280	VOUT_OV_FAULT_ LIMIT	Read/Write Word	40h	Returns the value of the output voltage, measured at the sense or output pins, that causes an output over voltage fault. Format and resolution according to VOUT_MODE.
0x282	VOUT_OV_FAULT_ RESPONSE	Read/Write Byte	41h	Instructs the device on what action to take in response to an output over voltage fault.
0x288	VOUT_UV_FAULT_ LIMIT	Read/Write Word	44h	Returns the value of the output voltage, measured at the sense or output pins, that causes an output under voltage fault. Format and resolution according to VOUT_MODE.
0x28A	VOUT_UV_FAULT_ RESPONSE	Read/Write Byte	45h	Instructs the device on what action to take in response to an output under voltage fault.
0x28C	IOUT_OC_FAULT_ LIMIT	Read/Write Word	46h	Sets the value of the output current, in amperes, that causes the over current detector to indicate an over current fault condition. Resolution is exponant -4.
0x28E	IOUT_OC_FAULT_ RESPONSE	Read/Write Byte	47h	Instructs the device on what action to take in response to an output over current fault.

0x29E	OT_FAULT_LIMIT	Read/Write Word	4Fh	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an over temperature fault. Resolution is exponant 0.
0x2A0	OT_FAULT_RESPONSE	Read/Write Byte	50h	Instructs the device on what action to take in response to an over temperature fault. Only shutdown and ignore are supported.
0x2A2	OT_WARN_LIMIT	Read/Write Word	51h	Sets the temperature, in degrees Celsius, of the unit at which it should indicate an over temperature Warning alarm. Resolution is exponant 0.
0x2AA	VIN_OV_FAULT_LIMIT	Read/Write Word	55h	Sets the value of the input voltage that causes an input over voltage fault. Resolution is exponant -4.
0x2AC	VIN_OV_FAULT_RESPONSE	Read/Write Byte	56h	Instructs the device on what action to take in response to an input over voltage fault. Only shutdown and ignore are supported.
0x2BC	POWER_GOOD_ON	Read/Write Word	5Eh	Sets the output voltage at which an optional POWER_GOOD signal should be asserted. Format and resolution according to VOUT_MODE. See Note 17
0x2BE	POWER_GOOD_OFF	Read/Write Word	5Fh	Sets the output voltage at which an optional POWER_GOOD signal should be negated. Format and resolution according to VOUT_MODE. See Note 17
0x2C0	TON_DELAY	Read/Write Word	60h	Sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. Resolution is exponant -1. See Note 18
0x2C2	TON_RISE	Read/Write Word	61h	Sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. Resolution is exponant -1.
0x2C8	TOFF_DELAY	Read/Write Word	64h	Sets the time (in ms) from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. Resolution is exponant -1.
0x2CA	TOFF_FALL	Read/Write Word	65h	Sets the time, in milliseconds, from the end of the turn-off delay time until the voltage is commanded to zero. Resolution is exponant -1.
0x2F0	STATUS_BYTE	Read/Write Byte	78h	Returns 1 byte where the bit meanings are: Bit <7> Reserved Bit <6> Output off (due to fault or enable) Bit <5> Output over-voltage fault Bit <4> Output over current fault Bit <3> Not Supported Bit <2> Temperature fault Bit <1> Communication/Memory/Logic fault Bit <0>: None of the Above

0x2F2	STATUS_WORD	Read/Write Word	79h	Returns 2 bytes where the Low byte is the same as the STATUS_BYTE data. The High byte has bit meanings are: Bit <7> Output voltage fault Bit <6> Output current fault Bit <5> Input voltage fault. Bit <4> MFR_SPECIFIC Bit <3> POWR GOOD# Bit <2:0> Not Supported
0x2F4	STATUS_VOUT	Read/Write Byte	7Ah	Bit <7> Output over voltage Fault Bit <6> Not Supported Bit <5> Not Supported Bit <4> Output under voltage Fault Bit <3> VOUT_MAX Warning Bit <2:0> Not Supported
0x2F6	STATUS_IOUT	Read/Write Byte	7Bh	Bit <7> Output Over current Fault Bit <6> Not Supported Bit <5> Not Supported Bit <4:0> Not Supported
0x2F8	STATUS_INPUT	Read/Write Byte	7Ch	Bit <7> Input over voltage Fault Bit <6:4> Not Supported Bit<3> Off due to VIN low Bit<2:0> Not Supported
0x2FA	STATUS_TEMPERATURE	Read/Write Byte	7Dh	Bit <7> Over Temperature Fault Bit <6> Over Temperature Warning Bit <5:0> Reserved
0x2FC	STATUS_CML	Read/Write Byte	7Eh	Returns 1 byte where the bit meanings are: Bit <7> Invalid or unsupported command Bit <6> Invalid or unsupported data Bit <5> PEC fault Bit <4> OTP store/restore error Bit <3:2> Reserved Bit <1> Other communication fault not listed here Bit <0> Reserved
0x310	READ_VIN	Read Word	88h	Returns the input voltage in Volts
0x312	READ_IIN	Read Word	89h	Returns the input current in Amperes
0x316	READ_VOUT	Read Word	8Bh	Returns the output voltage in the format set by VOUT_MODE
0x318	READ_IOUT	Read Word	8Ch	Returns the output current in Amperes
0x31A	READ_TEMPERATURE_1	Read Word	8Dh	Returns the addressed loop NTC temperature in degrees Celsius
0x32C	READ_POUT	Read Word	96h	Returns the output power in Watts
0x32E	READ_PIN	Read Word	97h	Returns the input power in Watts
0x330	PMBUS_REVISION	Read Byte	98h	PMBus Rev 1.3

0x332	MFR_ID	Block Read/Write Byte count = 2	99h	The MFR_ID is set to IR (ASCII 52 49) unless programmed differently in the USER registers of the controller.
0x334	MFR_MODEL	Block Read/Write, Byte count = 2	9Ah	The MFR_MODEL is the same as the device ID if the USER register for Manufacturer model is 00. Otherwise MFR_Model command returns the value in the USER register for MFR_MODEL.
0x336	MFR_REVISION	Block Read, Byte count = 2	9Bh	The MFR_REVISION is the same as the device revision if the USER register for Manufacturer revision is 00. Otherwise MFR_REVISION command returns the value in the USER register for MFR_REVISION.
0x35A	IC_DEVICE_ID	Block Read	ADh	Returns a 1-byte code with the following values: 84h = TDA38740 92h = TDA38725
0x35C	IC_DEVICE_REV	Block Read	AEh	The IC revision that is stored inside the IC
0x3A0	MFR_READ/WRITE_ REG	Custom MFR protocol	D0h	Read/Write I2C registers
0x382	MFR_VENDOR_INFO_1	Read Word	C1h	Returns the product id and silicon revision
0x384	MFR_VENDOR_INFO_2	Read/ write Wod	C2h	Available for vendor use. Default 0x0

Note:

17. *PGOOD_ON and PGOOD_OFF thresholds are asserted at half of the programmed value when VOUT_SCALE_LOOP is set to 1:2 mode. The threshold values should be set to twice of the desired PGOOD levels.*
18. *There is an additional delay of upto 100 us to the TON_DELAY.*
19. *OVP and UVP will operate at twice the threshold set by PMBUs commands VOUT_UV_FAULT_LIMIT and VOUT_OV_FAULT_LIMIT when relative_ovp_thresh_res=1.*

16.4 11-BIT Linear Data Format

Monitored parameters use the Linear Data Format encoding into 1 Word (2 bytes), where:

$$Value = Y * 2^{N}$$

Note N and Y are “signed” values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

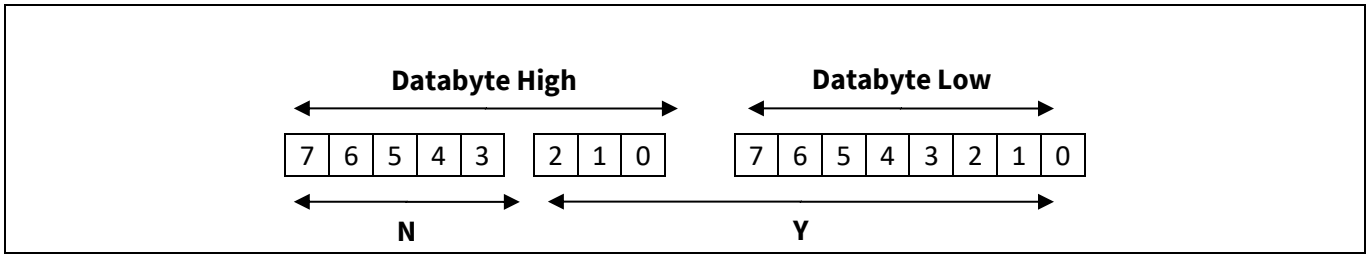


Figure 37 11-Bit Linear Data Format

16.5 16-BIT Linear Data Format

This format is only used for VOUT related commands (READ_VOUT, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, POWER_GOOD_ON, and POWER_GOOD_OFF):

$$Value = Y * 2^{N}$$

Note N and Y are “signed” values. If VOUT is set to linear format (by VOUT_MODE), then N is set by the VOUT_MODE command and only Y is returned in the data-field as a 16-bit unsigned number.

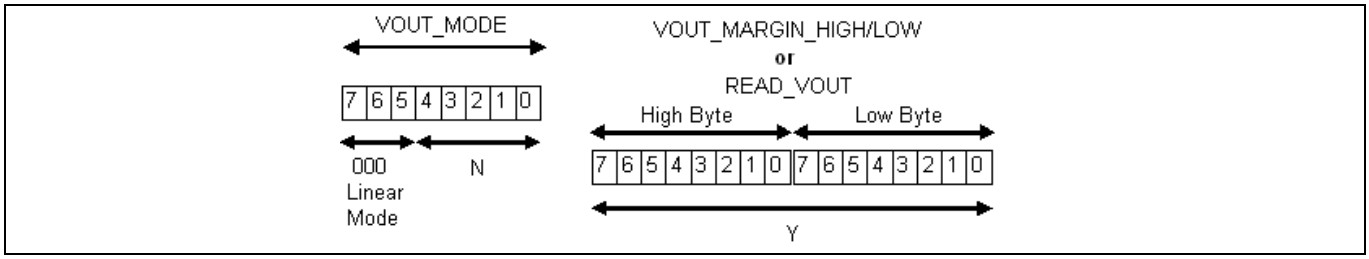


Figure 38 16-BIT Linear Data Format

17 Design example

In this section, an example is used to explain how to design a buck regulator with the TDA38740/725. The application circuit is shown in Figure 3. The design specifications are given below.

- PV_{in} = 12 V (±10%)
- V_o = 1.0 V
- I_o = 40 A
- V_o ripple voltage = ±1% of V_o
- Load transient response = ± 3% of V_o with a step load current = 9 A and slew rate = 30 A/µs

17.1 Enabling the TDA38740/725

The TDA38740/725 has a precise Enable threshold voltage, the Enable feedback resistor, R_{EN1} and R_{EN2}, can be calculated as follows.

$$PV_{in(\min)} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \geq V_{EN(\max)}$$

$$R_{EN2} \geq R_{EN1} \times \frac{V_{EN(\max)}}{PV_{in(\min)} - V_{EN(\max)}}$$

Where $V_{EN(max)}$ is the maximum spec of the En-start-threshold as defined in the Absolute Maximum Ratings table. For $PV_{in\ (min)}$ =10.8 V, select R_{EN1}=49.9 kΩ and R_{EN2} > 3.4 kΩ. R_{EN2} suggested = 7.5 kΩ

17.2 Programming the Switching Frequency and Operation Mode

The TDA38740/725 has very good efficiency performance and is suitable for high switching frequency operation. In this case, 800 kHz is selected to achieve a good compromise between efficiency, passive component size and dynamic response. In addition, FCCM operation is selected to ensure a small output ripple voltage over the entire load range. The switching frequency and FCCM operation can be selected via register bits.

17.3 Selecting Input Capacitors

Without input capacitors, the pulse current of the Control MOSFET is provided directly from the input supply power. Due to the impedance of the cable, the pulse current can cause disturbances in the input voltage and potential EMI issues. The input capacitors filter the pulse current, resulting in almost constant current from the input supply. The input capacitors should be selected to tolerate the input pulse current, and to reduce the input voltage ripple. The RMS value of the input ripple current can be expressed by:

$$I_{RMS} = I_o \times \sqrt{D \times (1 - D)}$$

$$D = \frac{V_o}{PV_{in}}$$

Where I_{RMS} is the RMS value of the input capacitor current. I_o is the output current and D is the Duty Cycle. For I_o = 40 A and $D_{(max)}$ = 0.09, the resulting RMS current flowing into the input capacitor is I_{rms} = 11.6 A.

To meet the requirement of the input ripple voltage, the minimum input capacitance can be calculated as follows.

$$C_{in(\min)} > \frac{I_o \times (1 - D) \times D}{f_{sw} \times (\Delta PV_{in} - ESR \times I_o \times (1 - D))}$$

Where ΔPV_{in} is the maximum allowable peak-to-peak input ripple voltage, and ESR is the equivalent series resistor of the input capacitors. Ceramic capacitors are recommended due to their low ESR, ESL and high RMS current capability. For I_o = 40 A, f_{sw} = 800 kHz, ESR = 3 mΩ, and ΔPV_{in} = 240 mV, $C_{in(min)}$ > 32 µF. To account for the de-rating of ceramic capacitors under a bias voltage, 8 x 22 µF/0805/25 V MLCC and 1 x 4.7uF/25 V MLCC are used for the input capacitors. In addition, a bulk capacitor is recommended if the input supply is not located close to the voltage regulator.

17.4 Inductor Selection

The inductor is selected based on output power, operating frequency and efficiency requirements. A low inductor value results in a large ripple current, lower efficiency and high output noise, but it helps with size reduction and transient load response. Generally, the desired peak-to-peak ripple current in the inductor (Δi) is found between 20% and 50% of the output current.

The inductor saturation current must be higher than the maximum specification of the OCP limit plus the peak-to-peak inductor ripple current. For some core materials, inductor saturation current may decrease as temperature increases. So it is important to check the inductor saturation current at the maximum operating temperature.

The inductor value for the desired operating ripple current can be determined using the following relation:

$$L = (PV_{in(\max)} - V_o) \times \frac{D_{min}}{\Delta i_{L(\max)} \times F_{sw}}$$

$$D_{min} = \frac{V_o}{PV_{in(\max)}}$$

$$I_{sat} \geq OCP_{max} + \Delta i_{L(\max)}$$

Where: $PV_{in(max)}$ = Maximum input voltage; ΔiL_{max} = Maximum peak-to-peak inductor ripple current; OCP_{max} = maximum spec of the OCP limit as defined in Section 15.1, and I_{sat} = inductor saturation current. In this case, select inductor L =150 nH to achieve ΔiL_{max} = 25% of I_{omax}. The I_{sat} should be no less than 52 A.

17.5 Output Capacitor Selection

The output capacitor selection is mainly determined by the output voltage ripple and transient requirements.

To satisfy the V_o ripple requirement, C_o should satisfy the following criterion.

$$C_o > \frac{\Delta i_{Lmax}}{8 \times \Delta V_{or} \times f_{sw}}$$

Where ΔV_{or} is the desired peak-to-peak output ripple voltage. For ΔiL_{max}= 7.5 A, ΔV_{or} =20 mV, f_{sw} = 800 kHz, C_o must be larger than 59 µF. The ESR and ESL of the output capacitors, as well as the parasitic resistance or inductance due to PCB layout, can also contribute to the output voltage ripple. It is suggested to use Multi-Layer Ceramic Capacitor (MLCC) for their low ESR, ESL and small size.

To meet the transient response requirements, the output capacitors should also meet the following criterion:

$$C_o > \frac{L \times \Delta I_{o(\max)}^2}{2 \times \Delta V_{oL} \times V_o}$$

Where ΔV_{OL} is the allowable V_o deviation during the load transient. $\Delta I_{o(max)}$ is the maximum step load current. Please note that the impact of ESL, ESR, control loop response, transient load slew rate, and PWM latency is not considered in the calculation shown above. Extra capacitance is usually needed to meet the transient requirements. As a rule of thumb, we can triple the C_o that is calculated above as a starting point, and then optimize the design based on the bench measurement. In this case, to meet the transient load requirement (i.e.

ΔV_{OL}= 30 mV, $\Delta I_{o(max)}$ = 9 A), select C_o = ~600 µF. For more accurate estimation of C_o, a simulation tool should be used to aid the design.

17.6 Bootstrap Capacitor

For most applications, a 0.1 µF ceramic capacitor is recommended for bootstrap capacitor placed between PHASE and BOOT Pin. For applications requiring PV_{in} equal to or above 14 V, a small resistor of 1~2 Ω should be used in series with the BOOT pin to ensure the maximum SW node spike voltage does not exceed 20 V.

17.7 VIN and Vcc/LDO bypass Capacitor

Please see the recommendation in 13.4 on the internal LDO. A 4.7µF MLCC is selected for the Vcc/LDO bypass capacitor and a 4.7 µF MLCC is selected for the VIN bypass capacitor.

17.8 Design Recommendations

Listed below are the design recommendations for proper device operation:

- A 100 Ohm minimum load resistor should be connected across the output
- Add a 0.1 uF and 1 uF ceramic cap across PVIN and PGND
- Add 0.1 uF and 4.7 uF across VDRV to PGND.
- The internal LDO should not be used to power external devices

18 Layout Recommendations

PCB layout is very important when designing high frequency switching converters. Layout will affect noise pickup and can cause a good design to perform with less than expected results. The following design guidelines are recommended to achieve the best performance.

- Bypass capacitors, including input/output capacitors, VIN, VCC and VDRV bypass capacitors, should be placed as close to the corresponding pins as possible.
- Place bypass capacitors from TDA38740/725 power input (Drain of Control MOSFET) to PGND (Source of Synchronous MOSFET) to reduce noise and ringing in the system. The output capacitors should be terminated to a ground plane that is away from the input PGND to mitigate the switching spikes on the Vo. The bypass capacitor shared by VCC and VDRV should be terminated to PGND.
- Place a boot strap capacitor near the TDA38740/725 BOOT and PHASE pin as close as possible to minimize the loop inductance.
- SW node copper should only be routed on the top layer to minimize the impact of switching noise.
- Connect the AGND pin to the PGND pad through a single point connection. On the TDA38740/725 demo board, the AGND pin is connected to the exposed PGND pad with a copper trace.
- Via holes can be placed on PVin and PGND pads to aid thermal dissipation.
- Wide copper polygons are desired for PVin and PGND connections in favor of power loss reduction and thermal dissipation. Sufficient via holes should be used to connect power traces between different layers.
- Output voltage sensing in TDA38740/725 is done differentially using the VOSENP and VOSENM pins.
    - A pair of PCB traces with at least 15 mil trace width, running close to each other and away from any noise sources such as inductors and SW nodes, should be used to implement Kelvin sensing of the voltage across a high-frequency bypass capacitor of 0.1 µF or higher.
    - The ground connection of the remote sensing signal must be terminated at the VOSENM pin.
    - The Vo connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor terminated at VOSENM pin for output voltages greater than 2.5 V.
    - Shield the pair of remote sensing lines with ground planes above and below.
    - Do **NOT** connect the VOSENM pin and the AGND pin in this configuration.
- The EN pin and configuration pins including SM_ADDRS/PROG, VBT, MODE/TON, and ILIM should be terminated to a quiet ground. On the TDA38740/725 standard demo board, they are terminated at the PGND copper plane away from the power current flow. Alternatively, they can be terminated to a dedicated AGND PCB trace.

18.1 PCB Metal and Component Placement

Evaluation has shown that the best overall performance is achieved using the substrate/PCB layout as shown in the following figures. PQFN devices should be placed to an accuracy of 0.050 mm on both X and Y axes. Self-centering behavior is highly dependent on solders and processes, and experiments should be run to confirm the limits of self-centering on specific processes.

For further information, please refer to the “Recommendations for Board Assembly of Infineon Integrated Packages without Lead” Application note https://ecmpub.infineon.com/dctm-publish/ecmdata/tech_0460/Z8F80291788.pdf.

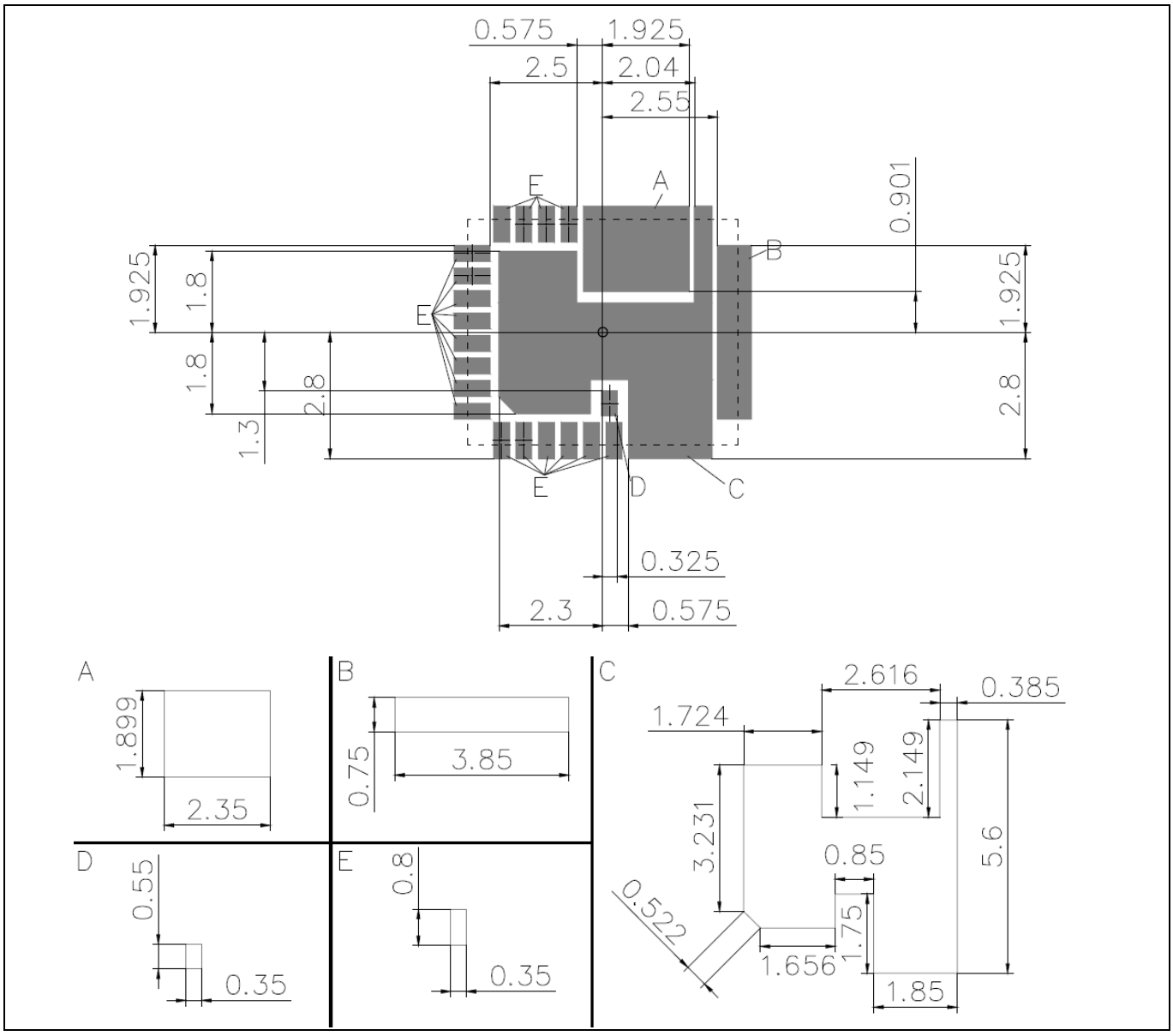


Figure 39 PCB metal pad sizing and spacing (all dimensions in mm)

18.2 Solder Resist

Infineon recommends that larger Power or Land Area pads are Solder Mask Defined (SMD.) This allows the underlying copper traces to be as large as possible, which helps in terms of current carrying capability and device cooling capability. When using SMD pads, the underlying copper traces should be at least 0.05 mm larger

(on each edge) than the Solder Mask window in order to accommodate any layer to layer misalignment. (i.e. 0.1 mm in X and Y.) When using NSMD pads, the Solder Resist Window should be larger than the Copper Pad by at least 0.025 mm on each edge, (i.e. 0.05 mm in X&Y,) in order to accommodate any layer to layer misalignment. Ensure that the solder resist in between the smaller signal lead areas is at least 0.15 mm wide, due to the high x/y aspect ratio of the solder mask strip.

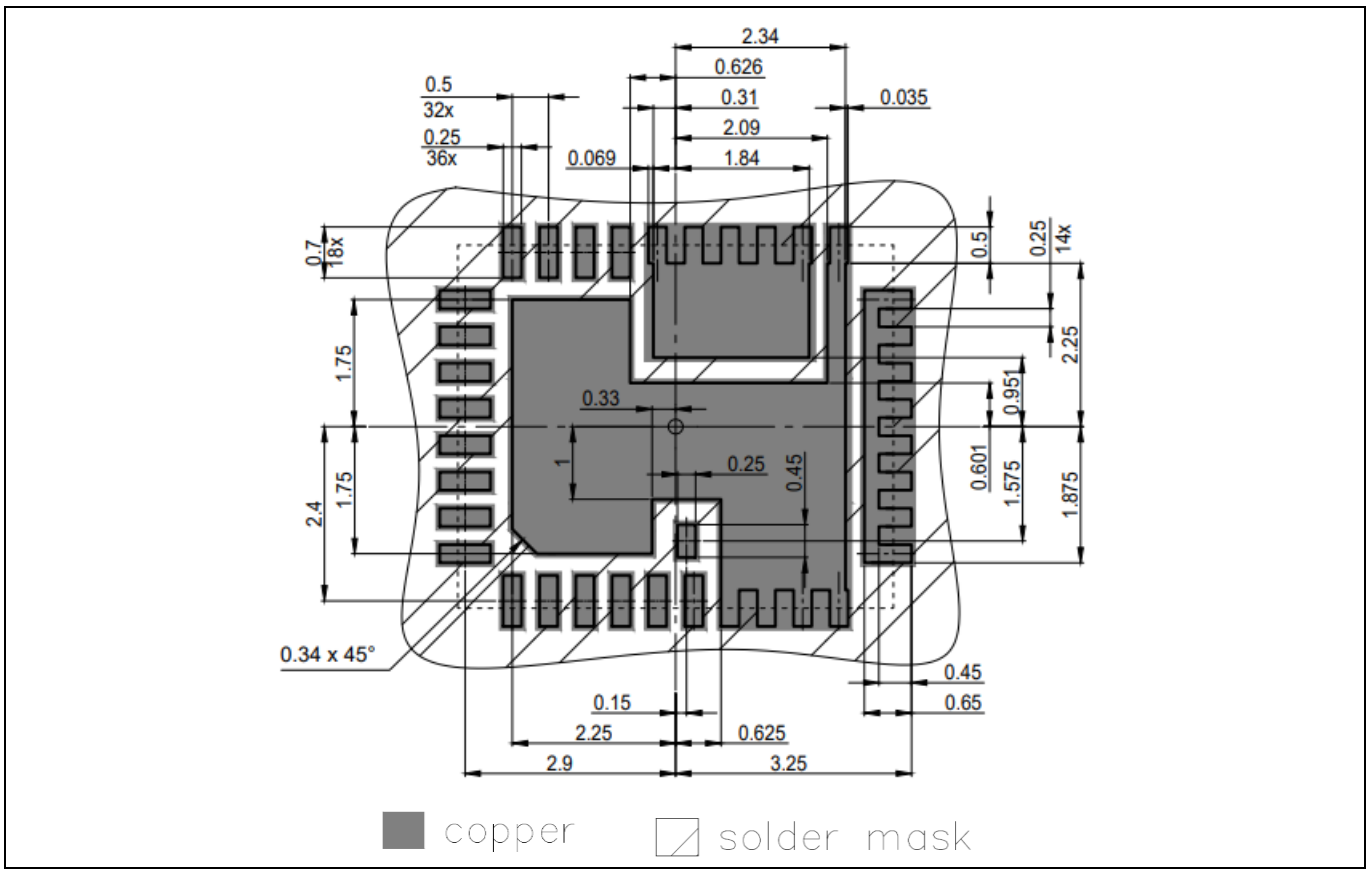


Figure 40 Solder resist

18.3 Stencil Design

Stencils for PQFN packages can be used with thicknesses of 0.100-0.250 mm (0.004-0.010”). Stencils thinner than 0.100 mm are unsuitable because they deposit insufficient solder paste to make good solder joints with the ground pad; high reductions sometimes create similar problems. Stencils in the range of 0.125 mm-0.200 mm (0.005-0.008”), with suitable reductions, give the best results.

A recommended stencil design is shown in Figure 41. This design is for a stencil thickness of 0.127 mm (0.005”). The reduction should be adjusted for stencils of other thicknesses.

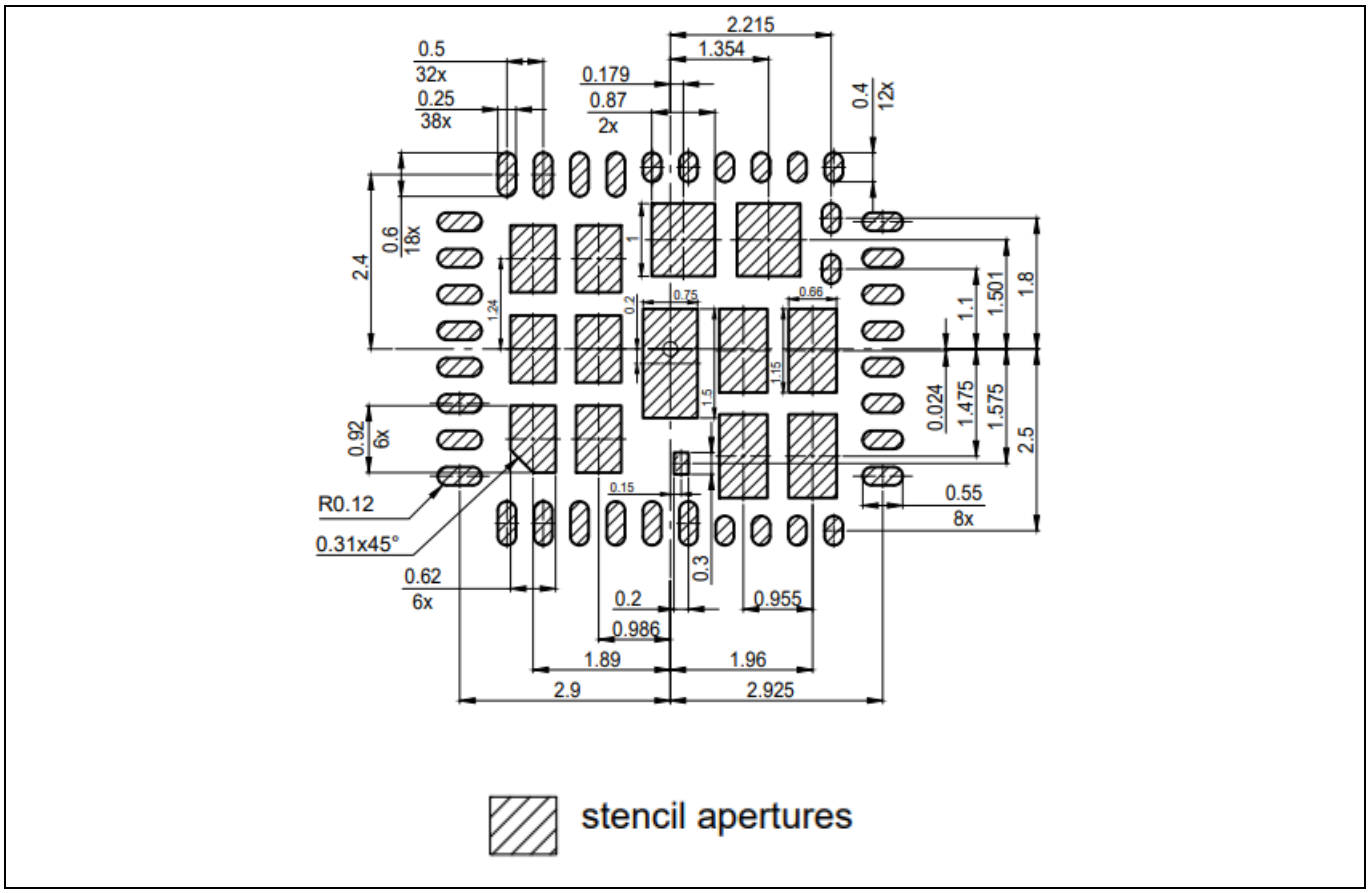


Figure 41 Stencil pad size and spacing (all dimensions in mm)

19 Package

19.1 Marking Information

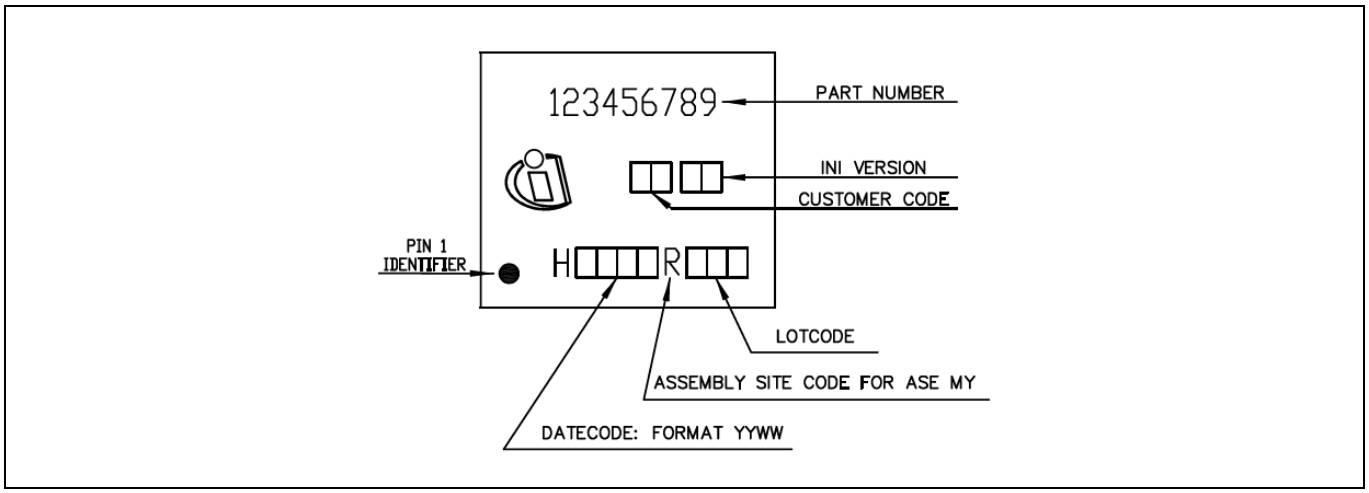


Figure 42 Package Marking

19.2 Dimensions

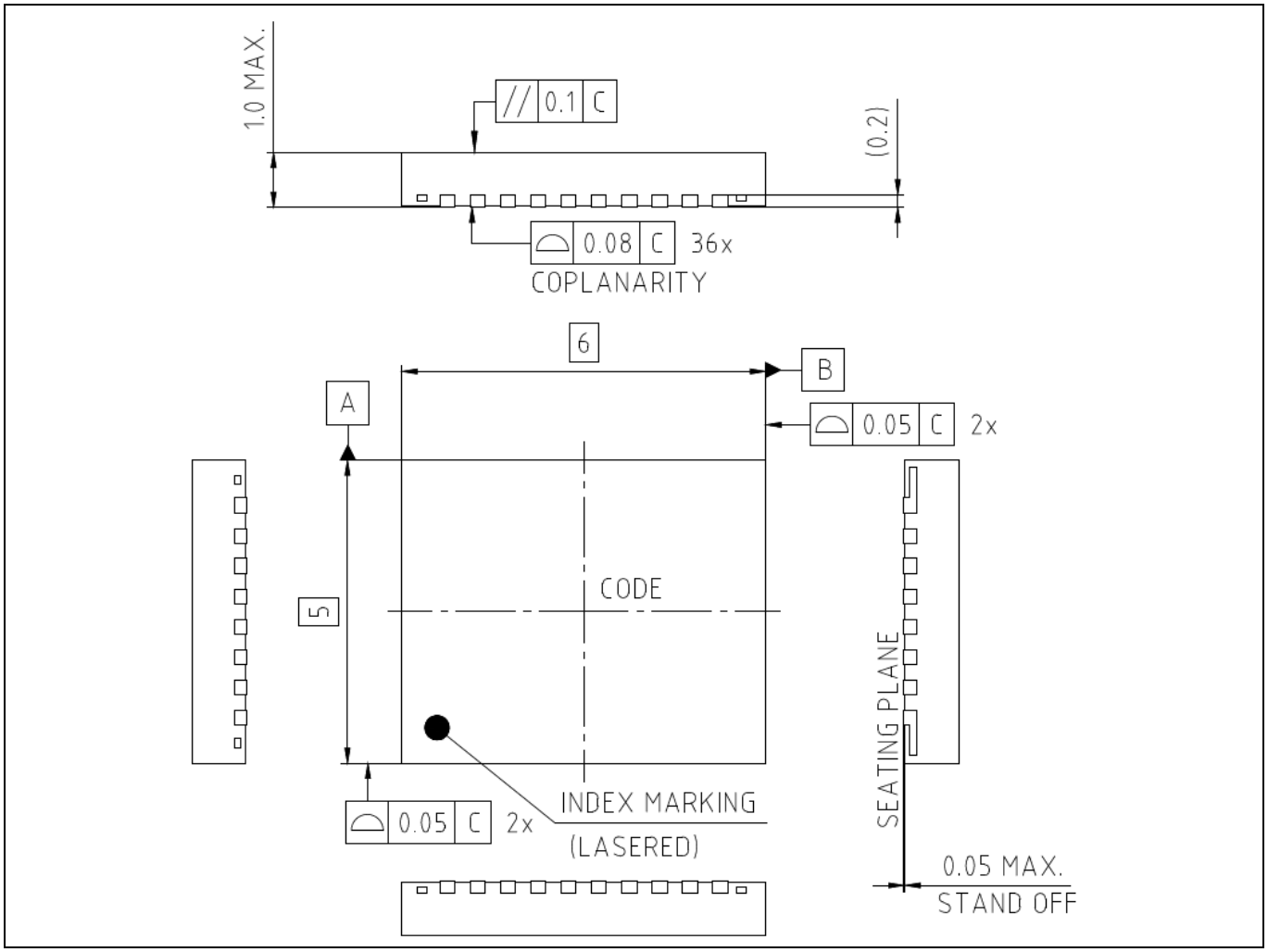
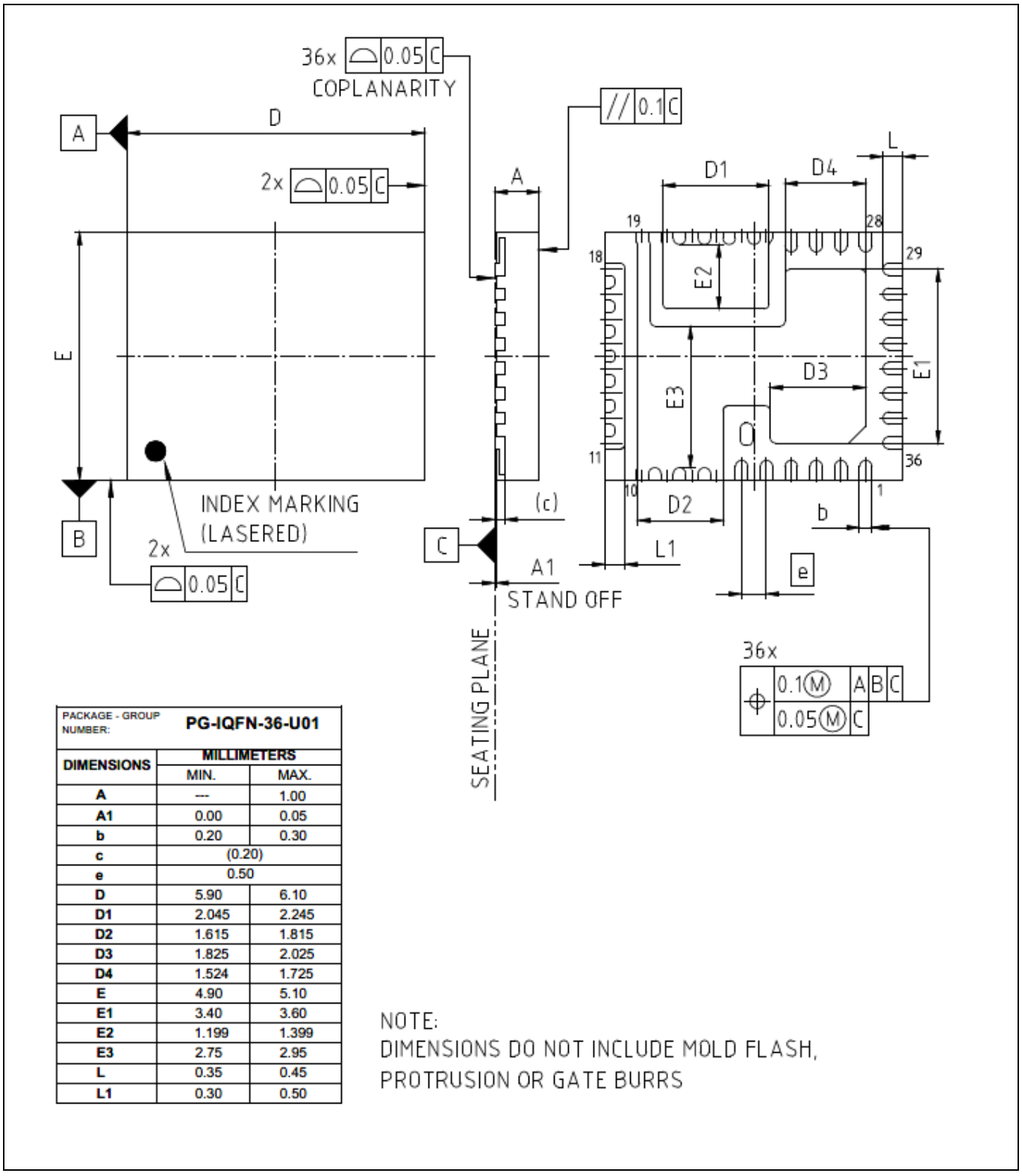


Figure 43 Package view



PACKAGE - GROUP NUMBER:	PG-IQFN-36-U01	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	---	1.00
A1	0.00	0.05
b	0.20	0.30
c	(0.20)	
e	0.50	
D	5.90	6.10
D1	2.045	2.245
D2	1.615	1.815
D3	1.825	2.025
D4	1.524	1.725
E	4.90	5.10
E1	3.40	3.60
E2	1.199	1.399
E3	2.75	2.95
L	0.35	0.45
L1	0.30	0.50

Figure 44 Package Dimensions in mm

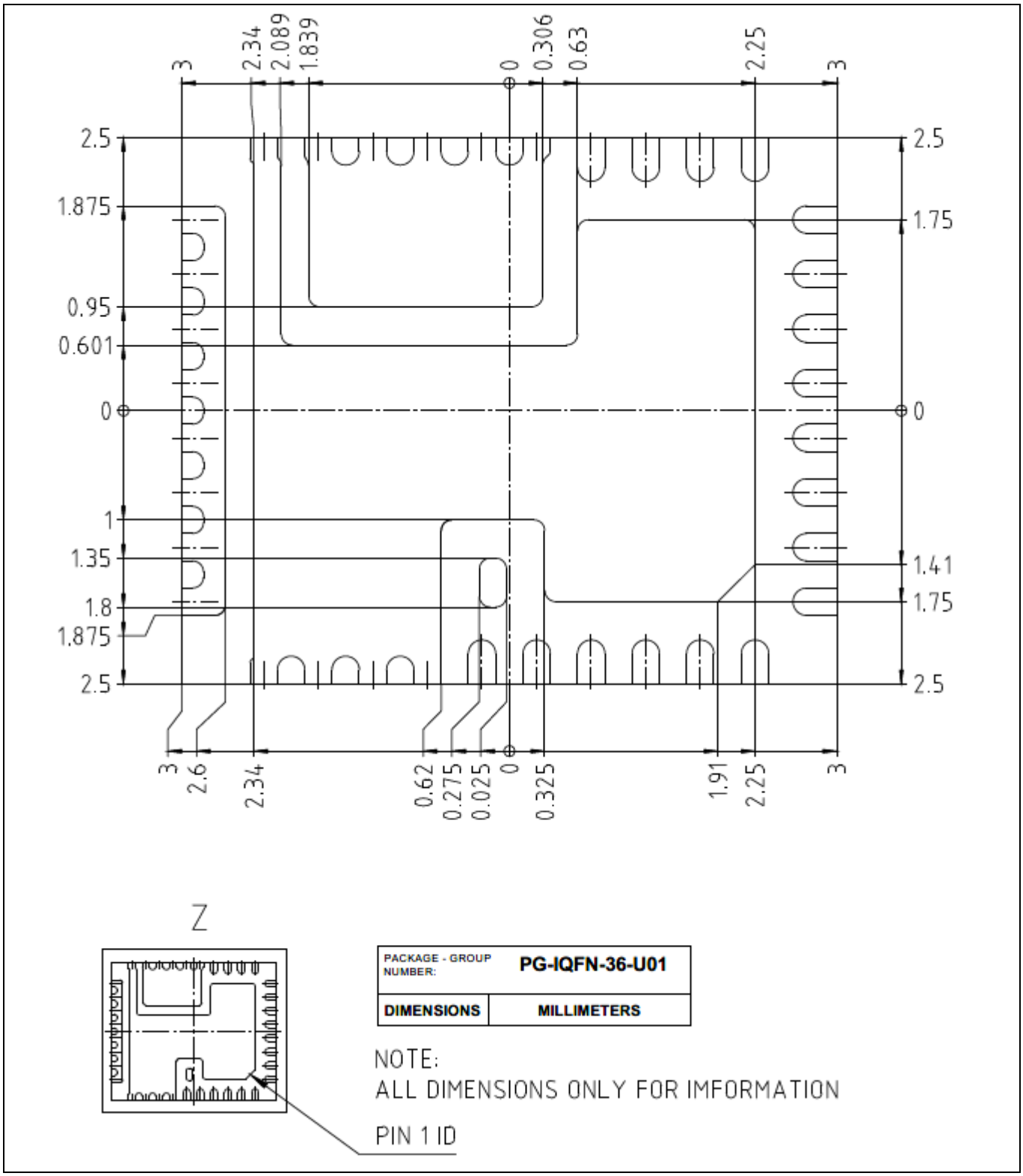


Figure 45 Package Dimensions – Pad Layout

19.3 Tape and Reel Information

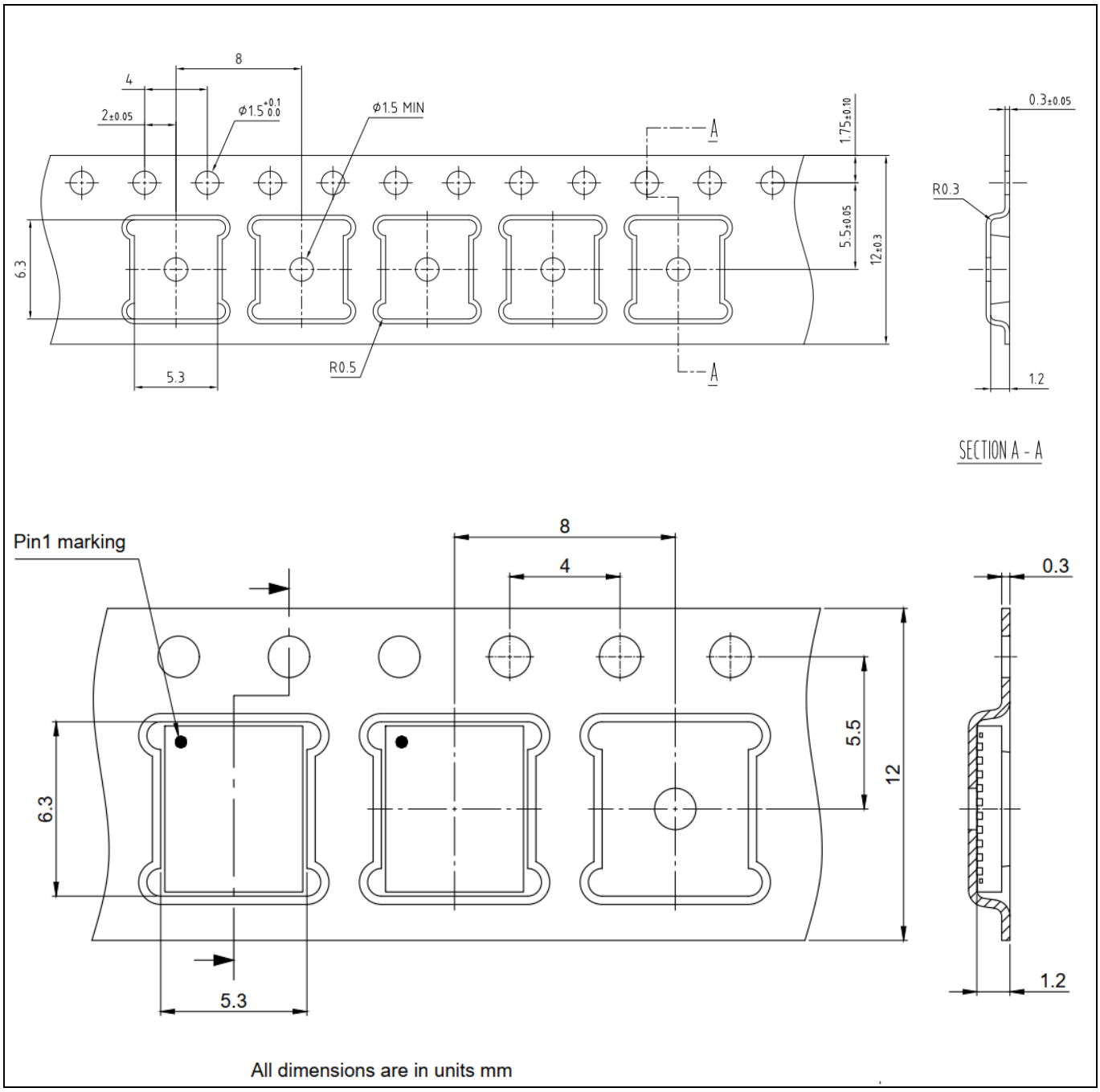


Figure 46 Dimensions and Pin 1 Orientation in Tape & Reel

20 Environmental Qualifications

Table 19

Qualification Level		Industrial	
Moisture Sensitivity		5 x 6 mm QFN Package	JEDEC Level 2 @ 260°C
ESD	**Human Body Model**	ANSI/ESDA/JEDEC JS-001, Class 2 (2000V to < 4000V)	
	Charged Device Model	ANSI/ESDA/JEDEC JS-002, Class C3 (≥ 1000V)	
RoHS2 Compliant		This product follows EU Directive 2015/863/EU amending annex II to EU Directive 2011/65/EU(RoHS) and contains Pb according RoHS exemption 7a, Lead in high melting temperature type solders	

Revision History

TDA38740/725

Revision 2024-04-18, Rev. 2.10

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-04-08	Release of final version
2.1	2022-04-13	Updated the Abs max table with VIN-PH voltage
2.2	2022-05-13	Final datasheet revision - updated block diagram and EC table
2.3	2022-08-12	Updated Multiple time programmable section
2.4	2022-08-19	corrected the number of MTP writes on page 1
2.5	2022-10-21	Added the setpoint accuracy data to table 6, updated the Pgood pull up resistor to 4.7k, updated the absolute max ratings (table 3) to align with 741 DS, Updated MTP capability of the device in section 13.2,Added description for pinstrapping in section 8
2.6	2022-11-21	Updated Prebias section, Programming Section, Absolute max ratings table, Electrical Characteristics Table, Updated page number formatting
2.7	2023-09-13	Updated the Ordering information in section 1 Added missing PMBus read and write protocols Corrected the description of the PMBus commands in table 18 Updated the OCP Fault description
2.8	2023-10-26	Updated the App note reference in Section 18, updated package drawing in Section 19
2.9	2023-12-20	Updated Table 1, Table 12, Section 13.3 and Table 18
2.10	2024-04-18	Updated Section 15.3 with OVP threshold setting, and section 16.3 VOUT_UV_FAULT_LIMIT and VOUT_OV_FAULT_LIMIT operation when relative_ovp_thresh_res=1 Updated ILIM resistor table in Section 8 Updated AOCP operation diagram in section 15.1

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