Optimos™ Powerstage

TDA21462

1 Description

- High frequency, low profile dc-dc converters
- Voltage Regulators for CPUs, GPUs, and DDR memory arrays

The TDA21462 power stage contains a low quiescent-current synchronous buck gate-driver IC co-packaged with Schottky diode, and high-side and low-side MOSFETs. The package is optimized for PCB layout, heat transfer, driver/MOSFET control timing, and minimal switch node ringing when layout guidelines are followed. The gate driver and MOSFET combination enables higher efficiency at the lower output voltages required by cutting edge CPU, GPU and DDR memory designs.

The TDA21462 internal MOSFET current sense algorithm with temperature compensation achieves superior current sense accuracy versus best-in-class controller-based inductor DCR sense methods. Protection includes cycle-by-cycle over current protection with programmable threshold, VCC/VDRV UVLO protection, phase fault detection, IC temperature reporting and thermal shutdown. The TDA21462 also features auto-replenishment of the bootstrap capacitor to prevent over-discharging. The TDA21462 features a deep-sleep power saving mode, which greatly reduces the power consumption when the multiphase system enters PS3/PS4 mode.

Operation at switching frequency as high as 1.5 MHz enables high performance transient response, allowing reduction of output inductance and output capacitance while maintaining industry leading efficiency.

The TDA21462 is optimized for CPU core power delivery in server applications. The ability to meet the stringent requirements of the server market also makes it ideally suited for powering GPU and DDR memory designs.

2 Features

- Co-packaged driver, Schottky diode, and high-side and low-side MOSFETs
- 5-mV/A on-chip MOSFET current sensing with temperature compensated reporting
- Input voltage (VIN) range of 4.25 V to 16 V
- VCC and VDRV supply of 4.25 V to 5.5 V
- Output voltage range from 0.25 V up to 5.5 V
- 70A Output Over-Current Protection (OCP) capability
- Operation up to 1.5 MHz
- VCC/VDRV under voltage lockout (UVLO)
- 8-mV/°C temperature analog output
- Thermal shutdown and fault flag
- Cycle-by-cycle over current protection with programmable threshold and fault flag
- MOSFET phase fault detection and flag
- Auto-replenishment of bootstrap capacitor
- Deep-sleep mode for power saving
- Compatible with 3.3-V tri-state PWM input
- Body-Braking load transient support
- Small 5 mm x 6 mm x 1 mm PQFN package
- Lead free RoHS compliant package

Table 1 Product Identification

Part Number	Temp Range	Package	Marking
TDA21462	-40°C to 125°C	PQFN 5 mm x 6 mm	TDA21462

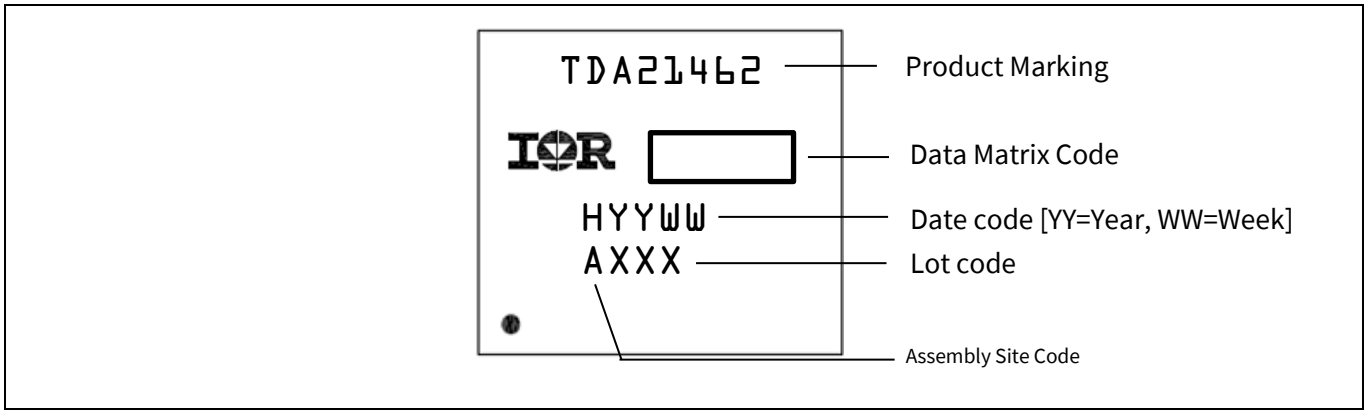


Figure 1 Picture of the Product

3 Description

3.1 Pinout

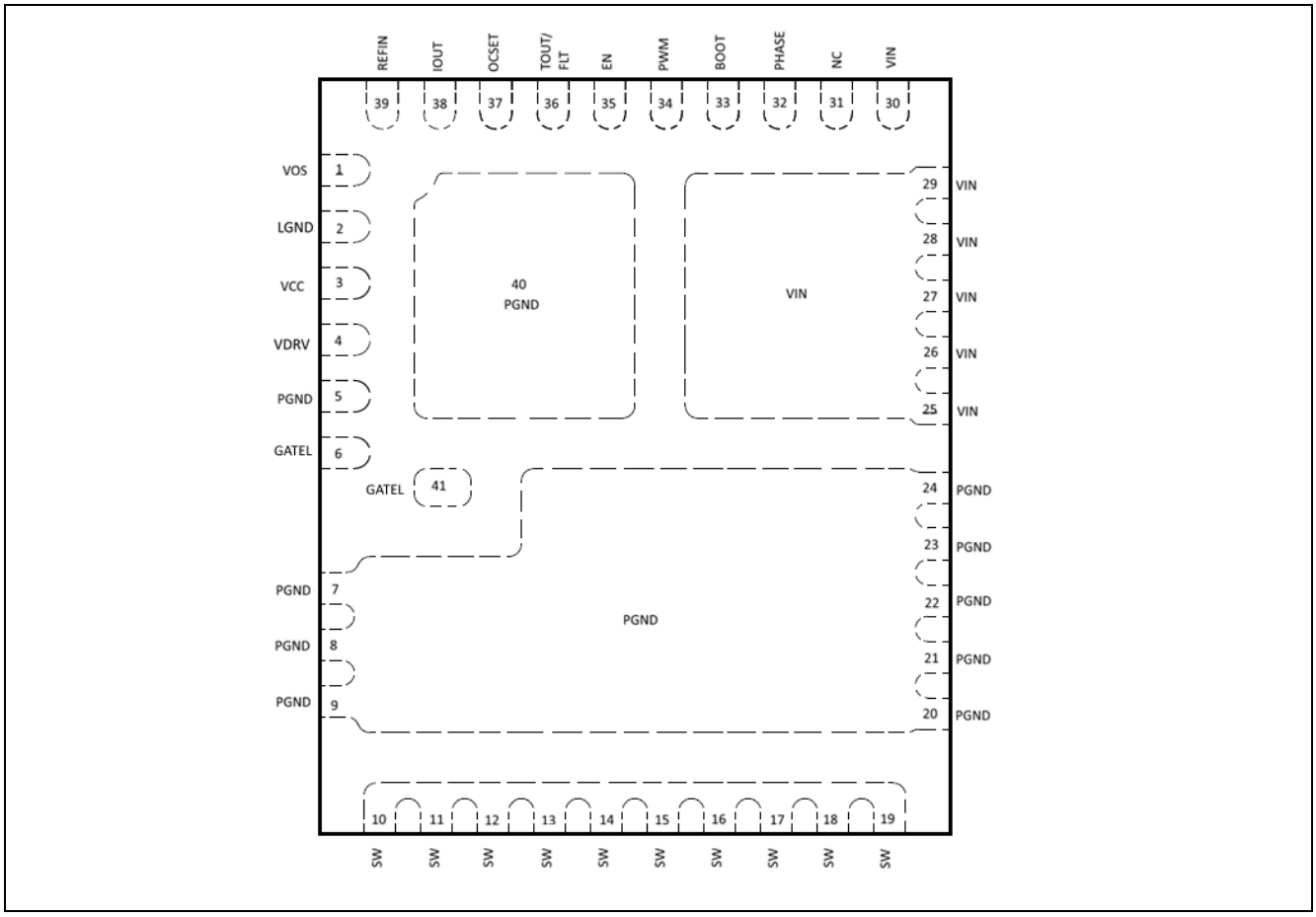


Figure 2 Pinout, Numbering and Name of Pins (transparent top view)

4 Block Diagram

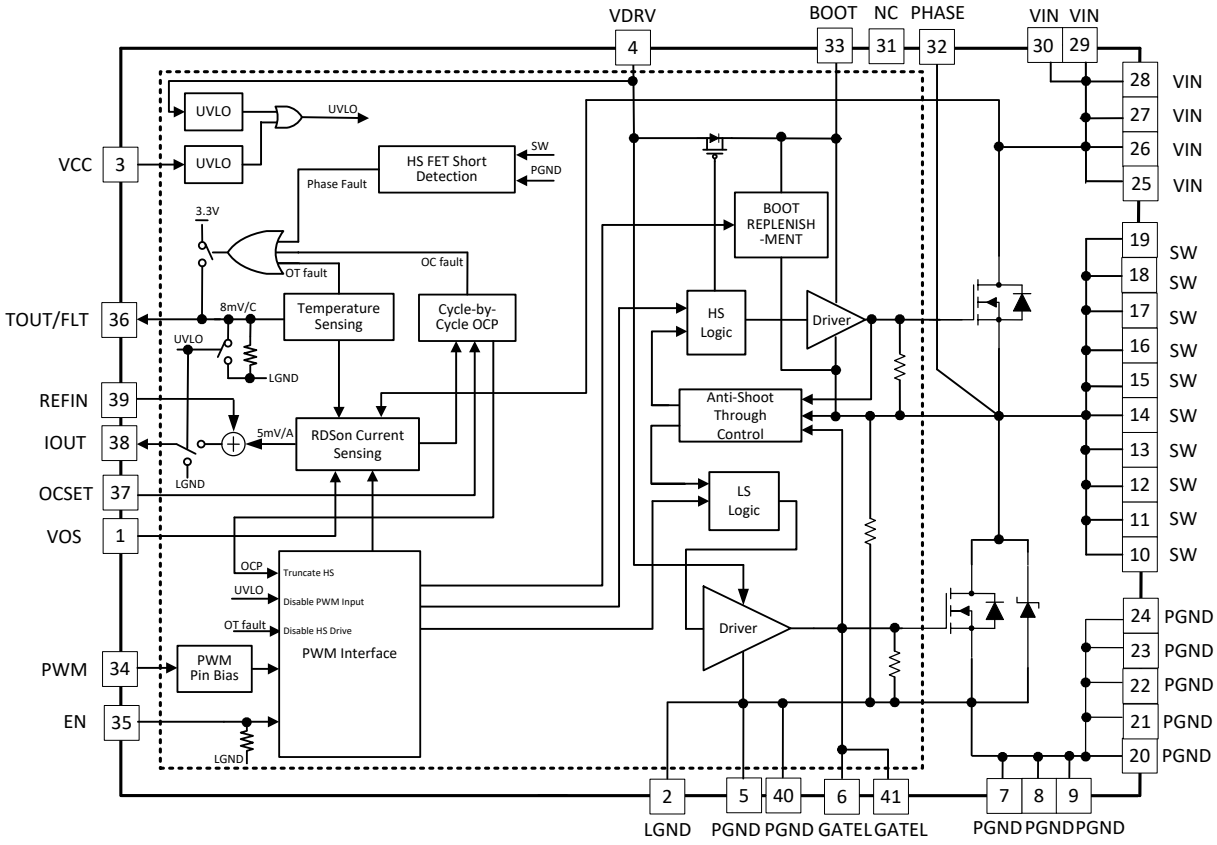


Figure 3 Block Diagram

Block Diagram

Table 2 I/O Signals

Pin No.	Name	Pin Type	Buffer Type	Function
1	VOS	I	Analog	Connect to output of the converter. It serves as the VOUT voltage sense input for inductor current emulation during body braking. Kelvin connection in layout is not required.
6, 41	GATEL	I/O	Analog	Low-side MOSFET driver pin that can be connected to a test point in order to observe the waveform.
10-19	SW	O	Analog	High Current switching node connection of the synchronous buck converter.
32	PHASE	I	Analog	Internal connection to the high-side MOSFET source. For Bootstrap capacitor connection only.
33	BOOT	I	Analog	Bootstrap capacitor connection. The bootstrap capacitor provides the charge to turn on the high-side MOSFET. Connect a minimum 0.22-µF, X7R ceramic capacitor from BOOT to PHASE pin. For VIN > 13.2 V, a 2-Ω bootstrap resistor is required.
34	PWM	I/O	Logic	3.3-V logic level PWM input. PWM input: “High” turns high-side MOSFET on; floating or driving PWM to the “Tri-state” turns both MOSFETs off; “Low” turns low-side MOSFET on.
35	EN	I	Logic	Pulling EN high enables the driver; pulling EN low disables the driver and enters ultra-low quiescent current mode. Floating this pin is not recommended, however a low current pull-down is embedded to keep the driver off if the pin is floating. The EN pin is VCC tolerant.
36	TOUT/FLT	O	Analog	The voltage at this pin is defined by the equation 8 mV * (Celsius Temperature) + 0.6 V. This pin will be pulled up to 3.3 V under severe over temperature, over current or phase fault condition.
37	OCSET	I/O	Analog	Program the over-current threshold by placing a resistor from OCSET pin to LGND. Floating OCSET or directly tying to VCC gives a fixed 80-A typical over-current threshold.
38	IOUT	O	Analog	Sensed current output signal referenced to the REFIN pin. V(IOUT – REFIN) voltage represents current information at 5 mV/A.
39	REFIN	I/O	Analog	The reference supply voltage for the IOUT information. This pin should be tied to a fixed voltage between 1.1 V and 2.0 V. The bias rails from typical PWM controllers are normally utilized with no additional decoupling needed at the power stage.

Block Diagram

Table 3 Power Supply

Pin No.	Name	Pin Type	Buffer Type	Function
4	VDRV	POWER	–	The gate driver supply. Connect a X7R, 1-µF ceramic capacitor between VDRV and PGND. VDRV should be connected to the +5 V power supply.
3	VCC	POWER	–	Bias voltage for control logic. Connect a X7R, 1-µF ceramic capacitor between VCC and LGND, and a 1-Ω resistor between VCC and VDRV.
25-30	VIN	POWER	–	4.25-V to 16-V high current input voltage connection. Place a 0402, X7R, 0.1-µF capacitor and a 0402 or 0603, X7R, 1-µF capacitor close to VIN pin and PGND pin. Also connect at least one X7R, 10-µF ceramic capacitor.

Table 4 Ground Pins

Pin No.	Name	Pin Type	Buffer Type	Function
2	LGND	GND	–	Signal ground. All signals are referenced to this pin.
5, 7-9, 20-24, 40	PGND	GND	–	Power ground. It is also the power ground of the low-side MOSFET.

Table 5 Not Connected

Pin No.	Name	Pin Type	Buffer Type	Function
31	NC	–	–	Leave this pin unconnected.

5 Electrical Specification

5.1 Absolute Maximum Ratings

Note: T_A = 25 °C

Stresses above those listed in Table 6 “Absolute Maximum Ratings” may cause permanent damage to the device. These are absolute stress ratings only and operation of the device is not implied or recommended at these or any other conditions in excess of those given in the operational sections of this specification. Exposure over values of the recommended ratings for extended periods may adversely affect the operation and reliability of the device.

Table 6 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Frequency of PWM input	f_{SW}	0.2	–	1.5	MHz	
Maximum average load current	I_{OUT}	–	–	OCP Threshold	A	
Input Voltage	V_{IN}	-0.30	–	25	V	Pin VIN
Logic supply voltage	V_{CC}	-0.30	–	6	V	Pin VCC
Driver voltage	V_{DRV}	-0.30	–	6	V	Pin VDRV
Switch node voltage	V_{SW}	Below -5 V for 5 ns, -0.3 V DC	–	32 V for 2ns, 25 V DC	V	Pin SW
PHASE voltage	V_{PHASE}	Below -5 V for 5 ns, -0.3 V DC	–	32 V for 2ns, 25 V DC	V	Pin PHASE
VIN – PHASE voltage	V_{VIN} - V_{PHASE}	Below -5 V for 5 ns, -0.3 V DC		32 V for 2ns, 25 V DC	V	VIN – PHASE
BOOT voltage	V_{BOOT}	Below -0.3 V for 5 ns, -0.3 V DC	–	29	V	Pin BOOT
	$V_{BOOT-PHASE}$	-0.3	–	7 V for 5 ns, 6 V DC	V	BOOT – PHASE
EN voltage	V_{EN}	-0.3	–	VCC + 0.3	V	Pin EN
PWM voltage	V_{PWM}	-0.3	–	VCC + 0.3	V	Pin PWM
TOUT	V_{TOUT}	-0.3	–	VCC + 0.3	V	Pin TOUT/FLT
IOUT	V_{IOUT}	-0.3	–	VCC + 0.3	V	Pin IOUT
VOS	V_{OS}	-0.3	–	VCC + 0.3	V	Pin VOS
OCSET	V_{OCSET}	-0.3	–	VCC + 0.3	V	Pin OCSET
REFIN	V_{REFIN}	-0.3	–	3.5	V	Pin REFIN
Junction temperature	T_{Jmax}	-40	–	150	°C	–
Storage temperature	T_{STG}	-65	–	150	°C	–

Note: All rated voltages are relative to voltages on the LGND and PGND pins unless otherwise specified.

5.2 Thermal Characteristics

Table 7 Thermal Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal Resistance-Junction to PCB	θ_{JC_PCB}	–	1.5	–	K/W	Referenced to Pin 24
Thermal Resistance-Junction to top of package	θ_{JC_Top}	–	16.7	–		–
Thermal Resistance to Ambient	θ_{JA} Note	–	20.5	–		–

Note: Thermal Resistance (θ_{JA}) is measured with the component mounted on a highly effective thermal conductivity test board in free air.

5.3 Recommended Operating Conditions

Table 8 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Voltage	V_{IN}	4.25	–	16	V	
MOSFET Driver Voltage	V_{DRV}	4.25	–	5.5		
Logic Supply Voltage	V_{CC}	4.25	–	5.5		
PWM Switching Frequency	f_{sw}	200	–	1500	kHz	
Reference Voltage	V_{REFIN}	1.1	–	2.0	V	Additional fixed current sense amplifier offset of –0.35 A at VREFIN = 1.8 V
Junction Temperature	$T_{JUNCTION}$	-40	–	+125	°C	

5.4 Electrical Characteristics

Note: $V_{DRV} = V_{CC} = 5$ V, $T_J = 65$ °C, $V_{REFIN} = 1.2$ V, $f_{sw} = 600$ kHz, $V_{out} = 1.8$ V

Table 9 Voltage Supply, Biasing Current

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
UVLO VCC / VDRV Rising	V_{UVLO_RISE}	-	3.85	4.0	V	
UVLO VCC / VDRV Falling	V_{UVLO_FALL}	3.3	3.45	-		
Hysteresis	V_{UVLO_HYS}		0.4			
Driver Current	I_{VDRV}	–	20	–	mA	EN = 3.3 V, f_{SW} = 600 kHz, D=15%
		–	15	–	µA	EN= 3.3 V , PWM floating
		–	0.2	–	µA	EN= 0 V
Supply Current	I_{VCC}	-	3.2	–	mA	EN= 3.3 V
		-	45	–	µA	EN= 0 V
VIN Bias Current	I_{VIN}	-	35	–	µA	VIN=15 V, EN= 3.3 V, V(PWM) = 1.7 V
		-	0.1	–	µA	EN= 0 V

Table 10 Current Sense and Temperature Sense

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
IOUT	Current Sense Gain	A_{CS}	4.8	5	5.2	mV/A	
	Offset at Trim	A_{CS_OST}	-0.8	-	0.8	A	0-A load

Table 11 Temperature Sense and Fault Communication

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
TOUT	Temperature Sense Slope	A_{TOUT_GAIN}	7.8	8.0	8.2	mV/°C	0°C ≤ T_J ≤ 125°C, Note 1
	Temperature Sense Offset Voltage	V_{TOUT_OFFSET}	1.108	1.120	1.132	V	T_J = 65°C, 0.6 V + 8 mV/°C * T_J

Table 12 Other Logic Functions, Inputs/Outputs And Thresholds

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
EN	Enable Power-on Delay	$t_{EN\_DELAY\_ON}$	-	5	–	µs	PWM=0. Measured from EN rising edge to GATEL > 1 V.
	Enable Power-off Delay	$t_{EN\_DELAY\_OFF}$	-	50	–	ns	PWM=0. Measured from EN falling edge to GATEL < 4 V.
	Internal Pull-down Resistance	R_{EN_PULLDN}	-	450	–	kΩ	EN floating
	Input High Voltage	V_{EN_HIGH}	2	-	-	V	
		V_{EN_LOW}	-	-	0.8		
PWM	PWM Input High Threshold	V_{IH}	2.4	-	-	V	PWM Low or Tri-state to High
	PWM Input Low Threshold	V_{IL}	-	-	0.8	V	PWM High or Tri-state to Low
	PWM Hysteresis	I_{PWM_HYS}	-	160	-	mV	Active to Tri-state or Tri-state to Active

Protection

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
OTP	Over Temp Rising Threshold	T_{OTP_RISE}	-	140	-	°C	TOUT/FLT pulled high, Note 1
	Over Temp Falling Threshold	T_{OTP_FALL}	-	120	-	°C	TOUT/FLT released, Note 1
PHASE FAULT	High-side MOSFET Short Threshold	V_{PHSFLT_TH}	-	850	-	mV	V(SW) – V(PGND)
	TOUT/FLT Delay	N_{FLT_DELAY}	-	7	-	Cycle	PWM High-Low Cycles to TOUT/FLT high
OCP	Programmable Over-Current Threshold Range	I_{OCP}	20	-	-	A	Program through R_{OCSET}
	Constant Over-Current Threshold	I_{OCP_CONST}	-	70	-	A	OCSET open or connected to VCC
	TOUT/FLT Delay	t_{FLT_DELY}	10	-	-	Cycle	PWM High-Low Cycles to TOUT/FLT high

Notes

1. Guaranteed by design but not tested in production.

6 Typical Operating Characteristics

Single Phase Circuit of Figure 12, V_{IN} = 12 V, V_{OUT} = 1.8V, f_{SW} = 600kHz, L = 150nH, VCC = VDRV = 5 V, $T_{AMBIENT}$ = 25°C, no heat sink, no air flow, 8-layer PCB board of 3.7"(L) x 2.6"(W), no PWM controller loss, no inductor loss, unless specified otherwise.

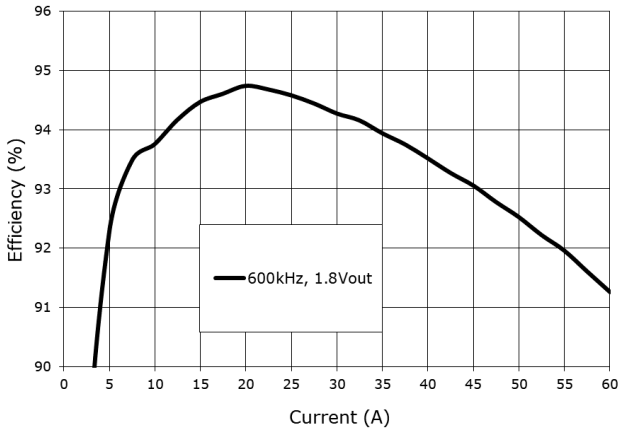


Figure 4 Power Stage Efficiency

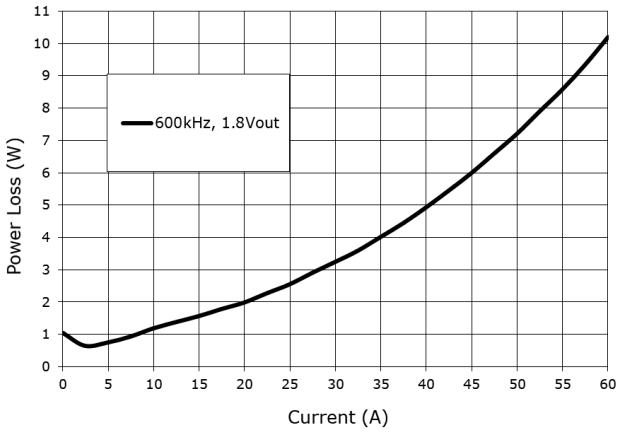


Figure 7 Power Stage Loss

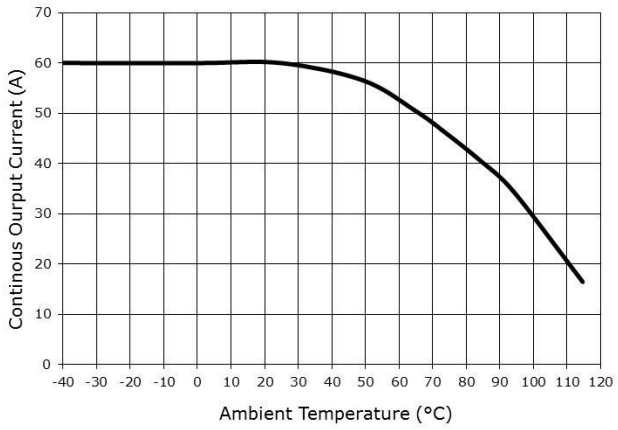


Figure 5 Thermal Derating, Tcase <= 125 °C

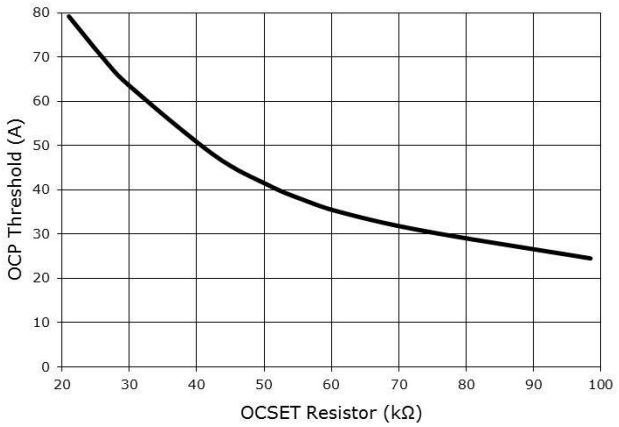


Figure 8 Programmable OCP Threshold

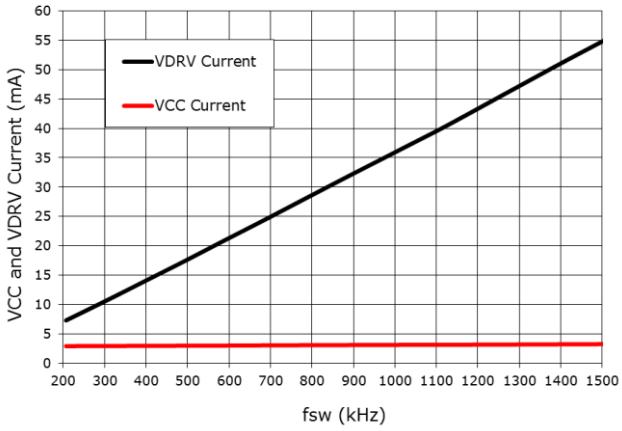


Figure 6 Vcc and Vdrv Current

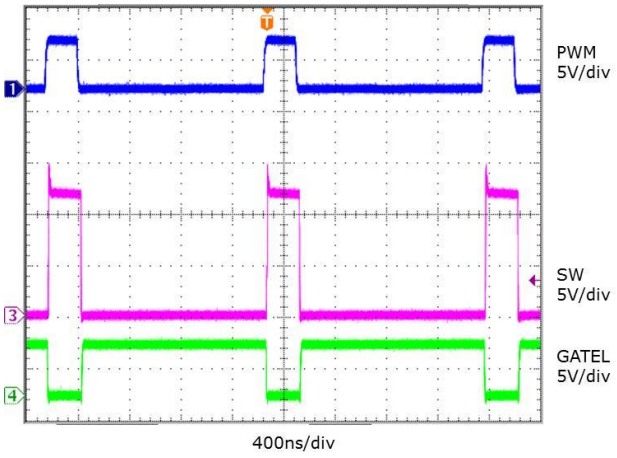


Figure 9 Switching Waveform at 0 A

7 Theory of Operation

7.1 Description

The TDA21462 contains a low-quiescent current, high-efficiency and high speed MOSFET driver optimized to drive a pair of co-packaged high-side and low-side N-channel MOSFETs with Schottky diode at frequency up to 1.5 MHz. Dc-dc controllers using traditional inductor DCR current sense typically have reduced accuracy. Over-reporting load current reduces CPU performance, while under reporting load current compromise system level reliability by over-stressing the voltage regulator and CPU. The TDA21462 incorporates a novel MOSFET-based current sense technique which improves accuracy and eliminates the complexities associated with inductor DCR sensing. Superior current sense accuracy is achieved with on-chip current sensing for enhanced system performance.

The TDA21462 provides a temperature report output at a linear slope of 8 mV / °C for monitoring power stage temperature. Multiple temperature outputs can be paralleled for reporting to Infineon's digital PWM controller.

The TDA21462 PWM input is compatible with industry standard 3.3V PWM input with tri-state.

The TDA21462 can enable Body-Braking mode by responding to PWM tri-state signals sent from the controller, quickly disabling both MOSFETs in the power stage in order to enhance transient performance or provide a high impedance output.

The TDA21462 supports diode emulation mode through the PWM tri-state signal. Controlled by Infineon's digital PWM controller, the PWM tri-state signal will force the low-side FET to be off when the inductor current is about to go negative. The light-load efficiency then can be increased by preventing conduction loss caused by negative inductor current.

The TDA21462 also supports deep-sleep power saving mode. When in deep-sleep mode, the driver will disable most of the function circuitry to greatly reduce power consumption.

The TDA21462 features a full-range of protection, including VCC/VDRV Under-Voltage-Lockout (UVLO), thermal shutdown against an internal over-temperature condition, phase fault detection of a shorted high-side MOSFET, and programmable cycle-by-cycle over-current protection due to an overload condition or saturated output inductor.

The TDA21462 also features internal protection circuitry to automatically replenish the voltage across the bootstrap capacitor. It avoids the gradual depletion of capacitor energy when the power stage sits in tri-state for a long period of time.

The TDA21462 provides an external fault signal on the TOUT/FLT pin. This pin is pulled high if a shorted high-side MOSFET, a prolonged over current event, or an over-temperature condition inside the power stage is detected.

7.2 Tri-State PWM Input

The TDA21462 PWM accepts standard three-level input signals. When the PWM input is high, the low-side MOSFET is turned off and the high-side MOSFET is turned on. When the PWM input is low, the high-side MOSFET is turned off and then the low-side MOSFET is turned on. If the PWM input is floated, the internal circuit will pull the PWM pin into the tri-state region and turn off both high-side and low-side MOSFETs.

7.3 Body-Braking Mode

The TDA21462 features the Body Braking mode to reduce output voltage overshoot during load release events by turning off the low-side MOSFET to channel the current through its body diode. The higher voltage drop of the low-side MOSFET body diode helps to discharge the stored energy in the inductor faster, which reduces the output voltage overshoot.

Body-Braking is controlled through standard PWM tri-state where both MOSFETs are placed in high impedance. The controller can momentarily drive the PWM input to the correct tri-state threshold. For better performance, no more than 100 pF parasitic capacitive load should be present on the PWM line of TDA21462.

7.4 Deep-Sleep mode

When EN is pulled low, the power stage will enter deep-sleep mode. The gate driver circuitry will be turned off immediately and most of the logic circuitry will be shut down to reduce the bias current to less than 100 µA. The IOUT output will be shorted to REFIN in deep sleep mode.

When EN toggles from low to high, the power stage will be active and able to accept PWM signals after a maximum delay of 10 µs.

7.5 Over-Temperature Protection and Flag (OTP)

An internal circuit monitors the temperature of the TDA21462. Once the temperature goes above the OTP rising threshold (140 °C), the TOUT/FLT output will be pulled high immediately and the driver will be turned off for self-preservation. The TOUT/FLT will remain high until temperature falls below the falling threshold (120 °C). The driver will then resume switching when the temperature falls below 120 °C.

7.6 Phase Fault Detection and Flag

The phase fault circuit looks at the switch node with respect to ground when PWM transits from Low to High and low-side MOSFET is still conducting. If there is a defective high-side MOSFET in the phase which causes the switch

node voltage to exceed the high-side MOSFET Short Threshold (800 mV), a phase fault will be registered. The TOUT/FLT will be pulled high to 3.3 V after 7 PWM cycles and will remain high until a PWM cycle does not result in a phase fault. PWM operation continues even when TOUT/FLT is flagged high.

The TOUT/FLT flag is monitored by Infineon controllers and could be used to manage the input supply or an e-fuse to disconnect the input voltage rail from the voltage regulator.

7.7 VCC/VDRV Under-Voltage Lockout (UVLO)

TDA21462 features internal UVLO circuitry to monitor the VCC and VDRV pins separately. When a VCC or VDRV UVLO condition is detected and remains after the glitch filter, the protection circuitry will prevent the PWM input from controlling the driver and the driver will be in tri-state with both MOSFETs off. In addition, the IOUT and TOUT/FLT pins will be pulled down to LGND to indicate there is a UVLO fault. When both VCC and VDRV UVLO faults are cleared, the TOUT/FLT and IOUT pins will be released and the driver will resume switching.

7.8 Cycle-by-cycle Over Current Protection and Flag (OCP)

This feature protects the power stage from self-destruction from repetitive high current events such as saturated inductors due to poor component selection or by incorrectly optimized control loops. These high current events could eventually lead to a shorted high-side MOSFET failure.

With cycle-by-cycle self-preservation, the current will be monitored every cycle. If the over-current threshold (default of 70 A) has been exceeded, the PWM high pulse will be truncated so that the inductor current is allowed to relax. The over-current threshold is programmable by connecting an external resistor ROCSET between pin OCSET and LGND, as shown in Figure 8. When the OCSET pin is floating or shorted to VCC, the typical over current threshold is fixed to 7c0 A.

The TOUT/FLT pin will be pulled high after a minimum 10 PWM rise-fall events when a severe over current event has been registered. PWM operation will continue while the TOUT/FLT flag is high. The TOUT/FLT fault flag will clear after three consecutive OCP-free PWM cycles are registered.

7.9 Temperature sense OUTPUT AND FAULT Flag (TOUT/FLT)

The TDA21462 incorporates an internal temperature sensing circuit that produces a linear voltage with a slope of 8 mV/°C and a 0.6 V offset at 0°C on the TOUT/FLT pin, as shown in Equation (1). In multi-phase systems the TDA21462 temperature outputs can be connected together to create a system in which the highest temperature will drive the bus. Infineon controllers can monitor this TOUT/FLT bus for temperature telemetry purposes.

$$V_{TOUT/FLT}(V) = 0.6V + 0.008V/°C \ \ x\ T_j(°C) \quad \text{.....(1)}$$

The TOUT/FLT also serves for the flag of three catastrophic faults inside the power stage, including over-temperature, phase fault, and over-current conditions. TOUT/FLT will be pulled up to 3.3 V if any catastrophic fault occurs. The TOUT/FLT can also be used as an indicator of low VCC voltage as it will be weakly pulled down to LGND under the VCC UVLO condition. In a multi-phase system where the TOUT/FLT pins are tied together, the phase which has a catastrophic fault will drive the TOUT/FLT bus and pull it up to 3.3 V.

7.10 Current Sensing and Reporting (IOUT, REFIN)

The TDA21462 integrates a novel real-time MOSFET current sense amplifier to provide real-time high-side and low-side MOSFET current information with 5%, 3-sigma accuracy. The current sense amplifier circuit in the TDA21462 is temperature compensated to track internal MOSFET variation. The current is reported to the controller as a differential voltage between the IOUT and REFIN pins with a conversion gain of 5 mV/A to represent the inductor current IL, as shown in Equation (2).

$$V_{IOUT}\,(\mathrm{V}) - V_{REFIN}\,(\mathrm{V}) = 0.005\ {}^{V}\!/\!_{A}\ \ x\, I_L(A) \quad \text{...(2)}$$

The internal current sense circuit of the TDA21462 removes the need for accurate inductor DCRs for accurate current reporting and allows the use of very low DCR inductors to maximize system efficiency.

7.11 Output Voltage Sensing (VOS)

VOS pin is not noise sensitive, and therefore, in a multiphase converter it is acceptable either to connect the VOS pin of each TDA21462 to the nearest converter output plane or to tie all VOS pins together and then connect to the converter output.

Because of limitation of the VOS sensing circuit, there is an extra current sense amplifier offset when VOS voltage is below 250 mV during a long PWM tri-state event subsequent to the first start-up of the converter. This can be avoided by connecting the VOS pin to a fixed voltage source that is close to the converter output voltage. The fixed voltage source can be the REFIN voltage or a resistor divider from the VCC voltage.

8 Design Procedures

8.1 Input Capacitors C_{VIN}

A 0402, X7R, 0.1-µF, a 0402 or 0603, X7R, 1-µF, and at least a 10-µF X7R ceramic capacitors are recommended at the VIN pins. Use of capacitors with lower ESR will improve efficiency, especially in single-phase operation. Layout guidelines and examples are available.

8.2 Bootstrap Capacitor C_{boot} and Resistor R_{boot}

A high temperature 0.22-uF or greater value 0402 X7R capacitor is recommended. It should be mounted on the same side of the PCB as the TDA21462 and as close as possible to the BOOT Pin. A Low inductance routing of the PHASE pin connection to the negative terminal of the bootstrap capacitor is strongly recommended. A bootstrap resistor in series with the bootstrap capacitor is rcommended. For applications with input voltage higher than 13.2 V, use a 2-Ω bootstrap resistor to reduce SW node voltage spike and improve switching noise immunity.

8.3 Vcc and Vdrv Decoupling Capacitors

A 1-µF X7R decoupling capacitor is required between VCC and LGND pins, and a 1-Ω VCC resistor is recommended. A 1-µF X7R decoupling capacitor is required between VDRV and PGND pins and can be directly connected to the 5-V supply. Both capacitors should be mounted on the same side of the PCB as the power stage and as close as possible to the VCC-LGND and VDRV-PGND pins. Low inductance routing between the capacitor and the TDA21462 is strongly recommended. Layout guidelines and examples are available.

8.4 Mounting of Heat Sinks

Care should be taken in the mounting of heat sinks so that even pressure is applied on the power stage surface. A thermal interface material should be used between the power stage and the heat sink to solve planarity issues and ensure even thermal conduction.

The VCC, VDRV, VIN and bootstrap capacitors are typically located on the same side of the PCB as the power stage. The height of these capacitors must be considered when using heat sinks.

8.5 Design for Electrical Test

Note that GATEL Pin (41) has NO TEST COVERAGE, and no external electrical connection should be made to this pin. Use Pin 6 if a test-point connection to GATEL is required by the application for Bed of Nails testing. Pin 41 PCB mounting pad should remain as part of the PCB footprint for optimum performance.

9 Application

9.1 Typical Multiphase Application Diagram

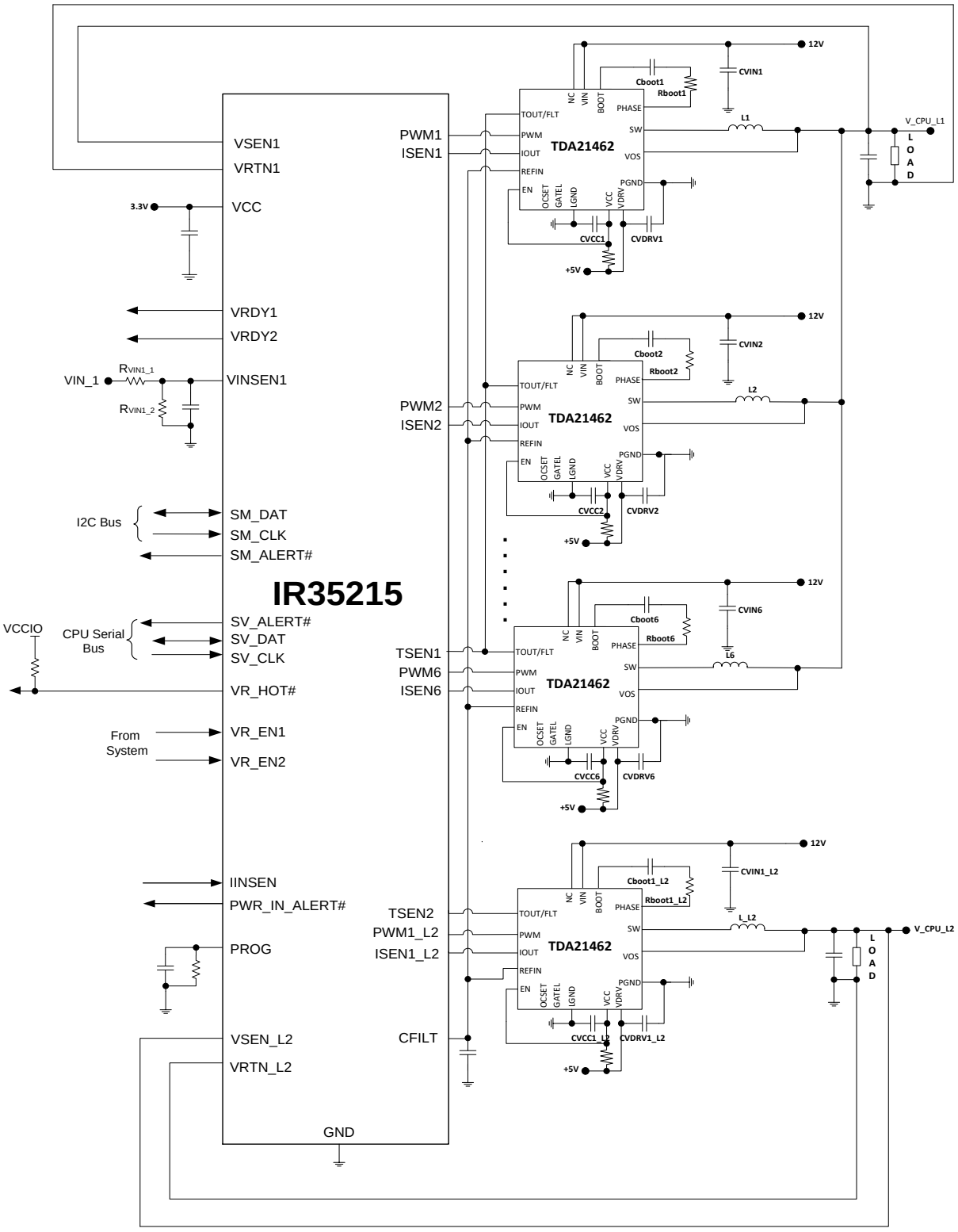


Figure 10 6+1 - Phase Voltage Regulator - Typical Application (simplified schematic)

9.2 Typical Multiphase Application Diagram

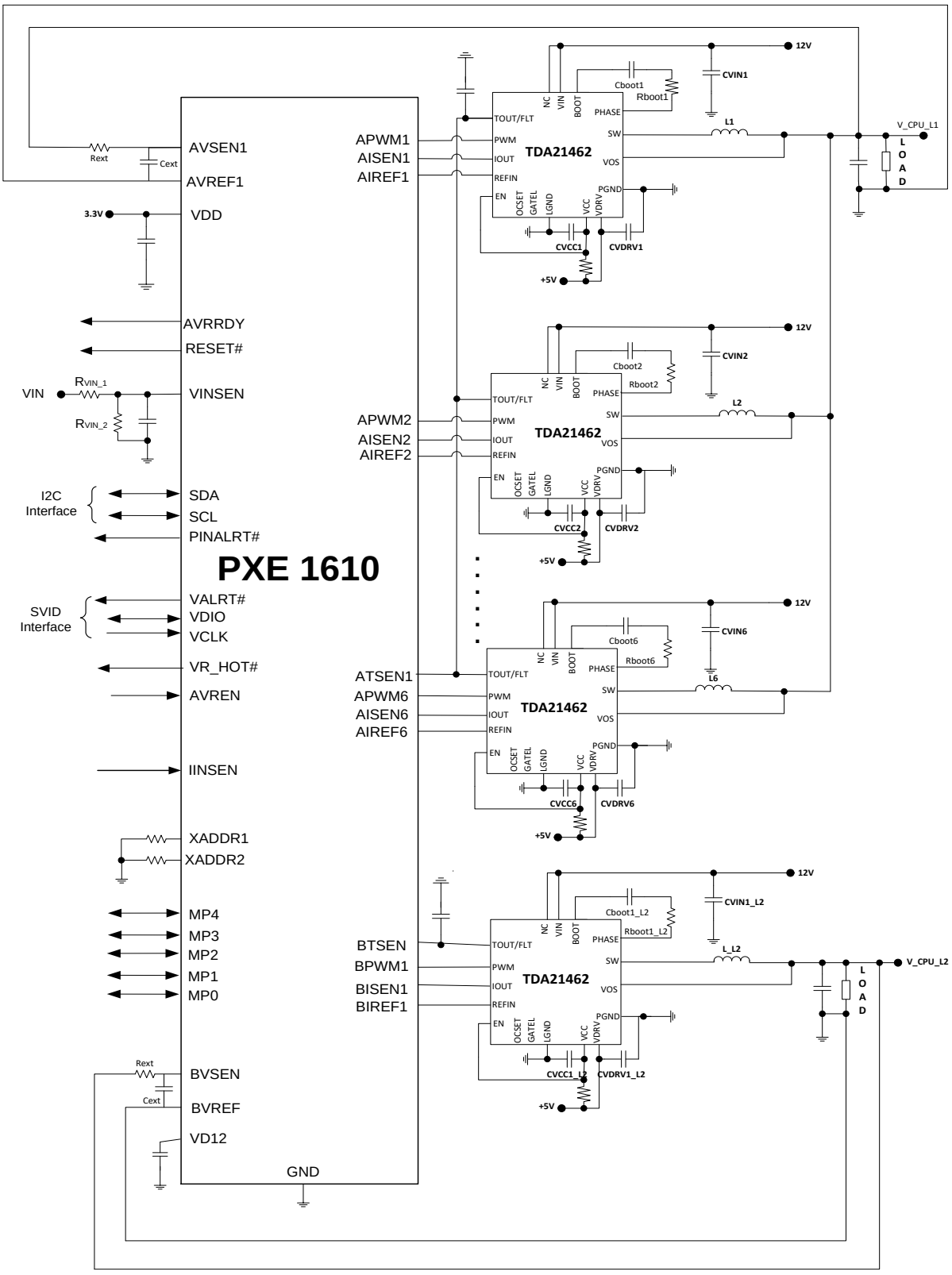


Figure 11 6+1 - Phase Voltage Regulator - Typical Application (simplified schematic)

9.3 Typical Single-phase Application Diagram

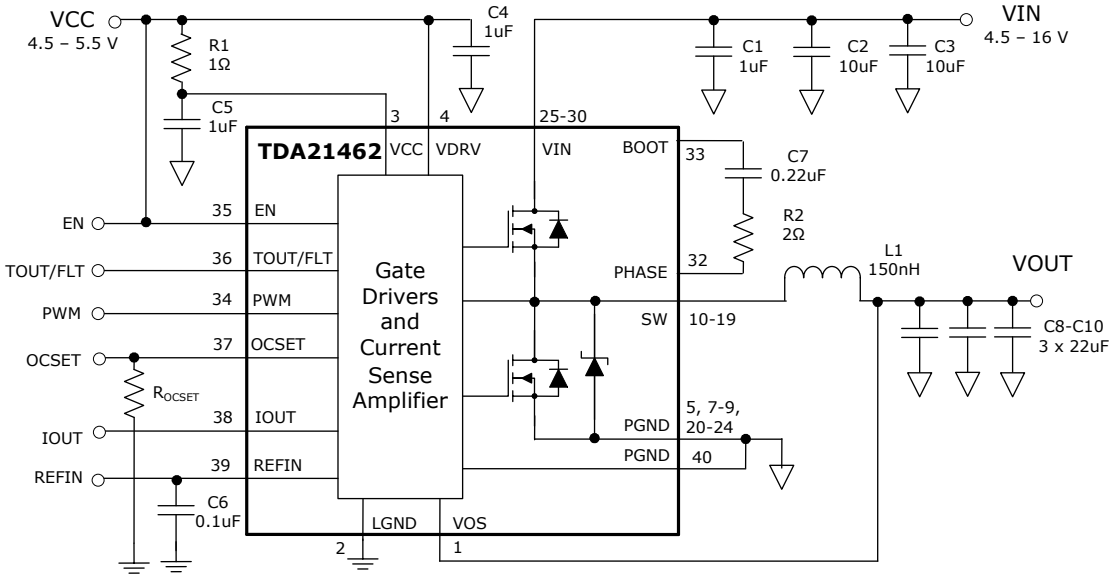
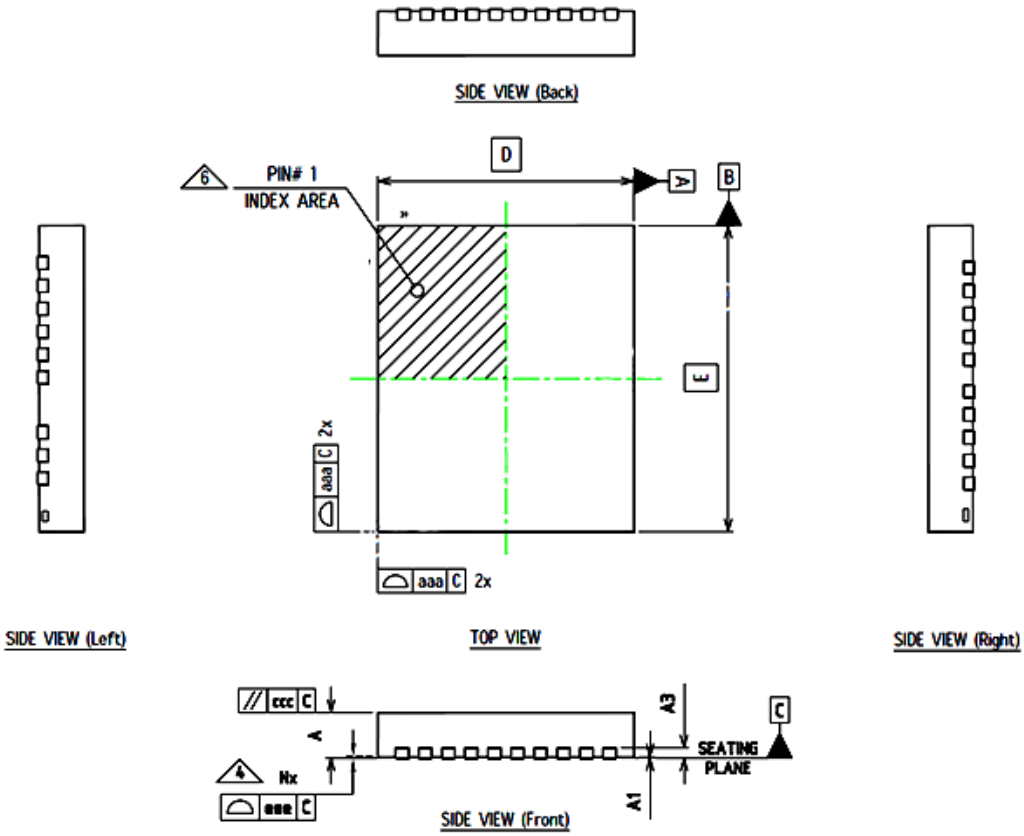


Figure 12 Typical Application Diagram for Single-Phase Voltage Regulator

10 Mechanical Drawing PQFN



Dimension Table				
Thickness / Symbol	V			Note
	MINIMUM	NOMINAL	MAXIMUM	
A	-0.10	Note 7	+0.10	7
A1	0.00	0.02	0.05	
A3	---	0.203 Ref	---	
b	0.18	0.25	0.30	5
D		5.00 BSC		
E		6.00 BSC		
e		0.45 BSC		
D1	4.393	4.443	4.493	
E1	2.05	2.10	2.15	
D2	1.70	1.75	1.80	
E2	1.90	1.95	2.00	
D3	1.768	1.818	1.868	
E3	1.90	1.95	2.00	
L	0.35	0.40	0.45	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		39		3
NOTES		1,2		

NOTE:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters.
3. N is the total number of terminals.

4. Complanarity applies to the terminals and all other bottom surface metallization.

5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.

6. The location of the marked terminal #1 identifier is within the hatched area.

7. Three packaging assembly sites support this product and are covered by this datasheet. Note that package thickness is slightly different.
"Assembly Site"= 4 has 0.9 mm nominal thickness
"Assembly Site" = E has 1 mm nominal thickness
"Assembly Site"= R has 0.9 mm nominal thickness

Figure 13 Mechanical Dimensions of Package (Top View and Side View) in mm

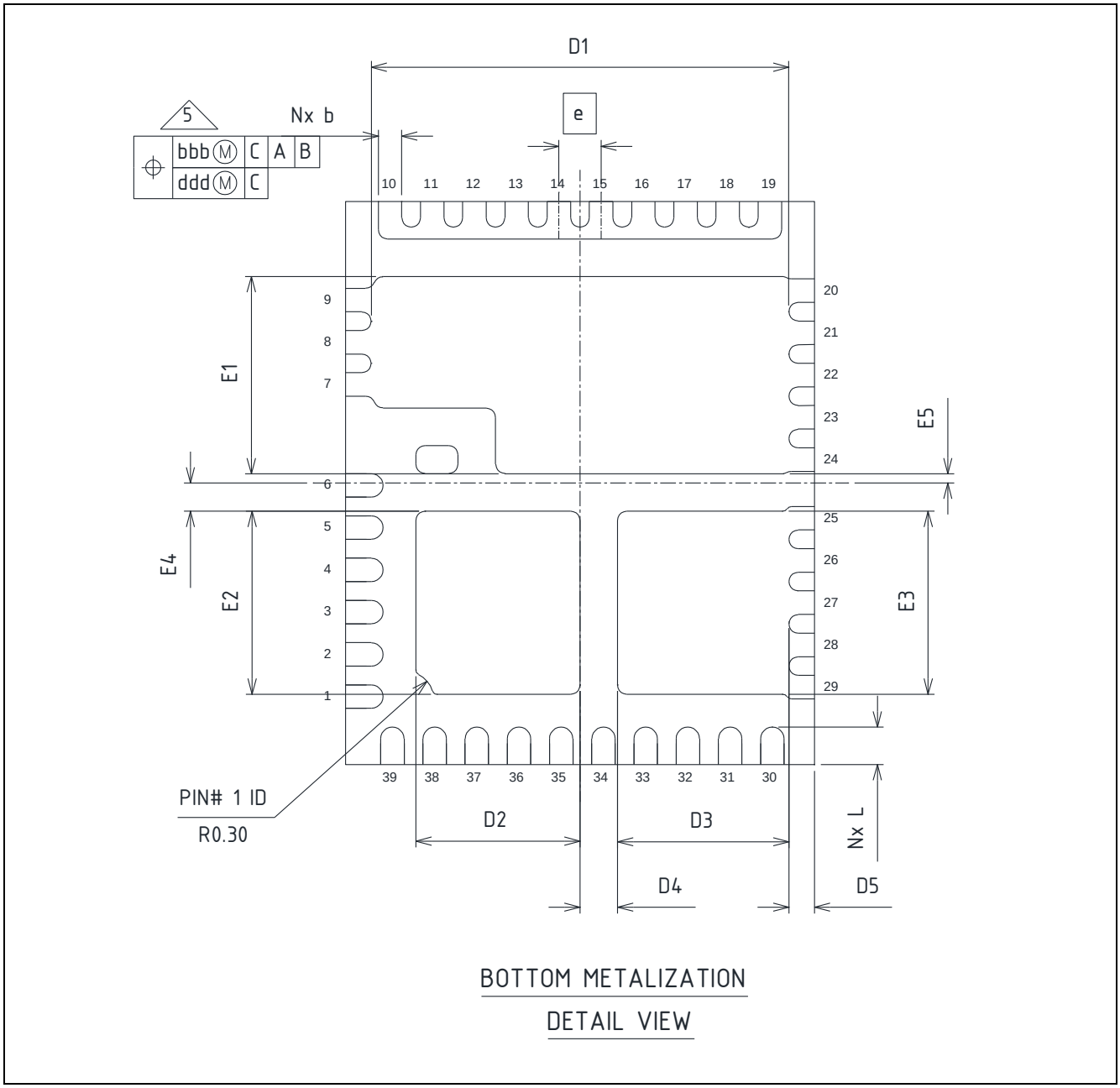


Figure 14 Mechanical Dimensions of Package (Bottom View) in mm

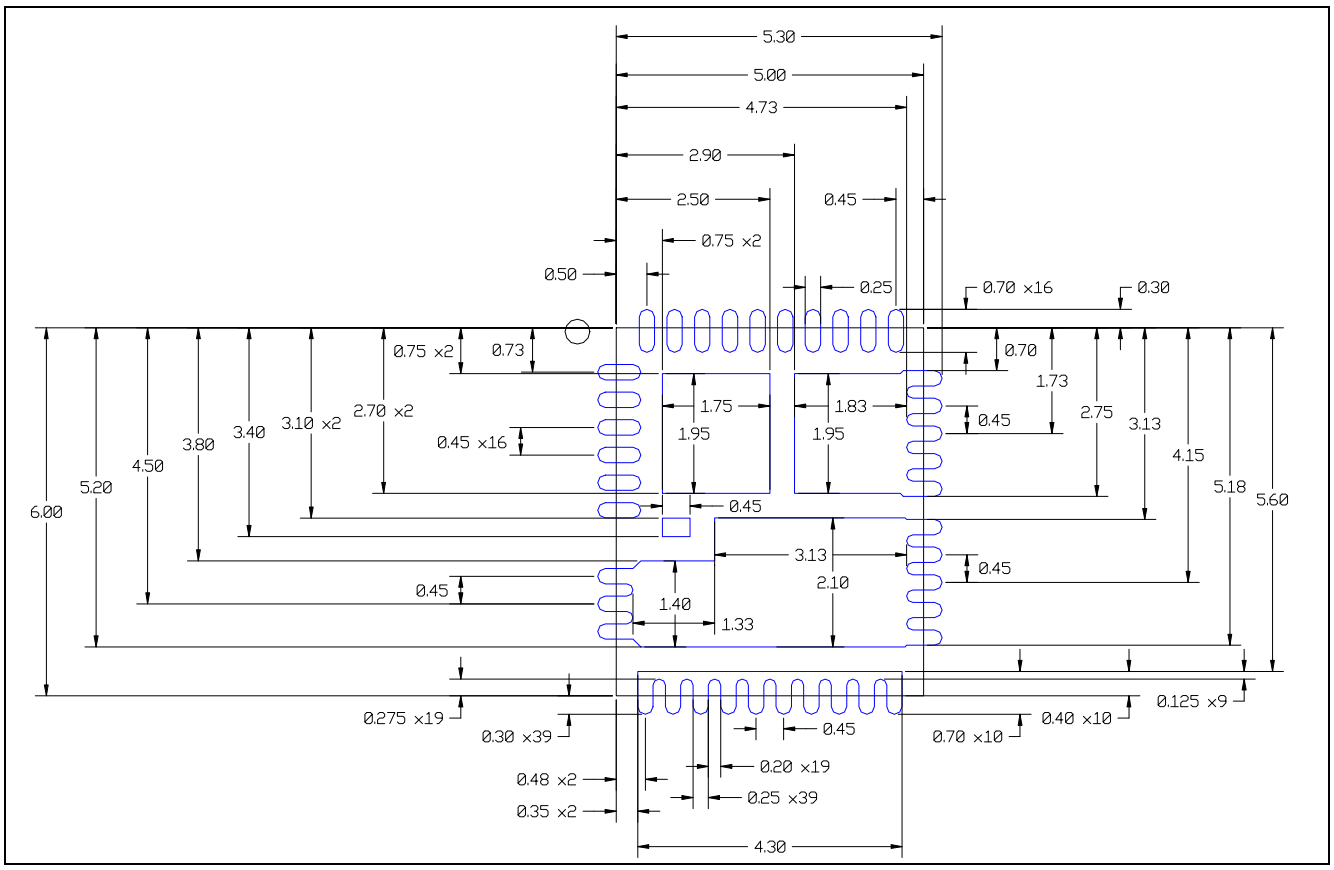


Figure 15 Metal and Component Placement

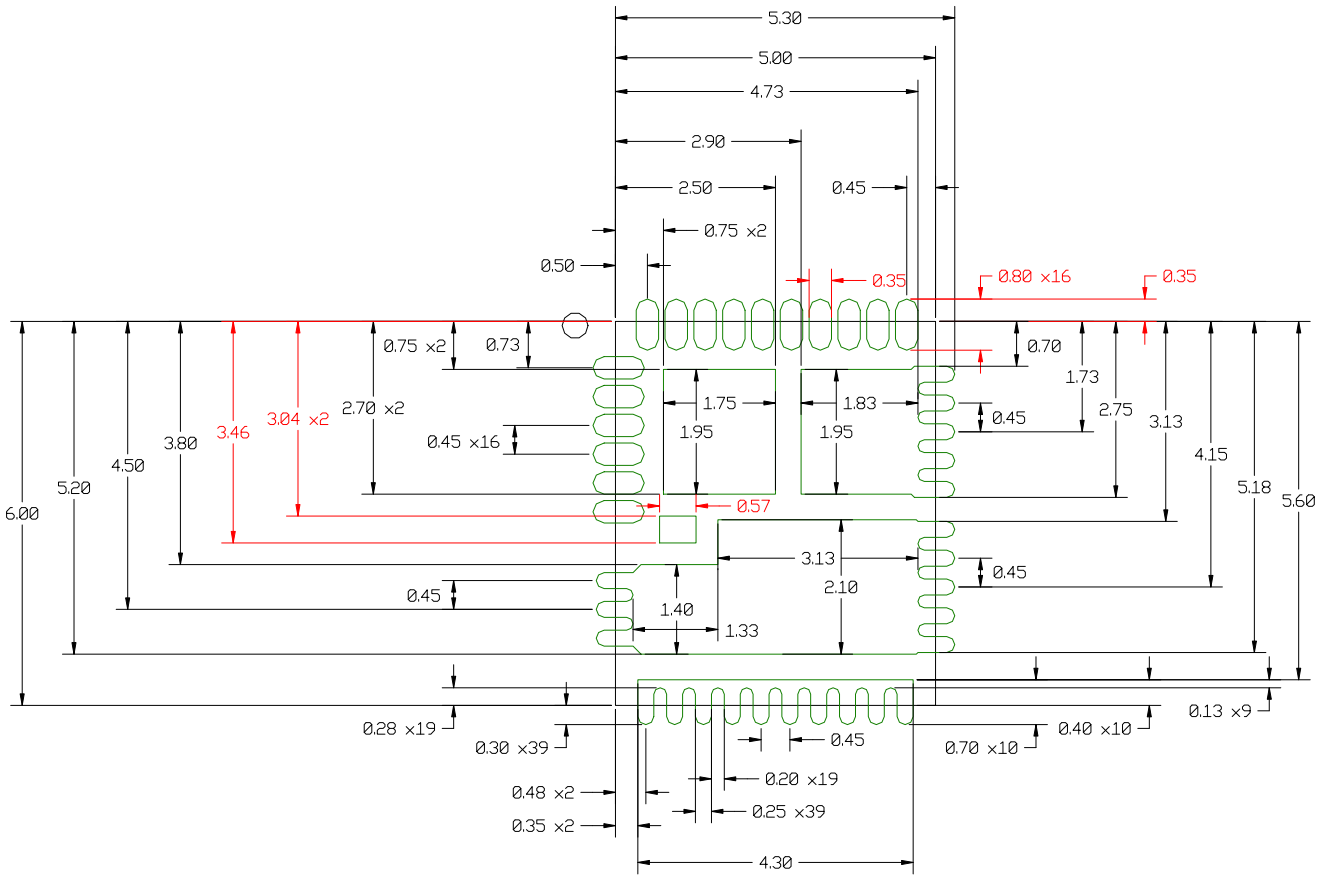


Figure 16 Solder Resist

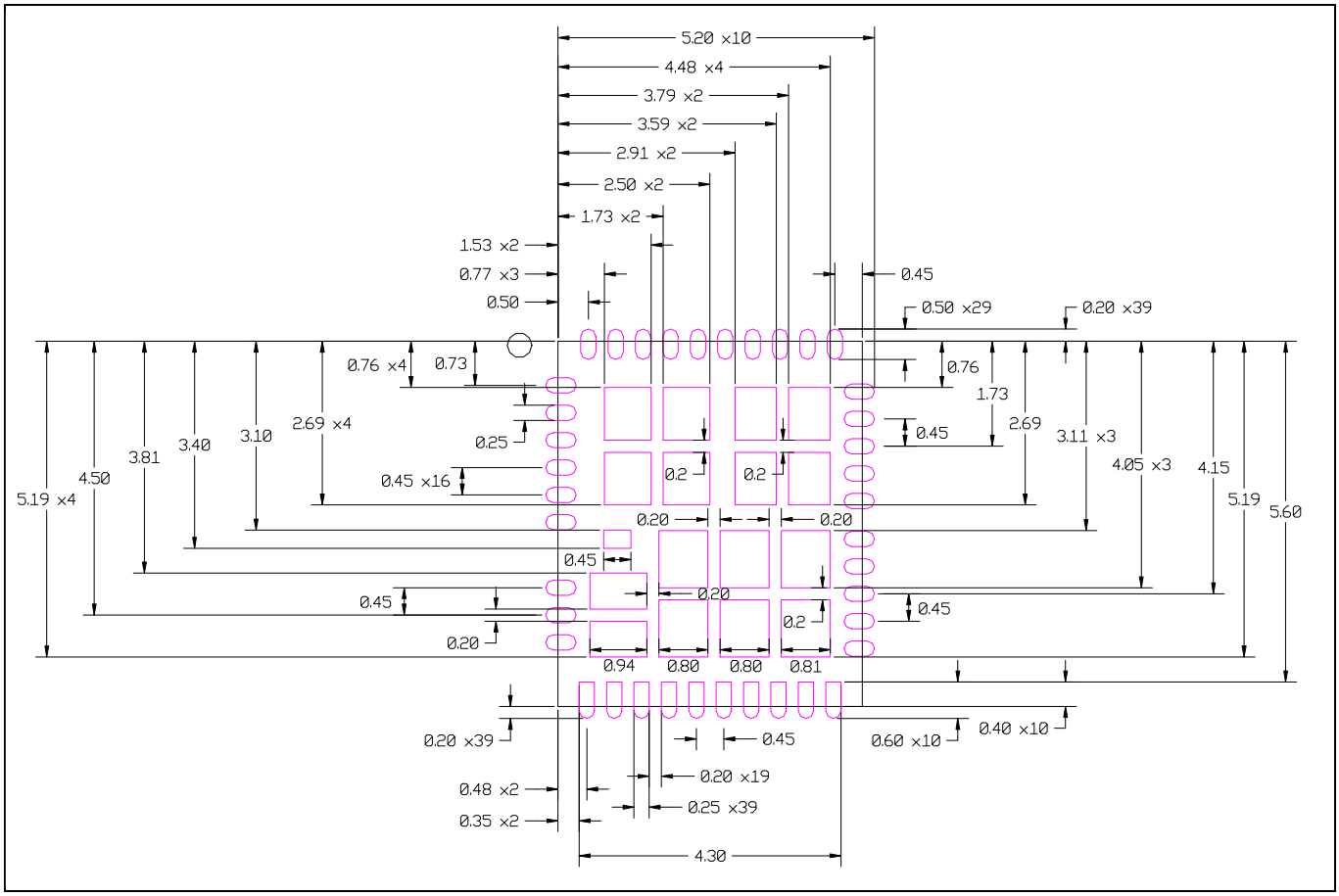


Figure 17 Recommended Stencil Design

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