

# AURIX™ TC39x variants

## About this document

### Scope and purpose

This document is an addendum to the TC39x Product Data Sheet and User's Manual, listing all planned product variants, key parameters such as memory size and optional features.

The User's Manual lists functions implemented on the Silicon, but this document counts functions that are pinning dependent; i.e. functions are counted that are connected to at least one package pin. As pins are overlaid with several functions the pinning needs to be checked (see Product Data Sheet) to determine the number of usable functions in an application.

### Naming conventions

Prefix:

- SAK:  $T_{\text{ambient}}$  Temperature Range from -40 °C up to +125 °C.
- SAL:  $T_{\text{ambient}}$  Temperature Range from -40 °C up to +150 °C (packaged device).

Feature package:

- P: Standard feature.
- E: Emulation device with all features of the emulated standard type, additionally full MCDS, overlay functionality for calibration, AGBT as trace interface for development (depending on the package). Refer to the Emulation devices Data Sheet for further details.
- C,V,Z: Customer Specific.
- A: ADAS ext. Memory.
- T: ADAS + emulation.
- X: Extended Feature device. These products contain the extended memory (EMEM) of the ADAS subsystem. The ADAS peripherals SPU and RIF are not available.
- M: MotionWise software.
- F: Extended Flash.
- G: Additional Connectivity.
- H: ADAS Standard feature.
- N: Standard feature with AMU.

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## 1 TC39x BD step variants

## 1 TC39x BD step variants

## 1.1 TC39x BD step (part 1)

A table listing the TC39x BD step variants.

Table 1 TC39x\_BD step (part 1)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
<b>Step</b>						
BD	BD	BD	BD	BD	BD	BD
<b>Production Status</b>						
Standard	Standard	Standard	Standard	Standard	Standard	Standard
<b>Package Type</b>						
PG-LFBGA-516	PG-LFBGA-516	PG-LFBGA-292	PG-LFBGA-516	PG-LFBGA-516	PG-LFBGA-292	PG-LFBGA-292
<b>Pinout</b>						
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	ADAS
<b>Reference Silicon</b>						
TC39x	TC39x	TC39x	TC39x	TC39x	TC39x	TC39x
<b>Temperature Range (Ambient)</b>						
SAL	SAL	SAL	SAK	SAK	SAK	SAK
<b>Chip ID</b>						
<b>Attention:</b> The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.						
0xAF019993	0x8F019993	0x8F019793	0x8F019993	0xAF019993	0x8F019793	0xBF019793
<b>Cores / Checker Cores</b>						
6/4	6/4	6/4	6/4	6/4	6/4	6/4
<b>Max. Freq. (MHz)</b>						
300	300	300	300	300	300	300
<b>Program Flash (MB)</b>						
16	16	16	16	16	16	16
<b>Data Flash0 (single-ended) (KB)</b>						
1024	1024	1024	1024	1024	1024	1024
<b>Total SRAM (without EMEM and Cache) (KB)</b>						
2528	2528	2528	2528	2528	2528	2528
<b>EMEM Size (KB)</b>						
4096	0	0	0	4096	0	4096
<b>DSPR (KB)</b>						

## 1 TC39x BD step variants

Table 1 TC39x\_BD step (part 1) (continued)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
<b>DLMU (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>PSPR (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>LMU (KB)</b>						
768	768	768	768	768	768	768
<b>DAM (KB)</b>						
128	128	128	128	128	128	128
<b>AMU<sup>1)</sup></b>						
No	No	No	No	No	No	No
<b>ADC (Primary Groups/Channels)</b>						
8/64	8/64	5/40	8/64	8/64	5/40	4/26
<b>ADC (Secondary Groups/Channels)</b>						
4/60	4/60	4/60	4/60	4/60	4/60	4/42
<b>ADC (Fast Compare Channels)</b>						
8	8	8	8	8	8	8
<b>ADC (EDSADC Channels)</b>						
14	14	6	14	14	6	6
<b>CAN (Modules/Nodes)</b>						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
<b>FlexRay (Modules/Channels)</b>						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
<b>HSSL Modules</b>						
2	2	2	2	2	2	2
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>						
12/12/12	12/12/12	12/12/11	12/12/12	12/12/12	12/12/11	12/12/9
<b>QSPI Modules / with LVDS</b>						
6/2	6/2	6/2	6/2	6/2	6/2	6/1

<sup>1</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

## 1 TC39x BD step variants

Table 1 TC39x\_BD step (part 1) (continued)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
<b>SENT Channels</b>						
25	25	20	25	25	20	17
<b>MSC Modules</b>						
4	4	2	4	4	2	1
<b>PSI5 Channels</b>						
4	4	4	4	4	4	4
<b>PSI5-S Module</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>SDMMC Module</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
<b>MCDS Availability<sup>2)</sup></b>						
MCDS	MCDS	MCDS	MCDS	MCDS	MCDS	MCDS
<b>ADAS Cluster Available</b>						
No	No	No	No	No	No	Yes
<b>CIF</b>						
No	No	No	No	No	No	No
<b>HSM Available</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

<sup>2</sup> Refer to the **MCDS availability** section of this document for additional details.

## 1 TC39x BD step variants

### 1.2 TC39x BD step (part 2)

A continuation table listing the TC39x BD step variants.

**Table 2 TC39x\_BD step (part 2)**

SAK-TC397QA-160 F300S	SAK-TC397XX-256 F300S	SAK-TC397QP-192 F300S	SAK-TC397QP-256 F300S	SAK-TC397XZ-256 F300S	SAK-TC397XM-256 F300S	SAL-TC397QP-192 F300S
<b>Step</b>						
BD	BD	BD	BD	BD	BD	BD
<b>Production Status</b>						
Standard	Standard	Customer Specific	Customer Specific	Customer Specific	Standard	Customer Specific
<b>Package Type</b>						
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
<b>Pinout</b>						
ADAS	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
<b>Reference Silicon</b>						
TC39x	TC39x	TC39x	TC39x	TC39x	TC39x	TC39x
<b>Temperature Range (Ambient)</b>						
SAK	SAK	SAK	SAK	SAK	SAK	SAL
<b>Chip ID</b>						
<b>Attention:</b> The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.						
0xCC019793	0xAF019793	0xCD019793	0xCF019793	0xFF019793	0x8F019793	0xCD019793
<b>Cores / Checker Cores</b>						
4/3	6/4	4/4	4/4	6/4	6/4	4/4
<b>Max. Freq. (MHz)</b>						
300	300	300	300	300	300	300
<b>Program Flash (MB)</b>						
10	16	12	16	16	16	12
<b>Data Flash0 (single-ended) (KB)</b>						
1024	1024	1024	1024	1024	1024	1024
<b>Total SRAM (without EMEM and Cache) (KB)</b>						
1696	2528	1184	2080	1632	2528	1184
<b>EMEM Size (KB)</b>						
4096	4096	0	0	0	0	0
<b>DSPR (KB)</b>						

## 1 TC39x BD step variants

Table 2 TC39x\_BD step (part 2) (continued)

SAK-TC397QA-160 F300S	SAK-TC397XX-256 F300S	SAK-TC397QP-192 F300S	SAK-TC397QP-256 F300S	SAK-TC397XZ-256 F300S	SAK-TC397XM-256 F300S	SAL-TC397QP-192 F300S
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
<b>DLMU (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>PSPR (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>LMU (KB)</b>						
512	768	0	768	0	768	0
<b>DAM (KB)</b>						
0	128	0	128	0	128	0
<b>AMU<sup>3)</sup></b>						
No	No	No	No	No	No	No
<b>ADC (Primary Groups/Channels)</b>						
4/26	5/40	5/40	5/40	5/40	5/40	5/40
<b>ADC (Secondary Groups/Channels)</b>						
4/42	4/60	4/60	4/60	4/60	4/60	4/60
<b>ADC (Fast Compare Channels)</b>						
8	8	8	8	8	8	8
<b>ADC (EDSADC Channels)</b>						
6	6	6	6	6	6	6
<b>CAN (Modules/Nodes)</b>						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
<b>FlexRay (Modules/Channels)</b>						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
<b>HSSL Modules</b>						
2	2	2	2	2	2	2
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>						
12/12/9	12/12/11	12/12/11	12/12/11	12/12/11	12/12/11	12/12/11
<b>QSPI Modules / with LVDS</b>						
6/1	6/2	6/2	6/2	6/2	6/2	6/2

<sup>3</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

## 1 TC39x BD step variants

Table 2 TC39x\_BD step (part 2) (continued)

SAK-TC397QA-160 F300S	SAK-TC397XX-256 F300S	SAK-TC397QP-192 F300S	SAK-TC397QP-256 F300S	SAK-TC397XZ-256 F300S	SAK-TC397XM-256 F300S	SAL-TC397QP-192 F300S
<b>SENT Channels</b>						
17	20	20	20	20	20	20
<b>MSC Modules</b>						
1	2	2	2	2	2	2
<b>PSI5 Channels</b>						
4	4	4	4	4	4	4
<b>PSI5-S Module</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>SDMMC Module</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
<b>MCDS Availability<sup>4)</sup></b>						
MCDS	MCDS	MCDS	MCDS	MCDS	MCDS	MCDS
<b>ADAS Cluster Available</b>						
Yes	No	No	No	No	No	No
<b>CIF</b>						
No	No	No	No	No	No	No
<b>HSM Available</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

<sup>4</sup> Refer to the **MCDS availability** section of this document for additional details.



## 1 TC39x BD step variants

## 1.3 TC39x BD step (part 3)

A continuation table listing the TC39x BD step variants.

Table 3 TC39x\_BD step (part 3)

SAL-TC397QP-256F300S	SAL-TC397XZ-256F300S	SAL-TC397XX-256F300S
<b>Step</b>		
BD	BD	BD
<b>Production Status</b>		
Customer Specific	Customer Specific	Standard
<b>Package Type</b>		
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
<b>Pinout</b>		
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
<b>Reference Silicon</b>		
TC39x	TC39x	TC39x
<b>Temperature Range (Ambient)</b>		
SAL	SAL	SAL
<b>Chip ID</b>		
<i>Attention: The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.</i>		
0xCF019793	0xFF019793	0xAF019793
<b>Cores / Checker Cores</b>		
4/4	6/4	6/4
<b>Max. Freq. (MHz)</b>		
300	300	300
<b>Program Flash (MB)</b>		
16	16	16
<b>Data Flash0 (single-ended) (KB)</b>		
1024	1024	1024
<b>Total SRAM (without EMEM and Cache) (KB)</b>		
2080	1632	2528
<b>EMEM Size (KB)</b>		
0	0	4096
<b>DSPR (KB)</b>		
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
<b>DLMU (KB)</b>		
64 per CPU	64 per CPU	64 per CPU

## 1 TC39x BD step variants

Table 3 TC39x\_BD step (part 3) (continued)

SAL-TC397QP-256F300S	SAL-TC397XZ-256F300S	SAL-TC397XX-256F300S
<b>PSPR (KB)</b>		
64 per CPU	64 per CPU	64 per CPU
<b>LMU (KB)</b>		
768	0	768
<b>DAM (KB)</b>		
128	0	128
<b>AMU<sup>5)</sup></b>		
No	No	No
<b>ADC (Primary Groups/Channels)</b>		
5/40	5/40	5/40
<b>ADC (Secondary Groups/Channels)</b>		
4/60	4/60	4/60
<b>ADC (Fast Compare Channels)</b>		
8	8	8
<b>ADC (EDSADC Channels)</b>		
6	6	6
<b>CAN (Modules/Nodes)</b>		
3/3x4	3/3x4	3/3x4
<b>FlexRay (Modules/Channels)</b>		
2/2x2	2/2x2	2/2x2
<b>HSSL Modules</b>		
2	2	2
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>		
12/12/11	12/12/11	12/12/11
<b>QSPI Modules / with LVDS</b>		
6/2	6/2	6/2
<b>SENT Channels</b>		
20	20	20
<b>MSC Modules</b>		
2	2	2
<b>PSI5 Channels</b>		
4	4	4

<sup>5</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

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**1 TC39x BD step variants**
**Table 3 TC39x\_BD step (part 3) (continued)**

	<b>SAL-TC397QP-256F300S</b>	<b>SAL-TC397XZ-256F300S</b>	<b>SAL-TC397XX-256F300S</b>
<b>PSI5-S Module</b>			
	Yes	Yes	Yes
<b>SDMMC Module</b>			
	Yes	Yes	Yes
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>			
	1Gbit/s	1Gbit/s	1Gbit/s
<b>MCDS Availability<sup>6)</sup></b>			
	MCDS	MCDS	MCDS
<b>ADAS Cluster Available</b>			
	No	No	No
<b>CIF</b>			
	No	No	No
<b>HSM Available</b>			
	Yes	Yes	Yes

<sup>6</sup> Refer to the **MCDS availability** section of this document for additional details.

## 2 TC39x BC step variants

## 2 TC39x BC step variants

## 2.1 TC39x BC step (part 1)

A table listing the TC39x BC step variants.

Table 4 TC39x\_BC step (part 1)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
<b>Step</b>						
BC	BC	BC	BC	BC	BC	BC
<b>Production Status</b>						
Standard	Standard	Standard	Standard	Standard	Standard	Standard
<b>Package Type</b>						
PG-LFBGA-516	PG-LFBGA-516	PG-LFBGA-292	PG-LFBGA-516	PG-LFBGA-516	PG-LFBGA-292	PG-LFBGA-292
<b>Pinout</b>						
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	ADAS
<b>Reference Silicon</b>						
TC39x	TC39x	TC39x	TC39x	TC39x	TC39x	TC39x
<b>Temperature Range (Ambient)</b>						
SAL	SAL	SAL	SAK	SAK	SAK	SAK
<b>Chip ID</b>						
<b>Attention:</b> The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.						
0xAF019992	0x8F019992	0x8F019792	0x8F019992	0xAF019992	0x8F019792	0xBF019792
<b>Cores / Checker Cores</b>						
6/4	6/4	6/4	6/4	6/4	6/4	6/4
<b>Max. Freq. (MHz)</b>						
300	300	300	300	300	300	300
<b>Program Flash (MB)</b>						
16	16	16	16	16	16	16
<b>Data Flash0 (single-ended) (KB)</b>						
1024	1024	1024	1024	1024	1024	1024
<b>Total SRAM (without EMEM and Cache) (KB)</b>						
2528	2528	2528	2528	2528	2528	2528
<b>EMEM Size (KB)</b>						
4096	0	0	0	4096	0	4096
<b>DSPR (KB)</b>						

## 2 TC39x BC step variants

Table 4 TC39x\_BC step (part 1) (continued)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
<b>DLMU (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>PSPR (KB)</b>						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>LMU (KB)</b>						
768	768	768	768	768	768	768
<b>DAM (KB)</b>						
128	128	128	128	128	128	128
<b>AMU<sup>7)</sup></b>						
No	No	No	No	No	No	No
<b>ADC (Primary Groups/Channels)</b>						
8/64	8/64	5/40	8/64	8/64	5/40	4/26
<b>ADC (Secondary Groups/Channels)</b>						
4/60	4/60	4/60	4/60	4/60	4/60	4/42
<b>ADC (Fast Compare Channels)</b>						
8	8	8	8	8	8	8
<b>ADC (EDSADC Channels)</b>						
14	14	6	14	14	6	6
<b>CAN (Modules/Nodes)</b>						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
<b>FlexRay (Modules/Channels)</b>						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
<b>HSSL Modules</b>						
2	2	2	2	2	2	2
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>						
12/12/12	12/12/12	12/12/11	12/12/12	12/12/12	12/12/11	12/12/9
<b>QSPI Modules / with LVDS</b>						
6/2	6/2	6/2	6/2	6/2	6/2	6/1

<sup>7</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

## 2 TC39x BC step variants

Table 4 TC39x\_BC step (part 1) (continued)

SAL-TC399XX-256F300S	SAL-TC399XP-256F300S	SAL-TC397XP-256F300S	SAK-TC399XP-256F300S	SAK-TC399XX-256F300S	SAK-TC397XP-256F300S	SAK-TC397XA-256F300S
<b>SENT Channels</b>						
25	25	20	25	25	20	17
<b>MSC Modules</b>						
4	4	2	4	4	2	1
<b>PSI5 Channels</b>						
4	4	4	4	4	4	4
<b>PSI5-S Module</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>SDMMC Module</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
<b>MCDS Availability<sup>8)</sup></b>						
MCDS	MCDS	MCDS	MCDS	MCDS	MCDS	MCDS
<b>ADAS Cluster Available</b>						
No	No	No	No	No	No	Yes
<b>CIF</b>						
No	No	No	No	No	No	No
<b>HSM Available</b>						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

<sup>8</sup> Refer to the **MCDS availability** section of this document for additional details.

## 2 TC39x BC step variants

## 2.2 TC39x BC step (part 2)

A continuation table listing the TC39x BC step variants.

Table 5 TC39x\_BC step (part 2)

SAK-TC397QA-160F300S	SAK-TC397XX-256F300S	SAK-TC397QP-192F300S	SAK-TC397QP-256F300S	SAK-TC397XZ-256F300S
<b>Step</b>				
BC	BC	BC	BC	BC
<b>Production Status</b>				
Standard	Standard	Customer Specific	Customer Specific	Customer Specific
<b>Package Type</b>				
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
<b>Pinout</b>				
ADAS	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
<b>Reference Silicon</b>				
TC39x	TC39x	TC39x	TC39x	TC39x
<b>Temperature Range (Ambient)</b>				
SAK	SAK	SAK	SAK	SAK
<b>Chip ID</b>				
<i>Attention: The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.</i>				
0xCC019792	0xAF019792	0xCD019792	0xCF019792	0xFF019792
<b>Cores / Checker Cores</b>				
4/3	6/4	4/4	4/4	6/4
<b>Max. Freq. (MHz)</b>				
300	300	300	300	300
<b>Program Flash (MB)</b>				
10	16	12	16	16
<b>Data Flash0 (single-ended) (KB)</b>				
1024	1024	1024	1024	1024
<b>Total SRAM (without EMEM and Cache) (KB)</b>				
1696	2528	1184	2080	1632
<b>EMEM Size (KB)</b>				
4096	4096	0	0	0
<b>DSPR (KB)</b>				
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
<b>DLMU (KB)</b>				

## 2 TC39x BC step variants

Table 5 TC39x\_BC step (part 2) (continued)

SAK-TC397QA-160F300S	SAK-TC397XX-256F300S	SAK-TC397QP-192F300S	SAK-TC397QP-256F300S	SAK-TC397XZ-256F300S
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>PSPR (KB)</b>				
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
<b>LMU (KB)</b>				
512	768	0	768	0
<b>DAM (KB)</b>				
0	128	0	128	0
<b>AMU<sup>9)</sup></b>				
No	No	No	No	No
<b>ADC (Primary Groups/Channels)</b>				
4/26	5/40	5/40	5/40	5/40
<b>ADC (Secondary Groups/Channels)</b>				
4/42	4/60	4/60	4/60	4/60
<b>ADC (Fast Compare Channels)</b>				
8	8	8	8	8
<b>ADC (EDSADC Channels)</b>				
6	6	6	6	6
<b>CAN (Modules/Nodes)</b>				
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
<b>FlexRay (Modules/Channels)</b>				
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
<b>HSSL Modules</b>				
2	2	2	2	2
<b>ASCLIN Modules / with ASC &amp; LIN / with 3-wire SPI</b>				
12/12/9	12/12/11	12/12/11	12/12/11	12/12/11
<b>QSPI Modules / with LVDS</b>				
6/1	6/2	6/2	6/2	6/2
<b>SENT Channels</b>				
17	20	20	20	20
<b>MSC Modules</b>				
1	2	2	2	2

<sup>9)</sup> AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative



## 2 TC39x BC step variants

Table 5 TC39x\_BC step (part 2) (continued)

SAK-TC397QA-160F300S	SAK-TC397XX-256F300S	SAK-TC397QP-192F300S	SAK-TC397QP-256F300S	SAK-TC397XZ-256F300S
<b>PSI5 Channels</b>				
4	4	4	4	4
<b>PSI5-S Module</b>				
Yes	Yes	Yes	Yes	Yes
<b>SDMMC Module</b>				
Yes	Yes	Yes	Yes	Yes
<b>Max. Ethernet Availability: 1Gbit/100Mbit/No</b>				
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
<b>MCDS Availability<sup>10)</sup></b>				
MCDS	MCDS	MCDS	MCDS	MCDS
<b>ADAS Cluster Available</b>				
Yes	No	No	No	No
<b>CIF</b>				
No	No	No	No	No
<b>HSM Available</b>				
Yes	Yes	Yes	Yes	Yes

<sup>10</sup> Refer to the **MCDS availability** section of this document for additional details.

3 Memory maps of TC39x variants

### 3 Memory maps of TC39x variants

This section describes the influence of the available feature variants on the memory map.

#### Program Flash

Variants:

- 16 MB: umbrella (5 x 3 MB, 1 x 1 MB), see User's Manual.
- 12 MB: 4 x 3 MB (see Figure below).
- 10 MB: 3 + 2 + 3 + 2 MB (see Figure below).

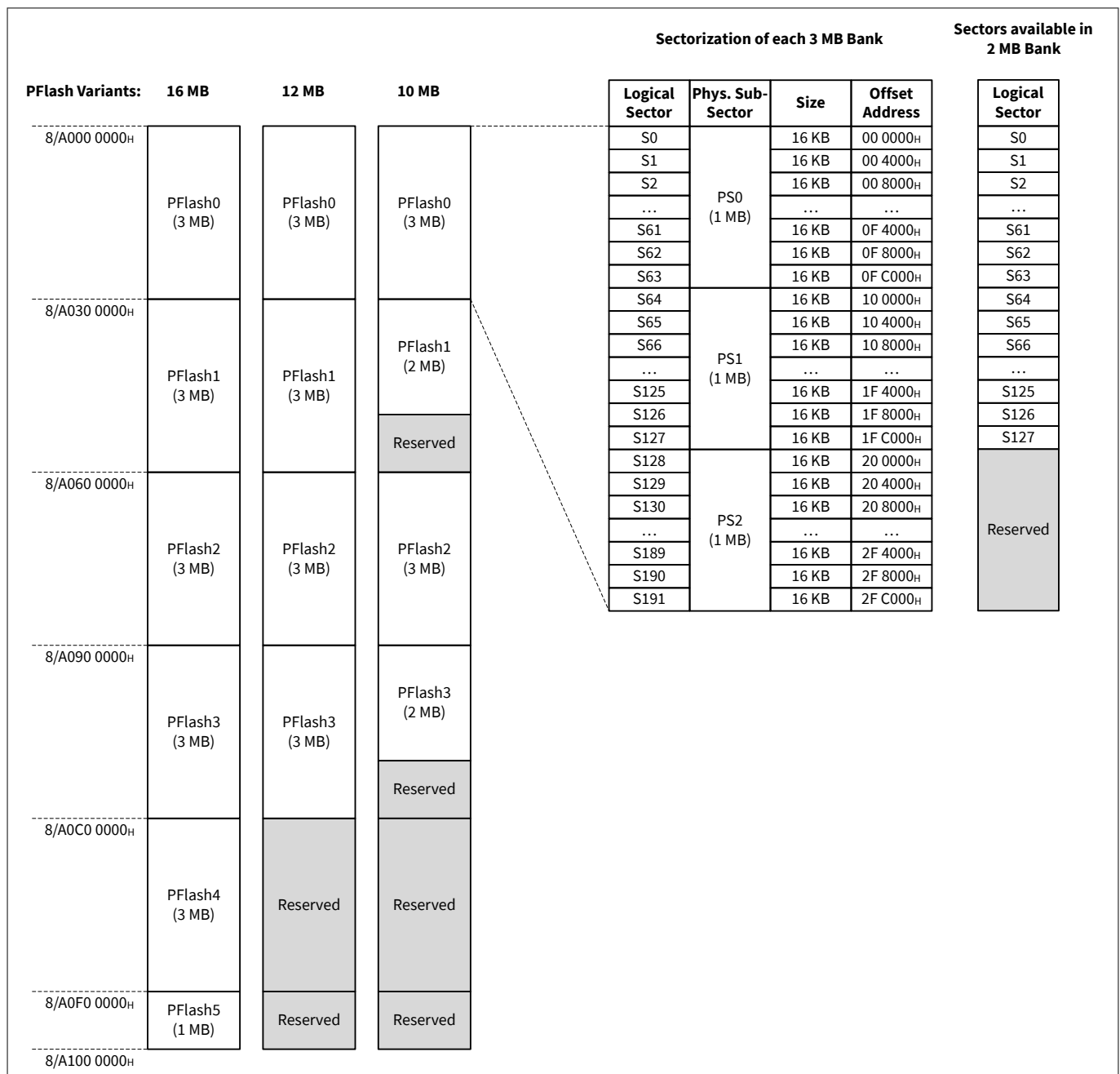


Figure 1 TC39x PFlash variants

#### Cores / checker cores

Variants:

### 3 Memory maps of TC39x variants

- 6/4: umbrella, see User's Manual
- 4/4: not available are CPU4 and CPU5 including their RAMs (DSPR, DCACHE, DTAG, PSPR, PCACHE, PTAG, DLMU)
- 4/3: not available are CPU4 and CPU5 including their RAMs (DSPR, DCACHE, DTAG, PSPR, PCACHE, PTAG, DLMU) and CPU3 lockstep is not available (LCLCON1.LEN3 must stay 0<sub>B</sub>).

#### LMU

Variants:

- 768 KB: umbrella, see User's Manual.
- 512 KB: only LMU0 and LMU1 LMU RAM are available (see Figure below).
- 0 KB: no LMURAM is available (see Figure below)

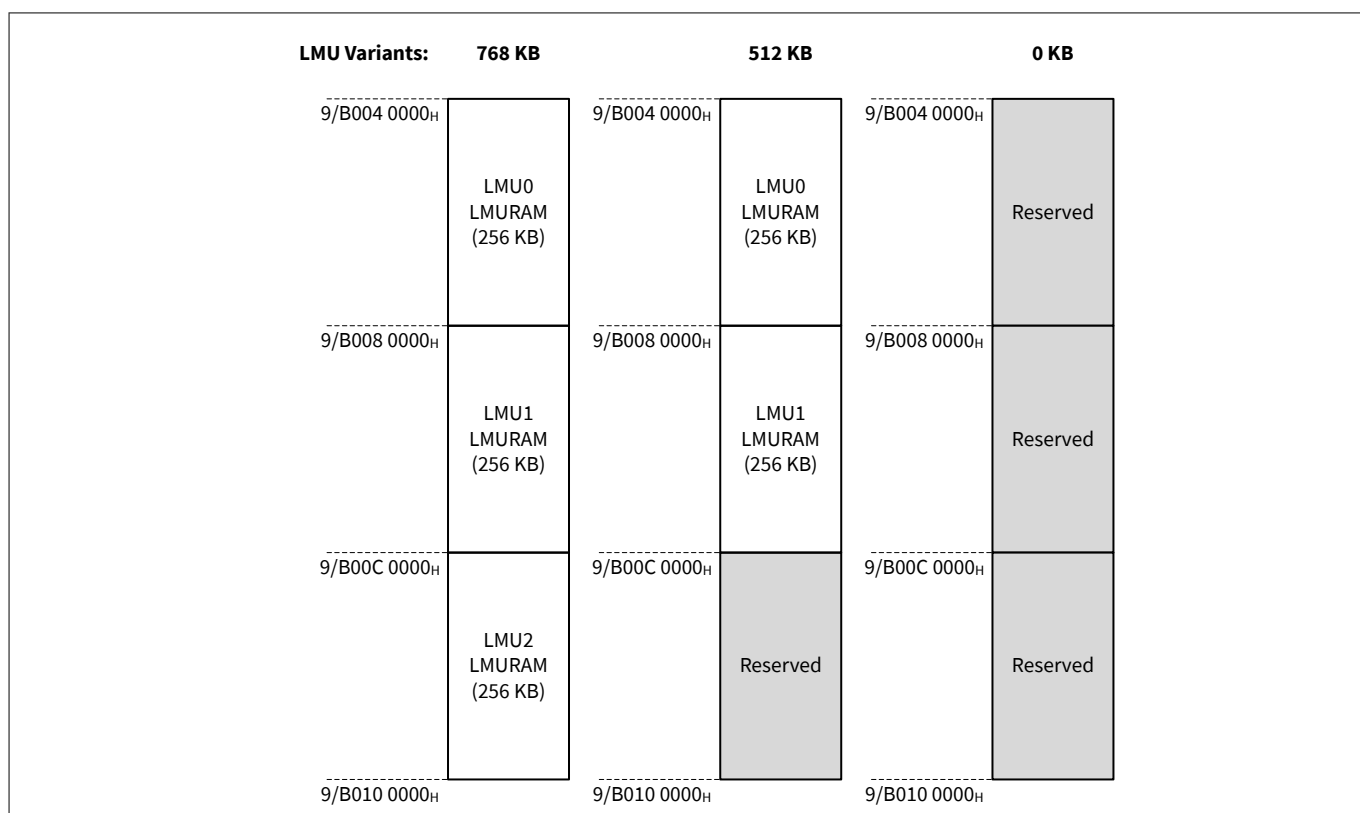


Figure 2 TC39x LMU Variants

#### DAM

Variants:

- 128 KB: umbrella, see User's Manual
- 0 KB: none of the DAM RAMs are available

#### ADAS cluster available

Variants:

- Yes: umbrella, see User's Manual
- No: the following instances are not available: HSPDM, RIF0, RIF1, SPU0, SPU1, SPUCFG0, SPUCFG1, SPU Lockstep SFR.

#### EMEM availability

Variants:

---

## 3 Memory maps of TC39x variants

- 4096 KB: umbrella, see User's Manual.
- 0 KB: no EMEM available.

### ADC availability

- Limitation on availability of ADC channels are caused by pin limitations. See Data Sheet for the pinning table of the package.

### MCDS availability

- MCDS is not intended for use in productive devices. It may not be tested and is not covered by the safety case. For this functionality, please refer to the Aurix 2G Emulation device Data Sheet.

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**Revision history**
**Revision history**

Document version	Date of release	Description of changes
V1.0	2018-06-08	<ul style="list-style-type: none"> <li>First release.</li> </ul>
V1.1	2018-08-06	<ul style="list-style-type: none"> <li>Added row "Reference Silicon" (needed e.g. for TC37x) to refer user to User's Manual Appx.</li> </ul>
V1.2	2019-03-01	<ul style="list-style-type: none"> <li>In "About this document": Corrected "overloaded" to "overlaid".</li> <li>In "About this document": Added Feature Package "M" and "E" and remove "R".</li> <li>In "About this document": Added clarification concerning AGBT in E, A and T.</li> <li>In "About this document": Removed feature packages B, C, H.</li> <li>In "Variant Tables of TC39x": added device "SAK-TC397XM-256F300S"</li> <li>In "Variant Tables of TC39x": added Feature Package "E" devices (Emulation Devices).</li> </ul>
V1.3	2019-06-12	<ul style="list-style-type: none"> <li>Added the TC39x "BD" step Variants to Chapter 1</li> <li>Removed the following Variants SAK-TC397XT-25 6F300S, SAK-TC397TT-25 6F300S for "BC" Step, Chapter 2</li> <li>Chapter 1 and 2: TC39x Bx step variants table format changed to fit all the contents.</li> <li>Chapter 1 and 2: Added new row in the variant tables called "AMU" with the footnote for additional details.</li> <li>Chapter: About this document: Feature package definitions are updated to consistent with the product naming nomenclature definition.</li> </ul>
V1.4	2020-01-09	<ul style="list-style-type: none"> <li>Added the new TC39x "BD" step Variants SAL-TC397QP-192F300S, SAL-TC397QP-256F300S, SAL-TC397XZ-256F300S, SAL-TC397XX-256F300S to Chapter 1</li> <li>Page 1: About the document: Feature Package 'X' definition is updated to remove CIF.</li> <li>Chapter 1 and 2: Added new row in the variant tables called "CIF" indicating the Camera Interface availability.</li> </ul>
V1.5	2020-04-29	<ul style="list-style-type: none"> <li>Chapter 3: Added a note on the MCDS availability in productive devices.</li> <li>About this document section: Added an additional note for the Feature package 'E'.</li> </ul>
V1.6	2020-11-19	<ul style="list-style-type: none"> <li>Chapter 1, 2: Added a Foot note for the 'MCDS Availability' to explain its usage.</li> <li>Chapter 3: Updated 'MCDS Availability' section to describe its usage.</li> </ul>

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