AURIX™ TC33xEXT

About this document

Scope and purpose

The Appendix supplies information specific for the TC33xEXT supplementing the family documentation.

Table of Contents

1 Introduction

For Introduction, block diagrams and feature set consult the family document.

For Pinning consult the Data Sheet.

2 Memory Maps (MEMMAP)

This is the automatically generated memory map of the TC33xEXT.

2.1 Overview

The memory map describes the address locations and access possibilities for the units, memories, and reserved areas as “seen” from the different on-chip buses’ point of view.

2.2 Functional Description

The bus-specific address maps describe how the different bus master devices react on accesses to on-chip memories and modules, and which address ranges are valid or invalid for the corresponding buses.

The detailed address mapping of e.g. control registers, SRAM blocks or flash banks/sectors within a module is described in the related module chapter.

The SFI is an uni-directional bridge for access from SPB to SRI and therefore not mentioned here as an SRI master in the Address Map. The SFI is fully transparent and does not include an address translation mechanism.

Note: In addition to the here described system address map, each TriCore has a TriCore IP internal access to its PSPR via $C000\_0000_H$ and an internal access to its DSPR via $D000\_0000_H$. This additional/private view to the local scratch pad SRAMs is described in the CPU chapter.

Table 1 defines the acronyms and other terms that are used in the address maps.

Table 1 Definition of Acronyms and Terms

Term	Description
BE	A bus access is terminated with a bus error.
ok	A bus access is allowed and is executed.
16	A bus access with width 16 and 32 bits is allowed and executed.
32	A bus access with width 32 bits is allowed and executed.
Access	A bus access is allowed and is executed.

2.2.1 Segments

This section summarizes the contents of the segments.

Segments 0 and 2

These memory segments are reserved.

Segments 1 and 3-7

These memory segments allow access to the CPUs Program and Data Scratch Pad SRAM (PSPR, DSPR), Program and Data Cache SRAMs (PCACHE, DCACHE) as well as TAG SRAMs related to Program and Data Cache (PTAG SRAM[1)] and DTAG SRAM[1)]).

Where DCACHE is supported, DCACHE and DTAG SRAM[1)] can be only accessed if the Data Cache is disabled.

PCACHE and PTAG SRAMs[1)] can be only accessed if the related Program Cache is disabled.

1) TAG SRAMs are not meant to be used as general SRAMs and can be accessed only with single data access and only with 64 bit aligned address.

The attribute of these segments (cached / non-cached) can be partially configured[1] for each CPUs data and program side individually (see CPU chapter: Physical Memory Attribute Registers, PMAx).

Segment 8

This memory segment allows cached access to PFlash and BROM.

Segment 9

This memory segment allows cached access to LMU and to EMEM.

Segment 10

This memory segment allows non-cached access to PFlash, DFlash and BROM.

Segment 11

This memory segment allows non-cached access to LMU and to EMEM.

Segment 12

This memory segment is reserved.

Segment 13

This memory segment is reserved.

Segment 14

This memory segment is reserved.

Segment 15

The lower 128 Mbyte is SPB address space and the upper 128 Mbyte is SRI address space.

2.3 Bus Fabric SRI

This is the merged view of all SRI Bus Segments as used in the TC33xEXT.

Table 2 Address Map as seen by Bus Masters on Bus SRI

Address Range		Size	Unit	Access Type	
from	to			Read	Write
00000000_H	$5FFFFFFF_H$	-	Reserved	BE	BE
60000000_H	$60017FFF_H$	96 Kbyte	Data ScratchPad RAM (CPU1)	ok	ok
60018000_H	$6001BFFF_H$	16 Kbyte	Data Cache RAM (CPU1)	ok	ok
$6001C000_H$	$600BFFFF_H$	-	Reserved	BE	BE
$600C0000_H$	$600C17FF_H$	6 Kbyte	Data Cache Tag RAM (CPU1)	ok	ok
$600C1800_H$	$600FFFFF_H$	-	Reserved	BE	BE
60100000_H	$6010FFFF_H$	64 Kbyte	Program ScratchPad RAM (CPU1)	ok	ok
60110000_H	$60117FFF_H$	32 Kbyte	Program Cache RAM (CPU1)	ok	ok
60118000_H	$601BFFFF_H$	-	Reserved	BE	BE

1) Mapping of Cache and TAG SRAMs is controlled via the MTU register MTU_MEMMAP.

Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
$601C0000_H$	$601C2FFF_H$	12 Kbyte	Program Cache TAG RAM (CPU1)	ok	ok
$601C3000_H$	$6FFFFFFF_H$	-	Reserved	BE	BE
70000000_H	$7002FFFF_H$	192 Kbyte	Data ScratchPad RAM (CPU0)	ok	ok
70030000_H	$70033FFF_H$	16 Kbyte	Data Cache RAM (CPU0)	ok	ok
70034000_H	$700BFFFF_H$	-	Reserved	BE	BE
$700C0000_H$	$700C17FF_H$	6 Kbyte	Data Cache Tag RAM (CPU0)	ok	ok
$700C1800_H$	$700FFFFF_H$	-	Reserved	BE	BE
70100000_H	$70107FFF_H$	32 Kbyte	Program ScratchPad RAM (CPU0)	ok	ok
70108000_H	$7010FFFF_H$	32 Kbyte	Program Cache RAM (CPU0)	ok	ok
70110000_H	$701BFFFF_H$	-	Reserved	BE	BE
$701C0000_H$	$701C2FFF_H$	12 Kbyte	Program Cache TAG RAM (CPU0)	ok	ok
$701C3000_H$	$7FFFFFFF_H$	-	Reserved	BE	BE
80000000_H	$802FFFFF_H$	3 Mbyte	Program Flash (PFI0)	ok	ok
80300000_H	$8FDFFFFF_H$	-	Reserved	BE	BE
$8FE00000_H$	$8FE7FFFF_H$	512 Kbyte	Online Data Acquisition (OLDA) (DOM0)	BE	ok
$8FE80000_H$	$8FFEFFFF_H$	-	Reserved	BE	BE
$8FFF0000_H$	$8FFFFFFF_H$	64 Kbyte	Boot ROM (BROM) (DMU)	ok	ok
90000000_H	$90001FFF_H$	8 Kbyte	DLMU RAM (CPU0)	ok	ok
90002000_H	$9000FFFF_H$	-	Reserved	BE	BE
90010000_H	$9001FFFF_H$	64 Kbyte	DLMU RAM (CPU1)	ok	ok
90020000_H	$98FFFFFF_H$	-	Reserved	BE	BE
99000000_H	$990FFFFF_H$	1 Mbyte	SRI slave interface 0 (access to EMEM module RAM, cached segment) (EMEMRAM0)	ok	ok
99100000_H	$9FFFFFFF_H$	-	Reserved	BE	BE
$A0000000_H$	$A02FFFFF_H$	3 Mbyte	Program Flash (PFI0_NC)	ok	ok
$A0300000_H$	$A7FFFFFF_H$	-	Reserved	BE	BE
$A8000000_H$	$A8003FFF_H$	16 Kbyte	Erase Counter (PFI0)	ok	ok
$A8004000_H$	$A807FFFF_H$	-	Reserved	BE	BE
$A8080000_H$	$A80FFFFF_H$	512 Kbyte	Register address space (PFI0)	ok	ok
$A8100000_H$	$AEFFFFFF_H$	-	Reserved	BE	BE
$AF000000_H$	$AF0FFFFF_H$	1 Mbyte	Data Flash 0 EEPROM (DF0) and Host Command Sequence Interpreter (DMU)	ok	ok
$AF100000_H$	$AF3FFFFF_H$	-	Reserved	BE	BE

Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
$AF400000_H$	$AF405FFF_H$	24 Kbyte	UCB_BMHD0_ORIG (UCB)	ok	ok
			UCB_BMHD1_ORIG (UCB)	ok	ok
			UCB_BMHD2_ORIG (UCB)	ok	ok
			UCB_BMHD3_ORIG (UCB)	ok	ok
			UCB_SSW (UCB)	ok	ok
			UCB_USER (UCB)	ok	ok
			UCB_TEST (UCB)	ok	ok
			UCB_HSMCFG (UCB)	ok	ok
			UCB_BMHD0_COPY (UCB)	ok	ok
			UCB_BMHD1_COPY (UCB)	ok	ok
			UCB_BMHD2_COPY (UCB)	ok	ok
			UCB_BMHD3_COPY (UCB)	ok	ok
			UCB_REDSEC (UCB)	ok	ok
			Reserved (UCB)	ok	ok
			Reserved (UCB)	ok	ok
			UCB_RETEST (UCB)	ok	ok
			UCB_PFLASH_ORIG (UCB)	ok	ok
			UCB_DFLASH_ORIG (UCB)	ok	ok
			UCB_DBG_ORIG (UCB)	ok	ok
			UCB_HSM_ORIG (UCB)	ok	ok
			UCB_HSMCOTP0_ORIG (UCB)	ok	ok
			UCB_HSMCOTP1_ORIG (UCB)	ok	ok
			UCB_ECPRIO_ORIG (UCB)	ok	ok
			UCB_SWAP_ORIG (UCB)	ok	ok
			UCB_PFLASH_COPY (UCB)	ok	ok
			UCB_DFLASH_COPY (UCB)	ok	ok
			UCB_DBG_COPY (UCB)	ok	ok
			UCB_HSM_COPY (UCB)	ok	ok
			UCB_HSMCOTP0_COPY (UCB)	ok	ok
			UCB_HSMCOTP1_COPY (UCB)	ok	ok
			UCB_ECPRIO_COPY (UCB)	ok	ok
			UCB_SWAP_COPY (UCB)	ok	ok

Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
cont'd			UCB_OTP0_ORIG (UCB) UCB_OTP1_ORIG (UCB) UCB_OTP2_ORIG (UCB) UCB_OTP3_ORIG (UCB) UCB_OTP4_ORIG (UCB) UCB_OTP5_ORIG (UCB) UCB_OTP6_ORIG (UCB) UCB_OTP7_ORIG (UCB) UCB_OTP0_COPY (UCB) UCB_OPT1_COPY (UCB) UCB_OPT2_COPY (UCB) UCB_OPT3_COPY (UCB) UCB_OPT4_COPY (UCB) UCB_OPT5_COPY (UCB) UCB_OPT6_COPY (UCB) UCB_OPT7_COPY (UCB)	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok	ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok ok
$AF406000_H$	$AF7FFFFF_H$	-	Reserved	BE	BE
$AF800000_H$	$AF80FFFF_H$	64 Kbyte	Configuration Sector Layout (CFS)	ok	ok
$AF810000_H$	$AFBFFFFF_H$	-	Reserved	BE	BE
$AFC00000_H$	$AFC1FFFF_H$	128 Kbyte	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter (DMU)	ok	ok
$AFC20000_H$	$AFDFFFFF_H$	-	Reserved	BE	BE
$AFE00000_H$	$AFE7FFFF_H$	512 Kbyte	Online Data Acquisition (OLDA) (DOM0_NC)	BE	ok
$AFE80000_H$	$AFFEFFFF_H$	-	Reserved	BE	BE
$AFFF0000_H$	$AFFFFFFF_H$	64 Kbyte	Boot ROM (BROM) (DMU)	ok	ok
$B0000000_H$	$B0001FFF_H$	8 Kbyte	DLMU RAM (CPU0_NC)	ok	ok
$B0002000_H$	$B000FFFF_H$	-	Reserved	BE	BE
$B0010000_H$	$B001FFFF_H$	64 Kbyte	DLMU RAM (CPU1_NC)	ok	ok
$B0020000_H$	$B8FFFFFF_H$	-	Reserved	BE	BE
$B9000000_H$	$B90FFFFF_H$	1 Mbyte	SRI slave interface 0 (access to EMEM module RAM, non-cached segment) (EMEMRAM0)	ok	ok
$B9100000_H$	$F801FFFF_H$	-	Reserved	BE	BE
$F8020000_H$	$F8029FFF_H$	40 Kbyte	sri slave interface (FSIRAM)	ok	ok
$F802A000_H$	$F802FFFF_H$	-	Reserved	BE	BE
$F8030000_H$	$F80300FF_H$	256 byte	sri slave interface (FSI)	ok	ok
$F8030100_H$	$F8037FFF_H$	-	Reserved	BE	BE
$F8038000_H$	$F803FFFF_H$	32 Kbyte	sri slave interface (PMU)	ok	ok
$F8040000_H$	$F807FFFF_H$	256 Kbyte	sri slave interface (DMU)	ok	ok
$F8080000_H$	$F86FFFFF_H$	-	Reserved	BE	BE
$F8700000_H$	$F870FFFF_H$	64 Kbyte	sri slave interface (DOM0)	ok	ok

Table 2 Address Map as seen by Bus Masters on Bus SRI (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
$F8710000_H$	$F87FFFFF_H$	-	Reserved	BE	BE
$F8800000_H$	$F881FFFF_H$	128 Kbyte	Safety Memory Protection Register (CPU0)	ok	ok
			DLMU Safety Memory Protection registers (CPU0)	ok	ok
			Safety register protection registers (CPU0)	ok	ok
			Kernel Reset registers (CPU0)	ok	ok
			Flash Configuration registers (CPU0)	ok	ok
			Overlay Block Control registers (CPU0)	ok	ok
			Memory Integrity Registers (CPU0)	ok	ok
			Core Special Function Registers (CPU0)	ok	ok
			General Purpose Registers (CPU0)	ok	ok
			Memory Protection Registers (CPU0)	ok	ok
			Temporal Protection System registers (CPU0)	ok	ok
			Floating point register (CPU0)	ok	ok
			Core Debug Performance Counter registers (CPU0)	ok	ok
			Data Memory Interface registers (CPU0)	ok	ok
			Program Memory Interface registers (CPU0)	ok	ok
$F8820000_H$	$F883FFFF_H$	128 Kbyte	Safety Memory Protection Register (CPU1)	ok	ok
			DLMU Safety Memory Protection registers (CPU1)	ok	ok
			Safety register protection registers (CPU1)	ok	ok
			Kernel Reset registers (CPU1)	ok	ok
			Flash Configuration registers (CPU1)	ok	ok
			Overlay Block Control registers (CPU1)	ok	ok
			Memory Integrity Registers (CPU1)	ok	ok
			Core Special Function Registers (CPU1)	ok	ok
			General Purpose Registers (CPU1)	ok	ok
			Memory Protection Registers (CPU1)	ok	ok
			Temporal Protection System registers (CPU1)	ok	ok
			Floating point register (CPU1)	ok	ok
			Core Debug Performance Counter registers (CPU1)	ok	ok
			Data Memory Interface registers (CPU1)	ok	ok
			Program Memory Interface registers (CPU1)	ok	ok
$F8840000_H$	$FAFFFFFF_H$	-	Reserved	BE	BE
$FB000000_H$	$FB00FFFF_H$	64 Kbyte	EMEM RAM SRI Interface Control Registers (EMEMMPU0)	ok	ok
$FB010000_H$	$FFBFFFFF_H$	-	Reserved	BE	BE
$FFC00000_H$	$FFC1FFFF_H$	128 Kbyte	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter (DMU)	ok	ok
$FFC20000_H$	$FFFFFFFF_H$	-	Reserved	BE	BE

2.4 Bus Instance SPB

Table 3 Address Map as seen by Bus Masters on Bus SPB

Address Range		Size	Unit	Access Type	
from	to			Read	Write
00000000_H	$0FFFFFFF_H$	-	Reserved	BE	BE
10000000_H	$EFFFFFFF_H$	3584 Mbyte	Redirection of SRI ranges (SFIBRIDGE1) Bridge to Bus Segment 00 of SRI (SFIBRIDGE1)	ok	ok
$F0000000_H$	$F00001FF_H$	512 byte	FPI slave interface (FCE)	ok	ok
$F0000200_H$	$F00003FF_H$	-	Reserved	BE	BE
$F0000400_H$	$F00005FF_H$	512 byte	FPI slave interface (CBS)	ok	ok
$F0000600_H$	$F00006FF_H$	256 byte	FPI slave interface (ASCLIN0)	ok	ok
$F0000700_H$	$F00007FF_H$	256 byte	FPI slave interface (ASCLIN1)	ok	ok
$F0000800_H$	$F00008FF_H$	256 byte	FPI slave interface (ASCLIN2)	ok	ok
$F0000900_H$	$F00009FF_H$	256 byte	FPI slave interface (ASCLIN3)	ok	ok
$F0000A00_H$	$F0000AFF_H$	256 byte	FPI slave interface (ASCLIN4)	ok	ok
$F0000B00_H$	$F0000BFF_H$	256 byte	FPI slave interface (ASCLIN5)	ok	ok
$F0000C00_H$	$F0000FFF_H$	-	Reserved	BE	BE
$F0001000_H$	$F00010FF_H$	256 byte	FPI slave interface (STM0)	ok	ok
$F0001100_H$	$F00011FF_H$	256 byte	FPI slave interface (STM1)	ok	ok
$F0001200_H$	$F00017FF_H$	-	Reserved	BE	BE
$F0001800_H$	$F00018FF_H$	256 byte	FPI slave interface (GPT120)	ok	ok
$F0001900_H$	$F0001BFF_H$	-	Reserved	BE	BE
$F0001C00_H$	$F0001CFF_H$	256 byte	Register block QSPI0 (QSPI0)	ok	ok
$F0001D00_H$	$F0001DFF_H$	256 byte	Register block QSPI1 (QSPI1)	ok	ok
$F0001E00_H$	$F0001EFF_H$	256 byte	Register block QSPI2 (QSPI2)	ok	ok
$F0001F00_H$	$F0001FFF_H$	256 byte	Register block QSPI3 (QSPI3)	ok	ok
$F0002000_H$	$F00029FF_H$	-	Reserved	BE	BE
$F0002A00_H$	$F0002AFF_H$	256 byte	FPI slave interface (CCU60)	ok	ok
$F0002B00_H$	$F0002BFF_H$	256 byte	FPI slave interface (CCU61)	ok	ok
$F0002C00_H$	$F0002FFF_H$	-	Reserved	BE	BE
$F0003000_H$	$F0003AFF_H$	2.7 Kbyte	FPI slave interface (SENT)	ok	ok
$F0003B00_H$	$F000FFFF_H$	-	Reserved	BE	BE
$F0010000_H$	$F0013FFF_H$	16 Kbyte	FPI slave interface (DMA)	ok	ok
$F0014000_H$	$F001CFFF_H$	-	Reserved	BE	BE
$F001D000_H$	$F001F0FF_H$	8.2 Kbyte	FPI bus interface (GETH) FPI bus interface (GETH)	ok ok	ok ok
$F001F100_H$	$F001FFFF_H$	-	Reserved	BE	BE
$F0020000_H$	$F0023FFF_H$	16 Kbyte	FPI slave interface (EVADC)	ok	ok
$F0024000_H$	$F0024FFF_H$	-	Reserved	BE	BE

Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
$F0025000_H$	$F00250FF_H$	256 byte	FPI slave interface (CONVCTRL)	ok	ok
$F0025100_H$	$F002FFFF_H$	-	Reserved	BE	BE
$F0030000_H$	$F00300FF_H$	256 byte	BCU Registers (SBCU)	ok	ok
$F0030100_H$	$F0035FFF_H$	-	Reserved	BE	BE
$F0036000_H$	$F00363FF_H$	1 Kbyte	SCU: Connections to FPI/BPI bus (SCU) Clocking System Registers (SCU) Power Management Registers (SCU)	ok ok ok	ok ok ok
$F0036400_H$	$F00367FF_H$	-	Reserved	BE	BE
$F0036800_H$	$F0036FFF_H$	2 Kbyte	FPI slave interface (SMU)	ok	ok
$F0037000_H$	$F0037FFF_H$	4 Kbyte	IR Status and Control Registers (INT)	ok	ok
$F0038000_H$	$F0039FFF_H$	8 Kbyte	IR Service Request Control Registers (SRC) (SRC)	ok	ok
$F003A000_H$	$F003A0FF_H$	256 byte	SPB bus slave interface (P00)	ok	ok
$F003A100_H$	$F003A1FF_H$	-	Reserved	BE	BE
$F003A200_H$	$F003A2FF_H$	256 byte	SPB bus slave interface (P02)	ok	ok
$F003A300_H$	$F003A9FF_H$	-	Reserved	BE	BE
$F003AA00_H$	$F003AAFF_H$	256 byte	SPB bus slave interface (P10)	ok	ok
$F003AB00_H$	$F003ABFF_H$	256 byte	SPB bus slave interface (P11)	ok	ok
$F003AC00_H$	$F003ACFF_H$	256 byte	SPB bus slave interface (P12)	ok	ok
$F003AD00_H$	$F003ADFF_H$	-	Reserved	BE	BE
$F003AE00_H$	$F003AEFF_H$	256 byte	SPB bus slave interface (P14)	ok	ok
$F003AF00_H$	$F003AFFF_H$	256 byte	SPB bus slave interface (P15)	ok	ok
$F003B000_H$	$F003B3FF_H$	-	Reserved	BE	BE
$F003B400_H$	$F003B4FF_H$	256 byte	SPB bus slave interface (P20)	ok	ok
$F003B500_H$	$F003B5FF_H$	256 byte	SPB bus slave interface (P21)	ok	ok
$F003B600_H$	$F003B6FF_H$	256 byte	SPB bus slave interface (P22)	ok	ok
$F003B700_H$	$F003B7FF_H$	256 byte	SPB bus slave interface (P23)	ok	ok
$F003B800_H$	$F003BFFF_H$	-	Reserved	BE	BE
$F003C000_H$	$F003C0FF_H$	256 byte	SPB bus slave interface (P32)	ok	ok
$F003C100_H$	$F003C1FF_H$	256 byte	SPB bus slave interface (P33)	ok	ok
$F003C200_H$	$F003C2FF_H$	256 byte	SPB bus slave interface (P34)	ok	ok
$F003C300_H$	$F003FFFF_H$	-	Reserved	BE	BE
$F0040000_H$	$F005FFFF_H$	128 Kbyte	System Registers (HSM) Debug Registers (HSM) Communication Registers (HSM) HSM Reset (HSM)	32 32 32 32	32 32 32 32
$F0060000_H$	$F006FFFF_H$	64 Kbyte	FPI slave interface (MTU) FPI slave interface (MTU)	ok ok	ok ok
$F0070000_H$	$F01FFFFF_H$	-	Reserved	BE	BE

Table 3 Address Map as seen by Bus Masters on Bus SPB (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
$F0200000_H$	$F0208FFF_H$	36 Kbyte	RAM Area (CAN0) Register Area (CAN0)	ok ok	ok ok
$F0209000_H$	$F023FFFF_H$	-	Reserved	BE	BE
$F0240000_H$	$F0241FFF_H$	8 Kbyte	Standby Controller XRAM (PMS)	ok	ok
$F0242000_H$	$F0247FFF_H$	-	Reserved	BE	BE
$F0248000_H$	$F02481FF_H$	512 byte	FPI slave interface (PMS) SMU registers in Standby power domain (PMS)	ok ok	ok ok
$F0248200_H$	$F027FFFF_H$	-	Reserved	BE	BE
$F0280000_H$	$F0281FFF_H$	8 Kbyte	RAM Area (HSPDM)	ok	ok
$F0282000_H$	$F02820FF_H$	256 byte	FPI slave interface for BPI registers access (HSPDM)	ok	ok
$F0282100_H$	$F02AFFFF_H$	-	Reserved	BE	BE
$F02B0000_H$	$F02B0FFF_H$	4 Kbyte	FPI slave interface (SDMMC0)	ok	ok
$F02B1000_H$	$F7FFFFFF_H$	-	Reserved	BE	BE
$F8000000_H$	$FFFFFFFF_H$	128 Mbyte	Redirection of SRI ranges (SFIBRIDGE1)	ok	ok

2.5 Bus Instance BBB

Table 4 Address Map as seen by Bus Masters on Bus BBB

Address Range		Size	Unit	Access Type	
from	to			Read	Write
00000000_H	$98FFFFFF_H$	-	Reserved	BE	BE
99000000_H	$990FFFFF_H$	1 Mbyte	BBB slave interface 0 (access to EMEM module RAM, cached segment) (EMEMRAM0)	ok	ok
99100000_H	$B8FFFFFF_H$	-	Reserved	BE	BE
$B9000000_H$	$B90FFFFF_H$	1 Mbyte	BBB slave interface 0 (access to EMEM module RAM, non-cached segment) (EMEMRAM0)	ok	ok
$B9100000_H$	$B93FFFFF_H$	-	Reserved	BE	BE
$B9400000_H$	$B947FFFF_H$	512 Kbyte	XTM FPI slave interface (XTM)	ok	ok
$B9480000_H$	$EFFFFFFF_H$	-	Reserved	BE	BE
$F0000000_H$	$FA0000FF_H$	-	Reserved	BE	BE
$FA000100_H$	$FA0001FF_H$	256 byte	BCU Registers (EBCU)	ok	ok
$FA000200_H$	$FA000FFF_H$	-	Reserved	BE	BE
$FA001000_H$	$FA0010FF_H$	256 byte	FPI slave interface (AGBT)	ok	ok
$FA001100_H$	$FA005FFF_H$	-	Reserved	BE	BE
$FA006000_H$	$FA0060FF_H$	256 byte	BPI SFF (access to EMEM core registers) (EMEM)	ok	ok
$FA006100_H$	$FA00FFFF_H$	-	Reserved	BE	BE
$FA010000_H$	$FA01FFFF_H$	64 Kbyte	FPI slave interface (MCDSLIGHT)	ok	ok
$FA020000_H$	$FA03FFFF_H$	-	Reserved	BE	BE

Table 4 Address Map as seen by Bus Masters on Bus BBB (cont'd)

Address Range		Size	Unit	Access Type	
from	to			Read	Write
$FA040000_H$	$FA0401FF_H$	512 byte	FPI slave interface (RIF0)	ok	ok
$FA040200_H$	$FA7FFFFF_H$	-	Reserved	BE	BE
$FA800000_H$	$FA8007FF_H$	2 Kbyte	SPU Registers (SPU0)	ok	ok
$FA800800_H$	$FA9FFFFF_H$	-	Reserved	BE	BE
$FAA00000_H$	$FAA0FFFF_H$	64 Kbyte	SPU Configuration Memory (SPU0)	32	32
$FAA10000_H$	$FFFFFFFF_H$	-	Reserved	BE	BE

2.6 Revision History

Table 5 Revision History

Reference	Change to Previous Version	Comment
V0.1.12		
–	First release for TC33xEXT.	–
V0.1.13		
–	No changes. Only version number changed to keep alignment with family address map.	–
V0.1.14		
–	No changes. Only version number changed to keep alignment with family address map.	–
V0.1.15		
–	No changes. Only version number changed to keep alignment with family address map.	–
V0.1.16		
–	No changes. Only version number changed to keep alignment with family address map.	–
V0.1.17		
–	No changes. Only version number changed to keep alignment with family address map.	–
V0.1.18		
–	No changes. Only version number changed to keep alignment with family address map.	–
V0.1.19		
–	No changes. Only version number changed to keep alignment with family address map.	
V0.1.20		
–	No changes. Only version number changed to keep alignment with family address map.	
V0.1.21		
Page 7, **Page 9**	In bus instances SPB and BBB several address ranges corrected to “BE”.	

3 TC33xEXT Firmware

This chapter supplements the family documentation with device specific information for TC33xEXT devices.

3.1 Checker Software exit information for ALL CHECKS PASSED

Below the SCU_STMEM3...SCU_STMEM6 registers' content corresponding to "ALL CHECKS PASSED" result from Checker Software (CHSW) upon different device reset types is shown.

Table 6 "ALL CHECKS PASSED" indication by CHSW for TC33xEXT

Reset type	Additional conditions	SCU_STMEM3	SCU_STMEM4	SCU_STMEM5	SCU_STMEM6
Cold power-on [1]	--	$A073FB1F_H$	00000001_H	$A073FB1F_H$	$A073FB1F_H$
Warm power-on	--	$A063F82F_H$	00000001_H	$A063F82F_H$	$A063F82F_H$
System reset	--	$2060B84F_H$	00000001_H	$2060B84F_H$	$2060B84F_H$
Application reset	CCUCON5.GETHDIV<>0 CCUCON5.ADASDIV<>0	$2060088F_H$	00000001_H	$2060088F_H$	$2060088F_H$
	CCUCON5.GETHDIV<>0 CCUCON5.ADASDIV=0	$2060088F_H$	00400001_H	$2020088F_H$	$2060088F_H$
	CCUCON5.GETHDIV=0 CCUCON5.ADASDIV<>0	$2060088F_H$	00200001_H	$2040088F_H$	$2060088F_H$
	CCUCON5.GETHDIV=0 CCUCON5.ADASDIV=0	$2060088F_H$	00600001_H	$2000088F_H$	$2060088F_H$

1) Device start-up after LBIST execution is handled by AURIX™ TC3xx Firmware as cold power-on, therefore the SCU_STMEMx values in this row apply also in such a case (after LBIST).

Note: The result from some check(s) depends on additional conditions as follows:

1. *The check for Gigabit Ethernet MAC module calibration will fail after application reset, if the application software has not enabled GETH clock (in SCU_CCUCON5.GETHDIV register) after the previous power-on/system reset(s) - meaning if the module is not used by application - therefore in such use-case anyway the check for this' module calibration is not relevant.*
2. *The check for RIF module calibration will fail after application reset, if the application software has not enabled ADAS clock (in SCU_CCUCON5.ADASDIV register) after the previous power-on/system reset(s) - meaning if the module is not used by application - therefore in such use-case anyway the check for this' module calibration is not relevant.*

3.2 Revision History

Table 7 Revision History

Reference	Change to Previous Version	Comment
V1.1.0.1.14		
	First version of this document	
V1.1.0.1.15, V1.1.0.1.16		
	No change	
V1.1.0.1.17		

Table 7 Revision History

Reference	Change to Previous Version	Comment
Table 6	Footnote added, explaining FW handling after LBIST execution (documentation improvement only, no change in implementation)	
V1.1.0.1.18		
–	No functional changes	

4 On-Chip System Connectivity {and Bridges}

Text with reference to family spec.

4.1 TC33xEXT Specific IP Configuration

Table 8 TC33xEXT specific configuration of DOM

Parameter	DOM0
Application Reset	Application Reset
Access only when any Endinit (SCU_WDTCPUxCON0.EI = 0 for any CPUx)	ENDINIT
Access only when Safety Endinit (SCU_SEICON.EI = 0)	Safety ENDINIT
Access only from HSM Master or HSM debug (or FPRO.PROINHSMCFG=0)	HSM Access
Access only when PSW = Supervisor Mode	Supervisor Mode
Access only when PSW = User Mode 0 or 1	User Mode
Access only when OCDS enabled	Debug Mode
Access only from Master x (when MOD_ACCEN0.ENx = 1 or MOD_ACCEN1.ENx = 1)	Valid Master
Access only from Master x (when MOD_ACCEN0.ENx = 1)	Valid Master (0)
Access only from Master x (when MOD_ACCEN1.ENx = 1)	Valid Master (1)
Number of SCI interfaces	16
sri base address	$F8700000_H$
sri address range	10000_H
OLDA base address	$8FE00000_H$
OLDA range	80000_H
OLDA base address (non-cached)	$AFE00000_H$
OLDA range (non-cached)	80000_H

4.2 TC33xEXT Specific Register Set

Register Address Space Table

Table 9 Register Address Space - DOM

Module	Base Address	End Address	Note
(DOM0)	$8FE00000_H$	$8FE7FFFF_H$	Online Data Acquisition (OLDA)
	$AFE00000_H$	$AFE7FFFF_H$	Online Data Acquisition (OLDA)
DOM0	$F8700000_H$	$F870FFFF_H$	sri slave interface

Register Overview Table

Table 10 Register Overview - DOM0 (ascending Offset Address)

Short Name	Description	Offset Address	Access Mode		Page Number
			Read	Write	
DOM0_PECONx (x=0-15)	Protocol Error Control Register x	00000_H+ x*20_H	32,U,SV	32,P,SV	See Family Spec
DOM0_PRIORITYx (x=0-15)	SCIx Arbiter Priority Register	00008_H+ x*20_H	32,U,SV	32,P,SV	See Family Spec
DOM0_ERRADDRx (x=0-15)	SCI x Error Address Capture Register	00010_H+ x*20_H	32,U,SV	32,P,SV	See Family Spec
DOM0_ERRx (x=0-15)	SCI x Error Capture Register	00018_H+ x*20_H	32,U,SV	32,P,SV	See Family Spec
DOM0_ID	Identification Register	00408_H	32,U,SV	BE	See Family Spec
DOM0_PESTAT	Protocol Error Status Register	00410_H	32,U,SV	32,P,SV	See Family Spec
DOM0_TIDSTAT	Transaction ID Status Register	00418_H	32,U,SV	32,P,SV	See Family Spec
DOM0_TIDEN	Transaction ID Enable Register	00420_H	32,U,SV	32,P,SV	See Family Spec
DOM0_BRCON	Domain 0 Bridge Control Register	00430_H	32,U,SV	32,P,SV	4

Table 10 Register Overview - DOM0 (ascending Offset Address) (cont'd)

Short Name	Description	Offset Address	Access Mode		Page Number
			Read	Write	
DOM0_ACCEN0	Access Enable Register 0	$004F0_H$	32,U,SV	32,SV,SE	See Family Spec
DOM0_ACCEN1	Access Enable Register 1	$004F8_H$	32,U,SV	32,SV,SE	See Family Spec

4.3 TC33xEXT Specific Registers

4.3.1 sri slave interface

Domain 0 Bridge Control Register

DOM0_BRCON
Domain 0 Bridge Control Register **(00430_H)** **Application Reset Value: $0000\ 0200_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												0			
r												rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			0		0	1	0		0	0					OLDAEN
rw			r		rw	rw	r		rw	r					rw

Field	Bits	Type	Description
OLDAEN	0	rw	**Online Data Acquisition Enable** This bit is used to control trap generated for write accesses to the OLDA address range associated with this domain. 0_B Trap generated on a write access to the OLDA memory range. 1_B No trap generated on a write access to the OLDA memory range.
0	5:1, 8:7, 12:11, 31:20	r	**Reserved** Read as 0; shall be written with 0.
0	6, 10, 19:13	rw	**Reserved** Read as 0; shall be written with 0.
1	9	rw	**Reserved** Read as 1; shall be written with 1.

4.4 Connectivity

No connections in TC33xEXT

4.5 Interconnection Matrices

4.5.1 Domain 0 Interconnection Matrix

By default the crossbar connects MCIs to SCIs. The following connectivity matrix highlights (in red and yellow) the MCI to SCI interconnects that are non-standard in the TC33xEXT. The unimplemented connections are redundant as they would not be useful (illegal or trapping) therefore do not restrict the functionality.

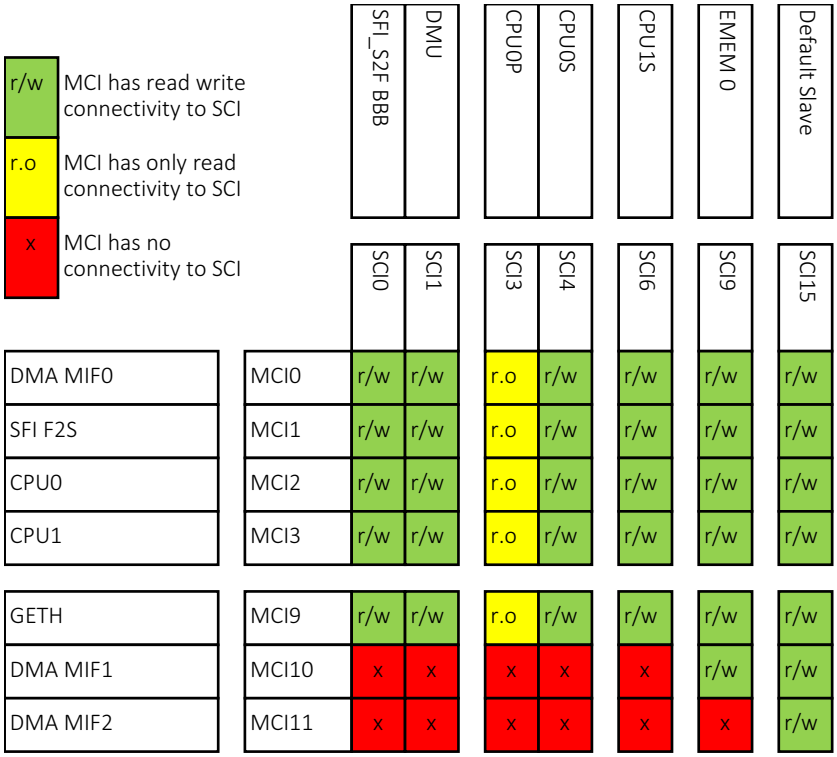


Figure 1 TC33xEXT Domain0 Connectivity Matrix

4.6 Revision History

Table 11 Revision History

Reference	Change to Previous Version	Comment
V1.1.13		
Page 4	Updated BRCON bitfield to show that bit 9 while reserved will read as 1 and should be updated to 1 (The bitfield was incorrectly showing value 0 previously). Restored correct access permission (r/w) for bit fields which are not intended for customer function.	
Page 5	Updated connectivity matrix to show 3 DMA MIF's. DMA MIF2 is not functional.	
V1.1.14		
	No change.	
V1.1.15		
	No change.	
V1.1.16		
	No change.	
V1.1.17		
	No change.	

4.7 FPI Bus Control Units (SBCU, EBCU)

This chapter supplements the family documentation with device specific information for TC33xEXT.

4.7.1 TC33xEXT Specific IP Configuration

The TC33xEXT includes two FPI Bus instances. Each FPI Bus instances has its dedicated Bus Control Unit:

Table 12 Register Address Space - BCU

Module	Base Address	End Address	Note
(EBCU)	$F0000000_H$	$FFFFFFFF_H$	FPI default slave
EBCU	$FA000100_H$	$FA0001FF_H$	BCU Registers
(SBCU)	$F0000000_H$	$F7FFFFFF_H$	FPI default slave
SBCU	$F0030000_H$	$F00300FF_H$	BCU Registers

- System Peripheral Bus (SPB) -> SBCU. The SBCU registers are described in **Chapter 4.7.2**
- Back Bone bus (BBB) -> EBCU. The EBCU registers are described in **Chapter 4.7.3**

4.7.2 SBCU Control Unit Registers

Figure 2 and **Table 13** are showing the address maps with all registers of the System Bus Control Unit (SBCU) module.

List of used Reset Class abbreviations:

- Reset Class 1 -> Debug Reset, Power-on Reset (see chapter SCU / Reset Types)
- Reset Class 3 -> Application Reset, System Reset, Power-on Reset (see chapter SCU / Reset Types)

SBCU Control Registers Overview

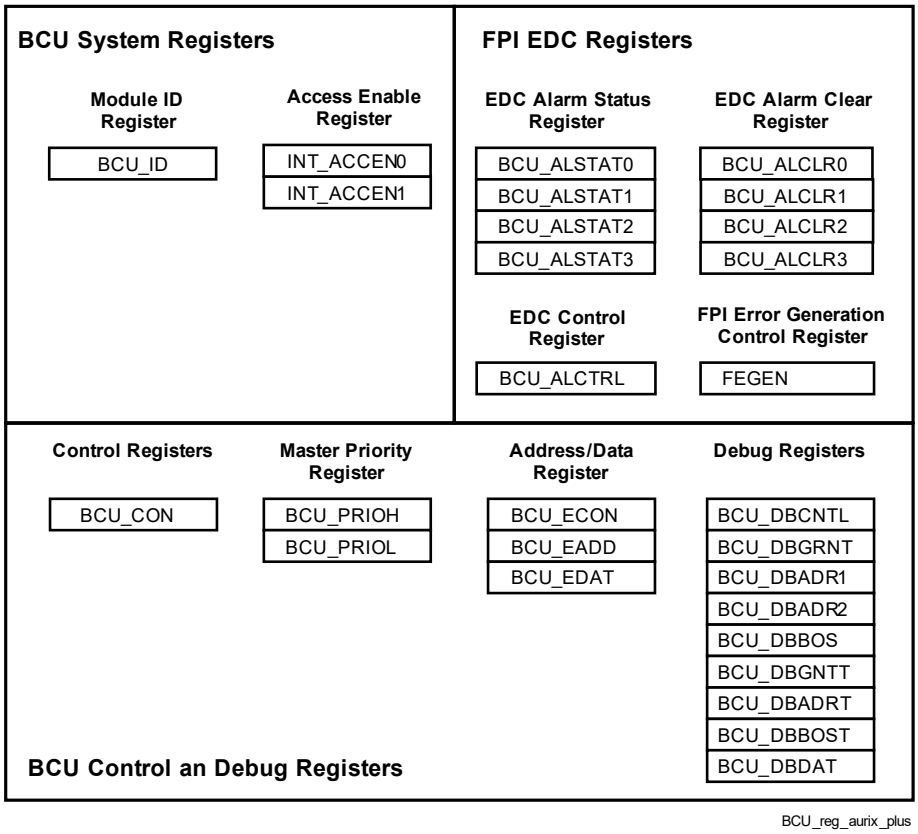


Figure 2 SBCU Registers

Table 13 Register Overview - SBCU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SBCU_ID	Module Identification Register	0008_H	U,SV	BE	Application Reset	See Family Spec
SBCU_CON	BCU Control Register	0010_H	U,SV	SV,P	Application Reset	See Family Spec
SBCU_PRIOH	Arbiter Priority Register High	0014_H	U,SV	SV,E,P	Application Reset	9
SBCU_PRIOL	Arbiter Priority Register Low	0018_H	U,SV	SV,E,P	Application Reset	10
SBCU_ECON	BCU Error Control Capture Register	0020_H	U,SV	SV,P	Application Reset	See Family Spec

Table 13 Register Overview - SBCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SBCU_EADD	BCU Error Address Capture Register	0024_H	U,SV	SV,P	Application Reset	See Family Spec
SBCU_EDAT	BCU Error Data Capture Register	0028_H	U,SV	SV,P	Application Reset	See Family Spec
SBCU_DBCNTL	BCU Debug Control Register	0030_H	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBGRNT	SBCU Debug Grant Mask Register	0034_H	U,SV	SV,P	Debug Reset	10
SBCU_DBADR1	BCU Debug Address 1 Register	0038_H	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBADR2	BCU Debug Address 2 Register	$003C_H$	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBBOS	BCU Debug Bus Operation Signals Register	0040_H	U,SV	SV,P	Debug Reset	See Family Spec
SBCU_DBGNTT	SBCU Debug Trapped Master Register	0044_H	U,SV	BE	Debug Reset	12
SBCU_DBADRT	BCU Debug Trapped Address Register	0048_H	U,SV	BE	Debug Reset	See Family Spec
SBCU_DBBOST	BCU Debug Trapped Bus Operation Signals Register	$004C_H$	U,SV	BE	Debug Reset	See Family Spec
SBCU_DBDAT	BCU Debug Data Status Register	0050_H	U,SV	BE	Debug Reset	See Family Spec
SBCU_ALSTATx (x=0-3)	BCU EDC Alarm Status Register x	0060_H+x *4	U,SV	SV,P	Application Reset	13
SBCU_ALCLRx (x=0-3)	BCU EDC Alarm Clear Register x	0070_H+x *4	U,SV	SV,P	Application Reset	See Family Spec
SBCU_ALCTRL	BCU EDC Alarm Control Register	0080_H	U,SV	SV,P	Application Reset	See Family Spec
SBCU_FEGEN	FPI Error Generation Control Register	0084_H	U,SV	SV,SE	Application Reset	See Family Spec

Table 13 Register Overview - SBCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SBCU_ACCEN1	Access Enable Register 1	$00F8_H$	U,SV	SV,SE	Application Reset	See Family Spec
SBCU_ACCEN0	Access Enable Register 0	$00FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

4.7.2.1 SBCU Control Registers Descriptions

Note: For all PRIOH / PRIOL bit fields, a lower number has a higher priority in the arbitration round than a higher one.

Arbiter Priority Register High

SBCU_PRIOH
Arbiter Priority Register High (0014_H) Application Reset Value: $FEDC\ 8888_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED				HSMCMI				HSMRMI			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
rw				rw				rw				rw			

Field	Bits	Type	Description
RESERVED	3:0, 7:4, 11:8, 15:12, 27:24, 31:28	rw	**Reserved** Read as reset value or last written value; should be written with 0.
HSMRMI	19:16	rw	**HSMRMI Priority (Index 12)** This bit field defines the priority on the SPB for HSMRMI access to the SPB.
HSMCMI	23:20	rw	**HSMCMI Priority (Index 13)** This bit field defines the priority on the SPB for HSMCMI access to the SPB.

Arbiter Priority Register Low

SBCU_PRIOL
Arbiter Priority Register Low **(0018_H)** **Application Reset Value: 8854 3210$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CPU1				CPU0				RESERVED				RESERVED			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				SDMMC				RESERVED				DMA			
rw				rw				rw				rw			

Field	Bits	Type	Description
DMA	3:0	rw	**DMA / Cerberus Priority (Index 0)** This bit field defines the priority on the SPB for DMA and Cerberus access to the SPB.
RESERVED	7:4, 15:12, 19:16, 23:20	rw	**Reserved** Read as reset value or last written value; should be written with 0.
SDMMC	11:8	rw	**SDMMC Priority (Index 2)** This bit field defines the priority on the SPB for SDMMC access to the SPB.
CPU0	27:24	rw	**CPU0 Priority (Index 6)** This bit field defines the priority on the SPB for CPU0 access to the SPB.
CPU1	31:28	rw	**CPU1 Priority (Index 7)** This bit field defines the priority on the SPB for CPU1 access to the SPB.

4.7.2.2 SBCU OCDS Registers Descriptions

SBCU Debug Grant Mask Register

SBCU_DBGRNT
SBCU Debug Grant Mask Register **(0034_H)** **Debug Reset Value: 0000 FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	HSMCMI	HSMRMI	1	1	1	1	CPU1	CPU0	1	1	1	SDMMC	1	DMA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
DMA	0	rw	**DMA / Cerberus Trigger Enable** 0_B FPI Bus transactions with DMA / Cerberus as bus master are enabled for grant trigger event generation. 1_B FPI Bus transactions with DMA / Cerberus as bus master are disabled for grant trigger event generation.
SDMMC	2	rw	**SDMMC Trigger Enable** 0_B FPI Bus transactions with SDMMC as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with SDMMC as bus master are disabled for grant trigger event generation
CPU0	6	rw	**CPU0 Grant Trigger Enable** 0_B FPI Bus transactions with CPU0 as bus master are enabled for grant trigger event generation. 1_B FPI Bus transactions with CPU as bus master are disabled for grant trigger event generation.
CPU1	7	rw	**CPU1 Grant Trigger Enable** 0_B FPI Bus transactions with CPU1 as bus master are enabled for grant trigger event generation. 1_B FPI Bus transactions with CPU1 as bus master are disabled for grant trigger event generation.
HSMRMI	12	rw	**HSM Register Master Interface Grant Trigger Enable** 0_B FPI Bus transactions requested by the HSM bus master are enabled for grant trigger event generation. 1_B FPI Bus transactions requested by the HSM bus master are disabled for grant trigger event generation.
HSMCMI	13	rw	**HSM Cache Master Interface Grant Trigger Enable** 0_B FPI Bus transactions requested by the HSM bus master are enabled for grant trigger event generation. 1_B FPI Bus transactions requested by the HSM bus master are disabled for grant trigger event generation.
1	1, 3, 4, 5, 8, 9, 10, 11, 14, 15	rw	**Reserved** Read as 1 after reset; reading these bits will return the value last written.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

SBCU Debug Trapped Master Register

SBCU_DBGNTT

SBCU Debug Trapped Master Register (0044$_H$) Debug Reset Value: 0000 FFFF$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**1**	**HSMCMI**	**HSMRMI**	**1**	**1**	**1**	**1**	**CPU1**	**CPU0**	**1**	**1**	**1**	**SDMMC**	**1**	**DMA**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DMA	0	rh	**DMA / Cerberus FPI Bus Master Status** 0_B The DMA or Cerberus was the FPI bus master. 1_B Neither DMA nor Cerberus was the FPI Bus master.
SDMMC	2	rh	**SDMMC FPI Bus Master Status** This bit indicates whether the SDMMC was FPI Bus master when the break trigger event occurred. 0_B The SDMMC was the FPI bus master. 1_B The SDMMC was not the FPI Bus master.
CPU0	6	rh	**CPU0 FPI Bus Master Status** This bit indicates whether the CPU0 was FPI Bus master when the break trigger event occurred. 0_B The CPU0 was the FPI Bus master. 1_B The CPU0 was not the FPI Bus master.
CPU1	7	rh	**CPU1 FPI Bus Master Status** This bit indicates whether the CPU1 was FPI Bus master when the break trigger event occurred. 0_B The CPU1 was the FPI Bus master. 1_B The CPU1 was not the FPI Bus master.
HSMRMI	12	rh	**HSM Register FPI Bus Master Interface Status** This bit indicates whether the HSM was FPI Bus master when the break trigger event occurred. 0_B HSMRMI was the FPI bus master. 1_B HSMRMI was not the FPI Bus master.
HSMCMI	13	rh	**HSM Cache FPI Bus Master Interface Status** This bit indicates whether the HSM was FPI Bus master when the break trigger event occurred. 0_B HSMCMI was the FPI bus master. 1_B HSMCMI was not the FPI Bus master.

Field	Bits	Type	Description
1	1, 3, 4, 5, 8, 9, 10, 11, 14, 15	rh	**Reserved** Read as 1 after reset; reading these bits will return the value last written.
0	31:16	rh	**Reserved** Read as 1 after reset; reading these bits will return the value last written.

BCU EDC Alarm Status Register x

The BCU provides one Alarm Status Register bit for each implemented FPI master and FPI slave.

Register bits without constant definition are reserved in this product.

SBCU_ALSTATx (x=0)

BCU EDC Alarm Status Register x **(0060_H+x*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	**AL30**	**AL29**	**AL28**	**AL27**	**AL26**	**AL25**	**AL24**	**AL23**	**AL22**	**AL21**	**AL20**	**AL19**	**AL18**	**AL17**	**AL16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	**AL14**	**AL13**	**AL12**	**AL11**	**AL10**	**AL09**	**AL08**	**AL07**	**AL06**	**AL05**	**AL04**	**AL03**	**AL02**	**AL01**	**AL00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	**Alarm y** 1_B **SBCU_S**, an EDC error was detected in an active phase of the SBCU Slave Interface.
ALy (y=01)	y	rh	**Alarm y** 1_B **DMA_S**,
ALy (y=02)	y	rh	**Alarm y** 1_B **IR_S**,
ALy (y=03)	y	rh	**Alarm y** 1_B **SFI_F2S_S**,
ALy (y=04)	y	rh	**Alarm y** 1_B **SCU_S**,
ALy (y=05)	y	rh	**Alarm y** 1_B **SMU_S**,
ALy (y=06)	y	rh	**Alarm y** 1_B **PMC_SCR_S**,

Field	Bits	Type	Description
ALy (y=07)	y	rh	**Alarm y** 1_B **MTU_S**,
ALy (y=08)	y	rh	**Alarm y** 1_B **IOM_S**,
ALy (y=09,13,18-19,21,24-31)	y	rh	**Alarm y**
ALy (y=10)	y	rh	**Alarm y** 1_B **ASCLIN01_S**,
ALy (y=11)	y	rh	**Alarm y** 1_B **ASCLIN23_S**,
ALy (y=12)	y	rh	**Alarm y** 1_B **ASCLIN45_S**,
ALy (y=14)	y	rh	**Alarm y** 1_B **QSPI0_S**,
ALy (y=15)	y	rh	**Alarm y** 1_B **QSPI1_S**,
ALy (y=16)	y	rh	**Alarm y** 1_B **QSPI2_S**,
ALy (y=17)	y	rh	**Alarm y** 1_B **QSPI3_S**,
ALy (y=20)	y	rh	**Alarm y** 1_B **FCE0_S**,
ALy (y=22)	y	rh	**Alarm y** 1_B **STM0_S**,
ALy (y=23)	y	rh	**Alarm y** 1_B **STM1_S**,

SBCU_ALSTATx (x=1)

BCU EDC Alarm Status Register x **(0060_H+x*4)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	**AL30**	**AL29**	**AL28**	**AL27**	**AL26**	**AL25**	**AL24**	**AL23**	**AL22**	**AL21**	**AL20**	**AL19**	**AL18**	**AL17**	**AL16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	**AL14**	**AL13**	**AL12**	**AL11**	**AL10**	**AL09**	**AL08**	**AL07**	**AL06**	**AL05**	**AL04**	**AL03**	**AL02**	**AL01**	**AL00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	**Alarm y** 1_B **GPT12_S**, an EDC error was detected in an active phase of the GPT12 Slave Interface.

Field	Bits	Type	Description
ALy (y=01)	y	rh	**Alarm y** 1_B **CCU6_S**,
ALy (y=02-06,10,12,14-18,20-27)	y	rh	**Alarm y**
ALy (y=07)	y	rh	**Alarm y** 1_B **SENT_S**,
ALy (y=08)	y	rh	**Alarm y** 1_B **ETH_S**,
ALy (y=09)	y	rh	**Alarm y** 1_B **EVADC_S**,
ALy (y=11)	y	rh	**Alarm y** 1_B **HSM_S**,
ALy (y=13)	y	rh	**Alarm y** 1_B **CAN0_S**,
ALy (y=19)	y	rh	**Alarm y** 1_B **CONVCTRL_S**,
ALy (y=28)	y	rh	**Alarm y** 1_B **HSPDM_SRAM_S**,
ALy (y=29)	y	rh	**Alarm y** 1_B **HSPDM_SFR_S**,
ALy (y=30)	y	rh	**Alarm y** 1_B **SDMMC_S**,
ALy (y=31)	y	rh	**Alarm y** 1_B **CERBERUS_S**,

SBCU_ALSTATx (x=2)

BCU EDC Alarm Status Register x **(0060_H+x*4)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	**AL30**	**AL29**	**AL28**	**AL27**	**AL26**	**AL25**	**AL24**	**AL23**	**AL22**	**AL21**	**AL20**	**AL19**	**AL18**	**AL17**	**AL16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	**AL14**	**AL13**	**AL12**	**AL11**	**AL10**	**AL09**	**AL08**	**AL07**	**AL06**	**AL05**	**AL04**	**AL03**	**AL02**	**AL01**	**AL00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	**Alarm y** 1_B **P00_S**, an EDC error was detected in an active phase of the Port 00 Slave Interface.

Field	Bits	Type	Description
ALy (y=01,03,07,10,15-20,24,26,28-30)	y	rh	**Alarm y**
ALy (y=02)	y	rh	**Alarm y** 1_B **P02_S**,
ALy (y=04)	y	rh	**Alarm y** 1_B **P10_S**,
ALy (y=05)	y	rh	**Alarm y** 1_B **P11_S**,
ALy (y=06)	y	rh	**Alarm y** 1_B **P12_S**,
ALy (y=08)	y	rh	**Alarm y** 1_B **P14_S**,
ALy (y=09)	y	rh	**Alarm y** 1_B **P15_S**,
ALy (y=11)	y	rh	**Alarm y** 1_B **P20_S**,
ALy (y=12)	y	rh	**Alarm y** 1_B **P21_S**,
ALy (y=13)	y	rh	**Alarm y** 1_B **P22_S**,
ALy (y=14)	y	rh	**Alarm y** 1_B **P23_S**,
ALy (y=21)	y	rh	**Alarm y** 1_B **P32_S**,
ALy (y=22)	y	rh	**Alarm y** 1_B **P33_S**,
ALy (y=23)	y	rh	**Alarm y** 1_B **P34_S**,
ALy (y=25)	y	rh	**Alarm y** 1_B **P40_S**,
ALy (y=27)	y	rh	**Alarm y** 1_B **P50_S**,
ALy (y=31)	y	rh	**Alarm y** 1_B **SBCU_M**, an EDC error was detected in an active phase of the SBCU Master Interface.

SBCU_ALSTATx (x=3)
BCU EDC Alarm Status Register x **(0060_H+x*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	**AL30**	**AL29**	**AL28**	**AL27**	**AL26**	**AL25**	**AL24**	**AL23**	**AL22**	**AL21**	**AL20**	**AL19**	**AL18**	**AL17**	**AL16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	**AL14**	**AL13**	**AL12**	**AL11**	**AL10**	**AL09**	**AL08**	**AL07**	**AL06**	**AL05**	**AL04**	**AL03**	**AL02**	**AL01**	**AL00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	**Alarm y** 1_B **A_EN**, multiple output enables active: A_EN_N (Master)
ALy (y=01)	y	rh	**Alarm y** 1_B **ABORT_EN**, multiple output enables active: ABORT_EN_N (Master)
ALy (y=02)	y	rh	**Alarm y** 1_B **ACK_EN**, multiple output enables active: ACK_EN_N (Default Master and Slave)
ALy (y=03)	y	rh	**Alarm y** 1_B **D_EN**, multiple output enables active: D_EN_N (Master and Slave)
ALy (y=04-15,17,19-21,24-27,30-31)	y	rh	**Alarm y**
ALy (y=16)	y	rh	**Alarm y** 1_B **DMA_M**, an EDC error was detected in an active phase of the DMA / Cerberus Master Interface.
ALy (y=18)	y	rh	**Alarm y** 1_B **SDMMC_M**,
ALy (y=22)	y	rh	**Alarm y** 1_B **CPU0_M**,
ALy (y=23)	y	rh	**Alarm y** 1_B **CPU1_M**,
ALy (y=28)	y	rh	**Alarm y** 1_B **HSMRMI_M**,
ALy (y=29)	y	rh	**Alarm y** 1_B **HSMCMI_M**,

4.7.3 EBCU Control Unit Registers

Figure 3 and **Table 14** are showing the address maps with all registers of the Back Bone Bus (BBB) Bus Control Unit (EBCU) module.

List of used Reset Class abbreviations:

- Reset Class 1 -> Debug Reset, Power-on Reset (see chapter SCU / Reset Types)

- Reset Class 3 -> Application Reset, System Reset, Power-on Reset (see chapter SCU / Reset Types)

EBCU Control Registers Overview

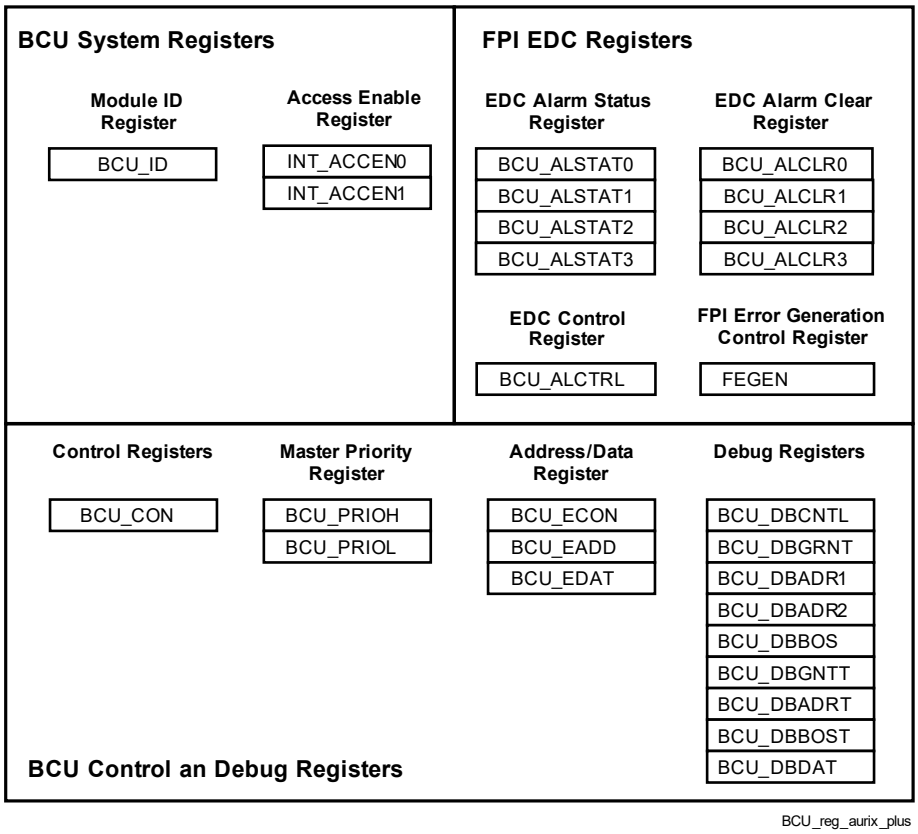


Figure 3 EBCU Registers

Table 14 Register Overview - EBCU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
EBCU_ID	Module Identification Register	0008_H	U,SV	BE	Application Reset	See Family Spec
EBCU_CON	BCU Control Register	0010_H	U,SV	SV,P	Application Reset	See Family Spec
EBCU_PRIOH	Arbiter Priority Register High	0014_H	U,SV	SV,E,P	Application Reset	20
EBCU_PRIOL	Arbiter Priority Register Low	0018_H	U,SV	SV,E,P	Application Reset	20
EBCU_ECON	BCU Error Control Capture Register	0020_H	U,SV	SV,P	Application Reset	See Family Spec

Table 14 Register Overview - EBCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
EBCU_EADD	BCU Error Address Capture Register	0024_H	U,SV	SV,P	Application Reset	See Family Spec
EBCU_EDAT	BCU Error Data Capture Register	0028_H	U,SV	SV,P	Application Reset	See Family Spec
EBCU_DBCNTL	BCU Debug Control Register	0030_H	U,SV	SV,P	Debug Reset	21
EBCU_DBGRNT	EBCU Debug Grant Mask Register	0034_H	U,SV	SV,P	Debug Reset	23
EBCU_DBADR1	BCU Debug Address 1 Register	0038_H	U,SV	SV,P	Debug Reset	See Family Spec
EBCU_DBADR2	BCU Debug Address 2 Register	$003C_H$	U,SV	SV,P	Debug Reset	See Family Spec
EBCU_DBBOS	BCU Debug Bus Operation Signals Register	0040_H	U,SV	SV,P	Debug Reset	See Family Spec
EBCU_DBGNTT	EBCU Debug Trapped Master Register	0044_H	U,SV	BE	Debug Reset	24
EBCU_DBADRT	BCU Debug Trapped Address Register	0048_H	U,SV	BE	Debug Reset	See Family Spec
EBCU_DBBOST	BCU Debug Trapped Bus Operation Signals Register	$004C_H$	U,SV	BE	Debug Reset	See Family Spec
EBCU_DBDAT	BCU Debug Data Status Register	0050_H	U,SV	BE	Debug Reset	See Family Spec
EBCU_ALSTATx (x=0-3)	BCU EDC Alarm Status Register x	0060_H+x *4	U,SV	SV,P	Application Reset	25
EBCU_ALCLRx (x=0-3)	BCU EDC Alarm Clear Register x	0070_H+x *4	U,SV	SV,P	Application Reset	See Family Spec
EBCU_ALCTRL	BCU EDC Alarm Control Register	0080_H	U,SV	SV,P	Application Reset	See Family Spec
EBCU_FEGEN	FPI Error Generation Control Register	0084_H	U,SV	SV,SE	Application Reset	See Family Spec

Table 14 Register Overview - EBCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
EBCU_ACCEN1	Access Enable Register 1	$00F8_H$	U,SV	SV,SE	Application Reset	See Family Spec
EBCU_ACCEN0	Access Enable Register 0	$00FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

4.7.3.1 EBCU Control Registers Descriptions

Note: For all PRIOH / PRIOL bit fields, a lower number has a higher priority in the arbitration round than a higher one.

Arbiter Priority Register High

EBCU_PRIOH
Arbiter Priority Register High (0014_H) Application Reset Value: FEDC BA98$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				RESERVED				RESERVED				RESERVED			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED				RESERVED				RESERVED				RESERVED			
rw				rw				rw				rw			

Field	Bits	Type	Description
RESERVED (i=8-15)	4*i-29:4*i-32	rw	**Reserved** Read as reset value or last written value; should be written with 0.

Arbiter Priority Register Low

EBCU_PRIOL
Arbiter Priority Register Low (0018_H) Application Reset Value: 7658 8210$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESERVED				SFI_S2F				RESERVED				RESERVED			
rw				rw				rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IOC32E				RESERVED				RESERVED				IOC32P			
rw				rw				rw				rw			

Field	Bits	Type	Description
IOC32P	3:0	rw	**IOC32P Priority (Index 0)** This bit field defines the priority on the BBB for IOC32P access to the BBB.
RESERVED	7:4, 11:8, 19:16, 23:20, 31:28	rw	**Reserved** Read as reset value or last written value; should be written with 0.
IOC32E	15:12	rw	**IOC32E Priority (Index 3)** This bit field defines the priority on the BBB for IOC32E access to the BBB.
SFI_S2F	27:24	rw	**SFI Bridge SRI2FPI Priority (Index 6)** This bit field defines the priority on the BPB for SFI_S2F access to the BBB.

4.7.3.2 EBCU OCDS Registers Descriptions

BCU Debug Control Register

EBCU_DBCNTL
BCU Debug Control Register **(0030_H)** **Debug Reset Value: $0000\ 7003_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ONBOS3	**ONBOS2**	**ONBOS1**	**ONBOS0**	**0**		**ONA2**		**0**		**ONA1**		**0**			**ONG**
rw	rw	rw	rw	r		rw		r		rw		r			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**CONCOM2**	**CONCOM1**	**CONCOM0**	**0**				**0**	**0**		**RA**	**0**		**OA**	**EO**
r	rw	rw	rw	r				r	r		w	r		rh	r

Field	Bits	Type	Description
EO	0	r	**Status of BCU Debug Support Enable** This bit is controlled by the Cerberus and enables the BCU debug support. 0_B BCU debug support is disabled 1_B BCU debug support is enabled (default after reset)
OA	1	rh	**Status of BCU Breakpoint Logic** The OA bit is set by writing a 1 to bit RA. When OA is set, registers DBGNTT, DBADRT and DBDAT are reset. Also DBBOST is reset with the exception of the bit field FPIRST. 0_B The BCU breakpoint logic is disarmed. Any further breakpoint activation is discarded 1_B The BCU breakpoint logic is armed

Field	Bits	Type	Description
RA	4	w	**Rearm BCU Breakpoint Logic** Writing a 1 to this bit rearms BCU breakpoint logic and sets bit OA = 1. RA is always reads as 0.
CONCOM0	12	rw	**Grant and Address Trigger Relation** 0_B The grant phase trigger condition and the address trigger condition (see CONCOM1) are combined with a logical OR for further control 1_B The grant phase trigger condition and the address trigger condition (see CONCOM1) are combined with a logical AND for further control.
CONCOM1	13	rw	**Address 1 and Address 2 Trigger Relation** 0_B Address 1 trigger condition and address 2 trigger condition are combined with a logical OR to the address trigger condition for further control 1_B Address 1 trigger condition and address 2 trigger condition are combined with a logical AND to the address trigger condition for further control
CONCOM2	14	rw	**Address and Signal Trigger Relation** 0_B Address trigger condition (see CONCOM1) and signal status trigger conditions are combined with a logical OR for further control 1_B Address phase trigger condition (see CONCOM1) and the signal status trigger conditions are combined with a logical AND for further control
ONG	16	rw	**Grant Trigger Enable** 0_B No grant debug event trigger is generated 1_B The grant debug event trigger is enabled and generated according the settings of register DBGRNT
ONA1	21:20	rw	**Address 1 Trigger Control** 00_B No address 1 trigger is generated 01_B An address 1 trigger event is generated if the FPI Bus address is equal to DBADR1 10_B An address 1 trigger event is generated if FPI Bus address is greater or equal to DBADR1 11_B same as 00_B
ONA2	25:24	rw	**Address 2 Trigger Control** 00_B No address 2 trigger is generated. 01_B An address 2 trigger event is generated if the FPI Bus address is equal to DBADR2 10_B An address 2 trigger event is generated if FPI Bus address is less or equal to DBADR2 11_B same as 00_B

Field	Bits	Type	Description
ONBOS0	28	rw	**Op code Signal Status Trigger Condition** 0_B A signal status trigger is generated for all FPI Bus op-codes except a “no operation” op-code 1_B A signal status trigger is generated if the FPI Bus op-code matches the op-code as defined in DBBOS.OPC
ONBOS1	29	rw	**Supervisor Mode Signal Trigger Condition** 0_B The signal status trigger generation for the FPI Bus Supervisor Mode signal is disabled. 1_B A signal status trigger is generated if the FPI Bus Supervisor Mode signal state is equal to the value of DBBOS.SVM
ONBOS2	30	rw	**Write Signal Trigger Condition** 0_B The signal status trigger generation for the FPI Bus write signal is disabled. 1_B A signal status trigger is generated if the FPI Bus write signal state is equal to the value of DBBOS.WR
ONBOS3	31	rw	**Read Signal Trigger Condition** 0_B The signal status trigger generation for the FPI Bus read signal is disabled. 1_B A signal status trigger is generated if the FPI Bus read signal state is equal to the value of DBBOS.RD
0	3:2, 6:5, 7, 11:8, 15, 19:17, 23:22, 27:26	r	**Reserved** Read as 0; should be written with 0.

EBCU Debug Grant Mask Register

EBCU_DBGRNT

EBCU Debug Grant Mask Register **(0034_H)** **Debug Reset Value: $0000\ FFFF_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**SFI_S2F**	**1**	**1**	**IOC32E**	**1**	**1**	**IOC32P**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
IOC32P	0	rw	**IOC32P Trigger Enable** 0_B FPI Bus transactions with IOC32P as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with IOC32P as bus master are disabled for grant trigger event generation
IOC32E	3	rw	**IOC32E Grant Trigger Enable** 0_B FPI Bus transactions with IOC32E as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with IOC32E as bus master are disabled for grant trigger event generation
SFI_S2F	6	rw	**SFI_S2F Grant Trigger Enable** 0_B FPI Bus transactions with SFI_S2F as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with SFI_S2F as bus master are disabled for grant trigger event generation
1	1, 2, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15	rw	**Reserved** Read as 1 after reset; reading these bits will return the value last written.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

EBCU Debug Trapped Master Register

EBCU_DBGNTT
EBCU Debug Trapped Master Register **(0044_H)** **Debug Reset Value: 0000 FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**SFI_S2F**	**1**	**1**	**IOC32E**	**1**	**1**	**IOC32P**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
IOC32P	0	rh	**IOC32P FPI Bus Master Status** This bit indicates whether the IOC32P was FPI Bus master when the break trigger event occurred. 0_B The IOC32P was the FPI bus master. 1_B The IOC32P was not the FPI Bus master.
IOC32E	3	rh	**IOC32E FPI Bus Master Status** This bit indicates whether the IOC32E was FPI Bus master when the break trigger event occurred. 0_B The IOC32E was the FPI bus master. 1_B The IOC32E was not the FPI Bus master.
SFI_S2F	6	rh	**SFI_S2F FPI Bus Master Status** This bit indicates whether the SFI_S2F with a medium priority request was FPI Bus master when the break trigger event occurred. 0_B The medium-priority SFI_S2F was the FPI bus master. 1_B The medium-priority SFI_S2F was not the FPI Bus master.
1	1, 2, 4, 5, 7, 8, 9, 10, 11, 12, 13, 14, 15	rh	**Reserved** Read as 1 after reset; reading these bits will return the value last written.
0	31:16	rh	**Reserved** Read as 1 after reset; reading these bits will return the value last written.

EBCU_ALSTATx (x=0)

BCU EDC Alarm Status Register x **(0060_H+x*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	**AL30**	**AL29**	**AL28**	**AL27**	**AL26**	**AL25**	**AL24**	**AL23**	**AL22**	**AL21**	**AL20**	**AL19**	**AL18**	**AL17**	**AL16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	**AL14**	**AL13**	**AL12**	**AL11**	**AL10**	**AL09**	**AL08**	**AL07**	**AL06**	**AL05**	**AL04**	**AL03**	**AL02**	**AL01**	**AL00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	**Alarm y** 1_B **EBCU_S**,
ALy (y=01)	y	rh	**Alarm y** 1_B **MCDS_S**,
ALy (y=02)	y	rh	**Alarm y** 1_B **AGBT_S**,
ALy (y=03-05,09-15,17,20-31)	y	rh	**Alarm y**
ALy (y=06)	y	rh	**Alarm y** 1_B **EMEM_XTMRAM_S**,
ALy (y=07)	y	rh	**Alarm y** 1_B **EMEM_CTRL_S**,
ALy (y=08)	y	rh	**Alarm y** 1_B **EMEM0_S**,
ALy (y=16)	y	rh	**Alarm y** 1_B **RIF0_S**,
ALy (y=18)	y	rh	**Alarm y** 1_B **SPU0_S**,
ALy (y=19)	y	rh	**Alarm y** 1_B **SPU_CFG0_S**,

EBCU_ALSTATx (x=1)
BCU EDC Alarm Status Register x **(0060_H+x*4)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	**AL30**	**AL29**	**AL28**	**AL27**	**AL26**	**AL25**	**AL24**	**AL23**	**AL22**	**AL21**	**AL20**	**AL19**	**AL18**	**AL17**	**AL16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	**AL14**	**AL13**	**AL12**	**AL11**	**AL10**	**AL09**	**AL08**	**AL07**	**AL06**	**AL05**	**AL04**	**AL03**	**AL02**	**AL01**	**AL00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00-31)	y	rh	**Alarm y**

EBCU_ALSTATx (x=2)
BCU EDC Alarm Status Register x **(0060_H+x*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	**AL30**	**AL29**	**AL28**	**AL27**	**AL26**	**AL25**	**AL24**	**AL23**	**AL22**	**AL21**	**AL20**	**AL19**	**AL18**	**AL17**	**AL16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	**AL14**	**AL13**	**AL12**	**AL11**	**AL10**	**AL09**	**AL08**	**AL07**	**AL06**	**AL05**	**AL04**	**AL03**	**AL02**	**AL01**	**AL00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00-30)	y	rh	**Alarm y**
ALy (y=31)	y	rh	**Alarm y** 1_B **EBCU_M**, an EDC error was detected in an active phase of the EBCU Master Interface.

EBCU_ALSTATx (x=3)
BCU EDC Alarm Status Register x **(0060_H+x*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL31	**AL30**	**AL29**	**AL28**	**AL27**	**AL26**	**AL25**	**AL24**	**AL23**	**AL22**	**AL21**	**AL20**	**AL19**	**AL18**	**AL17**	**AL16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AL15	**AL14**	**AL13**	**AL12**	**AL11**	**AL10**	**AL09**	**AL08**	**AL07**	**AL06**	**AL05**	**AL04**	**AL03**	**AL02**	**AL01**	**AL00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ALy (y=00)	y	rh	**Alarm y** 1_B **A_EN**, multiple output enables active: A_EN_N (Master)
ALy (y=01)	y	rh	**Alarm y** 1_B **ABORT_EN**, multiple output enables active: ABORT_EN_N (Master)
ALy (y=02)	y	rh	**Alarm y** 1_B **ACK_EN**, multiple output enables active: ACK_EN_N (Default Master and Slave)
ALy (y=03)	y	rh	**Alarm y** 1_B **D_EN**, multiple output enables active: D_EN_N (Master and Slave)
ALy (y=04-15,17-18,20-21,23-31)	y	rh	**Alarm y**
ALy (y=16)	y	rh	**Alarm y** 1_B **IOC32P_M**,

Field	Bits	Type	Description
ALy (y=19)	y	rh	**Alarm y** 1_B **IOC32E_M**,
ALy (y=22)	y	rh	**Alarm y** 1_B **SFI_S2F_M**,

4.7.4 Connectivity

4.7.4.1 SBCU Connectivity

Table 15 Connections of SBCU

Interface Signals	connects		Description
SBCU:INT	to	INT:sbcu_INT	Bus Control Unit SPB Service Request

4.7.4.2 EBCU Connectivity

Table 16 Connections of EBCU

Interface Signals	connects		Description
EBCU:INT	to	INT:bbbcu_INT	Bus Control Unit BBB Service Request

4.7.5 Revision History

Table 17 Revision History

Reference	Change to Previous Version	Comment
V1.2.7		
	No functional change.	
V1.2.8		
–	No functional changes.	–
V1.2.9		
Page 20, **Page 23**, **Page 24**	Wrongly mentioned CIF removed	

5 CPU Subsystem (CPU)

This chapter describes the CPU subsystem module of the TC33xEXT.

5.1 TC33xEXT Specific Configuration

No product specific configuration for CPU

5.2 TC33xEXT Specific Register Set

Register Address Space Table

Table 18 Register Address Space - CPU

Module	Base Address	End Address	Note
(CPU0)	70000000_H	$7002FFFF_H$	Data ScratchPad RAM interface
	70030000_H	$70033FFF_H$	Data Cache RAM interface
	$700C0000_H$	$700C17FF_H$	Data Cache Tag RAM interface
	70100000_H	$70107FFF_H$	Program ScratchPad RAM interface
	70108000_H	$7010FFFF_H$	Program Cache RAM interface
	$701C0000_H$	$701C2FFF_H$	Program Cache TAG RAM interface
	90000000_H	$90001FFF_H$	DLMU RAM interface (cached)
	$B0000000_H$	$B0001FFF_H$	DLMU RAM interface (non-cached)
CPU0	$F8800000_H$	$F881FFFF_H$	SRI slave interface for SFR+CSFR
(CPU1)	60000000_H	$60017FFF_H$	Data ScratchPad RAM interface
	60018000_H	$6001BFFF_H$	Data Cache RAM interface
	$600C0000_H$	$600C17FF_H$	Data Cache Tag RAM interface
	60100000_H	$6010FFFF_H$	Program ScratchPad RAM interface
	60110000_H	$60117FFF_H$	Program Cache RAM interface
	$601C0000_H$	$601C2FFF_H$	Program Cache TAG RAM interface
	90010000_H	$9001FFFF_H$	DLMU RAM interface (cached)
	$B0010000_H$	$B001FFFF_H$	DLMU RAM interface (non-cached)
CPU1	$F8820000_H$	$F883FFFF_H$	SRI slave interface for SFR+CSFR

Register Overview Table

Register Overview Tables of CPU

Table 19 Register Overview - CPU0 (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
CPU0_FLASHCON0	CPUx Flash Configuration Register 0	01100_H	17
CPU0_FLASHCON1	CPUx Flash Configuration Register 1	01104_H	See Family Spec
CPU0_FLASHCON2	CPUx Flash Configuration Register 2	01108_H	See Family Spec
CPU0_FLASHCON3	CPUx Flash Configuration Register 3	$0110C_H$	See Family Spec
CPU0_FLASHCON4	CPUx Flash Configuration Register 4	01110_H	See Family Spec
CPU0_KRST0	CPUx Reset Register 0	$0D000_H$	See Family Spec
CPU0_KRST1	CPUx Reset Register 1	$0D004_H$	See Family Spec
CPU0_KRSTCLR	CPUx Reset Clear Register	$0D008_H$	See Family Spec
CPU0_SPR_SPROT_RGNLAi (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	$0E000_H$+i*10_H	See Family Spec
CPU0_SPR_SPROT_RGNUAi (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	$0E004_H$+i*10_H	See Family Spec
CPU0_SPR_SPROT_RGNACCENAi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	$0E008_H$+i*10_H	See Family Spec
CPU0_SPR_SPROT_RGNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	$0E00C_H$+i*10_H	See Family Spec
CPU0_SPR_SPROT_RGNACCENAi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	$0E088_H$+i*10_H	See Family Spec
CPU0_SPR_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	$0E08C_H$+i*10_H	See Family Spec

Table 19 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_SFR_SPROT_ACCENA_W	CPUx Safety Protection Register Access Enable Register A	$0E100_H$	See Family Spec
CPU0_SFR_SPROT_ACCENB_W	CPUx Safety Protection Region Access Enable Register B	$0E104_H$	See Family Spec
CPU0_LPB_SPROT_ACCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	$0E110_H$	See Family Spec
CPU0_LPB_SPROT_ACCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	$0E114_H$	See Family Spec
CPU0_DLMU_SPROT_RGNLAi (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	$0E200_H+i*10_H$	See Family Spec
CPU0_DLMU_SPROT_RGNUAi (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	$0E204_H+i*10_H$	See Family Spec
CPU0_DLMU_SPROT_RGNACCENAi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	$0E208_H+i*10_H$	See Family Spec
CPU0_DLMU_SPROT_RGNACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	$0E20C_H+i*10_H$	See Family Spec
CPU0_DLMU_SPROT_RGNACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	$0E288_H+i*10_H$	See Family Spec
CPU0_DLMU_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	$0E28C_H+i*10_H$	See Family Spec
CPU0_OSEL	CPUx Overlay Range Select Register	$0FB00_H$	See Family Spec
CPU0_RABRi (i=0-31)	CPUx Redirected Address Base Register i	$0FB10_H+i*12$	See Family Spec
CPU0_OTARi (i=0-31)	CPUx Overlay Target Address Register i	$0FB14_H+i*12$	See Family Spec
CPU0_OMASKi (i=0-31)	CPUx Overlay Mask Register i	$0FB18_H+i*12$	See Family Spec

Table 19 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_SEGEN	CPUx SRI Error Generation Register	11030_H	See Family Spec
CPU0_TASK_ASI	CPUx Task Address Space Identifier Register	18004_H	See Family Spec
CPU0_PMA0	CPUx Data Access CacheabilityRegister	18100_H	See Family Spec
CPU0_PMA1	CPUx Code Access CacheabilityRegister	18104_H	See Family Spec
CPU0_PMA2	CPUx Peripheral Space Identifier register	18108_H	See Family Spec
CPU0_DCON2	CPUx Data Control Register 2	19000_H	See Family Spec
CPU0_SMACON	CPUx SIST Mode Access Control Register	$1900C_H$	See Family Spec
CPU0_DSTR	CPUx Data Synchronous Trap Register	19010_H	See Family Spec
CPU0_DATR	CPUx Data Asynchronous Trap Register	19018_H	See Family Spec
CPU0_DEADD	CPUx Data Error Address Register	$1901C_H$	See Family Spec
CPU0_DIEAR	CPUx Data Integrity Error Address Register	19020_H	See Family Spec
CPU0_DIETR	CPUx Data Integrity Error Trap Register	19024_H	See Family Spec
CPU0_DCON0	CPUx Data Memory Control Register	19040_H	See Family Spec
CPU0_PSTR	CPUx Program Synchronous Trap Register	19200_H	See Family Spec

Table 19 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_PCON1	CPUx Program Control 1	19204_H	See Family Spec
CPU0_PCON2	CPUx Program Control 2	19208_H	See Family Spec
CPU0_PCON0	CPUx Program Control 0	$1920C_H$	See Family Spec
CPU0_PIEAR	CPUx Program Integrity Error Address Register	19210_H	See Family Spec
CPU0_PIETR	CPUx Program Integrity Error Trap Register	19214_H	See Family Spec
CPU0_COMPAT	CPUx Compatibility Control Register	19400_H	See Family Spec
CPU0_FPU_TRAP_CON	CPUx Trap Control Register	$1A000_H$	See Family Spec
CPU0_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	$1A004_H$	See Family Spec
CPU0_FPU_TRAP_OPC	CPUx Trapping Instruction Opcode Register	$1A008_H$	See Family Spec
CPU0_FPU_TRAP_SRC1	CPUx Trapping Instruction Operand Register	$1A010_H$	See Family Spec
CPU0_FPU_TRAP_SRC2	CPUx Trapping Instruction Operand Register	$1A014_H$	See Family Spec
CPU0_FPU_TRAP_SRC3	CPUx Trapping Instruction Operand Register	$1A018_H$	See Family Spec
CPU0_DPRy_L (y=0-17)	CPUx Data Protection Range y, Lower Bound Register	$1C000_H$+y*8	See Family Spec
CPU0_DPRy_U (y=0-17)	CPUx Data Protection Range y, Upper Bound Register	$1C004_H$+y*8	See Family Spec

Table 19 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_CPRy_L (y=0-9)	CPUx Code Protection Range y Lower Bound Register	$1D000_H$+y*8	See Family Spec
CPU0_CPRy_U (y=0-9)	CPUx Code Protection Range y Upper Bound Register	$1D004_H$+y*8	See Family Spec
CPU0_CPXE_y (y=0-3)	CPUx Code Protection Execute Enable Register Set y	$1E000_H$+y*4	See Family Spec
CPU0_DPRE_y (y=0-3)	CPUx Data Protection Read Enable Register Set y	$1E010_H$+y*4	See Family Spec
CPU0_DPWE_y (y=0-3)	CPUx Data Protection Write Enable Register Set y	$1E020_H$+y*4	See Family Spec
CPU0_CPXE_y (y=4-5)	CPUx Code Protection Execute Enable Register Set y	$1E040_H$+(y-4)*4	See Family Spec
CPU0_DPRE_y (y=4-5)	CPUx Data Protection Read Enable Register Set y	$1E050_H$+(y-4)*4	See Family Spec
CPU0_DPWE_y (y=4-5)	CPUx Data Protection Write Enable Register Set y	$1E060_H$+(y-4)*4	See Family Spec
CPU0_TPS_CON	CPUx Temporal Protection System Control Register	$1E400_H$	See Family Spec
CPU0_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	$1E404_H$+y*4	See Family Spec
CPU0_TPS_EXTIM_ENTRY_LVAL	CPUx Exception Entry Timer Load Value	$1E440_H$	See Family Spec
CPU0_TPS_EXTIM_ENTRY_CVAL	CPUx Exception Entry Timer Current Value	$1E444_H$	See Family Spec
CPU0_TPS_EXTIM_EXIT_LVAL	CPUx Exception Exit Timer Load Value	$1E448_H$	See Family Spec
CPU0_TPS_EXTIM_EXIT_CVAL	CPUx Exception Exit Timer Current Value	$1E44C_H$	See Family Spec

Table 19 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_TPS_EXTIM_CLASS_EN	CPUx Exception Timer Class Enable Register	$1E450_H$	See Family Spec
CPU0_TPS_EXTIM_STAT	CPUx Exception Timer Status Register	$1E454_H$	See Family Spec
CPU0_TPS_EXTIM_FCX	CPUx Exception Timer FCX Register	$1E458_H$	See Family Spec
CPU0_TRiEVT (i=0-7)	CPUx Trigger Event i	$1F000_H$+i*8	See Family Spec
CPU0_TRiADR (i=0-7)	CPUx Trigger Address i	$1F004_H$+i*8	See Family Spec
CPU0_CCTRL	CPUx Counter Control	$1FC00_H$	See Family Spec
CPU0_CCNT	CPUx CPU Clock Cycle Count	$1FC04_H$	See Family Spec
CPU0_ICNT	CPUx Instruction Count	$1FC08_H$	See Family Spec
CPU0_M1CNT	CPUx Multi-Count Register 1	$1FC0C_H$	See Family Spec
CPU0_M2CNT	CPUx Multi-Count Register 2	$1FC10_H$	See Family Spec
CPU0_M3CNT	CPUx Multi-Count Register 3	$1FC14_H$	See Family Spec
CPU0_DBGSR	CPUx Debug Status Register	$1FD00_H$	See Family Spec
CPU0_EXEVT	CPUx External Event Register	$1FD08_H$	See Family Spec
CPU0_CREVT	CPUx Core Register Access Event	$1FD0C_H$	See Family Spec

Table 19 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_SWEVT	CPUx Software Debug Event	$1FD10_H$	See Family Spec
CPU0_TRIG_ACC	CPUx TriggerAddressx	$1FD30_H$	See Family Spec
CPU0_DMS	CPUx Debug Monitor Start Address	$1FD40_H$	See Family Spec
CPU0_DCX	CPUx Debug Context Save Area Pointer	$1FD44_H$	See Family Spec
CPU0_DBGTCR	CPUx Debug Trap Control Register	$1FD48_H$	See Family Spec
CPU0_PCXI	CPUx Previous Context Information Register	$1FE00_H$	See Family Spec
CPU0_PSW	CPUx Program Status Word	$1FE04_H$	See Family Spec
CPU0_PC	CPUx Program Counter	$1FE08_H$	See Family Spec
CPU0_SYSCON	CPUx System Configuration Register	$1FE14_H$	See Family Spec
CPU0_CPU_ID	CPUx Identification Register TC1.6.2P	$1FE18_H$	See Family Spec
CPU0_CORE_ID	CPUx Core Identification Register	$1FE1C_H$	See Family Spec
CPU0_BIV	CPUx Base Interrupt Vector Table Pointer	$1FE20_H$	See Family Spec
CPU0_BTV	CPUx Base Trap Vector Table Pointer	$1FE24_H$	See Family Spec
CPU0_ISP	CPUx Interrupt Stack Pointer	$1FE28_H$	See Family Spec

Table 19 Register Overview - CPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU0_ICR	CPUx Interrupt Control Register	$1FE2C_H$	See Family Spec
CPU0_FCX	CPUx Free CSA List Head Pointer	$1FE38_H$	See Family Spec
CPU0_LCX	CPUx Free CSA List Limit Pointer	$1FE3C_H$	See Family Spec
CPU0_CUS_ID	CPUx Customer ID register	$1FE50_H$	See Family Spec
CPU0_Dy (y=0-15)	CPUx Data General Purpose Register y	$1FF00_H$+y*4	See Family Spec
CPU0_Ay (y=0-15)	CPUx Address General Purpose Register y	$1FF80_H$+y*4	See Family Spec

Table 20 Register Overview - CPU1 (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
CPU1_FLASHCON0	CPUx Flash Configuration Register 0	01100_H	See Family Spec
CPU1_FLASHCON1	CPUx Flash Configuration Register 1	01104_H	See Family Spec
CPU1_FLASHCON2	CPUx Flash Configuration Register 2	01108_H	See Family Spec
CPU1_FLASHCON3	CPUx Flash Configuration Register 3	$0110C_H$	See Family Spec
CPU1_FLASHCON4	CPUx Flash Configuration Register 4	01110_H	See Family Spec
CPU1_KRST0	CPUx Reset Register 0	$0D000_H$	See Family Spec

Table 20 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_KRST1	CPUx Reset Register 1	$0D004_H$	See Family Spec
CPU1_KRSTCLR	CPUx Reset Clear Register	$0D008_H$	See Family Spec
CPU1_SPR_SPROT_RGNLAi (i=0-7)	CPUx Safety Protection SPR Region Lower Address Register i	$0E000_H$+i*10_H	See Family Spec
CPU1_SPR_SPROT_RGNUAi (i=0-7)	CPUx Safety Protection SPR Region Upper Address Register i	$0E004_H$+i*10_H	See Family Spec
CPU1_SPR_SPROT_RGNACCENAi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Ai	$0E008_H$+i*10_H	See Family Spec
CPU1_SPR_SPROT_RGNACCENBi_W (i=0-7)	CPUx Safety Protection SPR Region Write Access Enable Register Bi	$0E00C_H$+i*10_H	See Family Spec
CPU1_SPR_SPROT_RGNACCENAi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Ai	$0E088_H$+i*10_H	See Family Spec
CPU1_SPR_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection SPR Region Read Access Enable Register Bi	$0E08C_H$+i*10_H	See Family Spec
CPU1_SFR_SPROT_ACCENA_W	CPUx Safety Protection Register Access Enable Register A	$0E100_H$	See Family Spec
CPU1_SFR_SPROT_ACCENB_W	CPUx Safety Protection Region Access Enable Register B	$0E104_H$	See Family Spec
CPU1_LPB_SPROT_ACCENA_R	CPUx Safety Protection Region LPB Read Access Enable Register A	$0E110_H$	See Family Spec
CPU1_LPB_SPROT_ACCENB_R	CPUx Safety Protection Region LPB Read Access Enable Register B	$0E114_H$	See Family Spec
CPU1_DLMU_SPROT_RGNLAi (i=0-7)	CPUx Safety Protection DLMU Region Lower Address Register i	$0E200_H$+i*10_H	See Family Spec
CPU1_DLMU_SPROT_RGNUAi (i=0-7)	CPUx Safety protection DLMU Region Upper Address Register i	$0E204_H$+i*10_H	See Family Spec

Table 20 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_DLMU_SPROT_RGNACCENAi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Ai	$0E208_H$+i*10_H	See Family Spec
CPU1_DLMU_SPROT_RGNACCENBi_W (i=0-7)	CPUx Safety Protection Region DLMU Write Access Enable Register Bi	$0E20C_H$+i*10_H	See Family Spec
CPU1_DLMU_SPROT_RGNACCENAi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Ai	$0E288_H$+i*10_H	See Family Spec
CPU1_DLMU_SPROT_RGNACCENBi_R (i=0-7)	CPUx Safety Protection Region DLMU Read Access Enable Register Bi	$0E28C_H$+i*10_H	See Family Spec
CPU1_OSEL	CPUx Overlay Range Select Register	$0FB00_H$	See Family Spec
CPU1_RABRi (i=0-31)	CPUx Redirected Address Base Register i	$0FB10_H$+i*12	See Family Spec
CPU1_OTARi (i=0-31)	CPUx Overlay Target Address Register i	$0FB14_H$+i*12	See Family Spec
CPU1_OMASKi (i=0-31)	CPUx Overlay Mask Register i	$0FB18_H$+i*12	See Family Spec
CPU1_SEGEN	CPUx SRI Error Generation Register	11030_H	See Family Spec
CPU1_TASK_ASI	CPUx Task Address Space Identifier Register	18004_H	See Family Spec
CPU1_PMA0	CPUx Data Access CacheabilityRegister	18100_H	See Family Spec
CPU1_PMA1	CPUx Code Access CacheabilityRegister	18104_H	See Family Spec
CPU1_PMA2	CPUx Peripheral Space Identifier register	18108_H	See Family Spec
CPU1_DCON2	CPUx Data Control Register 2	19000_H	See Family Spec

Table 20 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_SMACON	CPUx SIST Mode Access Control Register	$1900C_H$	See Family Spec
CPU1_DSTR	CPUx Data Synchronous Trap Register	19010_H	See Family Spec
CPU1_DATR	CPUx Data Asynchronous Trap Register	19018_H	See Family Spec
CPU1_DEADD	CPUx Data Error Address Register	$1901C_H$	See Family Spec
CPU1_DIEAR	CPUx Data Integrity Error Address Register	19020_H	See Family Spec
CPU1_DIETR	CPUx Data Integrity Error Trap Register	19024_H	See Family Spec
CPU1_DCON0	CPUx Data Memory Control Register	19040_H	See Family Spec
CPU1_PSTR	CPUx Program Synchronous Trap Register	19200_H	See Family Spec
CPU1_PCON1	CPUx Program Control 1	19204_H	See Family Spec
CPU1_PCON2	CPUx Program Control 2	19208_H	See Family Spec
CPU1_PCON0	CPUx Program Control 0	$1920C_H$	See Family Spec
CPU1_PIEAR	CPUx Program Integrity Error Address Register	19210_H	See Family Spec
CPU1_PIETR	CPUx Program Integrity Error Trap Register	19214_H	See Family Spec
CPU1_COMPAT	CPUx Compatibility Control Register	19400_H	See Family Spec

Table 20 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_FPU_TRAP_CON	CPUx Trap Control Register	$1A000_H$	See Family Spec
CPU1_FPU_TRAP_PC	CPUx Trapping Instruction Program Counter Register	$1A004_H$	See Family Spec
CPU1_FPU_TRAP_OPC	CPUx Trapping Instruction Opcode Register	$1A008_H$	See Family Spec
CPU1_FPU_TRAP_SRC1	CPUx Trapping Instruction Operand Register	$1A010_H$	See Family Spec
CPU1_FPU_TRAP_SRC2	CPUx Trapping Instruction Operand Register	$1A014_H$	See Family Spec
CPU1_FPU_TRAP_SRC3	CPUx Trapping Instruction Operand Register	$1A018_H$	See Family Spec
CPU1_DPRy_L (y=0-17)	CPUx Data Protection Range y, Lower Bound Register	$1C000_H$+y*8	See Family Spec
CPU1_DPRy_U (y=0-17)	CPUx Data Protection Range y, Upper Bound Register	$1C004_H$+y*8	See Family Spec
CPU1_CPRy_L (y=0-9)	CPUx Code Protection Range y Lower Bound Register	$1D000_H$+y*8	See Family Spec
CPU1_CPRy_U (y=0-9)	CPUx Code Protection Range y Upper Bound Register	$1D004_H$+y*8	See Family Spec
CPU1_CPXE_y (y=0-3)	CPUx Code Protection Execute Enable Register Set y	$1E000_H$+y*4	See Family Spec
CPU1_DPRE_y (y=0-3)	CPUx Data Protection Read Enable Register Set y	$1E010_H$+y*4	See Family Spec
CPU1_DPWE_y (y=0-3)	CPUx Data Protection Write Enable Register Set y	$1E020_H$+y*4	See Family Spec
CPU1_CPXE_y (y=4-5)	CPUx Code Protection Execute Enable Register Set y	$1E040_H$+(y-4)*4	See Family Spec

Table 20 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_DPRE_y (y=4-5)	CPUx Data Protection Read Enable Register Set y	$1E050_H$+(y-4)*4	See Family Spec
CPU1_DPWE_y (y=4-5)	CPUx Data Protection Write Enable Register Set y	$1E060_H$+(y-4)*4	See Family Spec
CPU1_TPS_CON	CPUx Temporal Protection System Control Register	$1E400_H$	See Family Spec
CPU1_TPS_TIMERy (y=0-2)	CPUx Temporal Protection System Timer Register y	$1E404_H$+y*4	See Family Spec
CPU1_TPS_EXTIM_ENTRY_LVAL	CPUx Exception Entry Timer Load Value	$1E440_H$	See Family Spec
CPU1_TPS_EXTIM_ENTRY_CVAL	CPUx Exception Entry Timer Current Value	$1E444_H$	See Family Spec
CPU1_TPS_EXTIM_EXIT_LVAL	CPUx Exception Exit Timer Load Value	$1E448_H$	See Family Spec
CPU1_TPS_EXTIM_EXIT_CVAL	CPUx Exception Exit Timer Current Value	$1E44C_H$	See Family Spec
CPU1_TPS_EXTIM_CLASS_EN	CPUx Exception Timer Class Enable Register	$1E450_H$	See Family Spec
CPU1_TPS_EXTIM_STAT	CPUx Exception Timer Status Register	$1E454_H$	See Family Spec
CPU1_TPS_EXTIM_FCX	CPUx Exception Timer FCX Register	$1E458_H$	See Family Spec
CPU1_TRiEVT (i=0-7)	CPUx Trigger Event i	$1F000_H$+i*8	See Family Spec
CPU1_TRiADR (i=0-7)	CPUx Trigger Address i	$1F004_H$+i*8	See Family Spec
CPU1_CCTRL	CPUx Counter Control	$1FC00_H$	See Family Spec

Table 20 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_CCNT	CPUx CPU Clock Cycle Count	$1FC04_H$	See Family Spec
CPU1_ICNT	CPUx Instruction Count	$1FC08_H$	See Family Spec
CPU1_M1CNT	CPUx Multi-Count Register 1	$1FC0C_H$	See Family Spec
CPU1_M2CNT	CPUx Multi-Count Register 2	$1FC10_H$	See Family Spec
CPU1_M3CNT	CPUx Multi-Count Register 3	$1FC14_H$	See Family Spec
CPU1_DBGSR	CPUx Debug Status Register	$1FD00_H$	See Family Spec
CPU1_EXEVT	CPUx External Event Register	$1FD08_H$	See Family Spec
CPU1_CREVT	CPUx Core Register Access Event	$1FD0C_H$	See Family Spec
CPU1_SWEVT	CPUx Software Debug Event	$1FD10_H$	See Family Spec
CPU1_TRIG_ACC	CPUx TriggerAddressx	$1FD30_H$	See Family Spec
CPU1_DMS	CPUx Debug Monitor Start Address	$1FD40_H$	See Family Spec
CPU1_DCX	CPUx Debug Context Save Area Pointer	$1FD44_H$	See Family Spec
CPU1_DBGTCR	CPUx Debug Trap Control Register	$1FD48_H$	See Family Spec
CPU1_PCXI	CPUx Previous Context Information Register	$1FE00_H$	See Family Spec

Table 20 Register Overview - CPU1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CPU1_PSW	CPUx Program Status Word	$1FE04_H$	See Family Spec
CPU1_PC	CPUx Program Counter	$1FE08_H$	See Family Spec
CPU1_SYSCON	CPUx System Configuration Register	$1FE14_H$	See Family Spec
CPU1_CPU_ID	CPUx Identification Register TC1.6.2P	$1FE18_H$	See Family Spec
CPU1_CORE_ID	CPUx Core Identification Register	$1FE1C_H$	See Family Spec
CPU1_BIV	CPUx Base Interrupt Vector Table Pointer	$1FE20_H$	See Family Spec
CPU1_BTV	CPUx Base Trap Vector Table Pointer	$1FE24_H$	See Family Spec
CPU1_ISP	CPUx Interrupt Stack Pointer	$1FE28_H$	See Family Spec
CPU1_ICR	CPUx Interrupt Control Register	$1FE2C_H$	See Family Spec
CPU1_FCX	CPUx Free CSA List Head Pointer	$1FE38_H$	See Family Spec
CPU1_LCX	CPUx Free CSA List Limit Pointer	$1FE3C_H$	See Family Spec
CPU1_CUS_ID	CPUx Customer ID register	$1FE50_H$	See Family Spec
CPU1_Dy (y=0-15)	CPUx Data General Purpose Register y	$1FF00_H$+y*4	See Family Spec
CPU1_Ay (y=0-15)	CPUx Address General Purpose Register y	$1FF80_H$+y*4	See Family Spec

5.3 TC33xEXT Specific Registers

5.3.1 SRI slave interface for SFR+CSFR

CPUx Flash Configuration Register 0

Software may program a Flash Prefetch Buffer with a master tag identifier stored in Flash Configuration Register 0.

If a CPU instance does not have a local PFlash bank then the FLASHCON0 register associated with that instance will have no functionality.

CPU0_FLASHCON0

CPUx Flash Configuration Register 0 **(01100_H)** **Reset Value: Table 21**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES		TAG4						RES		TAG3					
r		rw						r		rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		TAG2						RES		TAG1					
r		rw						r		rw					

Field	Bits	Type	Description
TAG1	5:0	rw	**Flash Prefetch Buffer 1 Configuration** FPB is assigned to on chip bus master with master tag id equal to TAG1.
RES	7:6, 15:14, 23:22, 31:30	r	**Reserved** Always read as 0; should be written with 0.
TAG2	13:8	rw	**Flash Prefetch Buffer 2 Configuration** FPB is assigned to on chip bus master with master tag id equal to TAG2.
TAG3	21:16	rw	**Flash Prefetch Buffer 3 Configuration** FPB is assigned to on chip bus master with master tag id equal to TAG3.
TAG4	29:24	rw	**Flash Prefetch Buffer 4 Configuration** FPB is assigned to on chip bus master with master tag id equal to TAG4.

Table 21 Reset Values of CPU0_FLASHCON0

Reset Type	Reset Value	Note
Application Reset	3F3F 3F3F$_H$	
CFS Value	2121 2020$_H$	

5.4 Connectivity

No connections in TC33xEXT

5.5 Revision History

Table 22 Revision History

Reference	Change to Previous Version	Comment
V1.1.16		
	No change	
V1.1.17		
	No change	
V1.1.18		
	No change	
V1.1.19		
	No change	
V1.1.20		
Page 2, 9	Change index variable from 'x' to intended 'i' for registers SPR_SPROT_RGNACCENAi_R and SPR_SPROT_RGNACCENBi_R to remove confusion with CPU instance variable.	
Page 2, 9	Change index variable from 'x' to intended 'i' for registers all DLMU_SPROT registers to remove confusion with CPU instance variable.	
V1.1.21		
	No change	

6 Non Volatile Memory (NVM) Subsystem

6.1 Overview

The Non Volatile Memory (NVM) Subsystem comprises of the Data Memory Unit (DMU), Program Flash Interface (PFI), and Non Volatile Memory module (comprising of the Flash Standard Interface (FSI), Program and Data Flash memories and Program Flash Read Write buffer (PFRWB)).

- Data Memory Unit (DMU): Controls command sequences executed on all program and data flash memories.
- Flash Standard Interface (FSI): Executes erase, program and verify operations on all flash memories.
- Program Flash (PFLASH): Divided into one or more banks each connected to a CPU. It is used by the application to store program code and data constants. Compute performance is optimized by using a point-to-point interface to minimize latency and maximize bandwidth. Each PFLASH is connected to a PFlash Read Write Buffer (PFRWB) that performs the ECC correction and detection and provides the read data to the system.
- Program Flash Interface (PFI): Each PFLASH bank has a unique point-to-point fast connection to a CPU provided by a PFI. The PFI interfaces between the CPU and the PFRWB and contains the Prefetch Buffers for storing speculative data.
- Data Flash (DFLASH): The Data Flash Module is used to emulate EEPROM and store data and divided into two banks. DFLASH read accesses are relatively slow compared to PFLASH accesses. The DFlash Read Write Buffer (DFRWB) in the FSI interfaces to the DFLASH to provide the read data. Data Flash Module also contains regions to store configuration data - User Configuration Blocks (UCBs), and Configuration Sector (CFS) which is not accessible by user.
- Boot ROM (BROM): Connected to the system via the DMU SRI port.
  - Tuning protection (commonly called the “Secure Watchdog”) to protect user software and data from maltuning data.

Attention: ***The ‘Non Volatile Memory Subsystem’ chapter is the AURIX PMU chapter re-structured for closer alignment to AURIXTC3XX product architecture. It comprises of the DMU, PFI, NVM and UCB Chapters. Please note that the application accessible registers located in the FSI, and the PFLASH read status and control registers are described in the NVM chapter.***

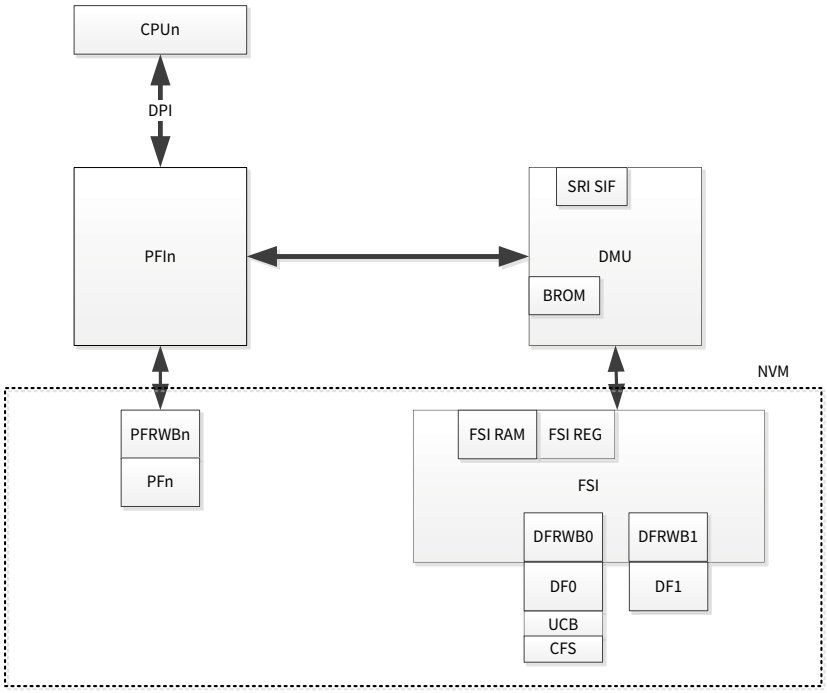


Figure 4 Non Volatile Memory (NVM) Subsystem

The purpose of the PFLASH NVM is:

- One or more PFLASH banks stores program code and data constants.
- Implementation of Erase Counters.

The purpose of the DFLASH NVM is:

- Emulation of Electrically Erasable Programmable Read Only Memory (EEPROM):
  - CPU-EEPROM used by the user application.
  - HSM-EEPROM used by the security application.
- Multiple User Configuration Blocks (UCB) used for:
  - Password based read protection combined with write protection.
  - Read-only UCB configured by IFX with unique chip identifier and trimming data.
- Configuration Sector (CFS) stores system set-up data not accessible by the user.

Data stored in the NVM is protected by ECC checksum.

- An ECC decoder at the output of the NVM corrects and detects faults in the NVM array.
- The NVM is fault tolerant and supports system operation in the presence of a number of NVM bit errors.
- For Program Flash the calculation of the ECC checksum is extended across the address to provide read protection against addressing faults.

If the Flash is not operating in the application then the NVM may be programmed and erased by command sequences executed by the FSI micro controller. All read accesses to Flash are memory mapped reads. Margin read levels may be used to check how completely a cell is programmed or erased.

The Non Volatile Memory interface micro architecture includes a security layer and a safety layer.

Security Layer (provided by DMU and PFI)

- Read protection is enabled/disabled with a Flash Module (Bank) granularity.

- Write protection is enabled/disabled with a Flash Module sector based granularity.

Safety Layer

- Master specific read access protection to each Flash Module (Bank).
- Master specific read and write access control to individual Special Function Registers (SFRs).
- Integrity of data stored in the NVM is ensured by an ECC checksum
- Integrity of PFlash read path is ensured by monitoring of read parameters in the FSI (MISR, redundant Flip Flops etc.), PFI partial lockstep mechanism, protection of PFlash wait cycles with ECC checksum, protection of data from PFI to CPU by ECC checksum and an additional safety mechanism to ensure that the local PFlash is not being programmed/erased when not expected by PFI.

6.2 Revision History

Table 23 Revision History

Reference	Change to Previous Version	Comment
V2.0.3		
	Created to form a concise introduction chapter for the appendices	
V2.0.4		
	No Changes.	
V2.0.5		
	No Changes.	
V2.0.6		
	No Changes.	
V2.0.7		
	No Changes.	

6.3 Data Memory Unit (DMU)

This chapter supplements the family documentation with the device specific information for TC33xEXT.

6.3.1 TC33xEXT Specific Register Set

Register Address Space Table

Table 24 Register Address Space - PMU

Module	Base Address	End Address	Note
PMU	$F8038000_H$	$F803FFFF_H$	sri slave interface

Table 25 Register Address Space - DMU

Module	Base Address	End Address	Note
(DMU)	$8FFF0000_H$	$8FFFFFFF_H$	Boot ROM (BROM)
	$AF000000_H$	$AF01FFFF_H$	Data Flash 0 EEPROM (DF0) and Host Command Sequence Interpreter
	$AFC00000_H$	$AFC1FFFF_H$	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter
	$AFFF0000_H$	$AFFFFFFF_H$	Boot ROM (BROM)
DMU	$F8040000_H$	$F807FFFF_H$	SRI slave interface - Register Address Space
(DMU)	$FFC00000_H$	$FFC1FFFF_H$	Data Flash 1 EEPROM (DF1) and HSM Command Sequence Interpreter

Register Overview Table

Table 26 Register Overview - PMU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMU_ID	Module Identification Register	0508_H	U,SV	BE	Application Reset	See Family Spec

Table 27 Register Overview - DMU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HF_ID	Module Identification Register	0000008 H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_STATUS	Flash Status Register	0000010 H	U,SV	BE	Application Reset	11

Table 27 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HF_CONTROL	Flash Control Register	0000014H	U,SV	P,SV,E	Application Reset	See Family Spec
DMU_HF_OPERATION	Flash Operation Register	0000018H	U,SV	BE	System Reset	See Family Spec
DMU_HF_PROTECT	Flash Protection Status Register	000001CH	U,SV	BE	Application Reset	13
DMU_HF_CONFIRM0	Flash Confirm Status Register 0	0000020H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CONFIRM1	Flash Confirm Status Register 1	0000024H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CONFIRM2	Flash Confirm Status Register 2	0000028H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_EER	Enable Error Interrupt Control Register	0000030H	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_ERRSR	Error Status Register	0000034H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_CLRE	Clear Error Register	0000038H	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_ECCR	DF0 ECC Read Register	0000040H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_ECCS	DF0 ECC Status Register	0000044H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_ECCC	DF0 ECC Control Register	0000048H	U,SV	P,SV,E	Application Reset	See Family Spec
DMU_HF_ECCW	DF0 ECC Write Register	000004CH	U,SV	P,SV,E	Application Reset	See Family Spec
DMU_HF_CCONTROL	Cranking Control Register	0000050H	U,SV	P,SV	System Reset	See Family Spec

Table 27 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HF_PSTATUS	Power Status Register	0000060H	U,SV	BE	Application Reset	See Family Spec
DMU_HF_PCONTROL	Power Control Register	0000064H	U,SV	P,SV	Application Reset	See Family Spec
DMU_HF_PWAIT	PFLASH Wait Cycle Register	0000068H	U,SV	P,SV,E	System Reset	See Family Spec
DMU_HF_DWAIT	DFLASH Wait Cycle Register	000006CH	U,SV	P,SV,E	System Reset	See Family Spec
DMU_HF_PROCONUSR	DF0 User Mode Control	0000074H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCONPF	PFLASH Protection Configuration	0000080H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCONTP	Tuning Protection Configuration	0000084H	U,SV	BE	See page 15	15
DMU_HF_PROCONDF	DFLASH Protection Configuration	0000088H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCONRAM	RAM Configuration	000008CH	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_PROCONDBG	Debug Interface Protection Configuration	0000090H	U,SV	BE	See Family Spec	See Family Spec
DMU_HF_SUSPEND	Suspend Control Register	00000F0H	U,SV	P,U,SV	Application Reset	See Family Spec
DMU_HF_MARGIN	Margin Control Register	00000F4H	U,SV	P,U,SV	Application Reset	See Family Spec
DMU_HF_ACCEN1	Access Enable Register 1	00000F8H	U,SV	SV,SE	Application Reset	See Family Spec
DMU_HF_ACCEN0	Access Enable Register 0	00000FCH	U,SV	SV,SE	Application Reset	See Family Spec

Table 27 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HP_PROCONPi0 (i=0)	PFLASH Bank i Protection Configuration 0	0010000H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONPi1 (i=0)	PFLASH Bank i Protection Configuration 1	0010004H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONPi2 (i=0)	PFLASH Bank i Protection Configuration 2	0010008H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONPi3 (i=0)	PFLASH Bank i Protection Configuration 3	001000CH	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONPi4 (i=0)	PFLASH Bank i Protection Configuration 4	0010010H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONPi5 (i=0)	PFLASH Bank i Protection Configuration 5	0010014H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONOTPi0 (i=0)	PFLASH Bank i OTP Protection Configuration 0	0010040H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONOTPi1 (i=0)	PFLASH Bank i OTP Protection Configuration 1	0010044H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONOTPi2 (i=0)	PFLASH Bank i OTP Protection Configuration 2	0010048H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONOTPi3 (i=0)	PFLASH Bank i OTP Protection Configuration 3	001004CH	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONOTPi4 (i=0)	PFLASH Bank i OTP Protection Configuration 4	0010050H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONOTPi5 (i=0)	PFLASH Bank i OTP Protection Configuration 5	0010054H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONWOPi0 (i=0)	PFLASH Bank i WOP Configuration 0	0010080H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONWOPi1 (i=0)	PFLASH Bank i WOP Configuration 1	0010084H	U,SV	BE	See Family Spec	See Family Spec

Table 27 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_HP_PROCONWOPi2 (i=0)	PFLASH Bank i WOP Configuration 2	0010088H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONWOPi3 (i=0)	PFLASH Bank i WOP Configuration 3	001008CH	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONWOPi4 (i=0)	PFLASH Bank i WOP Configuration 4	0010090H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_PROCONWOPi5 (i=0)	PFLASH Bank i WOP Configuration 5	0010094H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRIOi0 (i=0)	PFLASH Bank i Erase Counter Priority configuration 0	00100A0H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRIOi1 (i=0)	PFLASH Bank i Erase Counter Priority Configuration 1	00100A4H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRIOi2 (i=0)	PFLASH Bank i Erase Counter Priority Configuration 2	00100A8H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRIOi3 (i=0)	PFLASH Bank i Erase Counter Priority Configuration 3	00100ACH	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRIOi4 (i=0)	PFLASH Bank i Erase Counter Priority Configuration 4	00100B0H	U,SV	BE	See Family Spec	See Family Spec
DMU_HP_ECPRIOi5 (i=0)	PFLASH Bank i Erase Counter Priority Configuration 5	00100B4H	U,SV	BE	See Family Spec	See Family Spec
DMU_SF_STATUS	HSM Flash Status Register	0020010H	H	BE	Application Reset	See Family Spec
DMU_SF_CONTROL	HSM Flash Configuration Register	0020014H	H	H	Application Reset	See Family Spec
DMU_SF_OPERATION	HSM Flash Operation Register	0020018H	H	BE	System Reset	See Family Spec
DMU_SF_EER	HSM Enable Error Interrupt Control Register	0020030H	H	H	Application Reset	See Family Spec

Table 27 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_SF_ERRSR	HSM Error Status Register	0020034 H	H	BE	Application Reset	See Family Spec
DMU_SF_CLRE	HSM Clear Error Register	0020038 H	H	H	Application Reset	See Family Spec
DMU_SF_ECCR	HSM DF1 ECC Read Register	0020040 H	H	BE	Application Reset	See Family Spec
DMU_SF_ECCS	HSM DF1 ECC Status Register	0020044 H	H	BE	Application Reset	See Family Spec
DMU_SF_ECCC	HSM DF1 ECC Control Register	0020048 H	H	H	Application Reset	See Family Spec
DMU_SF_ECCW	HSM DF1 ECC Write Register	002004C H	H	H	Application Reset	See Family Spec
DMU_SF_PROCONUSR	HSM DF1 User Mode Control	0020074 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SF_SUSPEND	HSM Suspend Control Register	00200E8 H	H	H	Application Reset	See Family Spec
DMU_SF_MARGIN	HSM DF1 Margin Control Register	00200EC H	H	H	Application Reset	See Family Spec
DMU_SP_PROCONHSMCFG	HSM Protection Configuration	0030000 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSMCBS	HSM Code Boot Sector	0030004 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSMCX0	HSM Code Exclusive Protection Configuration	0030008 H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSMCX1	HSM Code Exclusive Protection Configuration	003000C H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSMCOTP0	HSM Code OTP Protection Configuration	0030010 H	U,SV	BE	See Family Spec	See Family Spec

Table 27 Register Overview - DMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMU_SP_PROCONHSMCOTP1	HSM Code OTP Protection Configuration	0030014H	U,SV	BE	See Family Spec	See Family Spec
DMU_SP_PROCONHSM	HSM Interface Protection Configuration	0030040H	U,SV	BE	See Family Spec	See Family Spec

6.3.2 TC33xEXT Specific Registers

6.3.2.1 SRI slave interface - Register Address Space

Flash Status Register

The Flash Status Register reflects the status of the Flash Banks after reset.

Note: The DxBUSY and PxBUSY flags cannot be cleared with the "Clear Status" command or with the "Reset to Read" command. These flags are controlled by HW.

Note: After every reset, the busy bits are set while the Flash module is busy with startup (until the operation mode is entered). Also the protection installation bits are always set until end of startup.

DMU_HF_STATUS
Flash Status Register (0000010$_H$) Application Reset Value: 0000 00FF$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES						RES		RES	RES	PFPAGE	DFPAGE	RES	RES	RES	RES
r						rX		r	rX	rh	rh	rX	rX	rX	rX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES								RES	RES	RES	RES	RES	P0BUSY	D1BUSY	D0BUSY
r								r	r	r	r	r	rh	rh	rh

Field	Bits	Type	Description
D0BUSY	0	rh	**Data Flash Bank 0 Busy** HW-controlled status flag. Indication of busy state of DFLASH bank 0 because of active execution of an operation; DF0 busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state the DF0 does not allow read access. 0_B DF0 ready, not busy; DF0 in operation mode. 1_B DF0 busy; DF0 not in operation mode.

Field	Bits	Type	Description
D1BUSY	1	rh	**Data Flash Bank 1 Busy** HW-controlled status flag. Indication of busy state of DFLASH bank 1 because of active execution of an operation; DF1 busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state the DF1 does not allow read access. Bit is not set for program/erase operations initiated by the HSM interface. 0_B DF1 ready, not busy; DF1 in operation mode. 1_B DF1 busy; DF1 not in operation mode.
PxBUSY (x=0)	x+2	rh	**Program Flash PFxBUSY** HW-controlled status flag. Indication of busy state of PFx because of active execution of an operation; PFx busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state the PFx does not allow read access. 0_B PFx ready, not busy; PFx in operation mode. 1_B PFx busy; PFx not in operation mode.
RES (x=1-5)	x+2	r	**Reserved** Always read as 0; should be written with 0.
RES	15:8, 23, 31:26	r	**Reserved** Always read as 0; should be written with 0.
RES	16, 17, 18, 19, 22, 25:24	rX	**Reserved** Undefined.
DFPAGE	20	rh	**Data Flash in Page Mode** HW-controlled status flag. Set with Enter Page Mode for DFLASH, cleared with Write Page command. This bit is not set by “Enter Page Mode” initiated by the HSM interface. *Note: Read accesses are allowed while in page mode.* 0_B Data Flash not in page mode 1_B Data Flash in page mode

Field	Bits	Type	Description
PFPAGE	21	rh	**Program Flash in Page Mode** HW-controlled status flag. Set with Enter Page Mode for Flash, cleared with Write Page command This bit is not set by “Enter Page Mode” initiated by the HSM interface. *Note: Read accesses are allowed while in page mode.* 0_B Flash not in page mode. 1_B Flash in page mode.

Flash Protection Status Register

This register reports the state of the Flash protection and contains protection relevant control fields.

DMU_HF_PROTECT
Flash Protection Status Register ($000001C_H$) Application Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES							SRT	RES							
r							rh	r							

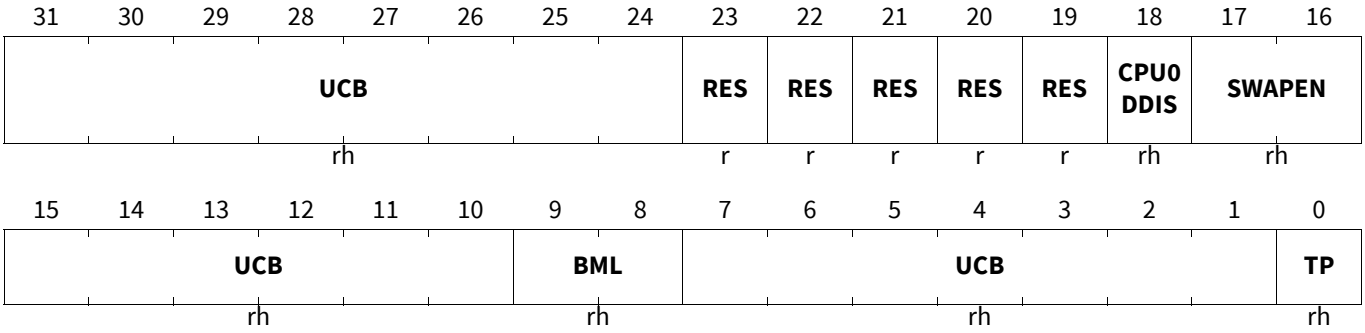
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES		RES	RES	RES	RES	RES	PRODISP0	RES		PRODISSWAP	PRODISBMHD	PRODISEC	PRODISDBG	PRODISD	PRODISP
r		r	r	r	r	r	rh	r		rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
PRODISP	0	rh	**PFLASH Protection Disabled** The protection configured by UCB_PFLASH_ORIG and UCB_PFLASH_COPY was successfully disabled by supplying the correct password to “Disable Protection”. *Note: Cleared with command “Resume Protection”.*
PRODISD	1	rh	**DFLASH Protection Disabled** The protection configured by UCB_DFLASH_ORIG and UCB_DFLASH_COPY was successfully disabled by supplying the correct password to “Disable Protection”. *Note: Cleared with command “Resume Protection”.*
PRODISDBG	2	rh	**Debug Interface Password Protection Disabled** The password configured by UCB_DBG_ORIG and UCB_DBG_COPY was correctly received with “Disable Protection”. When DMU_SP_PROCONHSMCFG.DESTDBG is “destructive” then only the SSW can disable this protection. *Note: Cleared with command “Resume Protection”.*

Field	Bits	Type	Description
PRODISEC	3	rh	**Erase Counter Priority Protection Disabled** The protection configured by UCB_ECPRIO_ORIG and UCB_ECPRIO_COPY was successfully disabled by supplying the correct password to “Disable Protection”. *Note: Cleared with command "Resume Protection".*
PRODISBMHD	4	rh	**BMHD Protection Disabled** The protection configured by UCB_BMHD0_ORIG and UCB_BMHD0_COPY was successfully disabled by supplying the correct password to “Disable Protection”. *Note: Cleared with command "Resume Protection".*
PRODISSWAP	5	rh	**UCB_SWAP protection Disabled** The protection configured by UCB_SWAP_ORIG and UCB_SWAP_COPY was successfully disabled by supplying the correct password to “Disable Protection”. *Note: Cleared with command "Resume Protection".*
RES	7:6, 23:14, 31:25	r	**Reserved** Always read as 0; should be written with 0.
PRODISPx (x=0)	x+8	rh	**Program Flash Protection Disable PRODISPx** The protection configured for PFx by UCB_PFLASH_ORIG and UCB_PFLASH_COPY was successfully disabled by supplying the correct password to “Disable Protection”. *Note: Cleared with command "Resume Protection".*
RES (x=1-5)	x+8	r	**Reserved** Always read as 0; should be written with 0.
SRT	24	rh	**Secure Retest Password Protection Disabled** *Note: Cleared with command “Resume Protection”.* 0_B Secure Retest protection is not disabled. 1_B Secure Retest protection is disabled.

Tuning Protection Configuration

DMU_HF_PROCONTP
Tuning Protection Configuration **(0000084_H)** **Reset Value: Table 28**



Field	Bits	Type	Description
TP	0	rh	**Tuning Protection** This bit indicates whether tuning protection is installed or not. 0_B Tuning protection is not configured. 1_B Tuning protection is configured and installed, if correctly confirmed.
UCB	7:1, 15:10, 31:24	rh	**Reserved for UCB** Deliver the corresponding content of UCB.
BML	9:8	rh	**Boot Mode Lock** Used by the SSW to restrict the boot mode selection. 00_B Boot flow with standard evaluation of boot headers. 01_B Restricted boot flow, never evaluating HWCFG pins and without fallback to boot loader. … 11_B Restricted boot flow, never evaluating HWCFG pins and without fallback to boot loader.
SWAPEN	17:16	rh	**Enable SOTA mode** This field enables the entry into "Software update Over the Air(SOTA) mode". In this mode, an alternate PFLASH address map can be selected. Please refer to the SOTA section of the Introduction chapter for more details. 00_B **Disabled**, SOTA mode disabled. … 10_B **Disabled**, SOTA mode disabled. 11_B **Enabled**, SOTA mode enabled.
CPUxDDIS (x=0)	x+18	rh	**Disable direct LPB access** Disable direct LPB access by the CPU to the Local PFlash Bank (LPB). 0_B Direct LPB access is enabled. 1_B Direct LPB access is disabled.
RES (x=1-5)	x+18	r	**Reserved** Always read as 0; should be written with 0.

Table 28 Reset Values of DMU_HF_PROCONTP

Reset Type	Reset Value	Note
Application Reset	0000 0000$_H$	
CFS Value	0000 0000$_H$	

6.3.3 Connectivity

Table 29 Connections of DMU

Interface Signals	connects		Description
DMU:HOST_INT	to	INT:dmu.HOST_INT	PMU Host Service Request
DMU:FSI_INT	to	INT:dmu.FSI_INT	PMU FSI Service Request

6.3.4 Revision History

Table 30 Revision History

Reference	Change to Previous Version	Comment
V2.0.8		
V2.0.9		
	No document changes - version update to remain aligned with family document.	
V2.0.10		
	No document changes - version update to remain aligned with family document.	
V2.0.11		
Page 11	Updated register **DMU_HF_STATUS**.	
Page 16	**Connectivity** - Table updated	
	No functional changes.	
V2.0.12		
–	No functional changes.	

6.4 Non Volatile Memory (NVM)

This chapter supplements the family documentation with the device specific information for TC33xEXT.

6.4.1 TC33xEXT Specific Register Set

Register Address Space Table

Table 31 Register Address Space - FSI

Module	Base Address	End Address	Note
FSI	$F8030000_H$	$F80300FF_H$	sri slave interface

Table 32 Register Address Space - PFI

Module	Base Address	End Address	Note
(PFI0)	80000000_H	$801FFFFF_H$	Program Flash cached address space
	$A0000000_H$	$A01FFFFF_H$	Program Flash non-cached address space
	$A8000000_H$	$A8003FFF_H$	Erase Counter address space
PFI0	$A8080000_H$	$A80FFFFF_H$	Register address space

Register Overview Table

Table 33 Register Overview - FSI (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FSI_COMM_1	Communication Register 1	0004_H	U,SV	U,SV	System Reset	See Family Spec
FSI_COMM_2	Communication Register 2	0005_H	U,SV	U,SV	System Reset	See Family Spec
FSI_HSMCOMM_1	HSM Communication Register 1	0006_H	H	H	System Reset	See Family Spec
FSI_HSMCOMM_2	HSM Communication Register 2	0007_H	H	H	System Reset	See Family Spec

Table 34 Register Overview - PFI (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
PFI0_ECCR	ECC Read Register	000000_H	See Family Spec
PFI0_ECCS	ECC Status Register	000020_H	See Family Spec
PFI0_SBABRECORDx (x=0-16)	SBAB Record x	002000_H+x*20 H	See Family Spec
PFI0_DBABRECORDx (x=0-1)	DBAB Record x	004000_H+x*20 H	See Family Spec
PFI0_MBABRECORDx (x=0)	MBAB Record 0	008000_H	See Family Spec
PFI0_ZBABRECORDx (x=0-3)	ZBAB Record x	$00C000_H$+x*20 H	See Family Spec

6.4.2 Connectivity

No connections in device.

6.4.3 Revision History

Table 35 Revision History

Reference	Change to Previous Version	Comment
V2.0.3		
	First version. Version number to remain aligned with family document.	
V2.0.4		
	No document changes - version update to remain aligned with family document.	
V2.0.5		
Page 17	**Register Address Space Table** - Updated PFI address ranges to match device size. PFI instances not used in this device removed.	
V2.0.6		
	No functional changes.	

7 Local Memory Unit (LMU)

This device doesn’t contain a LMU module.

8 Default Application Memory (LMU_DAM)

This device doesn’t contain LMU_DAM.

9 System Control Unit (SCU)

This chapter describes the System Control Unit (short SCU) Module of the TC33xEXT.

9.1 TC33xEXT Specific IP Configuration

Table 36 TC33xEXT specific configuration of SCU

Parameter	SCU
Number of WDT linked to the number of CPU	2
Name of the ssw value	After SSW execution
CFS value for DTSCBGOCTRL register	40_H
CFS value for DTSCCON register	200_H

The following sections describe several differences that are device specific at the SCU level.

9.1.1 LBIST considerations for TC33xEXT

The LBIST function can be controlled via four registers available at SCU level: LBISTCTRL0, LBISTCTRL1, LBISTCTRL2 and LBISTCTRL3 (for a complete description of these register, please address the family specification).

The LBISTCTRL3 register contains the MISR signature value that can be read back via software, after the LBIST execution (and the execution is valid).

9.1.1.1 TC33xEXT AA

LBIST Configuration A

LBISTCTRL0.PATTERNS = 0x140;

LBISTCTRL2.LENGTH = 0x3C;

With LBISTCTRL1.BODY = 0:

- LBISTCTRL1 = 0x54000007
- LBISTCTRL3 = 0x92B982C9

With LBISTCTRL1.BODY = 1:

- LBISTCTRL1 = 0x5C000007
- LBISTCTRL3 = 0x59124F97

9.2 TC33xEXT Specific Register Set

The address space for the module registers is defined in **Register Address Space - SCU**.

Table 37 Register Address Space - SCU

Module	Base Address	End Address	Note
SCU	$F0036000_H$	$F00363FF_H$	SCU: Connections to FPI/BPI bus

Table 38 Register Overview - SCU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (0010_H Byte)	0000_H	BE	BE		
SCU_ID	Identification Register	0008_H	U,SV	BE	System Reset	See Family Spec
	Reserved (0010_H Byte)	$000C_H$	BE	BE		
SCU_OSCCON	OSC Control Register	0010_H	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_SYSPLLSTAT	System PLL Status Register	0014_H	U,SV	BE	See Family Spec	See Family Spec
SCU_SYSPLLCON0	System PLL Configuration 0 Register	0018_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_SYSPLLCON1	System PLL Configuration 1 Register	$001C_H$	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_SYSPLLCON2	System PLL Configuration 2 Register	0020_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_PERPLLSTAT	Peripheral PLL Status Register	0024_H	U,SV	BE	System Reset	See Family Spec
SCU_PERPLLCON0	Peripheral PLL Configuration 0 Register	0028_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_PERPLLCON1	Peripheral PLL Configuration 1 Register	$002C_H$	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON0	CCU Clock Control Register 0	0030_H	U,SV	SV,SE,P0	See Family Spec	See Family Spec

Table 38 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_CCUCON1	CCU Clock Control Register 1	0034_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_FDR	Fractional Divider Register	0038_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_EXTCON	External Clock Control Register	$003C_H$	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON2	CCU Clock Control Register 2	0040_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON3	CCU Clock Control Register 3	0044_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON4	CCU Clock Control Register 4	0048_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON5	CCU Clock Control Register 5	$004C_H$	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_RSTSTAT	Reset Status Register	0050_H	U,SV	BE	See page **15**	**15**
	Reserved (0004_H Byte)	0054_H	BE	BE		
SCU_RSTCON	Reset Configuration Register	0058_H	U,SV	SV,SE,P0	See page **18**	**18**
SCU_ARSTDIS	Application Reset Disable Register	$005C_H$	U,SV	SV,E,P0	PowerOn Reset	**19**
SCU_SWRSTCON	Software Reset Configuration Register	0060_H	U,SV	SV,E,P0	See Family Spec	See Family Spec
SCU_RSTCON2	Additional Reset Control Register	0064_H	U,SV	SV,E,P0	See Family Spec	See Family Spec
SCU_RSTCON3	Reset Configuration Register 3	0068_H	U,SV	SV,E,P0	See Family Spec	See Family Spec
	Reserved (0004_H Byte)	$006C_H$	BE	BE		
SCU_ESRCFGx (x=0-1)	ESRx Input Configuration Register	0070_H+x *4	U,SV	SV,E,P0	System Reset	See Family Spec

Table 38 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_ESROCFG	ESR Output Configuration Register	0078_H	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_SYSCON	System Control Register	$007C_H$	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_CCUCON6	CCU Clock Control Register 6	0080_H	U,SV	SV,SE,P0	System Reset	See Family Spec
SCU_CCUCON7	CCU Clock Control Register 7	0084_H	U,SV	SV,SE,P0	System Reset	See Family Spec
	Reserved (0004_H Byte)	0098_H	BE	BE		
SCU_PDR	ESR Pad Driver Mode Register	$009C_H$	U,SV	SV,E,P0	System Reset	See Family Spec
SCU_IOCR	Input/Output Control Register	$00A0_H$	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_OUT	ESR Output Register	$00A4_H$	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_OMR	ESR Output Modification Register	$00A8_H$	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_IN	ESR Input Register	$00AC_H$	U,SV	BE	System Reset	See Family Spec
	Reserved (0004_H Byte)	$00BC_H$	BE	BE		
SCU_STSTAT	Start-up Status Register	$00C0_H$	U,SV	BE	PowerOn Reset	See Family Spec
SCU_STCON	Start-up Configuration Register	$00C4_H$	U,SV	ST,P0	Application Reset	See Family Spec
SCU_PMCSR0	Power Management Control and Status Register	$00C8_H$	U,SV	SE,CE0,SV, P0	Application Reset	See Family Spec
SCU_PMCSR1	Power Management Control and Status Register	$00CC_H$	U,SV	SE,CE1,SV, P0	Application Reset	See Family Spec

Table 38 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_PMCSR2	Power Management Control and Status Register	$00D0_H$	U,SV	SE,CE2,SV, P0	Application Reset	See Family Spec
SCU_PMCSR3	Power Management Control and Status Register	$00D4_H$	U,SV	SE,CE3,SV, P0	Application Reset	See Family Spec
SCU_PMCSR4	Power Management Control and Status Register	$00D8_H$	U,SV	SE,CE4,SV, P0	Application Reset	See Family Spec
SCU_PMCSR5	Power Management Control and Status Register	$00DC_H$	U,SV	SE,CE5,SV, P0	Application Reset	See Family Spec
SCU_PMSTAT0	Power Management Status Register 0	$00E4_H$	U,SV	BE	Application Reset	See Family Spec
SCU_PMSWCR1	Standby and Wake-up Control Register 1	$00E8_H$	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
	Reserved (0020_H Byte)	$00F0_H$	BE	BE		
SCU_EMSR	Emergency Stop Register	$00FC_H$	U,SV	SV,SE,P0	Application Reset	See Family Spec
SCU_EMSSW	Emergency Stop Software set and clear register	0100_H	U,SV	U,SV,P0	Application Reset	See Family Spec
SCU_DTSCSTAT	Core Die Temperature Sensor Status Register	0104_H	U,SV	BE	Application Reset	See Family Spec
SCU_DTSCLIM	Core Die Temperature Sensor Limit Register	0108_H	U,SV	U,SV,P	Application Reset	See Family Spec
	Reserved (0060_H Byte)	0114_H	BE	BE		
SCU_TRAPDIS1	Trap Disable Register 1	0120_H	U,SV	SV,E,P0	Application Reset	20
SCU_TRAPSTAT	Trap Status Register	0124_H	U,SV	BE	System Reset	See Family Spec
SCU_TRAPSET	Trap Set Register	0128_H	U,SV	SV,E,P0	System Reset	See Family Spec

Table 38 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_TRAPCLR	Trap Clear Register	$012C_H$	U,SV	U,SV,P0	System Reset	See Family Spec
SCU_TRAPDIS0	Trap Disable Register 0	0130_H	U,SV	SV,E,P0	Application Reset	21
SCU_LCLCON0	LCL CPU0 and CPU2 Control Register	0134_H	U,SV	SV,SE,ST,P0	See page 10	10
SCU_LCLCON1	LCL CPU1 and CPU3 Control Register	0138_H	U,SV	SV,SE,ST,P0	See page 10	10
SCU_LCLTEST	LCL Test Register	$013C_H$	U,SV	U,SV,P0	System Reset	11
SCU_CHIPID	Chip Identification Register	0140_H	U,SV	ST,P0	See Family Spec	See Family Spec
SCU_MANID	Manufacturer Identification Register	0144_H	U,SV	BE	System Reset	See Family Spec
SCU_SWAPCTRL	Address Map Control Register	$014C_H$	U,SV	ST,P0	System Reset	See Family Spec
	Reserved (0060_H Byte)	0158_H	BE	BE		
	Reserved (0060_H Byte)	$015C_H$	BE	BE		
	Reserved (0060_H Byte)	0160_H	BE	BE		
SCU_LBISTCTRL0	Logic BIST Control 0 Register	0164_H	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_LBISTCTRL1	Logic BIST Control 1 Register	0168_H	U,SV	SV,SE,P0	See Family Spec	See Family Spec
SCU_LBISTCTRL2	Logic BIST Control 2 Register	$016C_H$	U,SV	SV,SE,P0	See page 12	12
SCU_LBISTCTRL3	Logic BIST Control 3 Register	0170_H	U,SV	BE	See Family Spec	See Family Spec
	Reserved (0020_H Byte)	0178_H	BE	BE		
SCU_STMEM1	Start-up Memory Register 1	0184_H	U,SV	ST,P0	PowerOn Reset	See Family Spec
SCU_STMEM2	Start-up Memory Register 2	0188_H	U,SV	ST,P0	System Reset	See Family Spec

Table 38 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_PDISC	Pad Disable Control Register	$018C_H$	U,SV	SV,E,P0	System Reset	See Family Spec
	Reserved (0020_H Byte)	0194_H	BE	BE		
SCU_PMTRCSR0	Power Management Transition Control and Status Register 0	0198_H	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR1	Power Management Transition Control and Status Register 1	$019C_H$	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR2	Power Management Transition Control and Status Register 2	$01A0_H$	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_PMTRCSR3	Power Management Transition Control and Status Register 3	$01A4_H$	U,SV	SV,SE,P0	Cold PowerOn Reset	See Family Spec
SCU_STMEM3	Start-up Memory Register 3	$01C0_H$	U,SV	ST,P0	Application Reset	See Family Spec
SCU_STMEM4	Start-up Memory Register 4	$01C4_H$	U,SV	ST,P0	Cold PowerOn Reset	See Family Spec
SCU_STMEM5	Start-up Memory Register 5	$01C8_H$	U,SV	ST,P0	PowerOn Reset	See Family Spec
SCU_STMEM6	Start-up Memory Register 6	$01CC_H$	U,SV	ST,P0	System Reset	See Family Spec
SCU_OVCENABLE	Overlay Enable Register	$01E0_H$	U,SV	SV,SE,P0	Application Reset	13
SCU_OVCCON	Overlay Control Register	$01E4_H$	U,SV	SV,P0	Application Reset	14
SCU_EIFILT	External Input Filter Register	$020C_H$	U,SV	SE,SV,P0	Application Reset	See Family Spec
SCU_EICRi (i=0-3)	External Input Channel Register i	0210_H+i*4	U,SV	SE,SV,P0	Application Reset	See Family Spec
SCU_EIFR	External Input Flag Register	0220_H	U,SV	BE	Application Reset	See Family Spec

Table 38 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_FMR	Flag Modification Register	0224_H	U,SV	U,SV,P0	Application Reset	See Family Spec
SCU_PDRR	Pattern Detection Result Register	0228_H	U,SV	BE	Application Reset	See Family Spec
SCU_IGCRj (j=0-3)	Flag Gating Register j	$022C_H$+j*4	U,SV	SE,SV,P0	Application Reset	See Family Spec
	Reserved (0030_H Byte)	$023C_H$	BE	BE		
SCU_WDTCPUyCON0 (y=0) (y=1)	CPUy WDT Control Register 0	$024C_H$+y*12	U,SV	U,SV,32,CPUy (y=CPU number)	Application Reset	See Family Spec
SCU_WDTCPUyCON1 (y=0) (y=1)	CPUy WDT Control Register 1	0250_H+y*12	U,SV	SV,CEy,P0	Application Reset	See Family Spec
SCU_WDTCPUySR (y=0) (y=1)	CPUy WDT Status Register	0254_H+y*12	U,SV	BE	Application Reset	See Family Spec
	Reserved (0030_H Byte)	0264_H	BE	BE		
SCU_EICON0	ENDINIT Global Control Register 0	$029C_H$	U,SV	U,SV,32,P0	Application Reset	See Family Spec
SCU_EICON1	ENDINIT Global Control Register 1	$02A0_H$	U,SV	SV,E,P0	Application Reset	See Family Spec
SCU_EISR	ENDINIT Timeout Counter Status Register	$02A4_H$	U,SV	BE	Application Reset	See Family Spec
SCU_WDTSCON0	Safety WDT Control Register 0	$02A8_H$	U,SV	U,SV,32,P1	Application Reset	See Family Spec
SCU_WDTSCON1	Safety WDT Control Register 1	$02AC_H$	U,SV	SV,SE,P1	Application Reset	See Family Spec
SCU_WDTSSR	Safety WDT Status Register	$02B0_H$	U,SV	BE	Application Reset	See Family Spec

Table 38 Register Overview - SCU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SCU_SEICON0	Safety ENDINIT Control Register 0	$02B4_H$	U,SV	U,SV,32,P1	Application Reset	See Family Spec
SCU_SEICON1	Safety ENDINIT Control Register 1	$02B8_H$	U,SV	SV,SE,P1	Application Reset	See Family Spec
SCU_SEISR	Safety ENDINIT Timeout Status Register	$02BC_H$	U,SV	BE	Application Reset	See Family Spec
	Reserved (0440_H Byte)	$02DC_H$	BE	BE		
SCU_ACCEN11	Access Enable Register 11	$03F0_H$	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN10	Access Enable Register 10	$03F4_H$	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN01	Access Enable Register 01	$03F8_H$	U,SV	SV,SE	Application Reset	See Family Spec
SCU_ACCEN00	Access Enable Register 00	$03FC_H$	U,SV	SV,SE	Application Reset	See Family Spec
	Reserved (0440_H Byte)	0400_H	BE	BE		

9.3 TC33xEXT Specific Registers

9.3.1 SCU: Connections to FPI/BPI bus

LCL CPU0 and CPU2 Control Register

Provides control for CPU0and CPU2 Lockstep Comparator Logic blocks.

SCU_LCLCON0

LCL CPU0 and CPU2 Control Register **(0134_H)** **Reset Value: Table 39**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LSEN0								**0**							**LS0**
rw								r							rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1								**0**							**0**
rw								r							r

Field	Bits	Type	Description
LS0	16	rh	**Lockstep Mode Status** This bit indicates whether CPU0 is currently running in lockstep monitor mode 0_B Not in lockstep mode 1_B Running in lockstep mode
LSEN0	31	rw	**Lockstep Enable** This bit may only be written by SSW during boot. Enable lockstep CPU monitoring for the associated processor core, CPU0. After cold reset, lockstep is enabled by default. The LSEN bit may be cleared during the boot to disable lockstep mode. SMU lockstep fault reporting should be disabled when lockstep is disabled. 0_B Lockstep is disabled 1_B Lockstep enabled (Default after Cold Power-On Reset)
0	0, 14:1, 30:17	r	**Reserved in this product** Reserved
1	15	rw	**Reserved in this product** Reserved

Table 39 Reset Values of SCU_LCLCON0

Reset Type	Reset Value	Note
Cold PowerOn Reset	$8001\ 0000_H$	

LCL CPU1 and CPU3 Control Register

Provides control for CPU1 and CPU3 Lockstep Comparator Logic blocks.

SCU_LCLCON1

LCL CPU1 and CPU3 Control Register **(0138_H)** **Reset Value: Table 40**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
1							**0**								**0**
rw							r								r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1							**0**								**0**
rw							r								r

Field	Bits	Type	Description
0	0, 14:1, 16, 30:17	r	**Reserved in this product** Reserved
1	15, 31	rw	**Reserved in this product** Reserved

Table 40 Reset Values of SCU_LCLCON1

Reset Type	Reset Value	Note
Cold PowerOn Reset	$0000\ 0000_H$	

LCL Test Register

Provides the capability for software to inject a fault condition into the comparators of each Lockstep Comparator Logic block. The implementation should generate a single cycle fault each time the bit is written with '1'.

SCU_LCLTEST

LCL Test Register **($013C_H$)** **System Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
					0					**0**	**0**	**0**	**0**	**PLCLT1**	**PLCLT0**
					r					r	r	r	r	w	w

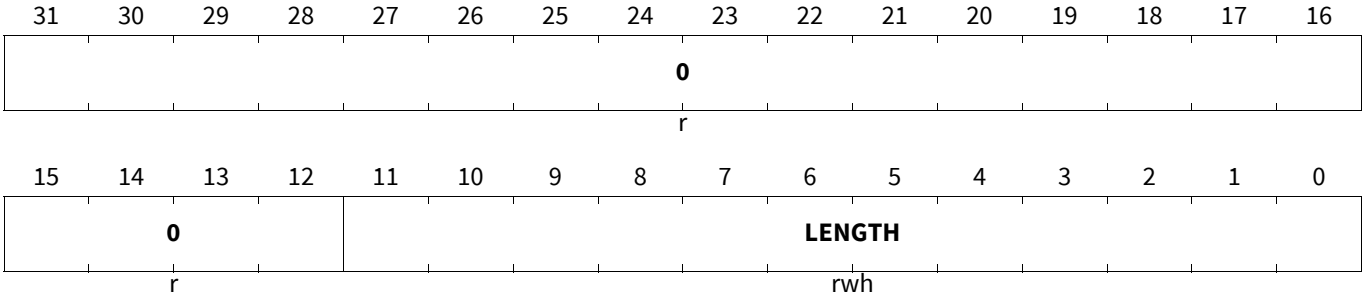
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					0					**0**	**0**	**0**	**0**	**LCLT1**	**LCLT0**
					r					r	r	r	r	w	w

Field	Bits	Type	Description
LCLT0	0	w	**LCL0 Lockstep Test** Fault injection for LCL0. Reads as zero. 0_B No action 1_B Inject single fault in LCL0

Field	Bits	Type	Description
LCLT1	1	w	**LCL1 Lockstep Test** Fault injection for LCL1. Reads as zero. 0_B No action 1_B Inject single fault in LCL1
PLCLT0	16	w	**PFI0 Lockstep Test** Fault injection for PFI0 lockstep. Reads as zero. 0_B No action 1_B Inject single fault in PFI0 lockstep
PLCLT1	17	w	**PFI1 Lockstep Test** Fault injection for PFI1 lockstep. Reads as zero. 0_B No action 1_B Inject single fault in PFI1 lockstep
0	2, 3, 4, 5, 15:6, 18, 19, 20, 21, 31:22	r	**Reserved in this product** will be read as 0 , should be written as 0

Logic BIST Control 2 Register

SCU_LBISTCTRL2
Logic BIST Control 2 Register **($016C_H$)** **Reset Value: Table 41**



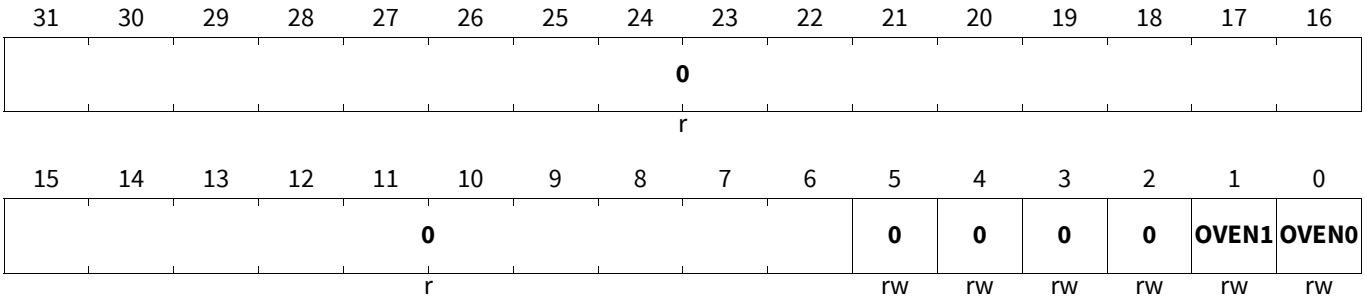
Field	Bits	Type	Description
LENGTH	11:0	rwh	**LBIST Maximum Scan-Chain Length** This field defines the number of shift-cycles for each LBIST scan-load. It will be automatically loaded with the product-specific value, stored in Flash config-sector during startup-software execution.
0	31:12	r	**Reserved** Read as 0; should be written with 0.

Table 41 Reset Values of SCU_LBISTCTRL2

Reset Type	Reset Value	Note
System Reset	$0000\ 0000_H$	
CFS Value	$0000\ 003C_H$	

Overlay Enable Register

SCU_OVCENABLE
Overlay Enable Register (01E0$_H$) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
OVEN0	0	rw	**Overlay Enable 0** 0_B OVC is disabled on CPU0. All Overlay redirections are disabled regardless of the state of OVC0_RABRy.OVEN. 1_B OVC is enabled on CPU0.
OVEN1	1	rw	**Overlay Enable 1 (If product has CPU1)** 0_B OVC is disabled on CPU1. All Overlay redirections are disabled regardless of the state of OVC1_RABRy.OVEN. 1_B OVC is enabled on CPU1.
0	2, 3, 4, 5	rw	**Reserved in this Product** will be read as 0 , should be written as 0
0	31:6	r	**Reserved** Read/write 0.

Overlay Control Register

SCU_OVCCON

Overlay Control Register **($01E4_H$)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						POVCONF	OVCONF	0					DCINVAL	OVSTP	OVSTRT
r						w	rw	r					w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										0	0	0	0	CSEL1	CSEL0
r										r	r	r	r	w	w

Field	Bits	Type	Description
CSEL0	0	w	**CPU Select 0** Return 0 if read. 0_B CPU0 not affected, 1_B Action selected by OVSTRT, OVSTP, DCINVAL bits, set by the same register write access, is applied to CPU0.
CSEL1	1	w	**CPU Select 1 (If product has CPU1)** Return 0 if read. 0_B CPU1 not affected, 1_B Action selected by OVSTRT, OVSTP, DCINVAL bits, set by the same register write access, is applied to CPU1.
OVSTRT	16	w	**Overlay Start** CPUs which are not selected are not affected. No action is taken if OVSTP is also set. Return 0 if read. 0_B No action 1_B For each CPU selected with CSEL, all the blocks selected with OVCx_OSEL will be activated. In the selected CPUs all the blocks deselected with OVCx_OSEL will be deactivated.
OVSTP	17	w	**Overlay Stop** CPUs which are not selected are not affected No action is taken if OVSTRT is also set. Return 0 if read. 0_B No action 1_B For CPUs selected with CSEL, all the overlay blocks are deactivated. OVCx_RABRy.OVEN bits are cleared.
DCINVAL	18	w	**Data Cache Invalidate** No function in devices without data cache in CPU. Data Cache is affected only in the CPUs selected with CSEL. Return 0 if read. 0_B No action 1_B Data Cache Lines in DMI are invalidated[1)]

Field	Bits	Type	Description
OVCONF	24	rw	**Overlay Configured** Overlay configured status bit This bit may be used as handshake bit between a debug device (via JTAG interface and Cerberus) and CPU(s). 0_B Overlay is not configured or it has been already started 1_B Overlay block control registers are configured and ready for overlay start
POVCONF	25	w	**Write Protection for OVCONF** This bit enables OVCONF write during OVCCON write. Return 0 if read. 0_B OVCONF remains unchanged. 1_B OVCONF can be changed with write access to register OVCCON
0	2, 3, 4, 5, 15:6, 23:19, 31:26	r	**Reserved in this Product** Return 0 if read.

1) Dirty (modified) cache lines are not effected by this operation. If data cache contains modified data, it is not invalidated, and has to be written-back and invalidated by the user. Therefore, it is highly recommended to either: access overlaid data in read-only mode, or use only non-cached access.

Reset Status Register

SCU_RSTSTAT

Reset Status Register **(0050_H)** **Reset Value: Table 42**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**LBTERM**	**LBPORST**	**STBYR**	**HSMA**	**HSMS**	**SWD**	**EVR33**	**EVRC**	**R22**	**R21**	**CB3**	**CB1**	**CB0**	**0**	**PORST**
r	rh	rh	rh	rh	rh	rh	rh	rh	rX	rX	rh	rh	rh	r	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		0			**0**	**0**	**0**	**0**	**STM1**	**STM0**	**SW**	**SMU**	**0**	**ESR1**	**ESR0**
		r			r	r	r	r	rh	rh	rh	rh	r	rh	rh

Field	Bits	Type	Description
ESR0	0	rh	**Reset Request Trigger Reset Status for ESR0** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
ESR1	1	rh	**Reset Request Trigger Reset Status for ESR1** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger

Field	Bits	Type	Description
SMU	3	rh	**Reset Request Trigger Reset Status for SMU** (See SMU section for SMU trigger sources, including Watchdog Timers) 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
SW	4	rh	**Reset Request Trigger Reset Status for SW** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
STM0	5	rh	**Reset Request Trigger Reset Status for STM0 Compare Match** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
STM1	6	rh	**Reset Request Trigger Reset Status for STM1 Compare Match (If Product has STM1)** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
PORST	16	rh	**Reset Request Trigger Reset Status for PORST** This bit is also set if the bits CB0, CB1, and CB3 are set in parallel. 0_B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1_B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)
CB0	18	rh	**Reset Request Trigger Reset Status for Cerberus System Reset** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
CB1	19	rh	**Reset Request Trigger Reset Status for Cerberus Debug Reset** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
CB3	20	rh	**Reset Request Trigger Reset Status for Cerberus Application Reset** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
R21	21	rX	**Reserved - 0** Read as 0; should be written with 0.
R22	22	rX	**Reserved - 0** Read as 0; should be written with 0.
EVRC	23	rh	**Reset Request Trigger Reset Status for EVRC** 0_B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1_B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)
EVR33	24	rh	**Reset Request Trigger Reset Status for EVR33** 0_B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1_B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)

Field	Bits	Type	Description
SWD	25	rh	**Reset Request Trigger Reset Status for Supply Watchdog (SWD)** The Supply Watchdog trigger is described in Power Management Controller “Supply Monitoring” chapter 0_B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1_B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)
HSMS	26	rh	**Reset Request Trigger Reset Status for HSM System Reset (HSM S)** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
HSMA	27	rh	**Reset Request Trigger Reset Status for HSM Application Reset (HSM A)** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
STBYR	28	rh	**Reset Request Trigger Reset Status for Standby Regulator Watchdog (STBYR)** 0_B This reset trigger has not occurred since the last clear (by RSTCON2.CLRC) 1_B This reset trigger has occurred since the last clear (by RSTCON2.CLRC)
LBPORST	29	rh	**LBIST termination due to PORST** This bitfield indicates if the LBIST was early terminated due to the occurrence of a Power On Reset. If the status of this bitfield is 0, the application must still check the LBTERM to check if the LBIST was terminated properly. This bitfield is cleared when the RSTCON2.CLRC is set. 0_B LBIST was not terminated early due to a Power On Reset 1_B LBIST early termination due to the occurrence of Power On Reset
LBTERM	30	rh	**LBIST was properly terminated** This bitfield indicates if the LBIST was terminated properly. This bitfield is cleared when the RSTCON2.CLRC is set. 0_B LBIST was not terminated properly 1_B LBIST was terminated properly
0	2, 7, 8, 9, 10, 15:11, 17, 31	r	**Reserved** Read as 0; should be written with 0.

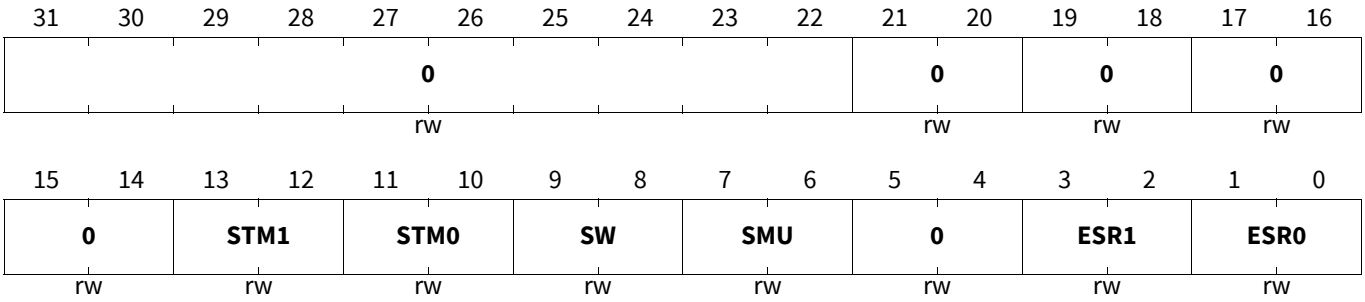
Table 42 Reset Values of SCU_RSTSTAT

Reset Type	Reset Value	Note
Cold PowerOn Reset	0XX1 0000$_H$	RSTSTAT
Cold PowerOn Reset	1001 0000$_H$	RSTSTAT (Triggered by LVD Reset)

Reset Configuration Register

SCU_RSTCON

Reset Configuration Register (0058$_H$) Reset Value: Table 43



Field	Bits	Type	Description
ESR0	1:0	rw	**ESR0 Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from ESR0 reset. 00_B No reset is generated for a trigger of ESR0 01_B A System Reset is generated for a trigger of ESR0 reset 10_B An Application Reset is generated for a trigger of ESR0 reset 11_B Reserved, do not use this combination
ESR1	3:2	rw	**ESR1 Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from ESR1 reset. 00_B No reset is generated for a trigger of ESR1 01_B A System Reset is generated for a trigger of ESR1 reset 10_B An Application Reset is generated for a trigger of ESR1 reset 11_B Reserved, do not use this combination
SMU	7:6	rw	**SMU Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from SMU reset. 00_B No reset is generated for a trigger of SMU 01_B A System Reset is generated for a trigger of SMU reset 10_B An Application Reset is generated for a trigger of SMU reset 11_B Reserved, do not use this combination

Field	Bits	Type	Description
SW	9:8	rw	**SW Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from software reset. 00_B No reset is generated for a trigger of software reset 01_B A System Reset is generated for a trigger of Software reset 10_B An Application Reset is generated for a trigger of Software reset 11_B Reserved, do not use this combination
STM0	11:10	rw	**STM0 Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from STM0 compare match reset. 00_B No reset is generated for an STM0 trigger 01_B A System Reset is generated for a trigger of STM0 reset 10_B An Application Reset is generated for a trigger of STM0 reset 11_B Reserved, do not use this combination
STM1	13:12	rw	**STM1 Reset Request Trigger Reset Configuration (If Product has STM1)** This bit field defines which reset is generated by a reset request trigger from STM1 compare match reset. 00_B No reset is generated for a trigger of STM1 01_B A System Reset is generated for a trigger of STM1 reset 10_B An Application Reset is generated for a trigger of STM1 reset 11_B Reserved, do not use this combination
0	5:4, 15:14, 17:16, 19:18, 21:20, 31:22	rw	**Reserved** Should be written with 0.

Table 43 Reset Values of SCU_RSTCON

Reset Type	Reset Value	Note
PowerOn Reset	$0000\ 0282_H$	RSTCON

Application Reset Disable Register

SCU_ARSTDIS

Application Reset Disable Register ($005C_H$) PowerOn Reset Value: $0000\ 0000_H$

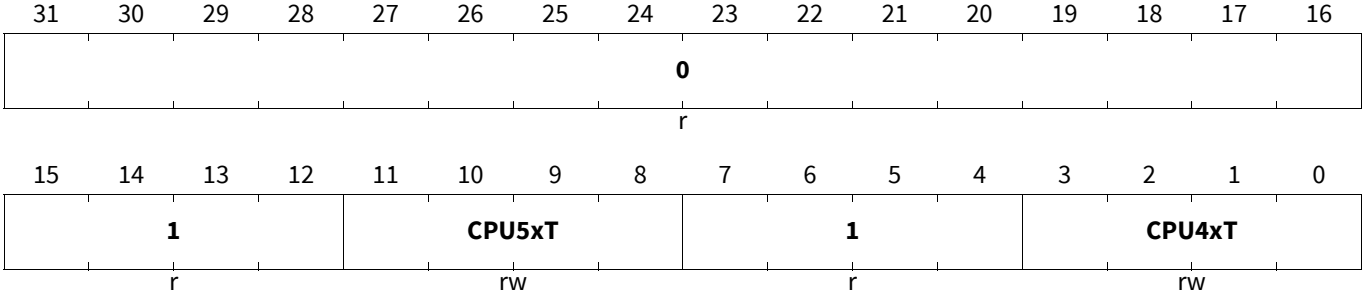
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								0		0	0	0	0	STM1 DIS	STM0 DIS
r								rw		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
STM0DIS	0	rw	**STM0 Disable Reset** This bit field defines if an Application Reset leads to an reset for the STM0. 0_B An Application Reset resets the STM0 1_B An Application Reset has no effect for the STM0
STM1DIS	1	rw	**STM1 Disable Reset** This bit field defines if an Application Reset leads to an reset for the STM1. 0_B An Application Reset resets the STM1 1_B An Application Reset has no effect for the STM1
0	2, 3, 4, 5, 7:6	rw	**Reserved** Should be written with 0.
0	31:8	r	**Reserved** Read as 0; should be written with 0.

Trap Disable Register 1

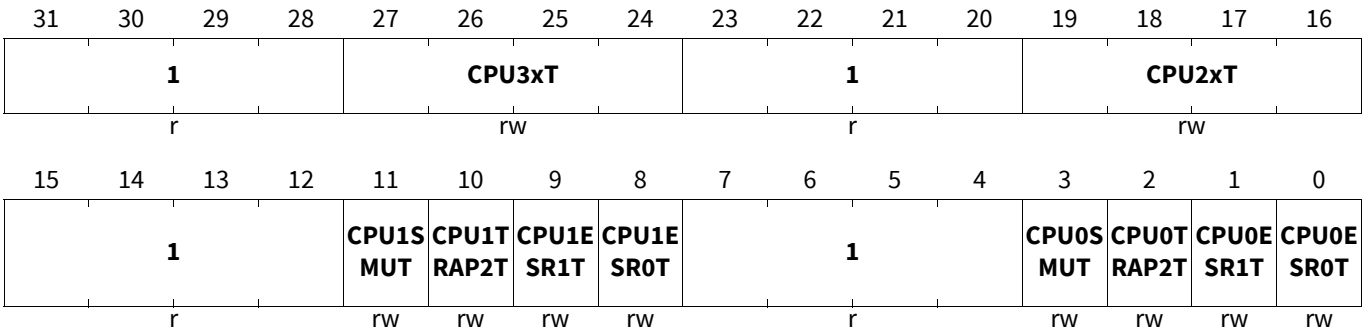
SCU_TRAPDIS1
Trap Disable Register 1 **(0120_H)** **Application Reset Value: 0000 FFFF$_H$**



Field	Bits	Type	Description
CPU4xT	3:0	rw	**Reserved in this product**
CPU5xT	11:8	rw	**Reserved in this product**
1	7:4, 15:12	r	**Reserved** Must only be written with one. Read as one.
0	31:16	r	**Reserved** Read as zero

Trap Disable Register 0

SCU_TRAPDIS0
Trap Disable Register 0 **(0130_H)** **Application Reset Value: FFFF FFFF$_H$**



Field	Bits	Type	Description
CPU0ESR0T	0	rw	**Disable Trap Request ESR0T on CPU0** 0_B A CPU0 trap request can be generated for this source 1_B No trap request can be generated for this source
CPU0ESR1T	1	rw	**Disable Trap Request ESR1T on CPU0** 0_B A CPU0 trap request can be generated for this source 1_B No trap request can be generated for this source
CPU0TRAP2T	2	rw	**Disable Trap Request TRAP2T on CPU0** 0_B A CPU0 trap request can be generated for this source 1_B No trap request can be generated for this source
CPU0SMUT	3	rw	**Disable Trap Request SMUT on CPU0** 0_B A CPU0 trap request can be generated for this source 1_B No trap request can be generated for this source
CPU1ESR0T	8	rw	**Disable Trap Request ESR0T on CPU1 (If product has CPU1)** 0_B A CPU1 trap request can be generated for this source 1_B No trap request can be generated for this source
CPU1ESR1T	9	rw	**Disable Trap Request ESR1T on CPU1 (If product has CPU1)** 0_B A CPU1 trap request can be generated for this source 1_B No trap request can be generated for this source
CPU1TRAP2T	10	rw	**Disable Trap Request TRAP2T on CPU1 (If product has CPU1)** 0_B A CPU1 trap request can be generated for this source 1_B No trap request can be generated for this source
CPU1SMUT	11	rw	**Disable Trap Request SMUT on CPU1 (If product has CPU1)** 0_B A CPU1 trap request can be generated for this source 1_B No trap request can be generated for this source
CPU2xT	19:16	rw	**Reserved in this product**
CPU3xT	27:24	rw	**Reserved in this product**
1	7:4, 15:12, 23:20, 31:28	r	**Reserved** Must only be written with one. Read as one.

9.4 Connectivity

Table 44 Connections of SCU

Interface Signals	connects		Description
SCU:CBS_ENDINIT_DIS	from	CBS:ocds_oc(3)	Watchdog ENDINIT disable from Cerberus
SCU:CBS_WDT_SUSP	from	CBS:ocds_wdtsus	Watchdog suspend from Cerberus
SCU:EMGSTOP_PORT_A	from	SMU:FSPSCU	Emergency stop Port Pin A input request
SCU:EMGSTOP_PORT_B	from	P21.2:IN	Emergency stop Port Pin B input request
SCU:ESR0_PORT_IN	from	TC33xEXT:ESR0	ESR0 Port Pin input - can be used to trigger a reset or an NMI
SCU:ESR1_PORT_IN	from	TC33xEXT:ESR1	ESR1 Port Pin input - can be used to trigger a reset or an NMI
SCU:E_IOUT(0)	to	RIF0:RAMP1C	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
		EVADC:G0REQTRH	
SCU:E_IOUT(1)	to	EVADC:G1REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(2)	to	EVADC:G2REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(3:2)	to	CAN0:ttc_ectt(4:3)	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(3)	to	EVADC:G3REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_IOUT(4)	to	CAN0:ttc_ltrc_trig(4)	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
		EVADC:G4REQTRH	
SCU:E_IOUT(5)	to	EVADC:G5REQTRH	ERU IOUTn output (MSB is IOUT7 and LSB is IOUT0)
SCU:E_PDOUT(0)	to	CCU60:CTRAPD	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		CCU60:T12HRH	
		EVADC:G0REQGTM	
SCU:E_PDOUT(1)	to	CCU61:CTRAPD	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		CCU61:T12HRH	
		EVADC:G1REQGTM	
SCU:E_PDOUT(2)	to	EVADC:G2REQGTM	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
SCU:E_PDOUT(3)	to	EVADC:G3REQGTM	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
SCU:E_PDOUT(4)	to	CCU60:CC62IND	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		GPT120:T3INC	
		EVADC:G4REQGTM	
SCU:E_PDOUT(5)	to	CCU61:CC62IND	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
		EVADC:G5REQGTM	

Table 44 Connections of SCU (cont'd)

Interface Signals	connects		Description
SCU:E_PDOUT(6)	to	GPT120:CAPINB	ERU PDOUTn output (MSB is PDOUT7 and LSB is PDOUT0)
SCU:E_REQ0(0)	from	P15.4:IN	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(1)	from	CCU60:COUT60	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ0(2)	from	P10.7:IN	ERU Channel 0 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(0)	from	P14.3:IN	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(1)	from	CCU61:COUT60	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(2)	from	P10.8:IN	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ1(3)	from	STM0:STMIR(0)	ERU Channel 1 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(0)	from	P10.2:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(1)	from	P02.1:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ2(2)	from	P00.4:IN	ERU Channel 2 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(0)	from	P10.3:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(1)	from	P14.1:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(2)	from	P02.0:IN	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ3(3)	from	STM1:STMIR(0)	ERU Channel 3 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(0)	from	P33.7:IN	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(2)	from	GPT120:T3OUT	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ4(3)	from	P15.5:IN	ERU Channel 4 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(0)	from	P15.8:IN	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ5(2)	from	GPT120:T6OUT	ERU Channel 5 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ6(0)	from	P20.0:IN	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.

Table 44 Connections of SCU (cont'd)

Interface Signals	connects		Description
SCU:E_REQ6(1)	from	TC33xEXT:ESR0	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ6(3)	from	P11.10:IN	ERU Channel 6 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(0)	from	P20.9:IN	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(1)	from	TC33xEXT:ESR1	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:E_REQ7(2)	from	P15.1:IN	ERU Channel 7 input X; x=0-5, where 0 is input A and 5 is input F.
SCU:RST_REQ_STM(10)	from	HSM:SYSRST	Reset request from STMn (MSB is STM5 and LSB is STM0)
SCU:RST_REQ_STM(11)	from	HSM:APPRST	Reset request from STMn (MSB is STM5 and LSB is STM0)
SCU:SMU_EMGSTP_REQ	from	SMU:EMERGENCYSTOPREQ	Emergency stop request from SMU
SCU:SMU_TRAP_REQ	from	SMU:NMIREQ	TRAP request from the SMU
SCU:TRAP_CPU(0)	to	cpu_pfi_pfrwb_0:tc162p_nmi_trap	TRAP output to CPUn (MSB is CPU5 and LSB is CPU0)
SCU:TRAP_CPU(1)	to	cpu_1:tc162p_nmi_trap	TRAP output to CPUn (MSB is CPU5 and LSB is CPU0)
SCU:ERU_INT(3:0)	to	INT:scu.ERU_INT(3:0)	SCU ERU Service Request x

9.5 Revision History

The following table contains the revision history of the SCU that is relevant for the TC33xEXT device. For a complete revision history please address the family user manual.

This section only includes entries, respective to the Clock System, that are related to register updates. For a complete Clock System revision history please address the family user manual.

Table 45 Revision History

Reference	Change to Previous Version	Comment
V2.1.21		
	Initial version for TC33x.	
V2.1.22		
Page 15	Cold PORST reset value changed from 1xx10000 to 0xx10000 in RSTSTAT register.	
Page 15	Additional cold_power_on_reset value "LVD Reset" added to RSTSTAT register.	
Page 10	LBISTCTRL0: System Reset value set to "Internal". Added note to CFS Value in reset table: "Value installed after System and Power-On Reset."	
Page 10	LCLCON0 and LCLCON1: Cold PORST reset table values updated/corrected.	

Table 45 Revision History (cont'd)

Reference	Change to Previous Version	Comment
Page 24	Revision History cleanup and update.	
V2.1.23		
Page 1	LBISTCTRL register configuration corrected.	
Page 2, Page 10	LBISTCTRL2 added at specific registers section.	
V2.1.24		
Page 10	Updated Cold PowerOn Reset Value of LCLCONx.	
V2.1.25		
	No functional changes.	
V2.1.26		
	No functional changes.	
V2.1.27		
	No functional changes.	

10 Clocking System

Device specific information about the clocking system is contained in the SCU chapter as both modules share a common bus interface.

11 Power Management System (PMS)

This chapter describes the Power Management System (PMS) Module of the TC33xEXT.

11.1 TC33xEXT Specific IP Configuration

Table 46 TC33xEXT specific configuration of PMS

Parameter	PMS
CFS value for the PMSWCR4 register	02000020_H

11.2 TC33xEXT Specific Register Set

The PMS related SCU registers are specified in the SCU section of this appendix.

Table 47 Register Address Space - PMS

Module	Base Address	End Address	Note
(PMS)	$F0240000_H$	$F0241FFF_H$	
PMS	$F0248000_H$	$F02481FF_H$	FPI slave interface

Table 48 Register Overview - PMS (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_ID	Identification Register	0008_H	U,SV	BE	Application Reset	See Family Spec
PMS_EVRSTAT	EVR Status Register	$002C_H$	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRADCSTAT	EVR Primary ADC Status Register	0034_H	U,SV	BE	LVD Reset	See Family Spec
PMS_EVRRSTCON	EVR Reset Control Register	$003C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRRSTSTAT	EVR Reset Status Register	0044_H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRTRIM	EVR Trim Control Register	$004C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRTRIMSTAT	EVR Trim Status Register	0050_H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONSTAT1	EVR Secondary ADC Status Register 1	0060_H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONSTAT2	EVR Secondary ADC Status Register 2	0064_H	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRMONCTRL	EVR Secondary Monitor Control Register	0068_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRMONFILT	EVR Secondary Monitor Filter Register	0070_H	U,SV	SV,SE,P	See Family Spec	See Family Spec

Table 48 Register Overview - PMS (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_PMSIEN	PMS Interrupt Enable Register	0074_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRUVMON	EVR Secondary Under-voltage Monitor Register	0078_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROVMON	EVR Secondary Over-voltage Monitor Register	$007C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRUVMON2	EVR Secondary Under-voltage Monitor Register 2	0080_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROVMON2	EVR Secondary Over-voltage Monitor Register 2	0084_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_HSMUVMON	EVR Primary HSM Under-voltage Monitor Register	0088_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_HSMOVMON	EVR Primary HSM Over-voltage Monitor Register	$008C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVR33CON	EVR33 Control Register	0090_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVROSCCTRL	EVR Oscillator Control Register	$00A0_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_PMSWCR0	Standby and Wake-up Control Register 0	$00B4_H$	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR2	Standby and Wake-up Control Register 2	$00B8_H$	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR3	Standby and Wake-up Control Register 3	$00C0_H$	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_PMSWCR4	Standby and Wake-up Control Register 4	$00C4_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_PMSWCR5	Standby and Wake-up Control Register 5	$00C8_H$	U,SV	SV,SE,P	LVD Reset	See Family Spec

Table 48 Register Overview - PMS (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_PMSWSTAT	Standby and Wake-up Status Register	$00D4_H$	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWSTAT2	Standby and Wake-up Status Register 2	$00D8_H$	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWUTCNT	Standby WUT Counter Register	$00DC_H$	U,SV	BE	LVD Reset	See Family Spec
PMS_PMSWSTATCLR	Standby and Wake-up Status Clear Register	$00E8_H$	U,SV	SV,SE,P	LVD Reset	See Family Spec
PMS_EVRSDSTAT0	EVR SD Status Register 0	$00FC_H$	U,SV	BE	See Family Spec	See Family Spec
PMS_EVRSDCTRL0	EVRC SD Control Register 0	0108_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL1	EVRC SD Control Register 1	$010C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL2	EVRC SD Control Register 2	0110_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL3	EVRC SD Control Register 3	0114_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL4	EVRC SD Control Register 4	0118_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL5	EVRC SD Control Register 5	$011C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL6	EVRC SD Control Register 6	0120_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL7	EVRC SD Control Register 7	0124_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL8	EVRC SD Control Register 8	0128_H	U,SV	SV,SE,P	See Family Spec	See Family Spec

Table 48 Register Overview - PMS (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_EVRSDCTRL9	EVRC SD Control Register 9	$012C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL10	EVRC SD Control Register 10	0130_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCTRL11	EVRC SD Control Register 11	0134_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF0	EVRC SD Coefficient Register 0	0148_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF1	EVRC SD Coefficient Register 1	$014C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF2	EVRC SD Coefficient Register 2	0150_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF3	EVRC SD Coefficient Register 3	0154_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF4	EVRC SD Coefficient Register 4	0158_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF5	EVRC SD Coefficient Register 5	$015C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF6	EVRC SD Coefficient Register 6	0160_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF7	EVRC SD Coefficient Register 7	0164_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF8	EVRC SD Coefficient Register 8	0168_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_EVRSDCOEFF9	EVRC SD Coefficient Register 9	$016C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_AG2i_STDBY (i=0-1)	Alarm Status Register	0188_H+i*4	U,SV	SV,SE,P	LVD Reset	See Family Spec

Table 48 Register Overview - PMS (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
PMS_MONBISTSTAT	SMU_stdby BIST Status Register	0190_H	U,SV	BE	See Family Spec	See Family Spec
PMS_MONBISTCTRL	SMU_stdby BIST Control Register	0198_H	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_CMD_STDBY	SMU_stdby Command Register	$019C_H$	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_AG2iFSP_STDBY (i=0-1)	SMU_stdby FSP Configuration Register	$01A4_H$+i*4	U,SV	SV,SE,P	See Family Spec	See Family Spec
PMS_DTSSTAT	Die Temperature Sensor Status Register	$01C0_H$	U,SV	BE	See Family Spec	See Family Spec
PMS_DTSLIM	Die Temperature Sensor Limit Register	$01C8_H$	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSS	OCDS Trigger Set Select Register	$01E0_H$	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSC0	OCDS Trigger Set Control 0 Register	$01E4_H$	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_OTSC1	OCDS Trigger Set Control 1 Register	$01E8_H$	U,SV	U,SV,P	See Family Spec	See Family Spec
PMS_ACCEN1	Access Enable Register 1	$01F8_H$	U,SV	SV,SE,32	Application Reset	See Family Spec
PMS_ACCEN0	Access Enable Register 0	$01FC_H$	U,SV	SV,SE,32	Application Reset	See Family Spec

11.3 TC33xEXT Specific Registers

11.3.1 FPI slave interface

11.4 Connectivity

Table 49 Connections of PMS

Interface Signals	connects		Description
PMS:DCDCSYNCO	to	P32.4:HWOUT(0)	DC-DC synchronization output
		P32.4:ALT(2)	
PMS:ESR0PORST	to	TC33xEXT:ESR0	ESR0 control output during PORST activation
PMS:ESR0WKP	from	TC33xEXT:ESR0	ESR0 pin input
PMS:ESR1WKP	from	TC33xEXT:ESR1	ESR1 pin input
PMS:HWCFG1IN	from	TC33xEXT:P14.5	HWCFG1 pin input
PMS:HWCFG2IN	from	TC33xEXT:P14.2	HWCFG2 pin input
PMS:HWCFG4IN	from	TC33xEXT:P10.5	HWCFG4 pin input
PMS:HWCFG5IN	from	TC33xEXT:P10.6	HWCFG5 pin input
PMS:HWCFG6IN	from	TC33xEXT:P14.4	HWCFG6 pin input
PMS:PINAWKP	from	TC33xEXT:P14.1	PINA (P14.1) pin input
PMS:PINBWKP	from	TC33xEXT:P33.12	PINB (P33.12) pin input
PMS:PORSTIN	from	TC33xEXT:PORST	PORST pin input
PMS:PORSTOUT	to	TC33xEXT:PORST	PORST pin output
PMS:TESTMODEIN	from	TC33xEXT:P20.2	TESTMODE pin input
PMS:VDDMLVL	to	converter_0:converter_low_supp	VDDM monitor signal to Converter
PMS:VGATE1N	to	TC33xEXT:CTRL1V3N	DCDC N ch. MOSFET gate driver output
		TC33xEXT:CTRL1V3N	
PMS:VGATE1P	to	TC33xEXT:CTRL1V3P	DCDC P ch. MOSFET gate driver output
		TC33xEXT:CTRL1V3P	

11.5 Revision History

Table 50 Revision History

Reference	Change to Previous Version	Comment
V2.2.28		
	Initial version for TC33X	
V2.2.29		
–	No functional changes.	
V2.2.30		
Page 2	Register “PMS_EVR33CON” now visible to the customer.	
V2.2.31		

Table 50 Revision History (cont'd)

Reference	Change to Previous Version	Comment
–	No functional changes.	
V2.2.32		
	No functional changes.	
V2.2.33		
–	No functional changes.	
V2.2.34		
–	No functional changes.	

12 Power Management System for Low-End (PMSLE)

This device doesn’t contain a PMSLE module.

13 Memory Test Unit (MTU)

For the generic description of the Memory Test Unit (MTU) and the SRAM Support Hardware (SSH), please refer to the platform chapter.

13.1 TC33xEXT Specific IP Configuration

There is no device specific IP configuration. MTU+SSH is generic across all derivates in the platforms. Only the SSH instances vary.

13.2 Handling of Large DSPR SRAMs

On this device, the CPU0 and CPU1 have large DSPR SRAMs. Therefore, there are two SSHs to support these SRAMs. These are named as CPUxDMEM and CPUxDMEM1 (x=0,1).

Logically, these 2 SSHs behave as separate SSHs, with their own MEMTEST_EN bits, Alarms to the SMU, error status flags etc. However special handling is required to enter test mode for these SSHs.

When running a Non-Destructive-test, only one of the DMEM SSHs shall be enabled at a time. This is because the ECC encoder and decoder are shared between the two SSHs.

However, as long as destructive tests or SSH register accesses are to be performed, then both SSHs can be enabled together.

Please note that when one of the DMEM SSH is enabled, the complete DSPR+DCACHE is unavailable for functional access. This is due to internal interleaving of the logical address space.

Although the DCACHE is also split equally between the two SRAMs, the entire cache has to be mapped at once to the system address map. Hence only a single bit is provided in the MTU_MEMMAP register for the entire DMEM.

The partial-erase (i.e. erasing the Cache area; refer the family spec) is triggered separately when each MEMTEST_EN bit is set.

The MEMMAP bit triggers the partial erase in both SSHs at the same time.

If both the SSHs are enabled / disabled at the same time, the software should check either the bits in the MTU_MEMSTAT register, or ensure that the EN bits for both the SSHs are set / cleared in the MEMTEST registers to ensure that the partial-erase has completed.

13.3 TC33xEXT Specific Register Set

Register Address Space Table

Table 51 Register Address Space - MTU

Module	Base Address	End Address	Note
MTU	$F0060000_H$	$F006FFFF_H$	FPI slave interface

Register Overview Table

Table 52 Register Overview - MTU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
MTU_CLC	Clock Control Register	0000_H	U,SV	SV,E,P	Application Reset	See Family Spec
MTU_ID	Identification Register	0008_H	U,SV	BE	Application Reset	See Family Spec
MTU_MEMTESTi (i=0-2)	Memory MBIST Enable Register i	0010_H+i* 4	U,SV	SV,SE,P	Application Reset	3
MTU_MEMMAP	Memory Mapping Enable Register	$001C_H$	U,SV	SV,SE,P	Application Reset	8
MTU_MEMSTATi (i=0-2)	Memory Status Register i	0038_H+i* 4	U,SV	BE	Application Reset	10
MTU_MEMDONEi (i=0-2)	Memory Test Done Status Register i	0050_H+i* 4	U,SV	BE	Application Reset	13
MTU_MEMFDAi (i=0-2)	Memory Test FDA Status Register i	0060_H+i* 4	U,SV	BE	Application Reset	17
MTU_ACCEN1	Access Enable Register 1	$00F8_H$	U,SV	BE	Application Reset	See Family Spec
MTU_ACCEN0	Access Enable Register 0	$00FC_H$	U,SV	SV,SE	Application Reset	See Family Spec
MTU_MCi_CONFIG0 (i=0-95)	Configuration Registers	1000_H+i* 100_H	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCi_CONFIG1 (i=0-95)	Configuration Register 1	1002_H+i* 100_H	U,SV,16	U,SV,P,16	Application Reset	See Family Spec

Table 52 Register Overview - MTU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
MTU_MCi_MCONTROL (i=0-95)	MBIST Control Register	1004_H+i* 100_H	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_MSTATUS (i=0-95)	Status Register	1006_H+i* 100_H	U,SV,16	BE	Application Reset	See Family Spec
MTU_MCi_RANGE (i=0-95)	Range Register, single address mode	1008_H+i* 100_H	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCi_REVID (i=0-95)	Revision ID Register	$100C_H$+i* 100_H	U,SV,16	BE	Application Reset	See Family Spec
MTU_MCi_ECCS (i=0-95)	ECC Safety Register	$100E_H$+i* 100_H	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_ECCD (i=0-95)	Memory ECC Detection Register	1010_H+i* 100_H	U,SV,16	SV,P,16	See Family Spec	See Family Spec
MTU_MCi_ETRRx (i=0-95;x=0-4)	Error Tracking Register x	1012_H+i* 100_H+x* 2	U,SV,16	BE	PowerOn Reset	See Family Spec
MTU_MCi_RDBFLy (i=0-95;y=0-66)	Read Data and Bit Flip Register y	1060_H+i* 100_H+y* 2	U,SV,16	U,SV,P,16	Application Reset	See Family Spec
MTU_MCi_ALMSRCS (i=0-95)	Alarm Sources Configuration Register	$10EE_H$+i* 100_H	U,SV,16	SV,SE,P,16	Application Reset	See Family Spec
MTU_MCi_FAULTSTS (i=0-95)	SSH Safety Faults Status Register	$10F0_H$+i* 100_H	U,SV,16	SV,SE,P,16	PowerOn Reset	See Family Spec
MTU_MCi_ERRINFOx (i=0-95;x=0-4)	Error Information Register x	$10F2_H$+i* 100_H+x* 2	U,SV,16	BE	PowerOn Reset	See Family Spec

13.4 TC33xEXT Specific Registers

13.4.1 MEMTEST Implementation

Memory MBIST Enable Register i

The memory test register MEMTEST holds CPU configurable select bits for the various SSH instances. See the product specific appendix for mapping of memory controller numbers.

MTU_MEMTESTi (i=0)

Memory MBIST Enable Register i **(0010_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	RES30	RES29	RES28	RES27	RES26	RES25	RES24	RES23	RES22	RES21	RES20	RES19	RES18	RES17	RES16
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	RES14	RES13	RES12	RES11	RES10	CPU1_DLMU_STBY_EN	CPU1_PTAG_EN	CPU1_PMEM_EN	CPU1_DTAG_EN	CPU1_DMEM_EN	CPU0_DLMU_STBY_EN	CPU0_PTAG_EN	CPU0_PMEM_EN	CPU0_DTAG_EN	CPU0_DMEM_EN
r	r	r	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CPU0_DMEM_EN	0	rwh	**CPU0 DMEM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
RESx (x=10-31)	x	r	**Reserved** Reserved. Shall be written with zero.
CPU0_DTAG_EN	1	rwh	**CPU0 DTAG SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
CPU0_PMEM_EN	2	rwh	**CPU0 PMEM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
CPU0_PTAG_EN	3	rwh	**CPU0 PTAG SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
CPU0_DLMU_STBY_EN	4	rwh	**CPU0 STANDBY DLMU SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
CPU1_DMEM_EN	5	rwh	**CPU1 DMEM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
CPU1_DTAG_EN	6	rwh	**CPU1 DTAG SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
CPU1_PMEM_EN	7	rwh	**CPU1 PMEM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
CPU1_PTAG_EN	8	rwh	**CPU1 PTAG SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled

Field	Bits	Type	Description
CPU1_DLMU_STBY_EN	9	rwh	**CPU1 STANDBY DLMU SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled

MTU_MEMTESTi (i=1)
Memory MBIST Enable Register i **(0010_H+i*4)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	**MCAN10_EN**	**RES29**	**RES28**	**RES27**	**RES26**	**RES25**	**RES24**	**RES23**	**RES22**	**RES21**	**RES20**	**SPU_CONFIG0_EN**	**RES18**	**SPU_BUFFER0_EN**	**EMEM_XTM_EN**
r	rwh	r	r	r	r	r	r	r	r	r	r	rwh	r	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	**RES14**	**RES13**	**EMEM0_EN**	**MCDS_EN**	**RES10**	**SADMA_EN**	**R8**	**RES7**	**RES6**	**RES5**	**RES4**	**RES3**	**CPU0_DMEM1_EN**	**RES1**	**RES0**
r	r	r	rwh	rwh	r	rwh	rwh	r	r	r	r	r	rwh	r	r

Field	Bits	Type	Description
RESx (x=0-1,3-7,10,13-15,18,20-29,31)	x	r	**Reserved** Reserved. Shall be written with zero.
CPU0_DMEM1_EN	2	rwh	**CPU0 DMEM1 SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled [1].
R8	8	rwh	**Reserved - Res** Reserved. Not used in this product. Shall be written with zero.
SADMA_EN	9	rwh	**Safety DMA SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
MCDS_EN	11	rwh	**MCDS memory SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
EMEM0_EN	12	rwh	**EMEM0 SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
EMEM_XTM_EN	16	rwh	**EMEM XTM memory SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
SPU_BUFFER0_EN	17	rwh	**SPU BUFFER0 SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled

Field	Bits	Type	Description
SPU_CONFIG0_EN	19	rwh	**SPU CONFIG0 memory SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
MCAN10_EN	30	rwh	**MCAN10 memory SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled

1) Please refer to separate section related to handling of the large DMEM on this device.

MTU_MEMTESTi (i=2)

Memory MBIST Enable Register i **(0010_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	**SPU_FFT30_RAM_EN**	**RES29**	**SPU_FFT20_RAM_EN**	**RES27**	**SPU_FFT10_RAM_EN**	**RES25**	**SPU_FFT00_RAM_EN**	**RES23**	**RES22**	**HSPDM_RAM_EN**	**SDMMC_EN**	**GIGETH_TX_EN**	**GIGETH_RX_EN**	**RES17**	**RES16**
r	rwh	r	rwh	r	rwh	r	rwh	r	r	rwh	rwh	rwh	rwh	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	**SCR_RAMINT_EN**	**SCR_XRAM_EN**	**R12**	**R11**	**R10**	**R9**	**R8**	**RES7**	**RES6**	**RES5**	**RES4**	**RES3**	**RES2**	**RES1**	**RES0**
r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RESx (x=0-7,15-17,22-23,25,27,29,31)	x	r	**Reserved** Reserved. Shall be written with zero.
R8	8	rwh	**Reserved - Res** Reserved. Not used in this product. Shall be written with zero.
R9	9	rwh	**Reserved - Res** Reserved. Not used in this product. Shall be written with zero.
R10	10	rwh	**Reserved - Res** Reserved. Not used in this product. Shall be written with zero.
R11	11	rwh	**Reserved - Res** Reserved. Not used in this product. Shall be written with zero.
R12	12	rwh	**Reserved - Res** Reserved. Not used in this product. Shall be written with zero.

Field	Bits	Type	Description
SCR_XRAM_EN	13	rwh	**SCR XRAM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
SCR_RAMINT_EN	14	rwh	**SCR Internal RAM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
GIGETH_RX_EN	18	rwh	**Gigabit Ethernet RX SSH instance Enable** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
GIGETH_TX_EN	19	rwh	**Gigabit Ethernet TX SSH instance Enable** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SDMMC_EN	20	rwh	**SDMMC memory SSH instance Enable** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
HSPDM_RAM_EN	21	rwh	**HDSPDM RAM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
SPU_FFT00_RAM_EN	24	rwh	**SPU FFT00 RAM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
SPU_FFT10_RAM_EN	26	rwh	**SPU FFT10 RAM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
SPU_FFT20_RAM_EN	28	rwh	**SPU FFT20 RAM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled
SPU_FFT30_RAM_EN	30	rwh	**SPU FFT30 RAM SSH instance Enable** 0_B SSH instance is disabled 1_B SSH instance is enabled

13.4.2 MEMMAP Implementation

The Memory Mapping Enable register MEMMAP has configurable control bits to select memory-mapped test mode for each CPU memory.

Cache and Scratchpad memories are physically implemented as a single RAM, but this register function assumes two separate logical RAM partitions. In this register additional bits CPUxDCMAP and CPUxPCMAP are defined. These control the Cache partitions of the RAMs for Data Side and Program side respectively. Since cache content and tags of a cache must be simultaneously switched from memory mapped to cache functional mode, the control bits are mirrored and only one bit is writeable for each cache. The bits corresponding to the tag memories of the same cache will always take the same value as that written to the main Cache Memory control bit. This linkage is product specific.

Please note that the MEMMAP register is used only to map the Cache/Tag memories to system address space. These bits have no effect on testing these memories itself. For system address range into which the memories will be mapped, please refer to the memory map chapter.

Memory Mapping Enable Register

The Memory Mapping Enable register MEMMAP has configurable control bits to select memory-mapped test mode. See the Integration Section for mapping of memory controller numbers.

MTU_MEMMAP
Memory Mapping Enable Register **($001C_H$)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R29			MEM28MAP	MEM27MAP	MEM26MAP	MEM25MAP	R24	MEM23MAP	MEM22MAP	MEM21MAP	MEM20MAP	R19	MEM18MAP	MEM17MAP	MEM16MAP
r			r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MEM15MAP	R14	MEM13MAP	MEM12MAP	MEM11MAP	MEM10MAP	R9	CPU1_PTMAP	CPU1_PCMAP	CPU1_DTMAP	CPU1_DCMAP	R4	CPU0_PTMAP	CPU0_PCMAP	CPU0_DTMAP	CPU0_DCMAP
r	r	r	r	r	r	r	rh	rwh	rh	rwh	r	rh	rwh	rh	rwh

Field	Bits	Type	Description
CPU0_DCMAP	0	rwh	**CPU0 DCache Mapping** 0_B Normal cache function 1_B Memory-mapped
MEMxMAP (x=10-13,15-18,20-23,25-28)	x	r	**MEMx Mapping Enable** Reserved; Not used in this product. Shall be written with zero.
CPU0_DTMAP	1	rh	**CPU0 DTAG Mapping** Read only. Mirrors the state of CPU0_DCMAP. CPU D-cache memories may only be mapped simultaneously. 0_B Normal cache function 1_B Memory-mapped

Field	Bits	Type	Description
CPU0_PCMAP	2	rwh	**CPU0 PCACHE Mapping** 0_B Normal cache function 1_B Memory-mapped
CPU0_PTMAP	3	rh	**CPU0 PTAG Mapping** Read only. Mirrors the state of CPU0_PCMAP. CPU P-cache memories may only be mapped simultaneously. 0_B Normal cache function 1_B Memory-mapped
R4	4	r	**Reserved - Res** Reserved. Not used in this product.
CPU1_DCMAP	5	rwh	**CPU1 DCache Mapping** 0_B Normal cache function 1_B Memory-mapped
CPU1_DTMAP	6	rh	**CPU1 DTAG Mapping** Read only. Mirrors the state of CPU1_DCMAP. CPU D-cache memories may only be mapped simultaneously. 0_B Normal cache function 1_B Memory-mapped
CPU1_PCMAP	7	rwh	**CPU1 PCACHE Mapping** 0_B Normal cache function 1_B Memory-mapped
CPU1_PTMAP	8	rh	**CPU1 PTAG Mapping** Read only. Mirrors the state of CPU1_PCMAP. CPU P-cache memories may only be mapped simultaneously. 0_B Normal cache function 1_B Memory-mapped
R9	9	r	**Reserved - Res** Reserved. Not used in this product.
R14	14	r	**Reserved - Res** Reserved. Not used in this product.
R19	19	r	**Reserved - Res** Reserved. Not used in this product.
R24	24	r	**Reserved - Res** Reserved. Not used in this product.
R29	31:29	r	**Reserved - Res** Reserved. Not used in this product.

13.4.3 MEMSTAT Implementation

The Memory Status Registers MEMSTATx have an implemented bit for each security relevant RAM.

The Data- and Program- Cache and Scratchpad memories are physically implemented as a single RAM with a single MBIST. Hence CPUx_DMEM_AIU and CPUx_PMEM_AIU give the status of the partial initialization of the cache partitions for the Data and Program memories respectively.

Memory Status Register i

The memory status register MEMSTAT shows whether each SSH instance is currently executing an automatic initialization sequence.

MTU_MEMSTATi (i=0)
Memory Status Register i **(0038_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R29			RES28	RES27	RES26	RES25	R24	RES23	RES22	RES21	RES20	R19	RES18	RES17	RES16
	r		r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	R14	RES13	RES12	RES11	RES10	R9	CPU1_PTAG_AIU	CPU1_PMEM_AIU	CPU1_DTAG_AIU	CPU1_DMEM_AIU	R4	CPU0_PTAG_AIU	CPU0_PMEM_AIU	CPU0_DTAG_AIU	CPU0_DMEM_AIU
r	r	r	r	r	r	r	rh	rh	rh	rh	r	rh	rh	rh	rh

Field	Bits	Type	Description
CPU0_DMEM_AIU	0	rh	**CPU0 DMEM Partial AutoInitialize of Cache Partition Underway** This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0_B MBIST not running autoinitialize 1_B MBIST running autoinitialize
RESx (x=10-13,15-18,20-23,25-28)	x	r	**Reserved** Reserved. Not used in this product.
CPU0_DTAG_AIU	1	rh	**CPU0 DTAG MBIST AutoInitialize Underway** This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0_B MBIST not running autoinitialize 1_B MBIST running autoinitialize
CPU0_PMEM_AIU	2	rh	**CPU0 PMEM Partial AutoInitialize of Cache Partition Underway** This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0_B MBIST not running autoinitialize 1_B MBIST running autoinitialize

Field	Bits	Type	Description
CPU0_PTAG_AIU	3	rh	**CPU0 PTAG MBIST AutoInitialize Underway** This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0_B MBIST not running autoinitialize 1_B MBIST running autoinitialize
R4	4	r	**Reserved - Res** Reserved. Not used in this product.
CPU1_DMEM_AIU	5	rh	**CPU1 DMEM Partial AutoInitialize of Cache Partition Underway** This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0_B MBIST not running autoinitialize 1_B MBIST running autoinitialize
CPU1_DTAG_AIU	6	rh	**CPU1 DTAG MBIST AutoInitialize Underway** This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0_B MBIST not running autoinitialize 1_B MBIST running autoinitialize
CPU1_PMEM_AIU	7	rh	**CPU1 PMEM Partial AutoInitialize of Cache Partition Underway** This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0_B MBIST not running autoinitialize 1_B MBIST running autoinitialize
CPU1_PTAG_AIU	8	rh	**CPU1 PTAG MBIST AutoInitialize Underway** This bit indicates whether an automatic data initialization has been triggered by a change of state of MEMTEST.MEMxEN or MEMxMAP but that the intialization sequence has not yet completed. 0_B MBIST not running autoinitialize 1_B MBIST running autoinitialize
R9	9	r	**Reserved - Res** Reserved. Not used in this product.
R14	14	r	**Reserved - Res** Reserved. Not used in this product.
R19	19	r	**Reserved - Res** Reserved. Not used in this product.
R24	24	r	**Reserved - Res** Reserved. Not used in this product.
R29	31:29	r	**Reserved - Res** Reserved. Not used in this product.

MTU_MEMSTATi (i=1)

Memory Status Register i **(0038_H+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R9															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R9							R8	R5			R4	CPU1_DMEM1_AIU	CPU0_DMEM1_AIU	R0	
r							rh	r			r	rh	rh	r	

Field	Bits	Type	Description
R0	1:0	r	**Reserved - Res** Reserved. Not used in this product.
CPU0_DMEM1_AIU	2	rh	**CPU0 DMEM1 Partial AutoInitialize of Cache Partition Underway** 0_B SSH instance is disabled 1_B SSH instance is enabled [1].
CPU1_DMEM1_AIU	3	rh	**CPU1 DMEM1 Partial AutoInitialize of Cache Partition Underway** 0_B SSH instance is disabled 1_B SSH instance is enabled [2].
R4	4	r	**Reserved - Res** Reserved. Not used in this product.
R5	7:5	r	**Reserved - Res** Reserved. Not used in this product.
R8	8	rh	**Reserved - Res** Reserved. Not used in this product.
R9	31:9	r	**Reserved - Res** Reserved. Not used in this product.

1) Please refer to separate section related to handling of the large DMEM on this device.

2) Please refer to separate section related to handling of the large DMEM on this device.

MTU_MEMSTATi (i=2)

Memory Status Register i **(0038_H+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
R18														R17	R13
r														r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R13			R12	R11	R10	R9	R8	R5			R4	R2		R0	
r			rh	rh	rh	rh	rh	r			r	r		r	

Field	Bits	Type	Description
R0	1:0	r	**Reserved - Res** Reserved. Not used in this product.
R2	3:2	r	**Reserved - Res** Reserved. Not used in this product.
R4	4	r	**Reserved - Res** Reserved. Not used in this product.
R5	7:5	r	**Reserved - Res** Reserved. Not used in this product.
R8	8	rh	**Reserved - Res** Reserved. Not used in this product.
R9	9	rh	**Reserved - Res** Reserved. Not used in this product.
R10	10	rh	**Reserved - Res** Reserved. Not used in this product.
R11	11	rh	**Reserved - Res** Reserved. Not used in this product.
R12	12	rh	**Reserved - Res** Reserved. Not used in this product.
R13	16:13	r	**Reserved - Res** Reserved. Not used in this product.
R17	17	r	**Reserved - Res** Reserved. Not used in this product.
R18	31:18	r	**Reserved - Res** Reserved. Not used in this product.

13.4.4 MEMDONE Implementation

Memory Test Done Status Register i

Each bit in one of the memory test done status registers MEMDONEx reflects the status of the MSTATUS.DONE bit in the corresponding SSH. See the implementation section for the implemented register bits.

MTU_MEMDONEi (i=0)
Memory Test Done Status Register i **(0050_H+i*4)** **Application Reset Value: FFFF FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	**RES30**	**RES29**	**RES28**	**RES27**	**RES26**	**RES25**	**RES24**	**RES23**	**RES22**	**RES21**	**RES20**	**RES19**	**RES18**	**RES17**	**RES16**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	**RES14**	**RES13**	**RES12**	**RES11**	**RES10**	**CPU1_DLMU_STBY_DON**	**CPU1_PTAG_DONE**	**CPU1_PMEM_DONE**	**CPU1_DTAG_DONE**	**CPU1_DMEM_DONE**	**CPU0_DLMU_STBY_DON**	**CPU0_PTAG_DONE**	**CPU0_PMEM_DONE**	**CPU0_DTAG_DONE**	**CPU0_DMEM_DONE**
r	r	r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CPU0_DMEM_DONE	0	rh	**CPU0 DMEM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
RESz (z=10-31)	z	r	**Reserved** Reserved. Not used in this product.
CPU0_DTAG_DONE	1	rh	**CPU0 DTAG Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
CPU0_PMEM_DONE	2	rh	**CPU0 PMEM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
CPU0_PTAG_DONE	3	rh	**CPU0 PTAG Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
CPU0_DLMU_STBY_DONE	4	rh	**CPU0 STANDBY DLMU Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
CPU1_DMEM_DONE	5	rh	**CPU1 DMEM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
CPU1_DTAG_DONE	6	rh	**CPU1 DTAG Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
CPU1_PMEM_DONE	7	rh	**CPU1 PMEM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
CPU1_PTAG_DONE	8	rh	**CPU1 PTAG Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
CPU1_DLMU_STBY_DONE	9	rh	**CPU1 STANDBY DLMU Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1

MTU_MEMDONEi (i=1)

Memory Test Done Status Register i **(0050_H+i*4)** **Application Reset Value: FFFF FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	MCAN10_DONE	RES29	RES28	RES27	RES26	RES25	RES24	RES23	RES22	RES21	RES20	SPU_CONFIG0_DONE	RES18	SPU_BUFFER0_DONE	EMEM_XTM_DONE
r	rh	r	r	r	r	r	r	r	r	r	r	rh	r	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	RES14	RES13	EMEM0_DONE	MCDS_DONE	RES10	SADMA_DONE	R8	RES7	RES6	RES5	RES4	RES3	CPU0_DMEM1_DONE	RES1	RES0
r	r	r	rh	rh	r	rh	rh	r	r	r	r	r	rh	r	r

Field	Bits	Type	Description
RESz (z=0-1,3-7,10,13-15,18,20-29,31)	z	r	**Reserved** Reserved. Not used in this product.
CPU0_DMEM1_DONE	2	rh	**CPU0 DMEM1 Test Done Status** 0_B SSH instance is disabled 1_B SSH instance is enabled [1].
R8	8	rh	**Reserved - Res** Reserved. Not used in this product.
SADMA_DONE	9	rh	**Safety DMA Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
MCDS_DONE	11	rh	**MCDS memory Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
EMEM0_DONE	12	rh	**EMEM0 Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
EMEM_XTM_DONE	16	rh	**EMEM XTM memory Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SPU_BUFFER0_DONE	17	rh	**SPU BUFFER0 Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SPU_CONFIG0_DONE	19	rh	**SPU CONFIG0 memory Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1

Field	Bits	Type	Description
MCAN10_DONE	30	rh	**MCAN10 memory Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1

1) Please refer to separate section related to handling of the large DMEM on this device.

MTU_MEMDONEi (i=2)

Memory Test Done Status Register i **(0050_H+i*4)** **Application Reset Value: FFFF $FFFF_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	**SPU_FFT30_RAM_DONE**	**RES29**	**SPU_FFT20_RAM_DONE**	**RES27**	**SPU_FFT10_RAM_DONE**	**RES25**	**SPU_FFT00_RAM_DONE**	**RES23**	**RES22**	**HSPDM_RAM_DONE**	**SDMMC_DONE**	**GIGETH_TX_DONE**	**GIGETH_RX_DONE**	**RES17**	**RES16**
r	rh	r	rh	r	rh	r	rh	r	r	rh	rh	rh	rh	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	**SCR_RAMINT_DONE**	**SCR_XRAM_DONE**	**R12**	**R11**	**R10**	**R9**	**R8**	**RES7**	**RES6**	**RES5**	**RES4**	**RES3**	**RES2**	**RES1**	**RES0**
r	rh	rh	rh	rh	rh	rh	rh	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RESz (z=0-7,15-17,22-23,25,27,29,31)	z	r	**Reserved** Reserved. Not used in this product.
R8	8	rh	**Reserved - Res** Reserved. Not used in this product.
R9	9	rh	**Reserved - Res** Reserved. Not used in this product.
R10	10	rh	**Reserved - Res** Reserved. Not used in this product.
R11	11	rh	**Reserved - Res** Reserved. Not used in this product.
R12	12	rh	**Reserved - Res** Reserved. Not used in this product.
SCR_XRAM_DONE	13	rh	**SCR XRAM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SCR_RAMINT_DONE	14	rh	**SCR Internal RAM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
GIGETH_RX_DONE	18	rh	**Gigabit Ethernet RX memoryTest Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1

Field	Bits	Type	Description
GIGETH_TX_DONE	19	rh	**Gigabit Ethernet TX memoryTest Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SDMMC_DONE	20	rh	**SDMMC memoryTest Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
HSPDM_RAM_DONE	21	rh	**HDSPDM RAM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SPU_FFT00_RAM_DONE	24	rh	**SPU FFT00 RAM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SPU_FFT10_RAM_DONE	26	rh	**SPU FFT10 RAM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SPU_FFT20_RAM_DONE	28	rh	**SPU FFT20 RAM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SPU_FFT30_RAM_DONE	30	rh	**SPU FFT30 RAM Test Done Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1

13.4.5 MEMFDA Implementation

Memory Test FDA Status Register i

Each bit in one of the memory test done status registers MEMFDAx reflects the status of the MSTATUS.FDA bit in the corresponding SSH. See the implementation section for the implemented register bits.

MTU_MEMFDAi (i=0)
Memory Test FDA Status Register i **(0060_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	**RES30**	**RES29**	**RES28**	**RES27**	**RES26**	**RES25**	**RES24**	**RES23**	**RES22**	**RES21**	**RES20**	**RES19**	**RES18**	**RES17**	**RES16**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	**RES14**	**RES13**	**RES12**	**RES11**	**RES10**	**CPU1_DLMU_STBY_FDA**	**CPU1_PTAG_FDA**	**CPU1_PMEM_FDA**	**CPU1_DTAG_FDA**	**CPU1_DMEM_FDA**	**CPU0_DLMU_STBY_FDA**	**CPU0_PTAG_FDA**	**CPU0_PMEM_FDA**	**CPU0_DTAG_FDA**	**CPU0_DMEM_FDA**
r	r	r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CPU0_DMEM_FDA	0	rh	**CPU0 DMEM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1

Field	Bits	Type	Description
RESz (z=10-31)	z	r	**Reserved** Reserved. Not used in this product.
CPU0_DTAG_FDA	1	rh	**CPU0 DTAG Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
CPU0_PMEM_FDA	2	rh	**CPU0 PMEM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
CPU0_PTAG_FDA	3	rh	**CPU0 PTAG Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
CPU0_DLMU_STBY_FDA	4	rh	**CPU0 STANDBY DLMU Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
CPU1_DMEM_FDA	5	rh	**CPU1 DMEM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
CPU1_DTAG_FDA	6	rh	**CPU1 DTAG Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
CPU1_PMEM_FDA	7	rh	**CPU1 PMEM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
CPU1_PTAG_FDA	8	rh	**CPU1 PTAG Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
CPU1_DLMU_STBY_FDA	9	rh	**CPU1 STANDBY DLMU Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1

MTU_MEMFDAi (i=1)

Memory Test FDA Status Register i **(0060_H+i*4)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	**MCAN10_FDA**	**RES29**	**RES28**	**RES27**	**RES26**	**RES25**	**RES24**	**RES23**	**RES22**	**RES21**	**RES20**	**SPU_CONFIG0_FDA**	**RES18**	**SPU_BUFFER0_FDA**	**EMEM_XTM_FDA**
r	rh	r	r	r	r	r	r	r	r	r	r	rh	r	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	**RES14**	**RES13**	**EMEM0_FDA**	**MCDS_FDA**	**RES10**	**SADMA_FDA**	**R8**	**RES7**	**RES6**	**RES5**	**RES4**	**RES3**	**CPU0_DMEM1_FDA**	**RES1**	**RES0**
r	r	r	rh	rh	r	rh	rh	r	r	r	r	r	rh	r	r

Field	Bits	Type	Description
RESz (z=0-1,3-7,10,13-15,18,20-29,31)	z	r	**Reserved** Reserved. Not used in this product.
CPU0_DMEM1_FDA	2	rh	**CPU0 DMEM1 Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
R8	8	rh	**Reserved - Res** Reserved. Not used in this product.
SADMA_FDA	9	rh	**Safety DMA Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
MCDS_FDA	11	rh	**MCDS memory Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
EMEM0_FDA	12	rh	**EMEM0 Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
EMEM_XTM_FDA	16	rh	**EMEM XTM memory Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
SPU_BUFFER0_FDA	17	rh	**SPU BUFFER0 Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
SPU_CONFIG0_FDA	19	rh	**SPU CONFIG0 memory Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
MCAN10_FDA	30	rh	**MCAN10 memory Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1

MTU_MEMFDAi (i=2)

Memory Test FDA Status Register i **(0060_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES31	SPU_FFT30_RAM_FDA	RES29	SPU_FFT20_RAM_FDA	RES27	SPU_FFT10_RAM_FDA	RES25	SPU_FFT00_RAM_FDA	RES23	RES22	HSPDM_RAM_FDA	SDMMC_FDA	GIGETH_TX_FDA	GIGETH_RX_FDA	RES17	RES16
r	rh	r	rh	r	rh	r	rh	r	r	rh	rh	rh	rh	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES15	SCR_RAMINT_FDA	SCR_XRAM_FDA	R12	R11	R10	R9	R8	RES7	RES6	RES5	RES4	RES3	RES2	RES1	RES0
r	rh	rh	rh	rh	rh	rh	rh	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
RESz (z=0-7,15-17,22-23,25,27,29,31)	z	r	**Reserved** Reserved. Not used in this product.
R8	8	rh	**Reserved - Res** Reserved. Not used in this product.
R9	9	rh	**Reserved - Res** Reserved. Not used in this product.
R10	10	rh	**Reserved - Res** Reserved. Not used in this product.
R11	11	rh	**Reserved - Res** Reserved. Not used in this product.
R12	12	rh	**Reserved - Res** Reserved. Not used in this product.
SCR_XRAM_FDA	13	rh	**SCR XRAM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
SCR_RAMINT_FDA	14	rh	**SCR Internal RAM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
GIGETH_RX_FDA	18	rh	**Gigabit Ethernet RX memory Test FDA Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
GIGETH_TX_FDA	19	rh	**Gigabit Ethernet TX SSH memory Test FDA Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1
SDMMC_FDA	20	rh	**SDMMC memory SSH Test FDA Status** 0_B SSH MSTATUS.DONE = 0 1_B SSH MSTATUS.DONE = 1

Field	Bits	Type	Description
HSPDM_RAM_FDA	21	rh	**HDSPDM RAM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
SPU_FFT00_RAM_FDA	24	rh	**SPU FFT00 RAM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
SPU_FFT10_RAM_FDA	26	rh	**SPU FFT10 RAM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
SPU_FFT20_RAM_FDA	28	rh	**SPU FFT20 RAM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1
SPU_FFT30_RAM_FDA	30	rh	**SPU FFT30 RAM Test FDA Status** 0_B SSH MSTATUS.FDA = 0 1_B SSH MSTATUS.FDA = 1

13.5 SSH Instances

The system SRAMs do not all have the same configuration. **Table 53 "SSH instances" on Page 22** shows the instance-specific configurations of the SRAM Support Hardware.

The ECC values for all SRAMs are computed only out of the data information*.

The base address of an SSH instance MCx can be calculated from the MC_BASE (defined in the platform chapter) as: Base Address of SSH instance x (MCx) = MC_BASE + x*0x100

Table 53 SSH instances

(MCx) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
0	CPU0_DMEM	5	SECDED	2	16
1	CPU0_DTAG	5	SECDED	2	4
2	CPU0_PMEM	5	SECDED	2	8
3	CPU0_PTAG	5	DED	2	4
4	CPU0_DLMU_STBY	5	SECDED	2	8
5	CPU1_DMEM	5	SECDED	2	16
6	CPU1_DTAG	5	SECDED	2	4
7	CPU1_PMEM	5	SECDED	2	8
8	CPU1_PTAG	5	DED	2	4
9	CPU1_DLMU_STBY	5	SECDED	2	8
10	Reserved				
11	Reserved				
12	Reserved				
13	Reserved				
14	Reserved				
15	Reserved				
16	Reserved				
17	Reserved				
18	Reserved				
19	Reserved				
20	Reserved				
21	Reserved				
22	Reserved				
23	Reserved				
24	Reserved				
25	Reserved				
26	Reserved				
27	Reserved				
28	Reserved				
29	Reserved				

Table 53 SSH instances (cont'd)

(MCx) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
30	Reserved				
31	Reserved				
32	Reserved				
33	Reserved				
34	CPU0_DMEM1	5	SECDED	2	16
35	Reserved				
36-37	Reserved				
38	Reserved				
39	Reserved				
41	SADMA	5	SECDED	1	4
42	Reserved				
43	MCDS	5	DED	1	4
44	EMEM	5	SECDED	1	8
45	Reserved				
46	Reserved				
47	Reserved				
48	EMEM_XTM	5	SECDED	1	4
49	SPU_Buffer	5	SECDED	1	4
50	Reserved				
51	SPU_Config	5	SECDED	2	8
52	Reserved				
53	Reserved				
54	Reserved				
55	Reserved				
56	Reserved				
57	Reserved				
58	Reserved				
59	Reserved				
60	Reserved				
61	Reserved				
62	MCAN10	5	SECDED	1	16
63	Reserved				
64	Reserved				
65	Reserved				
66	Reserved				
67	Reserved				
68	Reserved				

Table 53 SSH instances (cont'd)

(MCx) x =	Module	Error Addr Buffer (ETRR) Depth	ECC type	ECC granularity	Mux Factor
69	Reserved				
70	Reserved				
71	Reserved				
77	SCR_XRAM	5	SECDED	2	8
78	SCR_RAMINT	5	SECDED	1	4
79	Reserved				
80	Reserved				
81	Reserved				
82	GIGETH_RX_RAM	5	SECDED	1	4
83	GIGETH_TX_RAM	5	SECDED	1	4
84	SDMMC	5	SECDED	1	4
85	HSPDM	5	SECDED	1	8
86- 87	Reserved				
88	SPU_FFT0	5	SECDED	1	4
89	Reserved				
90	SPU_FFT1	5	SECDED	1	4
91	Reserved				
92	SPU_FFT2	5	SECDED	1	4
93	Reserved				
94	SPU_FFT3	5	SECDED	1	4
95	Reserved				

13.5.1 Ganging for SRAM test and initialization

Whenever an MBIST test or SRAM initialization is started via the MTU/SSH, there is a certain jump in the current consumption, due to the parallel accesses to the SRAM cells during the test or initialization. This current jump is different for the different SRAMs in the product, and depends on the size of the SRAM, the clock frequency e.t.c.

If too many SRAMs are tested or initialized in parallel, it may result in a significant current jump, which may put the device outside of the specified operating conditions. On the other hand, in order to reduce the overall test and/or initialization time, it may be imperative for the application to perform the test or initialization of many SRAMs in parallel.

In order to achieve this trade-off between current jump and test/initialization time - it is advised to partition the available SRAMs into different “Gangs”. This is referred to as Ganging. The SRAMs in each Gang are all initialized/tested in parallel - while the Gangs themselves are executed in sequence, one after the other. This ensures that the current jump never exceeds the allowed limits, while at the same time the overall test time is minimized.

Gangs 0-16 are defined for the platform. Depending on the device and the number of implemented SRAMs, the number of gangs needed may be less. The numbering of the gangs is not important and does not signify any order.

In the below ganging tables, a ganging configuration for this product is shown. This assumes a 4-march element (4N) non-destructive test (r,w*,r*,w) on a zero-data background (i.e. the SRAM is cleared with ECC-correct zero data). The same gangs may be used for SRAM initialization.

The provided ganging example is ensured to satisfy the specified limitations in current jumps of this device, while at the same time optimizing the overall test time. All implemented SRAMs are considered here. If certain SRAMs are not of interest to a particular application, then the gangs may be modified appropriately.

Table 54 GANG-0

MCx(x=)	Module / SRAM
43	MCDS
44	EMEM0
51	SPU_CONFIG0
62	MCAN10
77	SCR_XRAM
78	SCR_RAMINT
82	GIGETH_RX
83	GIGETH_TX
84	SDMMC_RAM
85	HSPDM_RAM

Table 55 GANG-1

MCx(x=)	Module / SRAM
00	CPU0_DMEM
05	CPU1_DMEM
09	CPU1_DLMU_STBY
34	CPU0_DMEM1

Table 56 GANG-2

MCx(x=)	Module / SRAM
02	CPU0_PMEM
03	CPU0_PTAG
04	CPU0_DLMU_STBY
06	CPU1_DTAG
07	CPU1_PMEM
08	CPU1_PTAG
48	EMEM_XTM
49	SPU_BUFFER0
88	SPU_FFT00

Table 57 GANG-3

MCx(x=)	Module / SRAM
01	CPU0_DTAG
41	SADMA
90	SPU_FFT10
92	SPU_FFT20
94	SPU_FFT30

13.6 Connectivity

Table 58 Connections of MTU

Interface Signals	connects		Description
MTU:CPU0DCMAP	to	cpu_pfi_pfrwb_0:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU1DCMAP	to	cpu_1:tc162p_dcache_map	CPU dcache mapped indicator per cpu
MTU:CPU0PCMAP	to	cpu_pfi_pfrwb_0:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:CPU1PCMAP	to	cpu_1:tc162p_pcache_map	CPU pcache mapped indicator per cpu
MTU:dmu_no_ram_init	from	DMU:MTU_NO_RAMIN	Disable RAM auto-initialization
MTU:scu_hsm_dbg	from	SCU:scu_hsm_dbg	HSM debug enable from SCU
MTU:sleep_n	from	SCU:scu_syst_sleep_n	Sleep request
MTU:DONE_INT	to	INT:mtu.DONE_INT	MTU Done Service Request
MTU:tcu_hsm_dbg_analysis_en	from	TCU:hsm_debug_mode	HSM debug request from TCU

13.7 Revision History

Table 59 Revision History

Reference	Change to Previous Version	Comment
V7.4.7		
	Initial version for TC33X.	
V7.4.8		
Page 27	Revision History entries up to V7.4.7 removed.	
Page 8	MEMMAP Reserved (not implemented) bits changed to “read”.	
	Settings for bitfield CPU1_DMEM1 corrected in MEMTEST, MEMSTAT, MEMDONE and MEMFDA registers.	
Page 25	Ganging information: Typo for CPU0_DMEM1 corrected.	
Page 3, **Page 13**, **Page 17**	"SADMA" changed to "Safety DMA" in short description of MEMTEST1/9, MEMDONE1/9 and MEMFDA1/9 bit fields.	
V7.4.9		
Page 25	Unhide for external audience: MCAN10.	
Page 25	Unhide for external audience: CPU1_DLMU_STBY.	
Page 26	Unhide for external audience: CPU0_PTAG, CPU1_DTAG, CPU1_PTAG, SPU_FFT00.	
Page 26	Unhide for external audience: CPU0_DTAG, SPU_FFT10, SPU_FFT20, SPU_FFT30.	
V7.4.10		
Page 3, **Page 13**, **Page 17**	Updated registers MEMTEST1, MEMDONE1, MEMFDA1.	
V7.4.11		
-	No functional changes.	
V7.4.12		
-	No functional changes.	
V7.4.13		
Page 10	Wrongly mentioned bit field in MTU_MEMSTATi (i=2) fixed.	

14 General Purpose I/O Ports and Peripheral I/O Lines (Ports)

This chapter supplements the family documentation with device specific information for TC33xEXT.

14.1 TC33xEXT Specific IP Configuration

The Ports configuration (which Port modules are implemented, their width and functionality) is represented by the device specific register set shown in this chapter.

14.2 TC33xEXT Specific Register Set

Table 60 Register Address Space - Pn

Module	Base Address	End Address	Note
P00	$F003A000_H$	$F003A0FF_H$	SPB bus slave interface
P02	$F003A200_H$	$F003A2FF_H$	SPB bus slave interface
P10	$F003AA00_H$	$F003AAFF_H$	SPB bus slave interface
P11	$F003AB00_H$	$F003ABFF_H$	SPB bus slave interface
P12	$F003AC00_H$	$F003ACFF_H$	SPB bus slave interface
P14	$F003AE00_H$	$F003AEFF_H$	SPB bus slave interface
P15	$F003AF00_H$	$F003AFFF_H$	SPB bus slave interface
P20	$F003B400_H$	$F003B4FF_H$	SPB bus slave interface
P21	$F003B500_H$	$F003B5FF_H$	SPB bus slave interface
P22	$F003B600_H$	$F003B6FF_H$	SPB bus slave interface
P23	$F003B700_H$	$F003B7FF_H$	SPB bus slave interface
P32	$F003C000_H$	$F003C0FF_H$	SPB bus slave interface
P33	$F003C100_H$	$F003C1FF_H$	SPB bus slave interface
P34	$F003C200_H$	$F003C2FF_H$	SPB bus slave interface

Register Overview Tables of Pn

Table 61 Register Overview - P00 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P00_OUT	Port 00 Output Register	000_H	U,SV	U,SV,P	Application Reset	23
P00_OMR	Port 00 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	26
P00_ID	Port 00 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P00_IOCR0	Port 00 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P00_IOCR4	Port 00 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36

Table 61 Register Overview - P00 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P00_IOCR8	Port 00 Input/Output Control Register 8	018_H	U,SV	U,SV,P	See page 39	39
P00_IOCR12	Port 00 Input/Output Control Register 12	$01C_H$	U,SV	U,SV,P	See page 41	41
	Reserved (004_H Byte)	020_H	BE	BE		
P00_IN	Port 00 Input Register	024_H	U,SV	BE	Application Reset	42
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P00_PDR0	Port 00 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
P00_PDR1	Port 00 Pad Driver Mode Register 1	044_H	U,SV	SV,E,P	See page 50	50
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		
P00_ESR	Port 00 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	52
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P00_PDISC	Port 00 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 58	58
P00_PCSR	Port 00 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	63
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P00_OMSR0	Port 00 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P00_OMSR4	Port 00 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P00_OMSR8	Port 00 Output Modification Set Register 8	078_H	U,SV	U,SV,P	Application Reset	74
P00_OMSR12	Port 00 Output Modification Set Register 12	$07C_H$	U,SV	U,SV,P	Application Reset	75
P00_OMCR0	Port 00 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P00_OMCR4	Port 00 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P00_OMCR8	Port 00 Output Modification Clear Register 8	088_H	U,SV	U,SV,P	Application Reset	81
P00_OMCR12	Port 00 Output Modification Clear Register 12	$08C_H$	U,SV	U,SV,P	Application Reset	82

Table 61 Register Overview - P00 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P00_OMSR	Port 00 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	83
P00_OMCR	Port 00 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	86
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P00_ACCEN1	Port 00 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P00_ACCEN0	Port 00 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 62 Register Overview - P02 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P02_OUT	Port 02 Output Register	000_H	U,SV	U,SV,P	Application Reset	24
P02_OMR	Port 02 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	28
P02_ID	Port 02 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P02_IOCR0	Port 02 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P02_IOCR4	Port 02 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
P02_IOCR8	Port 02 Input/Output Control Register 8	018_H	U,SV	U,SV,P	See page 39	39
	Reserved (004_H Byte)	020_H	BE	BE		
P02_IN	Port 02 Input Register	024_H	U,SV	BE	Application Reset	43
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P02_PDR0	Port 02 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
P02_PDR1	Port 02 Pad Driver Mode Register 1	044_H	U,SV	SV,E,P	See page 51	51
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		

Table 62 Register Overview - P02 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P02_ESR	Port 02 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	54
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P02_PDISC	Port 02 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 60	60
P02_PCSR	Port 02 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	64
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P02_OMSR0	Port 02 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P02_OMSR4	Port 02 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P02_OMSR8	Port 02 Output Modification Set Register 8	078_H	U,SV	U,SV,P	Application Reset	74
P02_OMCR0	Port 02 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P02_OMCR4	Port 02 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P02_OMCR8	Port 02 Output Modification Clear Register 8	088_H	U,SV	U,SV,P	Application Reset	81
P02_OMSR	Port 02 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	84
P02_OMCR	Port 02 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	88
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P02_ACCEN1	Port 02 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P02_ACCEN0	Port 02 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 63 Register Overview - P10 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P10_OUT	Port 10 Output Register	000_H	U,SV	U,SV,P	Application Reset	24
P10_OMR	Port 10 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	28
P10_ID	Port 10 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P10_IOCR0	Port 10 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P10_IOCR4	Port 10 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
P10_IOCR8	Port 10 Input/Output Control Register 8	018_H	U,SV	U,SV,P	See page 39	39
	Reserved (004_H Byte)	020_H	BE	BE		
P10_IN	Port 10 Input Register	024_H	U,SV	BE	Application Reset	43
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P10_PDR0	Port 10 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
P10_PDR1	Port 10 Pad Driver Mode Register 1	044_H	U,SV	SV,E,P	See page 51	51
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		
P10_ESR	Port 10 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	54
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P10_PDISC	Port 10 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 60	60
P10_PCSR	Port 10 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	64
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P10_OMSR0	Port 10 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P10_OMSR4	Port 10 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P10_OMSR8	Port 10 Output Modification Set Register 8	078_H	U,SV	U,SV,P	Application Reset	74

Table 63 Register Overview - P10 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P10_OMCR0	Port 10 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P10_OMCR4	Port 10 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P10_OMCR8	Port 10 Output Modification Clear Register 8	088_H	U,SV	U,SV,P	Application Reset	81
P10_OMSR	Port 10 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	84
P10_OMCR	Port 10 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	88
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P10_ACCEN1	Port 10 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P10_ACCEN0	Port 10 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 64 Register Overview - P11 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P11_OUT	Port 11 Output Register	000_H	U,SV	U,SV,P	Application Reset	23
P11_OMR	Port 11 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	26
P11_ID	Port 11 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P11_IOCR0	Port 11 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P11_IOCR4	Port 11 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
P11_IOCR8	Port 11 Input/Output Control Register 8	018_H	U,SV	U,SV,P	See page 39	39
P11_IOCR12	Port 11 Input/Output Control Register 12	$01C_H$	U,SV	U,SV,P	See page 41	41
	Reserved (004_H Byte)	020_H	BE	BE		
P11_IN	Port 11 Input Register	024_H	U,SV	BE	Application Reset	42

Table 64 Register Overview - P11 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P11_PDR0	Port 11 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
P11_PDR1	Port 11 Pad Driver Mode Register 1	044_H	U,SV	SV,E,P	See page 50	50
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		
P11_ESR	Port 11 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	52
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P11_PDISC	Port 11 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 58	58
P11_PCSR	Port 11 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	65
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P11_OMSR0	Port 11 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P11_OMSR4	Port 11 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P11_OMSR8	Port 11 Output Modification Set Register 8	078_H	U,SV	U,SV,P	Application Reset	74
P11_OMSR12	Port 11 Output Modification Set Register 12	$07C_H$	U,SV	U,SV,P	Application Reset	75
P11_OMCR0	Port 11 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P11_OMCR4	Port 11 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P11_OMCR8	Port 11 Output Modification Clear Register 8	088_H	U,SV	U,SV,P	Application Reset	81
P11_OMCR12	Port 11 Output Modification Clear Register 12	$08C_H$	U,SV	U,SV,P	Application Reset	82
P11_OMSR	Port 11 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	83
P11_OMCR	Port 11 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	86
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		

Table 64 Register Overview - P11 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x*4	BE	BE		
P11_ACCEN1	Port 11 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P11_ACCEN0	Port 11 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 65 Register Overview - P12 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P12_OUT	Port 12 Output Register	000_H	U,SV	U,SV,P	Application Reset	25
P12_OMR	Port 12 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	29
P12_ID	Port 12 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P12_IOCR0	Port 12 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
	Reserved (004_H Byte)	020_H	BE	BE		
P12_IN	Port 12 Input Register	024_H	U,SV	BE	Application Reset	44
	Reserved (004_H Byte) (x=0-5)	028_H+x*4	BE	BE		
P12_PDR0	Port 12 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 49	49
	Reserved (004_H Byte) (x=0-1)	048_H+x*4	BE	BE		
P12_ESR	Port 12 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	55
	Reserved (004_H Byte) (x=0-2)	054_H+x*4	BE	BE		
P12_PDISC	Port 12 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 61	61
P12_PCSR	Port 12 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	66
	Reserved (004_H Byte) (x=0-1)	068_H+x*4	BE	BE		
P12_OMSR0	Port 12 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69

Table 65 Register Overview - P12 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P12_OMCR0	Port 12 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P12_OMSR	Port 12 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	85
P12_OMCR	Port 12 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	89
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P12_ACCEN1	Port 12 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P12_ACCEN0	Port 12 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 66 Register Overview - P14 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P14_OUT	Port 14 Output Register	000_H	U,SV	U,SV,P	Application Reset	24
P14_OMR	Port 14 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	28
P14_ID	Port 14 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P14_IOCR0	Port 14 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P14_IOCR4	Port 14 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
P14_IOCR8	Port 14 Input/Output Control Register 8	018_H	U,SV	U,SV,P	See page 39	39
	Reserved (004_H Byte)	020_H	BE	BE		
P14_IN	Port 14 Input Register	024_H	U,SV	BE	Application Reset	43
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P14_PDR0	Port 14 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
P14_PDR1	Port 14 Pad Driver Mode Register 1	044_H	U,SV	SV,E,P	See page 51	51

Table 66 Register Overview - P14 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004_H Byte) (x=0-1)	048_H+x*4	BE	BE		
P14_ESR	Port 14 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	54
	Reserved (004_H Byte) (x=0-2)	054_H+x*4	BE	BE		
P14_PDISC	Port 14 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 60	60
P14_PCSR	Port 14 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	64
	Reserved (004_H Byte) (x=0-1)	068_H+x*4	BE	BE		
P14_OMSR0	Port 14 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P14_OMSR4	Port 14 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P14_OMSR8	Port 14 Output Modification Set Register 8	078_H	U,SV	U,SV,P	Application Reset	74
P14_OMCR0	Port 14 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P14_OMCR4	Port 14 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P14_OMCR8	Port 14 Output Modification Clear Register 8	088_H	U,SV	U,SV,P	Application Reset	81
P14_OMSR	Port 14 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	84
P14_OMCR	Port 14 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	88
	Reserved (004_H Byte) (x=0-1)	098_H+x*4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x*4	BE	BE		
P14_ACCEN1	Port 14 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P14_ACCEN0	Port 14 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 67 Register Overview - P15 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P15_OUT	Port 15 Output Register	000_H	U,SV	U,SV,P	Application Reset	24
P15_OMR	Port 15 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	28
P15_ID	Port 15 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P15_IOCR0	Port 15 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P15_IOCR4	Port 15 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
P15_IOCR8	Port 15 Input/Output Control Register 8	018_H	U,SV	U,SV,P	See page 39	39
	Reserved (004_H Byte)	020_H	BE	BE		
P15_IN	Port 15 Input Register	024_H	U,SV	BE	Application Reset	43
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P15_PDR0	Port 15 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
P15_PDR1	Port 15 Pad Driver Mode Register 1	044_H	U,SV	SV,E,P	See page 51	51
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		
P15_ESR	Port 15 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	54
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P15_PDISC	Port 15 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 60	60
P15_PCSR	Port 15 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	64
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P15_OMSR0	Port 15 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P15_OMSR4	Port 15 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P15_OMSR8	Port 15 Output Modification Set Register 8	078_H	U,SV	U,SV,P	Application Reset	74

Table 67 Register Overview - P15 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P15_OMCR0	Port 15 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P15_OMCR4	Port 15 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P15_OMCR8	Port 15 Output Modification Clear Register 8	088_H	U,SV	U,SV,P	Application Reset	81
P15_OMSR	Port 15 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	84
P15_OMCR	Port 15 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	88
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P15_ACCEN1	Port 15 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P15_ACCEN0	Port 15 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 68 Register Overview - P20 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P20_OUT	Port 20 Output Register	000_H	U,SV	U,SV,P	Application Reset	23
P20_OMR	Port 20 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	26
P20_ID	Port 20 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P20_IOCR0	Port 20 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P20_IOCR4	Port 20 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
P20_IOCR8	Port 20 Input/Output Control Register 8	018_H	U,SV	U,SV,P	See page 39	39
P20_IOCR12	Port 20 Input/Output Control Register 12	$01C_H$	U,SV	U,SV,P	See page 41	41
	Reserved (004_H Byte)	020_H	BE	BE		
P20_IN	Port 20 Input Register	024_H	U,SV	BE	Application Reset	42

Table 68 Register Overview - P20 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004_H Byte) (x=0-5)	028_H+x*4	BE	BE		
P20_PDR0	Port 20 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
P20_PDR1	Port 20 Pad Driver Mode Register 1	044_H	U,SV	SV,E,P	See page 50	50
	Reserved (004_H Byte) (x=0-1)	048_H+x*4	BE	BE		
P20_ESR	Port 20 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	52
	Reserved (004_H Byte) (x=0-2)	054_H+x*4	BE	BE		
P20_PDISC	Port 20 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 58	58
P20_PCSR	Port 20 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	63
	Reserved (004_H Byte) (x=0-1)	068_H+x*4	BE	BE		
P20_OMSR0	Port 20 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P20_OMSR4	Port 20 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P20_OMSR8	Port 20 Output Modification Set Register 8	078_H	U,SV	U,SV,P	Application Reset	74
P20_OMSR12	Port 20 Output Modification Set Register 12	$07C_H$	U,SV	U,SV,P	Application Reset	75
P20_OMCR0	Port 20 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P20_OMCR4	Port 20 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P20_OMCR8	Port 20 Output Modification Clear Register 8	088_H	U,SV	U,SV,P	Application Reset	81
P20_OMCR12	Port 20 Output Modification Clear Register 12	$08C_H$	U,SV	U,SV,P	Application Reset	82
P20_OMSR	Port 20 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	83
P20_OMCR	Port 20 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	86
	Reserved (004_H Byte) (x=0-1)	098_H+x*4	BE	BE		

Table 68 Register Overview - P20 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x*4	BE	BE		
P20_ACCEN1	Port 20 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P20_ACCEN0	Port 20 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 69 Register Overview - P21 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P21_OUT	Port 21 Output Register	000_H	U,SV	U,SV,P	Application Reset	26
P21_OMR	Port 21 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	30
P21_ID	Port 21 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P21_IOCR0	Port 21 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P21_IOCR4	Port 21 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
	Reserved (004_H Byte)	020_H	BE	BE		
P21_IN	Port 21 Input Register	024_H	U,SV	BE	Application Reset	44
	Reserved (004_H Byte) (x=0-5)	028_H+x*4	BE	BE		
P21_PDR0	Port 21 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
	Reserved (004_H Byte) (x=0-1)	048_H+x*4	BE	BE		
P21_ESR	Port 21 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	56
	Reserved (004_H Byte) (x=0-2)	054_H+x*4	BE	BE		
P21_PDISC	Port 21 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 62	62
P21_PCSR	Port 21 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	67
	Reserved (004_H Byte) (x=0-1)	068_H+x*4	BE	BE		

Table 69 Register Overview - P21 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P21_OMSR0	Port 21 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P21_OMSR4	Port 21 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P21_OMCR0	Port 21 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P21_OMCR4	Port 21 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P21_OMSR	Port 21 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	86
P21_OMCR	Port 21 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	90
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
P21_LPCRx	Port 21 LVDS Pad Control Register x	$0A0_H$+x* 4	U,SV	SV,E,P	See page 90	90
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P21_ACCEN1	Port 21 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P21_ACCEN0	Port 21 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 70 Register Overview - P22 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P22_OUT	Port 22 Output Register	000_H	U,SV	U,SV,P	Application Reset	26
P22_OMR	Port 22 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	30
P22_ID	Port 22 Identification Register	008_H	U,SV	BE	Application Reset	31
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P22_IOCR0	Port 22 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 32	32
P22_IOCR4	Port 22 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
	Reserved (004_H Byte)	020_H	BE	BE		
P22_IN	Port 22 Input Register	024_H	U,SV	BE	Application Reset	44

Table 70 Register Overview - P22 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
	Reserved (004_H Byte) (x=0-5)	028_H+x*4	BE	BE		
P22_PDR0	Port 22 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
	Reserved (004_H Byte) (x=0-1)	048_H+x*4	BE	BE		
P22_ESR	Port 22 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	57
	Reserved (004_H Byte) (x=0-2)	054_H+x*4	BE	BE		
P22_PDISC	Port 22 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 62	62
P22_PCSR	Port 22 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	67
	Reserved (004_H Byte) (x=0-1)	068_H+x*4	BE	BE		
P22_OMSR0	Port 22 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	69
P22_OMSR4	Port 22 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P22_OMCR0	Port 22 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	76
P22_OMCR4	Port 22 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P22_OMSR	Port 22 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	86
P22_OMCR	Port 22 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	90
	Reserved (004_H Byte) (x=0-1)	098_H+x*4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x*4	BE	BE		
P22_ACCEN1	Port 22 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	92
P22_ACCEN0	Port 22 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	94

Table 71 Register Overview - P23 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P23_OUT	Port 23 Output Register	000_H	U,SV	U,SV,P	Application Reset	26
P23_OMR	Port 23 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	30
P23_ID	Port 23 Identification Register	008_H	U,SV	BE	Application Reset	32
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P23_IOCR0	Port 23 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 35	35
P23_IOCR4	Port 23 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 36	36
	Reserved (004_H Byte)	020_H	BE	BE		
P23_IN	Port 23 Input Register	024_H	U,SV	BE	Application Reset	44
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P23_PDR0	Port 23 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 45	45
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		
P23_ESR	Port 23 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	57
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P23_PDISC	Port 23 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 62	62
P23_PCSR	Port 23 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	67
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P23_OMSR0	Port 23 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	71
P23_OMSR4	Port 23 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	72
P23_OMCR0	Port 23 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	77
P23_OMCR4	Port 23 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	78
P23_OMSR	Port 23 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	86

Table 71 Register Overview - P23 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P23_OMCR	Port 23 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	90
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P23_ACCEN1	Port 23 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	93
P23_ACCEN0	Port 23 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	96

Table 72 Register Overview - P32 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P32_OUT	Port 32 Output Register	000_H	U,SV	U,SV,P	Application Reset	26
P32_OMR	Port 32 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	30
P32_ID	Port 32 Identification Register	008_H	U,SV	BE	Application Reset	32
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P32_IOCR0	Port 32 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 35	35
P32_IOCR4	Port 32 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 38	38
	Reserved (004_H Byte)	020_H	BE	BE		
P32_IN	Port 32 Input Register	024_H	U,SV	BE	Application Reset	44
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P32_PDR0	Port 32 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 48	48
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		
P32_ESR	Port 32 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	57
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P32_PDISC	Port 32 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 62	62

Table 72 Register Overview - P32 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P32_PCSR	Port 32 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	67
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P32_OMSR0	Port 32 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	71
P32_OMSR4	Port 32 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	73
P32_OMCR0	Port 32 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	77
P32_OMCR4	Port 32 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	80
P32_OMSR	Port 32 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	86
P32_OMCR	Port 32 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	90
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P32_ACCEN1	Port 32 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	93
P32_ACCEN0	Port 32 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	96

Table 73 Register Overview - P33 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P33_OUT	Port 33 Output Register	000_H	U,SV	U,SV,P	Application Reset	23
P33_OMR	Port 33 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	26
P33_ID	Port 33 Identification Register	008_H	U,SV	BE	Application Reset	32
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P33_IOCR0	Port 33 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 35	35
P33_IOCR4	Port 33 Input/Output Control Register 4	014_H	U,SV	U,SV,P	See page 38	38

Table 73 Register Overview - P33 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P33_IOCR8	Port 33 Input/Output Control Register 8	018_H	U,SV	U,SV,P	See page 39	39
P33_IOCR12	Port 33 Input/Output Control Register 12	$01C_H$	U,SV	U,SV,P	See page 41	41
	Reserved (004_H Byte)	020_H	BE	BE		
P33_IN	Port 33 Input Register	024_H	U,SV	BE	Application Reset	42
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P33_PDR0	Port 33 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 48	48
P33_PDR1	Port 33 Pad Driver Mode Register 1	044_H	U,SV	SV,E,P	See page 50	50
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		
P33_ESR	Port 33 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	58
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P33_PDISC	Port 33 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 58	58
P33_PCSR	Port 33 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	68
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P33_OMSR0	Port 33 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	71
P33_OMSR4	Port 33 Output Modification Set Register 4	074_H	U,SV	U,SV,P	Application Reset	73
P33_OMSR8	Port 33 Output Modification Set Register 8	078_H	U,SV	U,SV,P	Application Reset	74
P33_OMSR12	Port 33 Output Modification Set Register 12	$07C_H$	U,SV	U,SV,P	Application Reset	75
P33_OMCR0	Port 33 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	77
P33_OMCR4	Port 33 Output Modification Clear Register 4	084_H	U,SV	U,SV,P	Application Reset	80
P33_OMCR8	Port 33 Output Modification Clear Register 8	088_H	U,SV	U,SV,P	Application Reset	81
P33_OMCR12	Port 33 Output Modification Clear Register 12	$08C_H$	U,SV	U,SV,P	Application Reset	82

Table 73 Register Overview - P33 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P33_OMSR	Port 33 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	83
P33_OMCR	Port 33 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	86
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P33_ACCEN1	Port 33 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	93
P33_ACCEN0	Port 33 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	96

Table 74 Register Overview - P34 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P34_OUT	Port 34 Output Register	000_H	U,SV	U,SV,P	Application Reset	25
P34_OMR	Port 34 Output Modification Register	004_H	U,SV	U,SV,P	Application Reset	29
P34_ID	Port 34 Identification Register	008_H	U,SV	BE	Application Reset	32
	Reserved (004_H Byte)	$00C_H$	BE	BE		
P34_IOCR0	Port 34 Input/Output Control Register 0	010_H	U,SV	U,SV,P	See page 35	35
	Reserved (004_H Byte)	020_H	BE	BE		
P34_IN	Port 34 Input Register	024_H	U,SV	BE	Application Reset	44
	Reserved (004_H Byte) (x=0-5)	028_H+x* 4	BE	BE		
P34_PDR0	Port 34 Pad Driver Mode Register 0	040_H	U,SV	SV,E,P	See page 49	49
	Reserved (004_H Byte) (x=0-1)	048_H+x* 4	BE	BE		
P34_ESR	Port 34 Emergency Stop Register	050_H	U,SV	SV,E,P	Application Reset	55
	Reserved (004_H Byte) (x=0-2)	054_H+x* 4	BE	BE		
P34_PDISC	Port 34 Pin Function Decision Control Register	060_H	U,SV	SV,E,P	See page 61	61

Table 74 Register Overview - P34 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
P34_PCSR	Port 34 Pin Controller Select Register	064_H	U,SV	SV,SE	Application Reset	69
	Reserved (004_H Byte) (x=0-1)	068_H+x* 4	BE	BE		
P34_OMSR0	Port 34 Output Modification Set Register 0	070_H	U,SV	U,SV,P	Application Reset	71
P34_OMCR0	Port 34 Output Modification Clear Register 0	080_H	U,SV	U,SV,P	Application Reset	77
P34_OMSR	Port 34 Output Modification Set Register	090_H	U,SV	U,SV,P	Application Reset	85
P34_OMCR	Port 34 Output Modification Clear Register	094_H	U,SV	U,SV,P	Application Reset	89
	Reserved (004_H Byte) (x=0-1)	098_H+x* 4	BE	BE		
	Reserved (004_H Byte) (x=0-13)	$0C0_H$+x* 4	BE	BE		
P34_ACCEN1	Port 34 Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	93
P34_ACCEN0	Port 34 Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	96

14.3 Pn Registers

14.3.1 SPB bus slave interface

Port 00 Output Register

The port output register determines the value of a GPIO pin when it is selected by Pn_IOCRx as output. Writing a 0 to a Pn_OUT.Px (x = 0-15) bit position delivers a low level at the corresponding output pin. A high level is output when the corresponding bit is written with a 1. Note that the bits of Pn_OUT.Px can be individually set or cleared by writing appropriate values into the port output modification set register Pn_OMSR or port output modification clear register Pn_OMCR, respectively. The Pn_OUT.Px bits can also be set, cleared or toggled with register Pn_OMR within the same write operation.

P00_OUT
Port 00 Output Register **(000_H)** **Application Reset Value: 0000 0000_H**
P11_OUT
Port 11 Output Register **(000_H)** **Application Reset Value: 0000 0000_H**
P20_OUT
Port 20 Output Register **(000_H)** **Application Reset Value: 0000 0000_H**
P33_OUT
Port 33 Output Register **(000_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	**P14**	**P13**	**P12**	**P11**	**P10**	**P9**	**P8**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x=0-15)	x	rwh	**Output Bit x** This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0_B The output level of Pn.x is 0. 1_B The output level of Pn.x is 1.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

Table 75 Access Mode Restrictions sorted by descending priority

Applies to **P00_OUT**
Applies to **P11_OUT**
Applies to **P20_OUT**
Applies to **P33_OUT**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-15)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-15)	

P02_OUT
Port 02 Output Register **(000_H)** **Application Reset Value: $0000\ 0000_H$**
P10_OUT
Port 10 Output Register **(000_H)** **Application Reset Value: $0000\ 0000_H$**
P14_OUT
Port 14 Output Register **(000_H)** **Application Reset Value: $0000\ 0000_H$**
P15_OUT
Port 15 Output Register **(000_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**P11**	**P10**	**P9**	**P8**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
r	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px (x=0-11)	x	rwh	**Output Bit x** This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0_B The output level of Pn.x is 0. 1_B The output level of Pn.x is 1.
0	15, 14, 13, 12, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 76 Access Mode Restrictions sorted by descending priority

Applies to **P02_OUT**
Applies to **P10_OUT**
Applies to **P14_OUT**
Applies to **P15_OUT**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-11)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-11)	

P12_OUT
Port 12 Output Register **(000_H)** **Application Reset Value: 0000 0000_H**
P34_OUT
Port 34 Output Register **(000_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	P3	P2	P1	P0
r	r	r	r	r	r	r	r	r	r	r	r	rwh	rwh	rwh	rwh

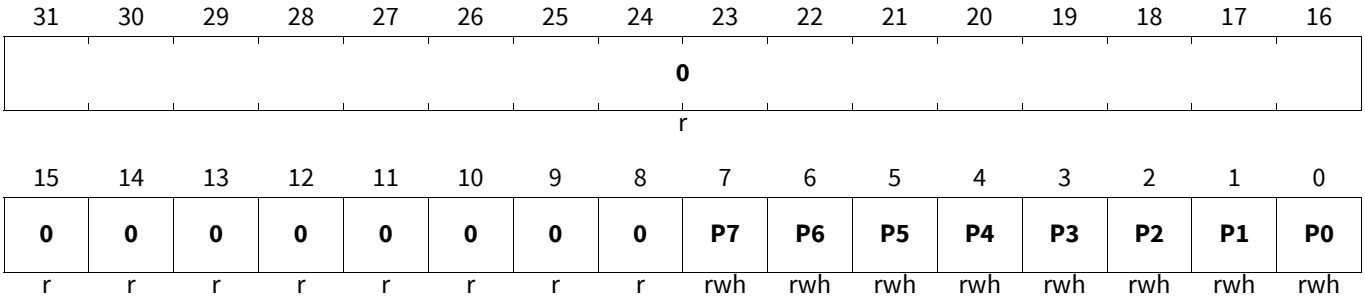
Field	Bits	Type	Description
Px (x=0-3)	x	rwh	**Output Bit x** This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0_B The output level of Pn.x is 0. 1_B The output level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 77 Access Mode Restrictions sorted by descending priority

Applies to **P12_OUT**
Applies to **P34_OUT**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-3)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-3)	

P21_OUT
Port 21 Output Register **(000_H)** **Application Reset Value: $0000\ 0000_H$**
P22_OUT
Port 22 Output Register **(000_H)** **Application Reset Value: $0000\ 0000_H$**
P23_OUT
Port 23 Output Register **(000_H)** **Application Reset Value: $0000\ 0000_H$**
P32_OUT
Port 32 Output Register **(000_H)** **Application Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
Px (x=0-7)	x	rwh	**Output Bit x** This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. Pn.x can also be set or cleared by control bits of the Pn_OMSR, Pn_OMCR or Pn_OMR registers. 0_B The output level of Pn.x is 0. 1_B The output level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 78 Access Mode Restrictions sorted by descending priority

Applies to **P21_OUT**
Applies to **P22_OUT**
Applies to **P23_OUT**
Applies to **P32_OUT**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rwh	Px (x=0-7)	write access for enabled masters
Otherwise (default)	rh	Px (x=0-7)	

Port 00 Output Modification Register

The port output modification register contains control bits that make it possible to individually set, clear or toggle the logic state of a single port line by manipulating the output register.

P00_OMR
Port 00 Output Modification Register **(004_H)** **Application Reset Value: 0000 0000$_H$**
P11_OMR
Port 11 Output Modification Register **(004_H)** **Application Reset Value: 0000 0000$_H$**
P20_OMR
Port 20 Output Modification Register **(004_H)** **Application Reset Value: 0000 0000$_H$**
P33_OMR
Port 33 Output Modification Register **(004_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PCL15	**PCL14**	**PCL13**	**PCL12**	**PCL11**	**PCL10**	**PCL9**	**PCL8**	**PCL7**	**PCL6**	**PCL5**	**PCL4**	**PCL3**	**PCL2**	**PCL1**	**PCL0**
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS15	**PS14**	**PS13**	**PS12**	**PS11**	**PS10**	**PS9**	**PS8**	**PS7**	**PS6**	**PS5**	**PS4**	**PS3**	**PS2**	**PS1**	**PS0**
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-15)	x	w0	**Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in **Table 80**. 0_B No operation 1_B Sets or toggles Pn_OUT.Px.
PCLx (x=0-15)	x+16	w0	**Clear Bit x** Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in **Table 80**. 0_B No operation 1_B Clears or toggles Pn_OUT.Px.

Table 79 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMR**
Applies to **P11_OMR**
Applies to **P20_OMR**
Applies to **P33_OMR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-15), PSx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-15), PSx (x=0-15)	

Note: Register Pn_OMR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Table 80 Function of the Bits PCLx and PSx

PCLx	PSx	Function
0	0	Bit Pn_OUT.Px is not changed.
0	1	Bit Pn_OUT.Px is set.
1	0	Bit Pn_OUT.Px is reset.
1	1	Bit Pn_OUT.Px is toggled.

P02_OMR
Port 02 Output Modification Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**
P10_OMR
Port 10 Output Modification Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**
P14_OMR
Port 14 Output Modification Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**
P15_OMR
Port 15 Output Modification Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**PCL11**	**PCL10**	**PCL9**	**PCL8**	**PCL7**	**PCL6**	**PCL5**	**PCL4**	**PCL3**	**PCL2**	**PCL1**	**PCL0**
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**PS11**	**PS10**	**PS9**	**PS8**	**PS7**	**PS6**	**PS5**	**PS4**	**PS3**	**PS2**	**PS1**	**PS0**
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-11)	x	w0	**Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in **Table 80**. 0_B No operation 1_B Sets or toggles Pn_OUT.Px.
PCLx (x=0-11)	x+16	w0	**Clear Bit x** Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in **Table 80**. 0_B No operation 1_B Clears or toggles Pn_OUT.Px.
0	15, 14, 13, 12, 31, 30, 29, 28	r	**Reserved** Read as 0; should be written with 0.

Table 81 Access Mode Restrictions sorted by descending priority

Applies to **P02_OMR**
Applies to **P10_OMR**
Applies to **P14_OMR**
Applies to **P15_OMR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-11), PSx (x=0-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-11), PSx (x=0-11)	

P12_OMR
Port 12 Output Modification Register **(004_H)** **Application Reset Value: 0000 0000$_H$**
P34_OMR
Port 34 Output Modification Register **(004_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**PCL3**	**PCL2**	**PCL1**	**PCL0**
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**PS3**	**PS2**	**PS1**	**PS0**
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-3)	x	w0	**Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in **Table 80**. 0_B No operation 1_B Sets or toggles Pn_OUT.Px.
PCLx (x=0-3)	x+16	w0	**Clear Bit x** Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in **Table 80**. 0_B No operation 1_B Clears or toggles Pn_OUT.Px.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20	r	**Reserved** Read as 0; should be written with 0.

Table 82 Access Mode Restrictions sorted by descending priority

Applies to **P12_OMR**
Applies to **P34_OMR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3), PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3), PSx (x=0-3)	

P21_OMR
Port 21 Output Modification Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**
P22_OMR
Port 22 Output Modification Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**
P23_OMR
Port 23 Output Modification Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**
P32_OMR
Port 32 Output Modification Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**PCL7**	**PCL6**	**PCL5**	**PCL4**	**PCL3**	**PCL2**	**PCL1**	**PCL0**
r	r	r	r	r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**PS7**	**PS6**	**PS5**	**PS4**	**PS3**	**PS2**	**PS1**	**PS0**
r	r	r	r	r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-7)	x	w0	**Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in **Table 80**. 0_B No operation 1_B Sets or toggles Pn_OUT.Px.
PCLx (x=0-7)	x+16	w0	**Clear Bit x** Setting this bit will clear or toggle the corresponding bit in the port output register Pn_OUT. Read as 0. The function of this bit is shown in **Table 80**. 0_B No operation 1_B Clears or toggles Pn_OUT.Px.
0	15, 14, 13, 12, 11, 10, 9, 8, 31, 30, 29, 28, 27, 26, 25, 24	r	**Reserved** Read as 0; should be written with 0.

Table 83 Access Mode Restrictions sorted by descending priority

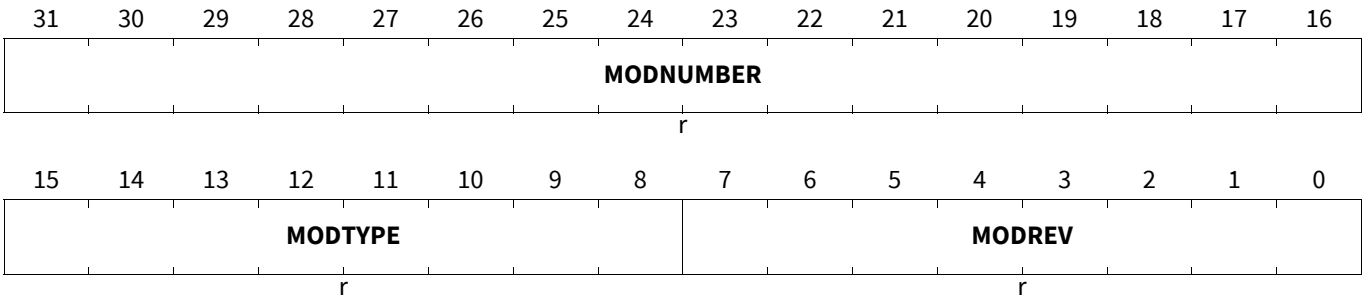
Applies to **P21_OMR**
Applies to **P22_OMR**
Applies to **P23_OMR**
Applies to **P32_OMR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-7), PSx (x=0-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-7), PSx (x=0-7)	

Port 00 Identification Register

The module Identification Register ID contains read-only information about the module version.

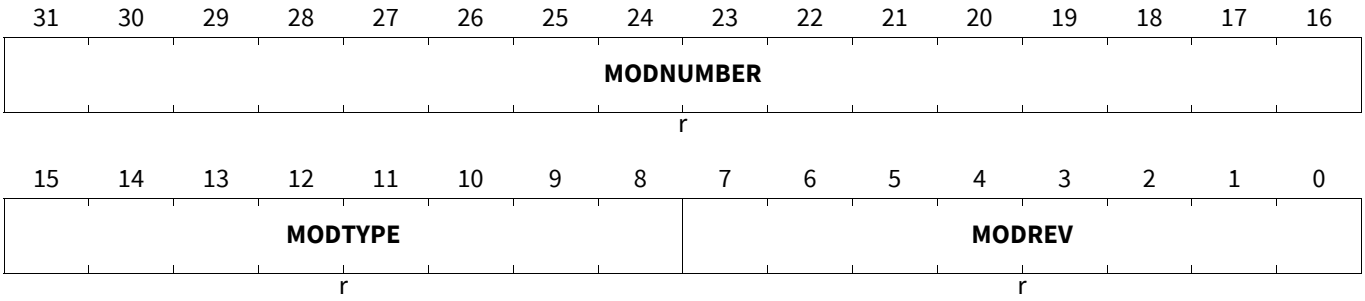
P00_ID
Port 00 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P02_ID
Port 02 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P10_ID
Port 10 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P11_ID
Port 11 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P12_ID
Port 12 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P14_ID
Port 14 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P15_ID
Port 15 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P20_ID
Port 20 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P21_ID
Port 21 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P22_ID
Port 22 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**



Field	Bits	Type	Description
MODREV	7:0	r	**Module Revision Number** This bit field indicates the revision number of the TC33xEXT module (01_H = first revision).

Field	Bits	Type	Description
MODTYPE	15:8	r	**Module Type** This bit field is $C0_H$. It defines a 32-bit module
MODNUMBER	31:16	r	**Module Number** This bit field defines the module identification number. The value for the Ports module is $00C8_H$

P23_ID
Port 23 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P32_ID
Port 32 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P33_ID
Port 33 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**
P34_ID
Port 34 Identification Register **(008_H)** **Application Reset Value: 00C8 C0XX$_H$**



Field	Bits	Type	Description
MODREV	7:0	r	**Module Revision Number** This bit field indicates the revision number of the TC33xEXT module (01_H = first revision).
MODTYPE	15:8	r	**Module Type** This bit field is $C0_H$. It defines a 32-bit module
MODNUMBER	31:16	r	**Module Number** This bit field defines the module identification number. The value for the Ports module is $00C8_H$

Port 00 Input/Output Control Register 0

The port input/output control registers select the digital output and input driver functionality and characteristics of a GPIO port pin. Port direction (input or output), pull-up, pull-down, or no pull devices for inputs, and push-pull or open-drain functionality for outputs can be selected by the corresponding bit fields PCx (x = 0-15). Each 32-bit wide port input/output control register controls four GPIO port lines:

Register Pn_IOCR0 controls the Pn.[3:0] port lines
Register Pn_IOCR4 controls the Pn.[7:4] port lines
Register Pn_IOCR8 controls the Pn.[11:8] port lines
Register Pn_IOCR12 controls the Pn.[15:12] port lines

The structure with one control bit field for each port pin located in different register bytes offers the possibility to configure the port pin functionality of a single pin with byte-oriented accesses without accessing the other PCx bit fields.

The reset values of 1010 1010_H and 0000 0000_H for Pn_IOCRx registers represents input pull-up and no input pull device (tri-state mode) being activated, respectively. The switching of the intended mode of the device is controlled by HWCFG6.When a cold reset is activated and HWCFG6=1, the port pins except P33.8, P40 and P41 are set to input pull-up mode, P33.8, P40 and P41 are in tri-state mode as long as PORST is activated.If HWCFG6=0, the pins have the default state of tri-state mode. The pad state can also be configured by software through PMSWCR5.TRISTREQ bit. In the event of a warm reset or wake-up from standby mode, PMSWCR5.TRISTREQ is not affected by reset, hence Pn_IOCRx registers have the reset values configured as per the last state of the TRISTREQ bit.

Note: In LVDS (RX and TX) operation the IOCR register of both pins of the LVDS pair must be configured as output, i.e. $1xxxx_B$. This ensures that the pull devices are disconnected and don't interfere with LVDS operation.

Register Pn_IOCR0 controls the Pn.[3:0] port lines

P00_IOCR0
Port 00 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P02_IOCR0
Port 02 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P10_IOCR0
Port 10 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P11_IOCR0
Port 11 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P12_IOCR0
Port 12 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P14_IOCR0
Port 14 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P15_IOCR0
Port 15 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P20_IOCR0
Port 20 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P21_IOCR0
Port 21 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**
P22_IOCR0
Port 22 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 85**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC3					0			PC2					0		
rw					r			rw					r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC1					0			PC0					0		
rw					r			rw					r		

Field	Bits	Type	Description
PCx (x=0-3)	8*x+7:8*x+3	rw	**Port Control for Pin x** This bit field defines the Port n line x functionality according to **Table 86**.

Field	Bits	Type	Description
0	26:24, 18:16, 10:8, 2:0	r	**Reserved** Read as 0; should be written with 0.

Table 84 Access Mode Restrictions sorted by descending priority

Applies to **P00_IOCR0**
Applies to **P02_IOCR0**
Applies to **P10_IOCR0**
Applies to **P11_IOCR0**
Applies to **P12_IOCR0**
Applies to **P14_IOCR0**
Applies to **P15_IOCR0**
Applies to **P20_IOCR0**
Applies to **P21_IOCR0**
Applies to **P22_IOCR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PCx (x=0-3)	

Table 85 Reset Values

Applies to **P00_IOCR0**
Applies to **P02_IOCR0**
Applies to **P10_IOCR0**
Applies to **P11_IOCR0**
Applies to **P12_IOCR0**
Applies to **P14_IOCR0**
Applies to **P15_IOCR0**
Applies to **P20_IOCR0**
Applies to **P21_IOCR0**
Applies to **P22_IOCR0**

Reset Type	Reset Value	Note
Application Reset	$0000\ 0000_H$	HWCFG6 is 0 (tri-state mode)
Application Reset	$1010\ 1010_H$	HWCFG6 is 1 (input pull-up mode)

Port Control Coding

Table 86 describes the coding of the PCx bit fields that determine the port line functionality.

Table 86 PCx Coding

PCx[4:0]	I/O	Characteristics	Selected Pull-up / Pull-down / Selected Output Function
$0XX00_B$	Input	–	No input pull device connected, tri-state mode
$0XX01_B$			Input pull-down device connected
$0XX10_B$			Input pull-up device connected[1)]
$0XX11_B$			No input pull device connected, tri-state mode
10000_B	Output	Push-pull	General-purpose output
10001_B			Alternate output function 1
10010_B			Alternate output function 2
10011_B			Alternate output function 3
10100_B			Alternate output function 4
10101_B			Alternate output function 5
10110_B			Alternate output function 6
10111_B			Alternate output function 7
11000_B		Open-drain	General-purpose output
11001_B			Alternate output function 1
11010_B			Alternate output function 2
11011_B			Alternate output function 3
11100_B			Alternate output function 4
11101_B			Alternate output function 5
11110_B			Alternate output function 6
11111_B			Alternate output function 7

1) This is the default pull device setting after reset for powertrain applications.

P23_IOCR0
Port 23 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 88**
P32_IOCR0
Port 32 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 88**
P33_IOCR0
Port 33 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 88**
P34_IOCR0
Port 34 Input/Output Control Register 0 **(010_H)** **Reset Value: Table 88**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC3					0			PC2					0		
rw					r			rw					r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC1					0			PC0					0		
rw					r			rw					r		

Field	Bits	Type	Description
PCx (x=0-3)	8*x+7:8*x+3	rw	**Port Control for Pin x** This bit field defines the Port n line x functionality according to **Table 86**.
0	26:24, 18:16, 10:8, 2:0	r	**Reserved** Read as 0; should be written with 0.

Table 87 Access Mode Restrictions sorted by descending priority

Applies to **P23_IOCR0**
Applies to **P32_IOCR0**
Applies to **P33_IOCR0**
Applies to **P34_IOCR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PCx (x=0-3)	

Table 88 Reset Values

Applies to **P23_IOCR0**
Applies to **P32_IOCR0**
Applies to **P33_IOCR0**
Applies to **P34_IOCR0**

Reset Type	Reset Value	Note
Application Reset	$0000\ 0000_H$	HWCFG6 is 0 (tri-state mode)
Application Reset	$1010\ 1010_H$	HWCFG6 is 1 (input pull-up mode)

Port 00 Input/Output Control Register 4

Register Pn_IOCR4 controls the Pn.[7:4] port lines

P00_IOCR4
Port 00 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P02_IOCR4
Port 02 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P10_IOCR4
Port 10 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P11_IOCR4
Port 11 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P14_IOCR4
Port 14 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P15_IOCR4
Port 15 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P20_IOCR4
Port 20 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P21_IOCR4
Port 21 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P22_IOCR4
Port 22 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**
P23_IOCR4
Port 23 Input/Output Control Register 4 **(014_H)** **Reset Value: Table 90**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC7					**0**			**PC6**					**0**		
rw					r			rw					r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC5					**0**			**PC4**					**0**		
rw					r			rw					r		

Field	Bits	Type	Description
PCx (x=4-7)	8*x-25:8*x-29	rw	**Port Control for Port 00 Pin x** This bit field defines the Port n line x functionality according to **Table 86**.
0	26:24, 18:16, 10:8, 2:0	r	**Reserved** Read as 0; should be written with 0.

Table 89 Access Mode Restrictions sorted by descending priority

Applies to **P00_IOCR4**
Applies to **P02_IOCR4**
Applies to **P10_IOCR4**
Applies to **P11_IOCR4**
Applies to **P14_IOCR4**
Applies to **P15_IOCR4**
Applies to **P20_IOCR4**
Applies to **P21_IOCR4**
Applies to **P22_IOCR4**
Applies to **P23_IOCR4**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=4-7)	write access for enabled masters
Otherwise (default)	r	PCx (x=4-7)	

Table 90 Reset Values

Applies to **P00_IOCR4**
Applies to **P02_IOCR4**
Applies to **P10_IOCR4**
Applies to **P11_IOCR4**
Applies to **P14_IOCR4**
Applies to **P15_IOCR4**
Applies to **P20_IOCR4**
Applies to **P21_IOCR4**
Applies to **P22_IOCR4**
Applies to **P23_IOCR4**

Reset Type	Reset Value	Note
Application Reset	$0000\ 0000_H$	HWCFG6 is 0 (tri-state mode)
Application Reset	$1010\ 1010_H$	HWCFG6 is 1 (input pull-up mode)

P32_IOCR4
Port 32 Input/Output Control Register 4 (014_H) Reset Value: Table 92
P33_IOCR4
Port 33 Input/Output Control Register 4 (014_H) Reset Value: Table 92

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC7					0			PC6					0		
rw					r			rw					r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC5					0			PC4					0		
rw					r			rw					r		

Field	Bits	Type	Description
PCx (x=4-7)	8*x-25:8*x-29	rw	**Port Control for Port 32 Pin x** This bit field defines the Port n line x functionality according to **Table 86**.
0	26:24, 18:16, 10:8, 2:0	r	**Reserved** Read as 0; should be written with 0.

Table 91 Access Mode Restrictions sorted by descending priority

Applies to **P32_IOCR4**
Applies to **P33_IOCR4**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=4-7)	write access for enabled masters
Otherwise (default)	r	PCx (x=4-7)	

Table 92 Reset Values

Applies to **P32_IOCR4**
Applies to **P33_IOCR4**

Reset Type	Reset Value	Note
Application Reset	$0000\ 0000_H$	HWCFG6 is 0 (tri-state mode)
Application Reset	$1010\ 1010_H$	HWCFG6 is 1 (input pull-up mode)

Port 00 Input/Output Control Register 8

Register Pn_IOCR8 controls the Pn.[11:8] port lines

P00_IOCR8
Port 00 Input/Output Control Register 8 **(018_H)** **Reset Value: Table 94**
P02_IOCR8
Port 02 Input/Output Control Register 8 **(018_H)** **Reset Value: Table 94**
P10_IOCR8
Port 10 Input/Output Control Register 8 **(018_H)** **Reset Value: Table 94**
P11_IOCR8
Port 11 Input/Output Control Register 8 **(018_H)** **Reset Value: Table 94**
P14_IOCR8
Port 14 Input/Output Control Register 8 **(018_H)** **Reset Value: Table 94**
P15_IOCR8
Port 15 Input/Output Control Register 8 **(018_H)** **Reset Value: Table 94**
P20_IOCR8
Port 20 Input/Output Control Register 8 **(018_H)** **Reset Value: Table 94**
P33_IOCR8
Port 33 Input/Output Control Register 8 **(018_H)** **Reset Value: Table 95**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC11					**0**			**PC10**					**0**		
rw					r			rw					r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC9					**0**			**PC8**					**0**		
rw					r			rw					r		

Field	Bits	Type	Description
PCx (x=8-11)	8*x-57:8*x-61	rw	**Port Control for Port 00 Pin x** This bit field defines the Port n line x functionality according to **Table 86**.
0	26:24, 18:16, 10:8, 2:0	r	**Reserved** Read as 0; should be written with 0.

Table 93 Access Mode Restrictions sorted by descending priority

Applies to **P00_IOCR8**
Applies to **P02_IOCR8**
Applies to **P10_IOCR8**
Applies to **P11_IOCR8**
Applies to **P14_IOCR8**
Applies to **P15_IOCR8**
Applies to **P20_IOCR8**
Applies to **P33_IOCR8**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=8-11)	write access for enabled masters
Otherwise (default)	r	PCx (x=8-11)	

Table 94 Reset Values variant 1

Applies to **P00_IOCR8**
Applies to **P02_IOCR8**
Applies to **P10_IOCR8**
Applies to **P11_IOCR8**
Applies to **P14_IOCR8**
Applies to **P15_IOCR8**
Applies to **P20_IOCR8**

Reset Type	Reset Value	Note
Application Reset	$0000\ 0000_H$	HWCFG6 is 0 (tri-state mode)
Application Reset	$1010\ 1010_H$	HWCFG6 is 1 (input pull-up mode)

Table 95 Reset Values of P33_IOCR8

Reset Type	Reset Value	Note
Application Reset	$0000\ 0000_H$	HWCFG6 is 0 (tri-state mode)
Application Reset	$1010\ 1000_H$	HWCFG6 is 1 (input pull-up mode)

Port 00 Input/Output Control Register 12

Register Pn_IOCR12 controls the Pn.[15:12] port lines

P00_IOCR12
Port 00 Input/Output Control Register 12 ($01C_H$) Reset Value: Table 97
P11_IOCR12
Port 11 Input/Output Control Register 12 ($01C_H$) Reset Value: Table 97
P20_IOCR12
Port 20 Input/Output Control Register 12 ($01C_H$) Reset Value: Table 97
P33_IOCR12
Port 33 Input/Output Control Register 12 ($01C_H$) Reset Value: Table 97

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PC15					0			PC14					0		
rw					r			rw					r		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PC13					0			PC12					0		
rw					r			rw					r		

Field	Bits	Type	Description
PCx (x=12-15)	8*x-89:8*x-93	rw	**Port Control for Port 00 Pin x** This bit field defines the Port n line x functionality according to **Table 86**.
0	26:24, 18:16, 10:8, 2:0	r	**Reserved** Read as 0; should be written with 0.

Table 96 Access Mode Restrictions sorted by descending priority

Applies to **P00_IOCR12**
Applies to **P11_IOCR12**
Applies to **P20_IOCR12**
Applies to **P33_IOCR12**

Mode Name	Access Mode		Description
Master enabled in ACCEN	rw	PCx (x=12-15)	write access for enabled masters
Otherwise (default)	r	PCx (x=12-15)	

Table 97 Reset Values

Applies to **P00_IOCR12**
Applies to **P11_IOCR12**
Applies to **P20_IOCR12**
Applies to **P33_IOCR12**

Reset Type	Reset Value	Note
Application Reset	$0000\ 0000_H$	HWCFG6 is 0 (tri-state mode)
Application Reset	$1010\ 1010_H$	HWCFG6 is 1 (input pull-up mode)

Port 00 Input Register

The logic level of a GPIO pin can be read via the read-only port input register Pn_IN.Reading the Pn_IN register always returns the current logical value at the GPIO pin independently whether the pin is selected as input or output.

P00_IN
Port 00 Input Register **(024_H)** **Application Reset Value: 0000 XXXX$_H$**
P11_IN
Port 11 Input Register **(024_H)** **Application Reset Value: 0000 XXXX$_H$**
P20_IN
Port 20 Input Register **(024_H)** **Application Reset Value: 0000 XXXX$_H$**
P33_IN
Port 33 Input Register **(024_H)** **Application Reset Value: 0000 XXXX$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-15)	x	rh	**Input Bit x** This bit indicates the level at the input pin Pn.x. 0_B The input level of Pn.x is 0. 1_B The input level of Pn.x is 1.
0	31:16	r	**Reserved** Read as 0.

P02_IN
Port 02 Input Register **(024_H)** **Application Reset Value: 0000 0XXX$_H$**
P10_IN
Port 10 Input Register **(024_H)** **Application Reset Value: 0000 0XXX$_H$**
P14_IN
Port 14 Input Register **(024_H)** **Application Reset Value: 0000 0XXX$_H$**
P15_IN
Port 15 Input Register **(024_H)** **Application Reset Value: 0000 0XXX$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**P11**	**P10**	**P9**	**P8**	**P7**	**P6**	**P5**	**P4**	**P3**	**P2**	**P1**	**P0**
r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-11)	x	rh	**Input Bit x** This bit indicates the level at the input pin Pn.x. 0_B The input level of Pn.x is 0. 1_B The input level of Pn.x is 1.
0	15, 14, 13, 12, 31:16	r	**Reserved** Read as 0; should be written with 0.

P12_IN
Port 12 Input Register **(024_H)** **Application Reset Value: 0000 000X$_H$**
P34_IN
Port 34 Input Register **(024_H)** **Application Reset Value: 0000 000X$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	P3	P2	P1	P0
r	r	r	r	r	r	r	r	r	r	r	r	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-3)	x	rh	**Input Bit x** This bit indicates the level at the input pin Pn.x. 0_B The input level of Pn.x is 0. 1_B The input level of Pn.x is 1.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	**Reserved** Read as 0; should be written with 0.

P21_IN
Port 21 Input Register **(024_H)** **Application Reset Value: 0000 00XX$_H$**
P22_IN
Port 22 Input Register **(024_H)** **Application Reset Value: 0000 00XX$_H$**
P23_IN
Port 23 Input Register **(024_H)** **Application Reset Value: 0000 00XX$_H$**
P32_IN
Port 32 Input Register **(024_H)** **Application Reset Value: 0000 00XX$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	P7	P6	P5	P4	P3	P2	P1	P0
r	r	r	r	r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px (x=0-7)	x	rh	**Input Bit x** This bit indicates the level at the input pin Pn.x. 0_B The input level of Pn.x is 0. 1_B The input level of Pn.x is 1.

Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	**Reserved** Read as 0; should be written with 0.

Port 00 Pad Driver Mode Register 0

P00_PDR0
Port 00 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P02_PDR0
Port 02 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P10_PDR0
Port 10 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P11_PDR0
Port 11 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P14_PDR0
Port 14 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P15_PDR0
Port 15 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P20_PDR0
Port 20 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P21_PDR0
Port 21 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P22_PDR0
Port 22 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**
P23_PDR0
Port 23 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 99**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PL7		**PD7**		**PL6**		**PD6**		**PL5**		**PD5**		**PL4**		**PD4**	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL3		**PD3**		**PL2**		**PD2**		**PL1**		**PD1**		**PL0**		**PD0**	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
PDx (x=0-7)	4*x+1:4*x	rw	**Pad Driver Mode for Pin x**
PLx (x=0-7)	4*x+3:4*x+2	rw	**Pad Level Selection for Pin x**

Table 98 Access Mode Restrictions sorted by descending priority

Applies to **P00_PDR0**
Applies to **P02_PDR0**
Applies to **P10_PDR0**
Applies to **P11_PDR0**
Applies to **P14_PDR0**
Applies to **P15_PDR0**
Applies to **P20_PDR0**
Applies to **P21_PDR0**
Applies to **P22_PDR0**
Applies to **P23_PDR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-7), PLx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDx (x=0-7), PLx (x=0-7)	

Table 99 Reset Values

Applies to **P00_PDR0**
Applies to **P02_PDR0**
Applies to **P10_PDR0**
Applies to **P11_PDR0**
Applies to **P14_PDR0**
Applies to **P15_PDR0**
Applies to **P20_PDR0**
Applies to **P21_PDR0**
Applies to **P22_PDR0**
Applies to **P23_PDR0**

Reset Type	Reset Value	Note
After SSW execution	$2222\ 2222_H$	Initial value in largest package
After SSW execution	$----\ ----_H$	Initial value package dependent

Output Characteristics

The pad structure of the GPIO lines offers the possibility to select the output driver strength and the slew rate. These two parameters are controlled by the PDx bit fields in the pad driver mode registers Pn_PDR0/1 for output modes. The available modes depend on the respective pad type.

Table 100 Pad Driver Mode Selection for RFast Pads

PDx.1	PDx.0	Speed Grade	Driver Setting
0	0	1	Strong driver, sharp edge (“ss”)
0	1	2	Strong driver, medium edge (“sm”)
1	0	3	Medium driver (“m”)
1	1	4	RGMII driver.

Table 101 Pad Driver Mode Selection for Fast Pads

PDx.1	PDx.0	Speed Grade	Driver Setting
0	0	1	Strong driver, sharp edge (“ss”)
0	1	2	Strong driver, medium edge (“sm”)
1	0	3	Medium driver (“m”)
1	1	4	TC39x A-Step: Medium driver (“m”) Else: Reserved when operating as output. When operating as input see below “Pad Level Selection for Input Function”.

Table 102 Pad Driver Mode Selection for Slow Pads

PDx.1	PDx.0	Speed Grade	Driver Setting
X	0	1	Medium driver, sharp edge (“sm”)[1)]
X	1	2	Medium driver (“m”)

1) This setting is marked “sm” as the electrical characteristics are identical to the strong driver medium edge setting. The Data Sheet contains also only common “sm” tables.

Note: The Data Sheet describes the DC characteristics of all pad classes.

TTL/Automotive Input Selection

The input function can operate with different VIH and VIL levels depending on the pad supply voltage, the pad type and the selection done by the PLx bits of the Pn_PDRx as of **Table 103**. PLx.1 changes additionally the pull-up and pull-down resistors.

Table 103 Pad Level Selection for Input Function

PLx.1	PLx.0	Input Levels
0	X	Automotive level “AL”.
1	0	TTL level for 5V pad supply. Degraded TTL level used for CIF when pad supply is 3.3V
1	1	TTL level for 3.3V pad supply.
X	X	Only for pads with RGMII input buffer (marked “RGMII_Input” in the pinning table): • when PDx.1=1 and PDx.0=1 the input level RGMII is selected. • for other PDx values the input level is determined by PLx as for all other pads (first three rows of this table).

LVDS

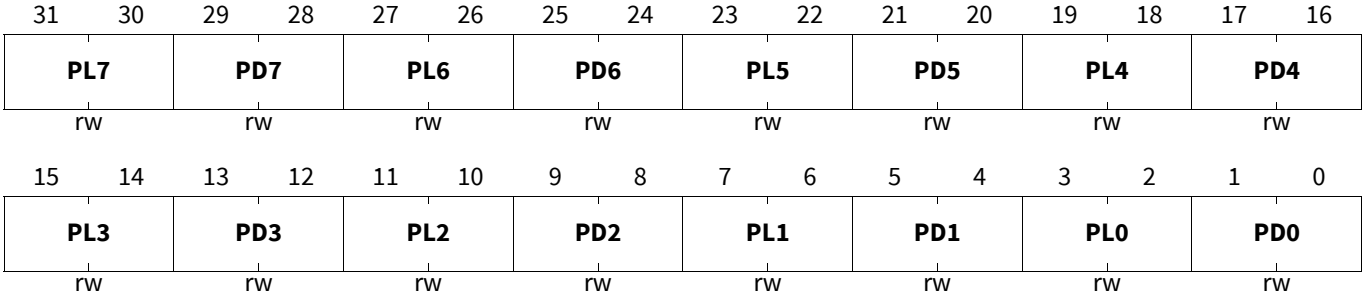
The default CMOS mode can be switched to LVDS mode in LVDS pads through the LPCRx register.

Pad Driver Mode Registers

This is the general description of the PDR registers. Each port contains its own specific PDR registers, described additionally at each port, that can contain between one and eight PDx fields for PDR0 and PDR1 registers, respectively. Each PDx field controls 1 pin. For coding of PDx, see **Table 100**, **Table 101** and **Table 102**. Similarly, each PLx bit controls 1 pin. For coding of PLx, see **Table 103**.

The boot software configures the reset value of Pn_PDR0 and Pn_PDR1 registers from 0000 0000$_H$ to 2222 2222$_H$ except for analog ports and if the package doesn't make any of the related pins available. The resulting value depends on the implemented port width. The documented value is valid for the largest package.

P32_PDR0
Port 32 Pad Driver Mode Register 0 **(040$_H$)** **Reset Value: Table 105**
P33_PDR0
Port 33 Pad Driver Mode Register 0 **(040$_H$)** **Reset Value: Table 105**



Field	Bits	Type	Description
PDx (x=0-7)	4*x+1:4*x	rw	**Pad Driver Mode for Pin x**
PLx (x=0-7)	4*x+3:4*x+2	rw	**Pad Level Selection for Pin x**

Table 104 Access Mode Restrictions sorted by descending priority

Applies to **P32_PDR0**
Applies to **P33_PDR0**

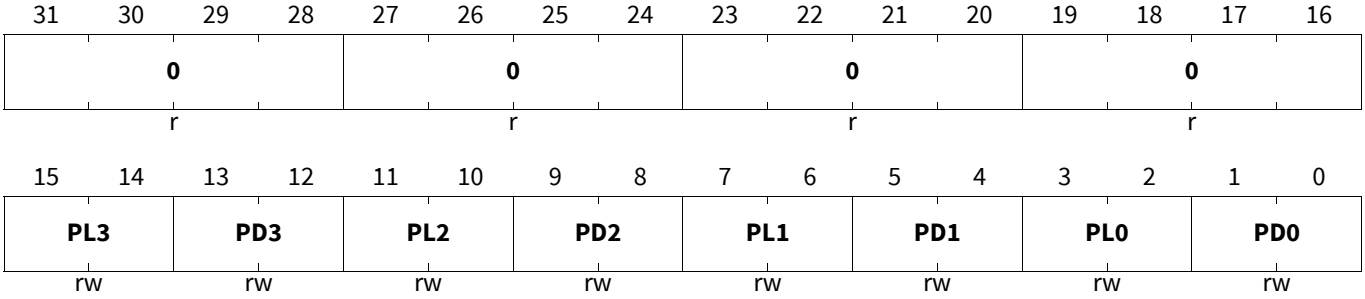
Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-7), PLx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDx (x=0-7), PLx (x=0-7)	

Table 105 Reset Values

Applies to **P32_PDR0**
Applies to **P33_PDR0**

Reset Type	Reset Value	Note
After SSW execution	2222 2222$_H$	Initial value in largest package
After SSW execution	---- ----$_H$	Initial value package dependent

P12_PDR0
Port 12 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 107**
P34_PDR0
Port 34 Pad Driver Mode Register 0 **(040_H)** **Reset Value: Table 107**



Field	Bits	Type	Description
PDx (x=0-3)	4*x+1:4*x	rw	**Pad Driver Mode for Pin x**
PLx (x=0-3)	4*x+3:4*x+2	rw	**Pad Level Selection for Pin x**
0	31:28, 27:24, 23:20, 19:16	r	**Reserved** Read as 0; should be written with 0.

Table 106 Access Mode Restrictions sorted by descending priority

Applies to **P12_PDR0**
Applies to **P34_PDR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=0-3), PLx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PDx (x=0-3), PLx (x=0-3)	

Table 107 Reset Values

Applies to **P12_PDR0**
Applies to **P34_PDR0**

Reset Type	Reset Value	Note
After SSW execution	0000 2222_H	Initial value in largest package
After SSW execution	0000 $----_H$	Initial value package dependent

Port 00 Pad Driver Mode Register 1

P00_PDR1
Port 00 Pad Driver Mode Register 1 **(044_H)** **Reset Value: Table 109**
P11_PDR1
Port 11 Pad Driver Mode Register 1 **(044_H)** **Reset Value: Table 109**
P20_PDR1
Port 20 Pad Driver Mode Register 1 **(044_H)** **Reset Value: Table 109**
P33_PDR1
Port 33 Pad Driver Mode Register 1 **(044_H)** **Reset Value: Table 109**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PL15		PD15		PL14		PD14		PL13		PD13		PL12		PD12	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PL11		PD11		PL10		PD10		PL9		PD9		PL8		PD8	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
PDx (x=8-15)	4*x-31:4*x-32	rw	**Pad Driver Mode for Pin x**
PLx (x=8-15)	4*x-29:4*x-30	rw	**Pad Level Selection for Pin x**

Table 108 Access Mode Restrictions sorted by descending priority

Applies to **P00_PDR1**
Applies to **P11_PDR1**
Applies to **P20_PDR1**
Applies to **P33_PDR1**

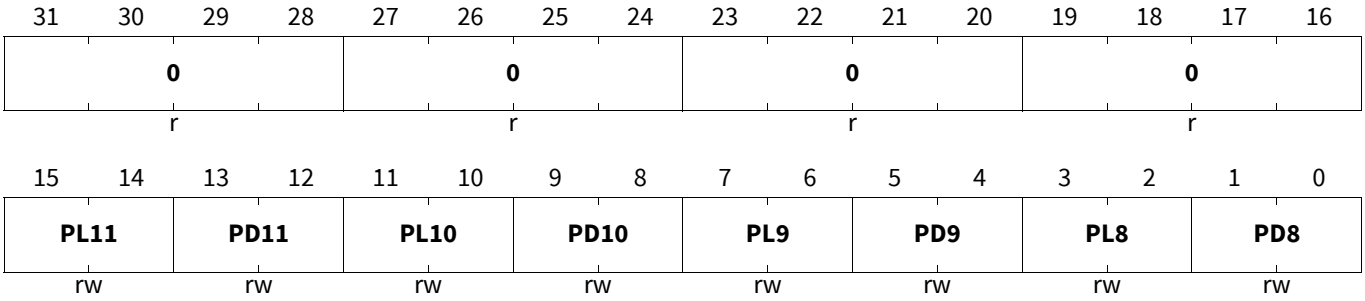
Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=8-15), PLx (x=8-15)	write access for enabled masters
Otherwise (default)	r	PDx (x=8-15), PLx (x=8-15)	

Table 109 Reset Values

Applies to **P00_PDR1**
Applies to **P11_PDR1**
Applies to **P20_PDR1**
Applies to **P33_PDR1**

Reset Type	Reset Value	Note
After SSW execution	2222 2222_H	Initial value in largest package
After SSW execution	---- $----_H$	Initial value package dependent

P02_PDR1
Port 02 Pad Driver Mode Register 1 **(044_H)** **Reset Value: Table 111**
P10_PDR1
Port 10 Pad Driver Mode Register 1 **(044_H)** **Reset Value: Table 111**
P14_PDR1
Port 14 Pad Driver Mode Register 1 **(044_H)** **Reset Value: Table 111**
P15_PDR1
Port 15 Pad Driver Mode Register 1 **(044_H)** **Reset Value: Table 111**



Field	Bits	Type	Description
PDx (x=8-11)	4*x-31:4*x-32	rw	**Pad Driver Mode for Pin x**
PLx (x=8-11)	4*x-29:4*x-30	rw	**Pad Level Selection for Pin x**
0	31:28, 27:24, 23:20, 19:16	r	**Reserved** Read as 0; should be written with 0.

Table 110 Access Mode Restrictions sorted by descending priority

Applies to **P02_PDR1**
Applies to **P10_PDR1**
Applies to **P14_PDR1**
Applies to **P15_PDR1**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDx (x=8-11), PLx (x=8-11)	write access for enabled masters
Otherwise (default)	r	PDx (x=8-11), PLx (x=8-11)	

Table 111 Reset Values

Applies to **P02_PDR1**
Applies to **P10_PDR1**
Applies to **P14_PDR1**
Applies to **P15_PDR1**

Reset Type	Reset Value	Note
After SSW execution	0000 2222_H	Initial value in largest package
After SSW execution	0000 $----_H$	Initial value package dependent

Port 00 Emergency Stop Register

P00_ESR
Port 00 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000_H**
P11_ESR
Port 11 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000_H**
P20_ESR
Port 20 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-15)	x	rw	**Emergency Stop Enable for Pin x** This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0_B Emergency stop function for Pn.x is disabled. 1_B Emergency stop function for Pn.x is enabled.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

Table 112 Access Mode Restrictions sorted by descending priority

Applies to **P00_ESR**
Applies to **P11_ESR**
Applies to **P20_ESR**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-15)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-15)	

Most GPIO lines have an emergency stop logic implemented (see Figure “General Structure of a Port Pin” in the Family chapter).

Each of these GPIO lines has its own emergency stop enable bit ENx that is located in the emergency stop register Pn_ESR of Port n. If the emergency stop signal becomes active, one of two states can be selected:

- Emergency stop function disabled (ENx = 0):
  The output line remains connected (alternate function).
- Emergency stop function enabled (ENx = 1):
  The mapped output function is disconnected and the safe state is entered by switching to input function with internal pull-up connected or tri-state, depending on the configured reset value of the corresponding Pn_IOCR register through PMSWCR5.TRISTREQ or setting of HWCFG[6].(the content of the corresponding PCx bit fields in register Pn_IOCR will not be considered).

Exceptions for Emergency Stop Implementation

The Emergency Stop function is available for all GPIO Ports with the following exceptions:

- Not available for P20.2 (General Purpose Input/GPI only, overlayed with Testmode)
- Not available for P40.x and P41.x (analog input ANx overlayed with GPI)
- Not available for P32.0 and P32.1 when using EVRC regulator.
- Not available for P21.2 (used as EMGSTOPB pin).
- Not available for P33.8 (used as EMGSTOPA pin).
- Not available for dedicated I/O without General Purpose Output function (e.g ESRx, TMS, TCK)

The Emergency Stop function can be overruled on the following GPIO Ports:

- P00.x: Emergency Stop can be overruled by the VADC. Overruling can be disabled via the control register P00_PCSR.
- P14.0 and P14.1: Emergency Stop can be overruled in the DXCPL (DAP over CAN physical layer) mode. No Overruling in the DXCM (Debug over can message) mode
- P21.6: Emergency Stop can be overruled in JTAG mode if this pin is used as TDI
- P21.7: Emergency Stop can be overruled in JTAG or Three Pin DAP mode.
- P33.0-7, P33.9-15 and P34.1: Emergency Stop can be overruled by the 8-Bit Standby Controller (SCR), if implemented. Overruling can be disabled via the control register P33_PCSR and P34_PCSR.

On pins with LVDS TX pads the Emergency Stop affects only the CMOS driver not the LVDS driver. Thus only when LPCRx.TX_EN selects CMOS mode the output is switched off. When TX_EN selects LVDS mode the output is not switched off.

P02_ESR
Port 02 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**
P10_ESR
Port 10 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**
P14_ESR
Port 14 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**
P15_ESR
Port 15 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**EN11**	**EN10**	**EN9**	**EN8**	**EN7**	**EN6**	**EN5**	**EN4**	**EN3**	**EN2**	**EN1**	**EN0**
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-11)	x	rw	**Emergency Stop Enable for Pin x** This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0_B Emergency stop function for Pn.x is disabled. 1_B Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 113 Access Mode Restrictions sorted by descending priority

Applies to **P02_ESR**
Applies to **P10_ESR**
Applies to **P14_ESR**
Applies to **P15_ESR**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-11)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-11)	

P12_ESR
Port 12 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**
P34_ESR
Port 34 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	EN3	EN2	EN1	EN0
r	r	r	r	r	r	r	r	r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-3)	x	rw	**Emergency Stop Enable for Pin x** This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0_B Emergency stop function for Pn.x is disabled. 1_B Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 114 Access Mode Restrictions sorted by descending priority

Applies to **P12_ESR**
Applies to **P34_ESR**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-3)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-3)	

P21_ESR

Port 21 Emergency Stop Register **(050_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

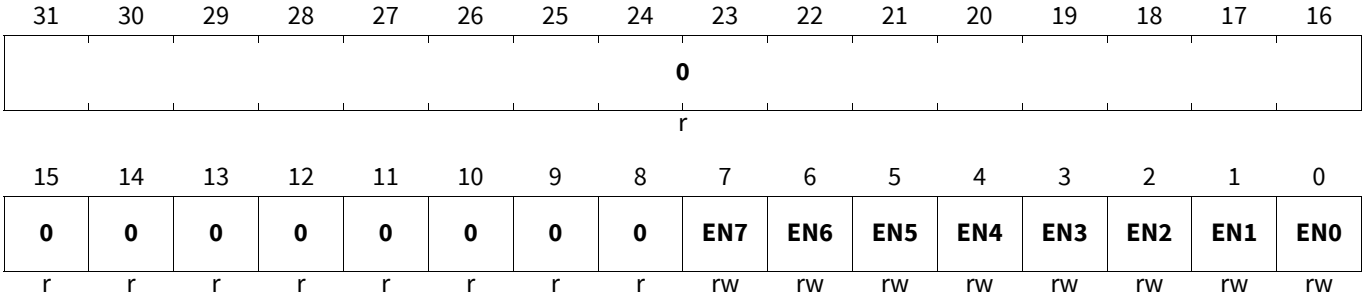
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	EN7	EN6	EN5	EN4	EN3	0	EN1	EN0
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	r	rw	rw

Field	Bits	Type	Description
ENx (x=0-1,3-7)	x	rw	**Emergency Stop Enable for Pin x** This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0_B Emergency stop function for Pn.x is disabled. 1_B Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 11, 10, 9, 8, 2, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 115 Access Mode Restrictions of P21_ESR sorted by descending priority

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-1,3-7)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-1,3-7)	

P22_ESR
Port 22 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**
P23_ESR
Port 23 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**
P32_ESR
Port 32 Emergency Stop Register **(050_H)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
ENx (x=0-7)	x	rw	**Emergency Stop Enable for Pin x** This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0_B Emergency stop function for Pn.x is disabled. 1_B Emergency stop function for Pn.x is enabled.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 116 Access Mode Restrictions sorted by descending priority

Applies to **P22_ESR**
Applies to **P23_ESR**
Applies to **P32_ESR**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-7)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-7)	

P33_ESR

Port 33 Emergency Stop Register **(050_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	EN14	EN13	EN12	EN11	EN10	EN9	0	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0
rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-7,9-15)	x	rw	**Emergency Stop Enable for Pin x** This bit enables the emergency stop function for all GPIO lines. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate output function to GPIO input function. 0_B Emergency stop function for Pn.x is disabled. 1_B Emergency stop function for Pn.x is enabled.
0	8, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 117 Access Mode Restrictions of P33_ESR sorted by descending priority

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	ENx (x=0-7,9-15)	write access for enabled masters
Otherwise (default)	r	ENx (x=0-7,9-15)	

Port 00 Pin Function Decision Control Register

The pad structure of the GPIO lines offers the possibility to disable/enable port pad, select digital input or analog ADC input functionalities. Note that Class S pads have different characteristics than other digital input pads. For analog inputs, setting PDISx to 1 disables the Schmitt trigger input buffer, which would otherwise reduce analog input accuracy. For the ADC diagnostic features “PDD” and “MD” however the corresponding PDISx needs to be 0 to allow activation of their pull resistors. This feature can be controlled by individual bits in the Pn_PDISC register, independently from input/output and pull-up/pull-down control functionality as programmed in the Pn_IOCR register. One Pn_PDISC register is assigned to each port.

Note: After reset, all Px_PDISC registers have the reset value of $0000\ 0000_H$. The startup software enables only the pads with digital input/output functionality which are available in that package. P40_PDISC and P41_PDISC are configured by the SSW for analog input function (kept disabled). The documented reset value shows the value in the largest package.

P00_PDISC
Port 00 Pin Function Decision Control Register (060_H) **Reset Value: Table 119**
P11_PDISC
Port 11 Pin Function Decision Control Register (060_H) **Reset Value: Table 119**
P20_PDISC
Port 20 Pin Function Decision Control Register (060_H) **Reset Value: Table 119**
P33_PDISC
Port 33 Pin Function Decision Control Register (060_H) **Reset Value: Table 119**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIS15	PDIS14	PDIS13	PDIS12	PDIS11	PDIS10	PDIS9	PDIS8	PDIS7	PDIS6	PDIS5	PDIS4	PDIS3	PDIS2	PDIS1	PDIS0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PDISx (x=0-15)	x	rw	**Pin Function Decision Control for Pin x** This bit selects the function of the port pad. 0_B Digital functionality of pad Pn.x is enabled. 1_B Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	31:16	r	**Reserved** Read as 0; should be written with 0.

Table 118 Access Mode Restrictions sorted by descending priority

Applies to **P00_PDISC**
Applies to **P11_PDISC**
Applies to **P20_PDISC**
Applies to **P33_PDISC**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-15)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-15)	

Table 119 Reset Values

Applies to **P00_PDISC**
Applies to **P11_PDISC**
Applies to **P20_PDISC**
Applies to **P33_PDISC**

Reset Type	Reset Value	Note
After SSW execution	0000 0000_H	Initial value in largest package
After SSW execution	0000 $----_H$	Initial value package dependent

P02_PDISC
Port 02 Pin Function Decision Control Register (060_H) **Reset Value: Table 121**
P10_PDISC
Port 10 Pin Function Decision Control Register (060_H) **Reset Value: Table 121**
P14_PDISC
Port 14 Pin Function Decision Control Register (060_H) **Reset Value: Table 121**
P15_PDISC
Port 15 Pin Function Decision Control Register (060_H) **Reset Value: Table 121**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**PDIS11**	**PDIS10**	**PDIS9**	**PDIS8**	**PDIS7**	**PDIS6**	**PDIS5**	**PDIS4**	**PDIS3**	**PDIS2**	**PDIS1**	**PDIS0**
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PDISx (x=0-11)	x	rw	**Pin Function Decision Control for Pin x** This bit selects the function of the port pad. 0_B Digital functionality of pad Pn.x is enabled. 1_B Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	15, 14, 13, 12, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 120 Access Mode Restrictions sorted by descending priority

Applies to **P02_PDISC**
Applies to **P10_PDISC**
Applies to **P14_PDISC**
Applies to **P15_PDISC**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-11)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-11)	

Table 121 Reset Values

Applies to **P02_PDISC**
Applies to **P10_PDISC**
Applies to **P14_PDISC**
Applies to **P15_PDISC**

Reset Type	Reset Value	Note
After SSW execution	0000 0000_H	Initial value in largest package
After SSW execution	0000 $0---_H$	Initial value package dependent

P12_PDISC
Port 12 Pin Function Decision Control Register (060_H) **Reset Value: Table 123**
P34_PDISC
Port 34 Pin Function Decision Control Register (060_H) **Reset Value: Table 123**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	PDIS3	PDIS2	PDIS1	PDIS0
r	r	r	r	r	r	r	r	r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
PDISx (x=0-3)	x	rw	**Pin Function Decision Control for Pin x** This bit selects the function of the port pad. 0_B Digital functionality of pad Pn.x is enabled. 1_B Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.

Field	Bits	Type	Description
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 122 Access Mode Restrictions sorted by descending priority

Applies to **P12_PDISC**
Applies to **P34_PDISC**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-3)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-3)	

Table 123 Reset Values

Applies to **P12_PDISC**
Applies to **P34_PDISC**

Reset Type	Reset Value	Note
After SSW execution	0000 0000$_H$	Initial value in largest package
After SSW execution	0000 000–$_H$	Initial value package dependent

P21_PDISC
Port 21 Pin Function Decision Control Register (060$_H$) **Reset Value: Table 125**
P22_PDISC
Port 22 Pin Function Decision Control Register (060$_H$) **Reset Value: Table 125**
P23_PDISC
Port 23 Pin Function Decision Control Register (060$_H$) **Reset Value: Table 125**
P32_PDISC
Port 32 Pin Function Decision Control Register (060$_H$) **Reset Value: Table 125**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**PDIS7**	**PDIS6**	**PDIS5**	**PDIS4**	**PDIS3**	**PDIS2**	**PDIS1**	**PDIS0**
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PDISx (x=0-7)	x	rw	**Pin Function Decision Control for Pin x** This bit selects the function of the port pad. 0_B Digital functionality of pad Pn.x is enabled. 1_B Digital functionality (including pull resistors) of pad Pn.x is disabled. Analog input function (where this is available) can be used.
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 124 Access Mode Restrictions sorted by descending priority

Applies to **P21_PDISC**
Applies to **P22_PDISC**
Applies to **P23_PDISC**
Applies to **P32_PDISC**

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PDISx (x=0-7)	write access for enabled masters
Otherwise (default)	r	PDISx (x=0-7)	

Table 125 Reset Values

Applies to **P21_PDISC**
Applies to **P22_PDISC**
Applies to **P23_PDISC**
Applies to **P32_PDISC**

Reset Type	Reset Value	Note
After SSW execution	$0000\ 0000_H$	Initial value in largest package
After SSW execution	$0000\ 00--_H$	Initial value package dependent

Port 00 Pin Controller Select Register

This register has different functionality in each port:

- In Ports shared with the standby controller (SCR) it selects if the SCR or the Tricore system control data and control functions of these port lines.
- In Ports with analog inputs to the EVADC it enables control of pull by the EVADC for the Pull Down Diagnostics (PDD) / Multiplexer Diagnostics (MD) feature.
- In Ports with Ethernet output it selects between alternate output and fast RGMII/RMII/MII mode.
- In Ports with SMU FSP pin (P33.8) the PCSR.SEL bit enables the SMU to override pad configuration signals. Therefore this bit has the reset value 1_B and shall be kept 1_B by the application. The SMU override is documented in the SMU chapter (see SMU_PCTL.PCFG and Figure “SMU/PAD Control Interface to the PADs”).

P00_PCSR
Port 00 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**
P20_PCSR
Port 20 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								**0**							
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	**R14**	**R13**	**R12**	**R11**	**R10**	**R9**	**R8**	**R7**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-15)	x	rw	**Reserved** Read as 0; should be written with 0.
0	30:16, 31	r	**Reserved** Read as 0; should be written with 0.

Table 126 Access Mode Restrictions sorted by descending priority

Applies to **P00_PCSR**
Applies to **P20_PCSR**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-15)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-15)	

P02_PCSR
Port 02 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**
P10_PCSR
Port 10 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**
P14_PCSR
Port 14 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**
P15_PCSR
Port 15 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								**0**							
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**R11**	**R10**	**R9**	**R8**	**R7**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-11)	x	rw	**Reserved** Read as 0; should be written with 0.
0	15, 14, 13, 12, 30:16, 31	r	**Reserved** Read as 0; should be written with 0.

Table 127 Access Mode Restrictions sorted by descending priority

Applies to **P02_PCSR**
Applies to **P10_PCSR**
Applies to **P14_PCSR**
Applies to **P15_PCSR**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-11)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-11)	

P11_PCSR
Port 11 Pin Controller Select Register **(064$_H$)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								**0**							
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R15	**R14**	**R13**	**R12**	**R11**	**R10**	**R9**	**R8**	**R7**	**SEL6**	**R5**	**SEL4**	**SEL3**	**SEL2**	**SEL1**	**SEL0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SELx (x=0-4,6)	x	rw	**Output Select for Pin x** This bit enables or disables alternate/fast Ethernet output. 0_B Ethernet output via ports alternate output of pin x. 1_B Ethernet output via fast RGMII/RMII/MII mode of pin x.
Rx (x=5,7-15)	x	rw	**Reserved** Read as 0; should be written with 0.
0	30:16, 31	r	**Reserved** Read as 0; should be written with 0.

Table 128 Access Mode Restrictions of P11_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=5,7-15)	write access only for masters with supervisor mode
	rw	SELx (x=0-4,6)	
Otherwise (default)	r	Rx (x=5,7-15), SELx (x=0-4,6)	

P12_PCSR

Port 12 Pin Controller Select Register (064_H) Application Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								**0**							
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**R3**	**R2**	**R1**	**R0**
r	r	r	r	r	r	r	r	r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-3)	x	rw	**Reserved** Read as 0; should be written with 0.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 30:16, 31	r	**Reserved** Read as 0; should be written with 0.

Table 129 Access Mode Restrictions of P12_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-3)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-3)	

P21_PCSR
Port 21 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**
P22_PCSR
Port 22 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**
P23_PCSR
Port 23 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**
P32_PCSR
Port 32 Pin Controller Select Register **(064_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								**0**							
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**R7**	**R6**	**R5**	**R4**	**R3**	**R2**	**R1**	**R0**
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Rx (x=0-7)	x	rw	**Reserved** Read as 0; should be written with 0.
0	15, 14, 13, 12, 11, 10, 9, 8, 30:16, 31	r	**Reserved** Read as 0; should be written with 0.

Table 130 Access Mode Restrictions sorted by descending priority

Applies to **P21_PCSR**
Applies to **P22_PCSR**
Applies to **P23_PCSR**
Applies to **P32_PCSR**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0-7)	write access only for masters with supervisor mode
Otherwise (default)	r	Rx (x=0-7)	

P33_PCSR

Port 33 Pin Controller Select Register **(064_H)** **Application Reset Value: $0000\ 0100_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LCK								**0**							
rh								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SEL15	**SEL14**	**SEL13**	**SEL12**	**SEL11**	**SEL10**	**SEL9**	**SEL8**	**SEL7**	**SEL6**	**SEL5**	**SEL4**	**SEL3**	**SEL2**	**SEL1**	**SEL0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SELx (x=0-7,9-15)	x	rw	**Output Select for Pin x** This bit enables or disables SCR control. 0_B Tricore selected for data and control of pin x and not SCR. 1_B SCR selected for data and control of pin x.
SELx (x=8)	x	rw	**Output Select for Pin x** This bit enables or disables SMU to override pad configuration. 0_B Disable SMU override of pad configuration for FSP pin x. 1_B Enable SMU to override pad configuration for FSP pin x.
LCK	31	rh	**Lock Status** This bit indicates if the register can be updated with a new value or if the register is locked due to an ongoing transfer to the SCR and a write action from the bus has no effect. In Ports without SCR overlay this bit is always 0_B. 0_B The register is unlocked and can be updated. 1_B The register is locked (a write transfer to SCR is ongoing) and can not be updated.
0	30:16	r	**Reserved** Read as 0; should be written with 0.

Table 131 Access Mode Restrictions of P33_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	rh	LCK	write access only for masters with supervisor mode
	rw	SELx (x=0-7,9-15), SELx (x=8)	
Otherwise (default)	r	SELx (x=0-7,9-15), SELx (x=8)	
	rh	LCK	

P34_PCSR

Port 34 Pin Controller Select Register **(064_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LCK								**0**							
rh								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**R3**	**R2**	**SEL1**	**R0**
r	r	r	r	r	r	r	r	r	r	r	r	rw	rw	rw	rw

Field	Bits	Type	Description
SELx (x=1)	x	rw	**Output Select for Pin x** This bit enables or disables SCR control. 0_B Tricore selected for data and control of pin x and not SCR. 1_B SCR selected for data and control of pin x.
Rx (x=0,2-3)	x	rw	**Reserved** Read as 0; should be written with 0.
LCK	31	rh	**Lock Status** This bit indicates if the register can be updated with a new value or if the register is locked due to an ongoing transfer to the SCR and a write action from the bus has no effect. In Ports without SCR overlay this bit is always 0_B. 0_B The register is unlocked and can be updated. 1_B The register is locked (a write transfer to SCR is ongoing) and can not be updated.
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 30:16	r	**Reserved** Read as 0; should be written with 0.

Table 132 Access Mode Restrictions of P34_PCSR sorted by descending priority

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	r	Rx (x=0,2-3)	write access only for masters with supervisor mode
	rh	LCK	
	rw	SELx (x=1)	
Otherwise (default)	r	Rx (x=0,2-3), SELx (x=1)	
	rh	LCK	

Port 00 Output Modification Set Register 0

The port output modification set register x, (x = 0, 4, 8, 12) contains control bits to individually set the logic state of a single port line by manipulating the output register.

Note: Registers Pn_OMSRx (x = 0, 4, 8, 12) are virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Register Pn_OMSR0 sets the logic state of Pn.[3:0] port lines

P00_OMSR0
Port 00 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P02_OMSR0
Port 02 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P10_OMSR0
Port 10 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P11_OMSR0
Port 11 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P12_OMSR0
Port 12 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P14_OMSR0
Port 14 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P15_OMSR0
Port 15 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P20_OMSR0
Port 20 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P21_OMSR0
Port 21 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P22_OMSR0
Port 22 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												PS3	PS2	PS1	PS0
r												w0	w0	w0	w0

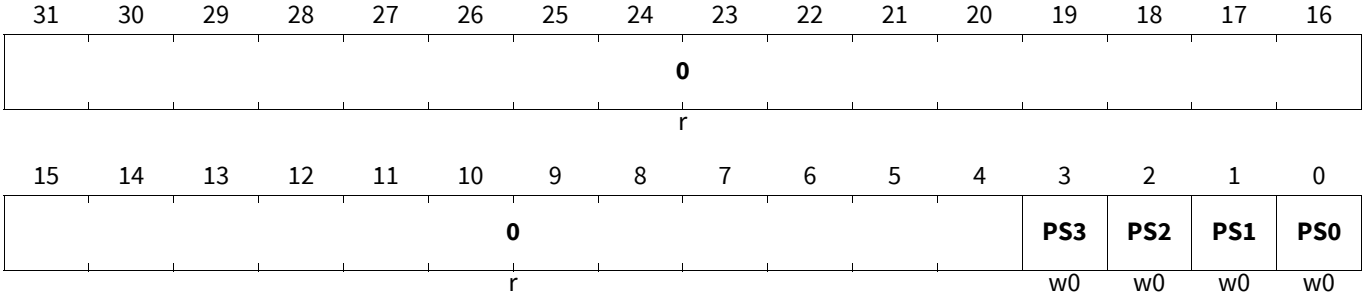
Field	Bits	Type	Description
PSx (x=0-3)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px
0	31:4	r	**Reserved** Read as 0; should be written with 0.

Table 133 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMSR0**
Applies to **P02_OMSR0**
Applies to **P10_OMSR0**
Applies to **P11_OMSR0**
Applies to **P12_OMSR0**
Applies to **P14_OMSR0**
Applies to **P15_OMSR0**
Applies to **P20_OMSR0**
Applies to **P21_OMSR0**
Applies to **P22_OMSR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-3)	

P23_OMSR0
Port 23 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P32_OMSR0
Port 32 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P33_OMSR0
Port 33 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**
P34_OMSR0
Port 34 Output Modification Set Register 0 **(070_H)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
PSx (x=0-3)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px
0	31:4	r	**Reserved** Read as 0; should be written with 0.

Table 134 Access Mode Restrictions sorted by descending priority

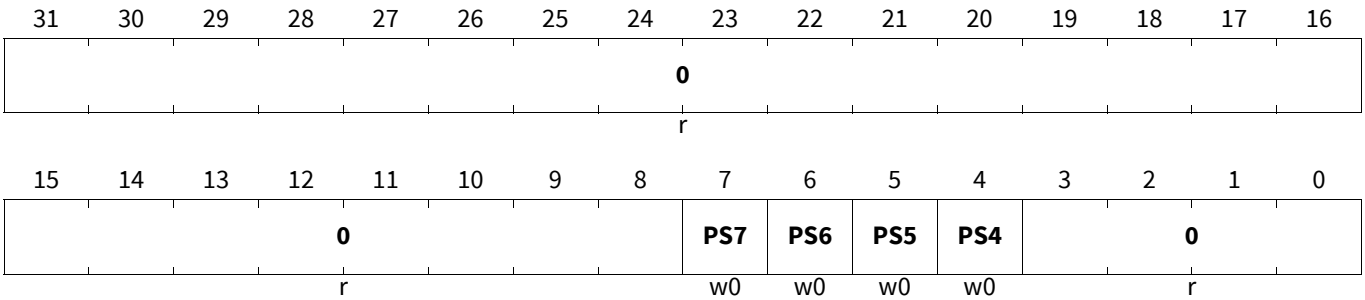
Applies to **P23_OMSR0**
Applies to **P32_OMSR0**
Applies to **P33_OMSR0**
Applies to **P34_OMSR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-3)	

Port 00 Output Modification Set Register 4

Register Pn_OMSR4 sets the logic state of Pn.[7:4] port lines

P00_OMSR4
Port 00 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P02_OMSR4
Port 02 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P10_OMSR4
Port 10 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P11_OMSR4
Port 11 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P14_OMSR4
Port 14 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P15_OMSR4
Port 15 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P20_OMSR4
Port 20 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P21_OMSR4
Port 21 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P22_OMSR4
Port 22 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P23_OMSR4
Port 23 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$



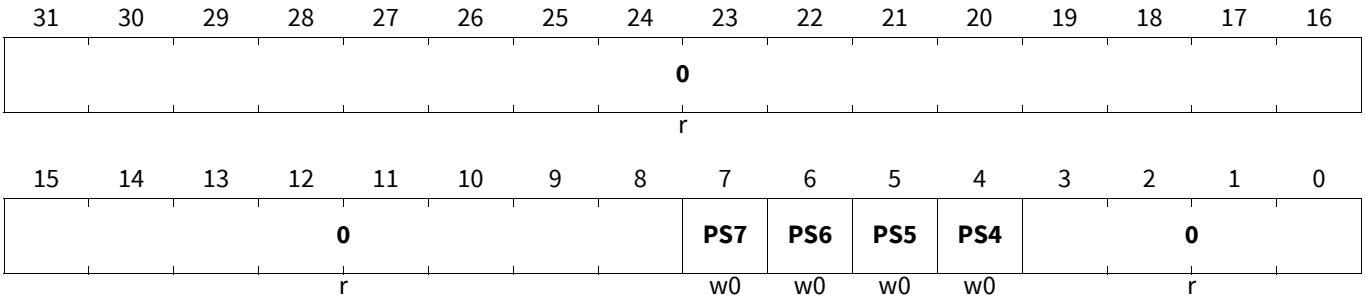
Field	Bits	Type	Description
PSx (x=4-7)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px
0	3:0, 31:8	r	**Reserved** Read as 0; should be written with 0.

Table 135 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMSR4**
Applies to **P02_OMSR4**
Applies to **P10_OMSR4**
Applies to **P11_OMSR4**
Applies to **P14_OMSR4**
Applies to **P15_OMSR4**
Applies to **P20_OMSR4**
Applies to **P21_OMSR4**
Applies to **P22_OMSR4**
Applies to **P23_OMSR4**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PSx (x=4-7)	

P32_OMSR4
Port 32 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$
P33_OMSR4
Port 33 Output Modification Set Register 4 (074_H) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PSx (x=4-7)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px

Field	Bits	Type	Description
0	3:0, 31:8	r	**Reserved** Read as 0; should be written with 0.

Table 136 Access Mode Restrictions sorted by descending priority

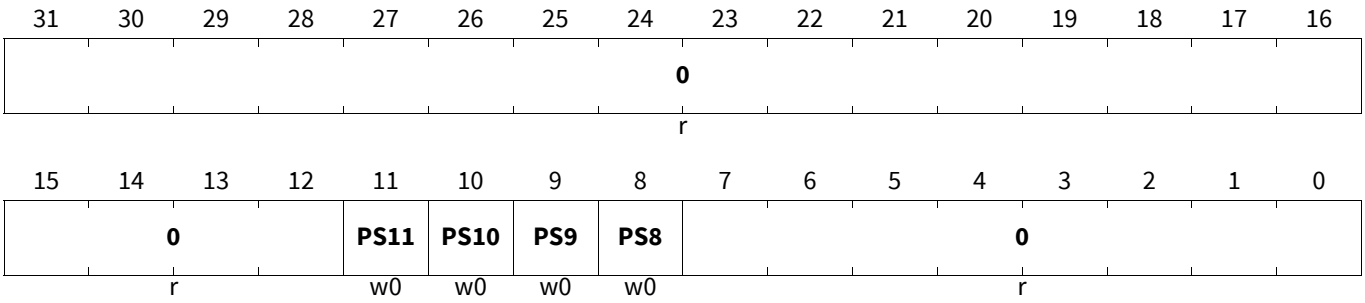
Applies to **P32_OMSR4**
Applies to **P33_OMSR4**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PSx (x=4-7)	

Port 00 Output Modification Set Register 8

Register Pn_OMSR8 sets the logic state of Pn.[11:8] port lines

P00_OMSR8
Port 00 Output Modification Set Register 8 (078_H) Application Reset Value: 0000 0000$_H$
P02_OMSR8
Port 02 Output Modification Set Register 8 (078_H) Application Reset Value: 0000 0000$_H$
P10_OMSR8
Port 10 Output Modification Set Register 8 (078_H) Application Reset Value: 0000 0000$_H$
P11_OMSR8
Port 11 Output Modification Set Register 8 (078_H) Application Reset Value: 0000 0000$_H$
P14_OMSR8
Port 14 Output Modification Set Register 8 (078_H) Application Reset Value: 0000 0000$_H$
P15_OMSR8
Port 15 Output Modification Set Register 8 (078_H) Application Reset Value: 0000 0000$_H$
P20_OMSR8
Port 20 Output Modification Set Register 8 (078_H) Application Reset Value: 0000 0000$_H$
P33_OMSR8
Port 33 Output Modification Set Register 8 (078_H) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PSx (x=8-11)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px

Field	Bits	Type	Description
0	7:0, 31:12	r	**Reserved** Read as 0; should be written with 0.

Table 137 Access Mode Restrictions sorted by descending priority

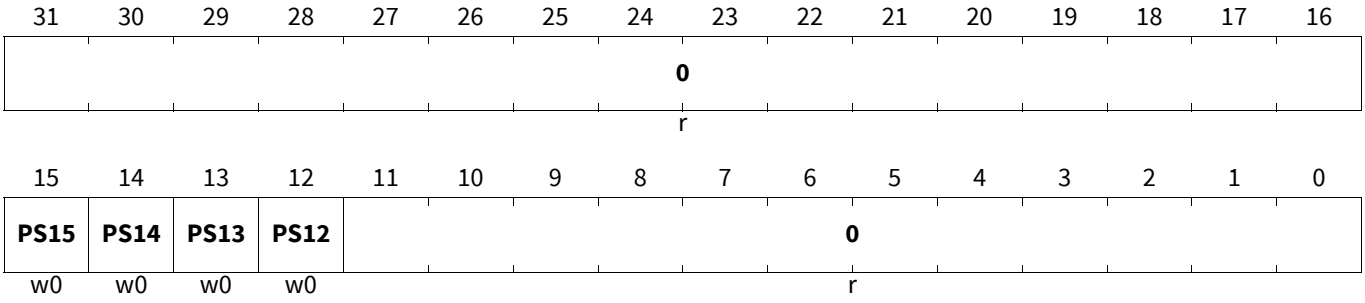
Applies to **P00_OMSR8**
Applies to **P02_OMSR8**
Applies to **P10_OMSR8**
Applies to **P11_OMSR8**
Applies to **P14_OMSR8**
Applies to **P15_OMSR8**
Applies to **P20_OMSR8**
Applies to **P33_OMSR8**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=8-11)	write access for enabled masters
Otherwise (default)	r0	PSx (x=8-11)	

Port 00 Output Modification Set Register 12

Register Pn_OMSR12 sets the logic state of Pn.[15:12] port lines

P00_OMSR12
Port 00 Output Modification Set Register 12 ($07C_H$) Application Reset Value: 0000 0000$_H$
P11_OMSR12
Port 11 Output Modification Set Register 12 ($07C_H$) Application Reset Value: 0000 0000$_H$
P20_OMSR12
Port 20 Output Modification Set Register 12 ($07C_H$) Application Reset Value: 0000 0000$_H$
P33_OMSR12
Port 33 Output Modification Set Register 12 ($07C_H$) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PSx (x=12-15)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px
0	11:0, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 138 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMSR12**
Applies to **P11_OMSR12**
Applies to **P20_OMSR12**
Applies to **P33_OMSR12**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=12-15)	write access for enabled masters
Otherwise (default)	r0	PSx (x=12-15)	

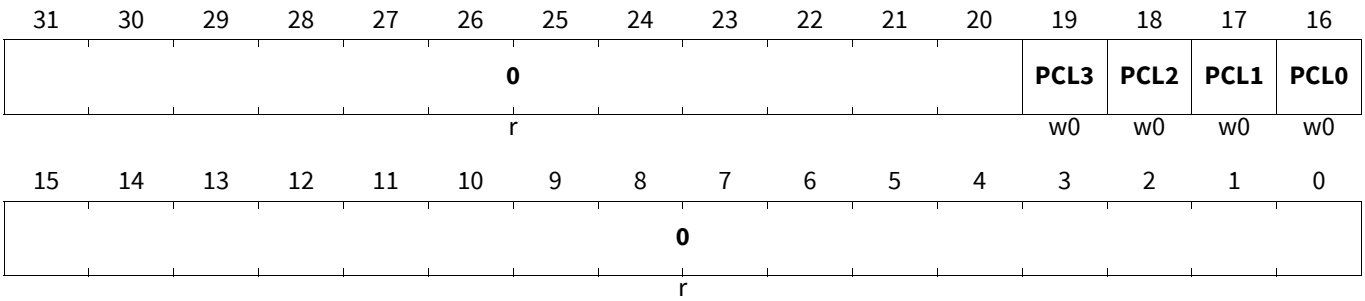
Port 00 Output Modification Clear Register 0

The port output modification clear register x, (x = 0, 4, 8, 12) contains control bits to individually clear the logic state of a single port line by manipulating the output register.

Note: Registers Pn_OMCRx (x = 0, 4, 8, 12) are virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Register Pn_OMCR0 clears the logic state of Pn.[3:0] port lines

P00_OMCR0
Port 00 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P02_OMCR0
Port 02 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P10_OMCR0
Port 10 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P11_OMCR0
Port 11 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P12_OMCR0
Port 12 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P14_OMCR0
Port 14 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P15_OMCR0
Port 15 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P20_OMCR0
Port 20 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P21_OMCR0
Port 21 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$
P22_OMCR0
Port 22 Output Modification Clear Register 0 (080_H) Application Reset Value: $0000\ 0000_H$



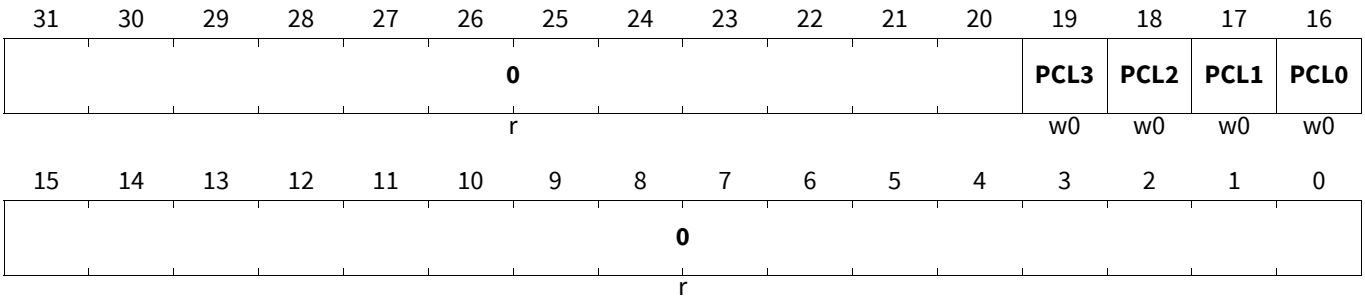
Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px
0	15:0, 31:20	r	**Reserved** Read as 0; should be written with 0.

Table 139 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMCR0**
Applies to **P02_OMCR0**
Applies to **P10_OMCR0**
Applies to **P11_OMCR0**
Applies to **P12_OMCR0**
Applies to **P14_OMCR0**
Applies to **P15_OMCR0**
Applies to **P20_OMCR0**
Applies to **P21_OMCR0**
Applies to **P22_OMCR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

P23_OMCR0
Port 23 Output Modification Clear Register 0 (080_H) Application Reset Value: 0000 0000$_H$
P32_OMCR0
Port 32 Output Modification Clear Register 0 (080_H) Application Reset Value: 0000 0000$_H$
P33_OMCR0
Port 33 Output Modification Clear Register 0 (080_H) Application Reset Value: 0000 0000$_H$
P34_OMCR0
Port 34 Output Modification Clear Register 0 (080_H) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px
0	15:0, 31:20	r	**Reserved** Read as 0; should be written with 0.

Table 140 Access Mode Restrictions sorted by descending priority

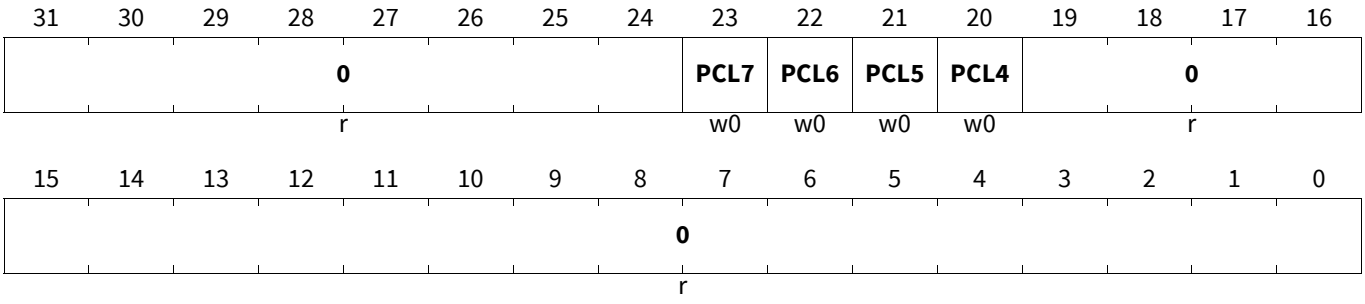
Applies to **P23_OMCR0**
Applies to **P32_OMCR0**
Applies to **P33_OMCR0**
Applies to **P34_OMCR0**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

Port 00 Output Modification Clear Register 4

Register Pn_OMCR4 clears the logic state of Pn.[7:4] port lines

P00_OMCR4
Port 00 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P02_OMCR4
Port 02 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P10_OMCR4
Port 10 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P11_OMCR4
Port 11 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P14_OMCR4
Port 14 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P15_OMCR4
Port 15 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P20_OMCR4
Port 20 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P21_OMCR4
Port 21 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P22_OMCR4
Port 22 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**
P23_OMCR4
Port 23 Output Modification Clear Register 4 **(084_H)** **Application Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
PCLx (x=4-7)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px
0	19:0, 31:24	r	**Reserved** Read as 0; should be written with 0

Table 141 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMCR4**
Applies to **P02_OMCR4**
Applies to **P10_OMCR4**
Applies to **P11_OMCR4**
Applies to **P14_OMCR4**
Applies to **P15_OMCR4**
Applies to **P20_OMCR4**
Applies to **P21_OMCR4**
Applies to **P22_OMCR4**
Applies to **P23_OMCR4**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=4-7)	

P32_OMCR4
Port 32 Output Modification Clear Register 4 (084_H) Application Reset Value: $0000\ 0000_H$
P33_OMCR4
Port 33 Output Modification Clear Register 4 (084_H) Application Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								PCL7	PCL6	PCL5	PCL4	0			
r								w0	w0	w0	w0	r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
PCLx (x=4-7)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px
0	19:0, 31:24	r	**Reserved** Read as 0; should be written with 0

Table 142 Access Mode Restrictions sorted by descending priority

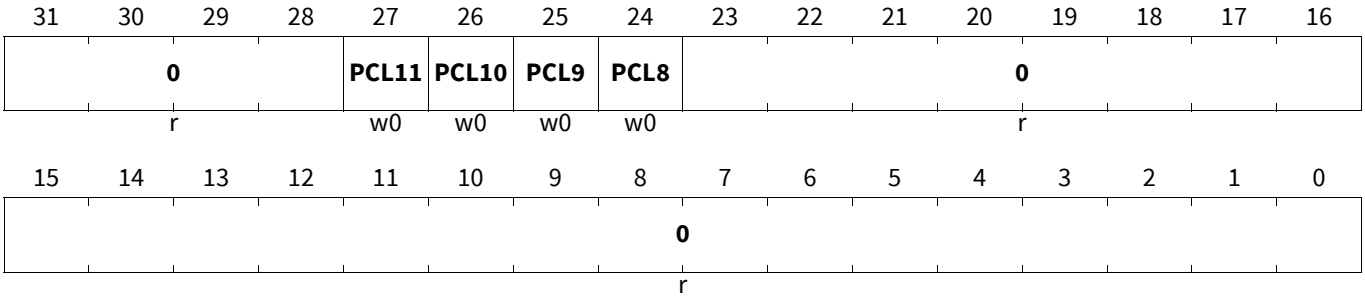
Applies to **P32_OMCR4**
Applies to **P33_OMCR4**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=4-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=4-7)	

Port 00 Output Modification Clear Register 8

Register Pn_OMCR8 clears the logic state of Pn.[11:8] port lines

P00_OMCR8
Port 00 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000$_H$
P02_OMCR8
Port 02 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000$_H$
P10_OMCR8
Port 10 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000$_H$
P11_OMCR8
Port 11 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000$_H$
P14_OMCR8
Port 14 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000$_H$
P15_OMCR8
Port 15 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000$_H$
P20_OMCR8
Port 20 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000$_H$
P33_OMCR8
Port 33 Output Modification Clear Register 8 (088_H) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PCLx (x=8-11)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px
0	23:0, 31:28	r	**Reserved** Read as 0; should be written with 0

Table 143 Access Mode Restrictions sorted by descending priority

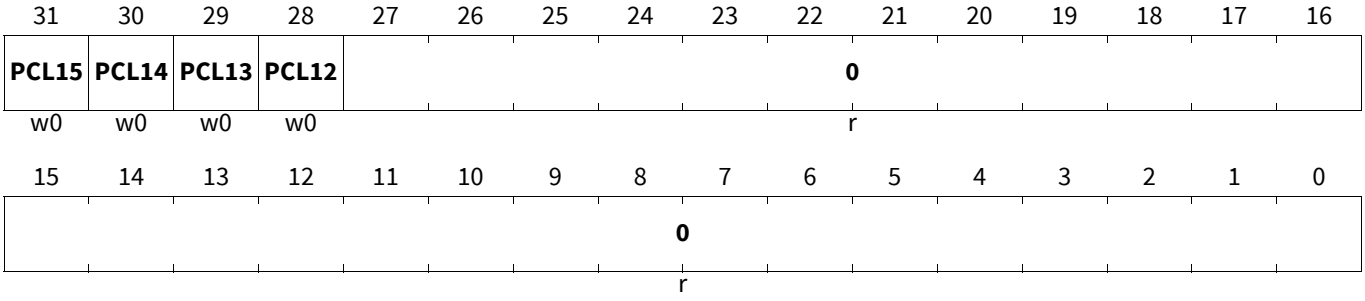
Applies to **P00_OMCR8**
Applies to **P02_OMCR8**
Applies to **P10_OMCR8**
Applies to **P11_OMCR8**
Applies to **P14_OMCR8**
Applies to **P15_OMCR8**
Applies to **P20_OMCR8**
Applies to **P33_OMCR8**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=8-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=8-11)	

Port 00 Output Modification Clear Register 12

Register Pn_OMCR12 clears the logic state of Pn.[15:12] port lines

P00_OMCR12
Port 00 Output Modification Clear Register 12 ($08C_H$) Application Reset Value: 0000 0000$_H$
P11_OMCR12
Port 11 Output Modification Clear Register 12 ($08C_H$) Application Reset Value: 0000 0000$_H$
P20_OMCR12
Port 20 Output Modification Clear Register 12 ($08C_H$) Application Reset Value: 0000 0000$_H$
P33_OMCR12
Port 33 Output Modification Clear Register 12 ($08C_H$) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PCLx (x=12-15)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px
0	27:0	r	**Reserved** Read as 0; should be written with 0

Table 144 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMCR12**
Applies to **P11_OMCR12**
Applies to **P20_OMCR12**
Applies to **P33_OMCR12**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=12-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=12-15)	

Port 00 Output Modification Set Register

The port output modification set register contains control bits that make it possible to individually set the logic state of a single port line by manipulating the output register.

Note: Register Pn_OMSR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

P00_OMSR
Port 00 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P11_OMSR
Port 11 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P20_OMSR
Port 20 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P33_OMSR
Port 33 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS15	PS14	PS13	PS12	PS11	PS10	PS9	PS8	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0
w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-15)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px
0	31:16	r	**Reserved** Read as 0; should be written with 0.

Table 145 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMSR**
Applies to **P11_OMSR**
Applies to **P20_OMSR**
Applies to **P33_OMSR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-15)	

P02_OMSR
Port 02 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P10_OMSR
Port 10 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P14_OMSR
Port 14 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P15_OMSR
Port 15 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**PS11**	**PS10**	**PS9**	**PS8**	**PS7**	**PS6**	**PS5**	**PS4**	**PS3**	**PS2**	**PS1**	**PS0**
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

Field	Bits	Type	Description
PSx (x=0-11)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px
0	15, 14, 13, 12, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 146 Access Mode Restrictions sorted by descending priority

Applies to **P02_OMSR**
Applies to **P10_OMSR**
Applies to **P14_OMSR**
Applies to **P15_OMSR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-11)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-11)	

P12_OMSR
Port 12 Output Modification Set Register (090$_H$) Application Reset Value: 0000 0000$_H$
P34_OMSR
Port 34 Output Modification Set Register (090$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	PS3	PS2	PS1	PS0
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0

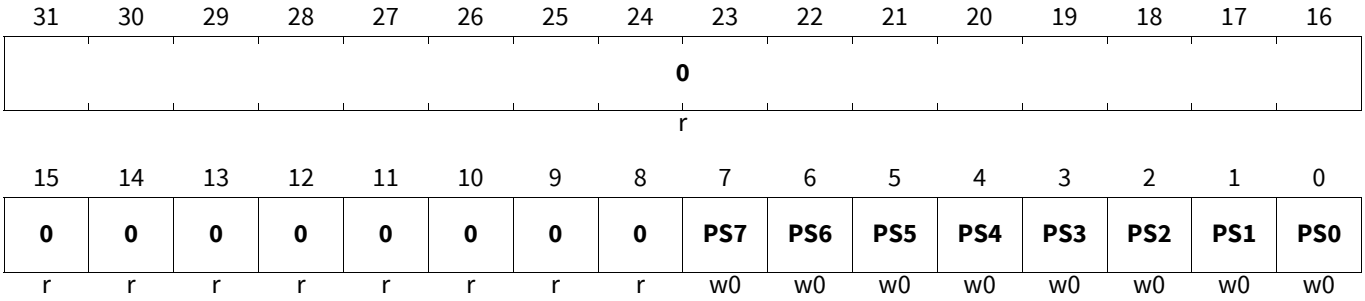
Field	Bits	Type	Description
PSx (x=0-3)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px
0	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 147 Access Mode Restrictions sorted by descending priority

Applies to **P12_OMSR**
Applies to **P34_OMSR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-3)	

P21_OMSR
Port 21 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P22_OMSR
Port 22 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P23_OMSR
Port 23 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**
P32_OMSR
Port 32 Output Modification Set Register **(090_H)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
PSx (x=0-7)	x	w0	**Set Bit x** Setting this bit will set the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Sets Pn_OUT.Px
0	15, 14, 13, 12, 11, 10, 9, 8, 31:16	r	**Reserved** Read as 0; should be written with 0.

Table 148 Access Mode Restrictions sorted by descending priority

Applies to **P21_OMSR**
Applies to **P22_OMSR**
Applies to **P23_OMSR**
Applies to **P32_OMSR**

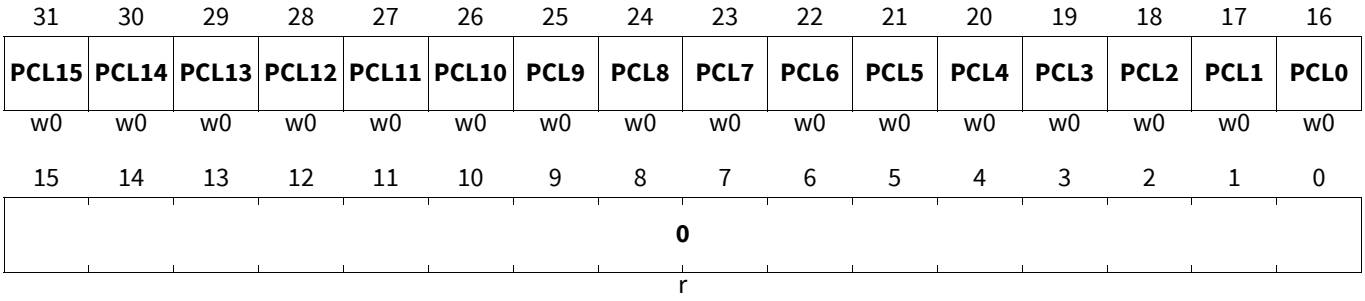
Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PSx (x=0-7)	write access for enabled masters
Otherwise (default)	r0	PSx (x=0-7)	

Port 00 Output Modification Clear Register

The port output modification clear register contains control bits that make it possible to individually clear the logic state of a single port line by manipulating the output register.

Note: Register Pn_OMCR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

P00_OMCR
Port 00 Output Modification Clear Register **(094_H)** **Application Reset Value: 0000 0000$_H$**
P11_OMCR
Port 11 Output Modification Clear Register **(094_H)** **Application Reset Value: 0000 0000$_H$**
P20_OMCR
Port 20 Output Modification Clear Register **(094_H)** **Application Reset Value: 0000 0000$_H$**
P33_OMCR
Port 33 Output Modification Clear Register **(094_H)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
PCLx (x=0-15)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px.
0	15:0	r	**Reserved** Read as 0; should be written with 0

Table 149 Access Mode Restrictions sorted by descending priority

Applies to **P00_OMCR**
Applies to **P11_OMCR**
Applies to **P20_OMCR**
Applies to **P33_OMCR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-15)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-15)	

P02_OMCR
Port 02 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**
P10_OMCR
Port 10 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**
P14_OMCR
Port 14 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**
P15_OMCR
Port 15 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**PCL11**	**PCL10**	**PCL9**	**PCL8**	**PCL7**	**PCL6**	**PCL5**	**PCL4**	**PCL3**	**PCL2**	**PCL1**	**PCL0**
r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
PCLx (x=0-11)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28	r	**Reserved** Read as 0; should be written with 0

Table 150 Access Mode Restrictions sorted by descending priority

Applies to **P02_OMCR**
Applies to **P10_OMCR**
Applies to **P14_OMCR**
Applies to **P15_OMCR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-11)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-11)	

P12_OMCR
Port 12 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**
P34_OMCR
Port 34 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**PCL3**	**PCL2**	**PCL1**	**PCL0**
r	r	r	r	r	r	r	r	r	r	r	r	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
PCLx (x=0-3)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20	r	**Reserved** Read as 0; should be written with 0

Table 151 Access Mode Restrictions sorted by descending priority

Applies to **P12_OMCR**
Applies to **P34_OMCR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-3)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-3)	

P21_OMCR
Port 21 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**
P22_OMCR
Port 22 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**
P23_OMCR
Port 23 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**
P32_OMCR
Port 32 Output Modification Clear Register **(094_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**PCL7**	**PCL6**	**PCL5**	**PCL4**	**PCL3**	**PCL2**	**PCL1**	**PCL0**
r	r	r	r	r	r	r	r	w0	w0	w0	w0	w0	w0	w0	w0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
PCLx (x=0-7)	x+16	w0	**Clear Bit x** Setting this bit will clear the corresponding bit in the port output register Pn_OUT. Read as 0. 0_B No operation 1_B Clears Pn_OUT.Px.
0	15:0, 31, 30, 29, 28, 27, 26, 25, 24	r	**Reserved** Read as 0; should be written with 0

Table 152 Access Mode Restrictions sorted by descending priority

Applies to **P21_OMCR**
Applies to **P22_OMCR**
Applies to **P23_OMCR**
Applies to **P32_OMCR**

Mode Name	Access Mode		Description
Master enabled in ACCEN	w0	PCLx (x=0-7)	write access for enabled masters
Otherwise (default)	r0	PCLx (x=0-7)	

Port 21 LVDS Pad Control Register x

The LVDS Pad Control Register controls the RX or TX functions of the LVDS pads. For usage of RX pad, bit field [7:0] are applicable. If used for TX pad, bit field [15:7] apply.

The sleep functionality of the LVDS pads is not controllable via this register. This is exclusively controlled by the HSCT module when this is connected.

The register x controls in general the pad pair 2*x and 2*x+1 of the port n.

Exceptionally when available the pad pair P14.9 and P14.10 is controlled by P14_LPCR5.

Attention: ***The bit field P21_LPCR2.PS configures the pad supply for the LVDS bias distributor for all (not-RIF) LVDS pads and for the oscillator. Therefore even if no LVDS pad is used, this field has to be configured to the correct pad supply level.***

P21_LPCRx (x=2)
Port 21 LVDS Pad Control Register x **($0A0_H$+x*4)** **Reset Value: Table 154**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0		0	0	PS	0		0		0	0	0
r	r	r	r	r		r	r	rw	r		r		r	r	r

Field	Bits	Type	Description
PS	7	rw	**Pad Supply Selection** Selects between 5V or 3.3V supply on V_{EXT} for the pad-pair. Used in RX and TX pads! 0_B 3.3V supply 1_B 5V supply
0	0, 1, 2, 5:3, 6, 8, 9, 11:10, 12, 13, 14, 15, 31:16	r	**Reserved** Read as 0; should be written with 0

Table 153 Access Mode Restrictions of P21_LPCRx (x=2) sorted by descending priority

Mode Name	Access Mode		Description
Master enabled in ACCEN and Supervisor Mode and ENDINIT	rw	PS	write access for enabled masters
Otherwise (default)	r	PS	

Table 154 Reset Values of P21_LPCRx (x=2)

Reset Type	Reset Value	Note
After SSW execution	0000 0080$_H$	Initial value of RX depends on trimming

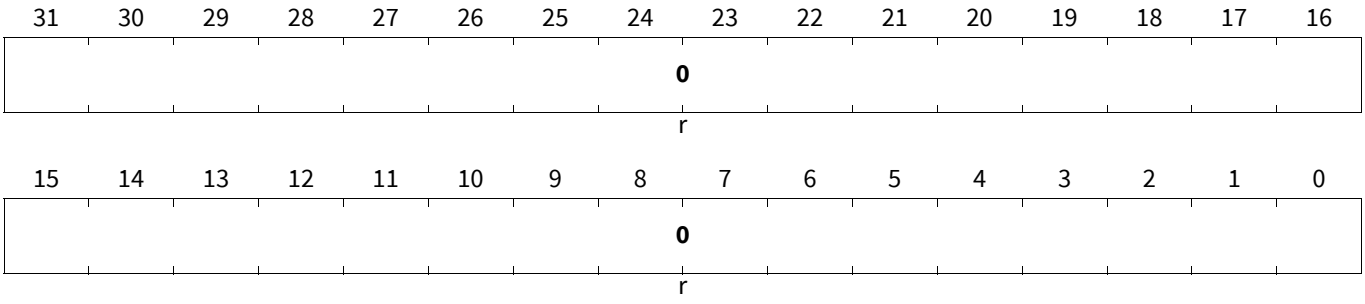
Port 00 Access Enable Register 1

Each port has its own dedicated ACCEN0 and ACCEN1 registers.

The Access Enable Register 1 controls write[1)] access for transactions with the on chip bus master TAG ID 100000B to 111111B (see On Chip Bus chapter for the products TAG ID <-> master peripheral mapping). The BPI_FPI is prepared for a 6-bit TAG ID. ACCEN1 is not implemented with register bits as the related TAG IDs are not used in this product.

Mapping of TAG IDs to ACCEN1.ENx: EN0 -> TAG ID 100000B, EN1 -> TAG ID 100001B, ... ,EN31 -> TAG ID 111111B.

P00_ACCEN1
Port 00 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P02_ACCEN1
Port 02 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P10_ACCEN1
Port 10 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P11_ACCEN1
Port 11 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P12_ACCEN1
Port 12 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P14_ACCEN1
Port 14 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P15_ACCEN1
Port 15 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P20_ACCEN1
Port 20 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P21_ACCEN1
Port 21 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P22_ACCEN1
Port 22 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**



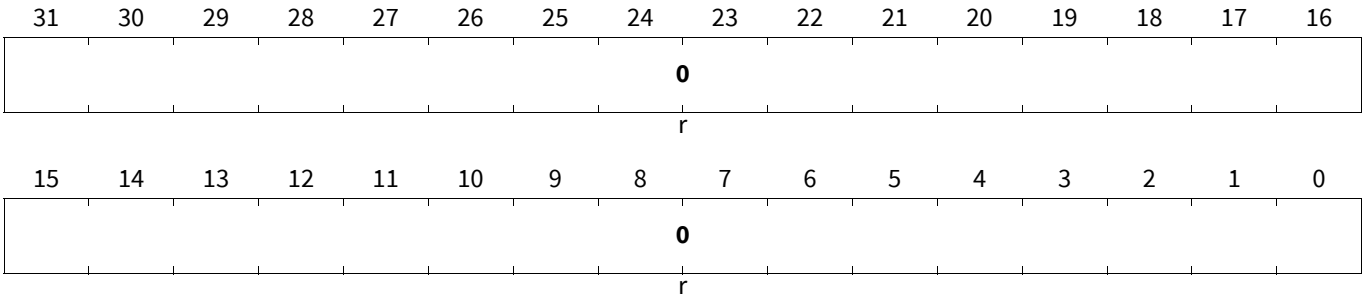
Field	Bits	Type	Description
0	31:0	r	**Reserved** Read as 0; should be written with 0

Table 155 Access Mode Restrictions sorted by descending priority

Applies to **P00_ACCEN1**
Applies to **P02_ACCEN1**
Applies to **P10_ACCEN1**
Applies to **P11_ACCEN1**
Applies to **P12_ACCEN1**
Applies to **P14_ACCEN1**
Applies to **P15_ACCEN1**
Applies to **P20_ACCEN1**
Applies to **P21_ACCEN1**
Applies to **P22_ACCEN1**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	-	See bit field definitions above	write access only for masters with supervisor mode
Otherwise (default)	-	See bit field definitions above	

P23_ACCEN1
Port 23 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P32_ACCEN1
Port 32 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P33_ACCEN1
Port 33 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**
P34_ACCEN1
Port 34 Access Enable Register 1 **(0F8$_H$)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
0	31:0	r	**Reserved** Read as 0; should be written with 0

Table 156 Access Mode Restrictions sorted by descending priority

Applies to **P23_ACCEN1**
Applies to **P32_ACCEN1**
Applies to **P33_ACCEN1**
Applies to **P34_ACCEN1**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	-	See bit field definitions above	write access only for masters with supervisor mode
Otherwise (default)	-	See bit field definitions above	

Port 00 Access Enable Register 0

Each port has its own dedicated ACCEN0 and ACCEN1 registers.

The Access Enable Register 0 controls write[1)] access for transactions with the on chip bus master TAG ID 000000B to 011111B (see On Chip Bus chapter for the products TAG ID <-> master peripheral mapping). The BPI_FPI is prepared for a 6-bit TAG ID.The registers ACCEN0 and ACCEN1 are providing one enable bit for each possible 6-bit TAG ID encoding.

Mapping of TAG IDs to ACCEN0.ENx: EN0 -> TAG ID 000000B, EN1 -> TAG ID 000001B , ... ,EN31 -> TAG ID 011111B.

1) The BPI_FPI Access Enable functionality controls only write transactions to the kernel registers. Read transactions are not influenced. SW has to take care for destructive/modifying read functionality in kernel registers.

P00_ACCEN0
Port 00 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P02_ACCEN0
Port 02 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P10_ACCEN0
Port 10 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P11_ACCEN0
Port 11 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P12_ACCEN0
Port 12 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P14_ACCEN0
Port 14 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P15_ACCEN0
Port 15 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P20_ACCEN0
Port 20 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P21_ACCEN0
Port 21 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P22_ACCEN0
Port 22 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN31	**EN30**	**EN29**	**EN28**	**EN27**	**EN26**	**EN25**	**EN24**	**EN23**	**EN22**	**EN21**	**EN20**	**EN19**	**EN18**	**EN17**	**EN16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	**EN14**	**EN13**	**EN12**	**EN11**	**EN10**	**EN9**	**EN8**	**EN7**	**EN6**	**EN5**	**EN4**	**EN3**	**EN2**	**EN1**	**EN0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-31)	x	rw	**Access Enable for Master TAG ID x** This bit enables write access to the module kernel addresses for transactions with the Master TAG ID n 0_B Write access will not be executed 1_B Write access will be executed

Table 157 Access Mode Restrictions sorted by descending priority

Applies to **P00_ACCEN0**
Applies to **P02_ACCEN0**
Applies to **P10_ACCEN0**
Applies to **P11_ACCEN0**
Applies to **P12_ACCEN0**
Applies to **P14_ACCEN0**
Applies to **P15_ACCEN0**
Applies to **P20_ACCEN0**
Applies to **P21_ACCEN0**
Applies to **P22_ACCEN0**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	rw	ENx (x=0-31)	write access only for masters with supervisor mode
Otherwise (default)	r	ENx (x=0-31)	

P23_ACCEN0
Port 23 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P32_ACCEN0
Port 32 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P33_ACCEN0
Port 33 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**
P34_ACCEN0
Port 34 Access Enable Register 0 **(0FC$_H$)** **Application Reset Value: FFFF FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN31	**EN30**	**EN29**	**EN28**	**EN27**	**EN26**	**EN25**	**EN24**	**EN23**	**EN22**	**EN21**	**EN20**	**EN19**	**EN18**	**EN17**	**EN16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN15	**EN14**	**EN13**	**EN12**	**EN11**	**EN10**	**EN9**	**EN8**	**EN7**	**EN6**	**EN5**	**EN4**	**EN3**	**EN2**	**EN1**	**EN0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-31)	x	rw	**Access Enable for Master TAG ID x** This bit enables write access to the module kernel addresses for transactions with the Master TAG ID n 0_B Write access will not be executed 1_B Write access will be executed

Table 158 Access Mode Restrictions sorted by descending priority

Applies to **P23_ACCEN0**
Applies to **P32_ACCEN0**
Applies to **P33_ACCEN0**
Applies to **P34_ACCEN0**

Mode Name	Access Mode		Description
Supervisor Mode and Safety ENDINIT	rw	ENx (x=0-31)	write access only for masters with supervisor mode
Otherwise (default)	r	ENx (x=0-31)	

14.4 Device Specific Connectivity Documentation

The connectivity of the Ports is documented in the Pinning documentation of each device.

14.5 Revision History

Table 159 Revision History

Reference	Changes to Previous Version	Comment
V1.8.20		
–	This is the first version for TC33xEXT.	–
V1.8.21		
–	No content of this Appx changed. TC3Ax Appx added to delivery package and change in Feature List of family chapter.	

15 Safety Management Unit (SMU)

This chapter describes the Safety Management Unit (short SMU) module of the TC33xEXT.

15.1 TC33xEXT Specific IP Configuration

See features in family spec.

15.2 TC33xEXT Specific Register Set

SMU_core Specific Register Set

Register Address Space Table

Table 160 Register Address Space - SMU

Module	Base Address	End Address	Note
SMU	$F0036800_H$	$F0036FFF_H$	FPI slave interface

Register Overview Table

Table 161 Register Overview - SMU (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SMU_CLC	Clock Control Register	000_H	U,SV	SV,P	Application Reset	See Family Spec
SMU_ID	Module Identification Register	008_H	U,SV	BE	Application Reset	See Family Spec
SMU_CMD	Command Register	020_H	U,SV	SV,P,32	Application Reset	See Family Spec
SMU_STS	Status Register	024_H	U,SV	SV,P,32	Application Reset	See Family Spec
SMU_FSP	Fault Signaling Protocol	028_H	U,SV	SV,P,SE,32	PowerOn Reset	See Family Spec
SMU_AGC	Alarm Global Configuration	$02C_H$	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTC	Recovery Timer Configuration	030_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_KEYS	Key Register	034_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_DBG	Debug Register	038_H	U,SV	BE	PowerOn Reset	See Family Spec

Table 161 Register Overview - SMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SMU_PCTL	Port Control	$03C_H$	U,SV	SV,P,SE,32	PowerOn Reset	See Family Spec
SMU_AFCNT	Alarm and Fault Counter	040_H	U,SV	BE	PowerOn Reset	See Family Spec
SMU_RTAC00	Recovery Timer 0 Alarm Configuration 0	060_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC01	Recovery Timer 0 Alarm Configuration 1	064_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC10	Recovery Timer 1 Alarm Configuration 0	068_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RTAC11	Recovery Timer 1 Alarm Configuration 1	$06C_H$	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_AEX	Alarm Executed Status Register	070_H	U,SV	BE	Application Reset	See Family Spec
SMU_AEXCLR	Alarm Executed Status Clear Register	074_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_AGiCFj (i=0-1;j=0-2) (i=2-5;j=0-2) (i=6;j=0-2) (i=7;j=0-2) (i=8;j=0-2) (i=9;j=0-2) (i=10;j=0-2) (i=11;j=0-2)	Alarm Configuration Register	100_H+i*12+j*4	U,SV	SV,P,SE,32	Application Reset	5
SMU_AGiFSP (i=0-11)	SMU_core FSP Configuration Register	190_H+i*4	U,SV	SV,P,SE,32	Application Reset	9
SMU_AGi (i=0-11)	Alarm Status Register	$1C0_H$+i*4	U,SV	SV,P,SE,32	Application Reset	13
SMU_ADi (i=0-11)	Alarm Debug Register	200_H+i*4	U,SV	BE	PowerOn Reset	17
SMU_RMCTL	Register Monitor Control	300_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec

Table 161 Register Overview - SMU (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SMU_RMEF	Register Monitor Error Flags	304_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_RMSTS	Register Monitor Self Test Status	308_H	U,SV	SV,P,SE,32	Application Reset	See Family Spec
SMU_OCS	OCDS Control and Status	$7E8_H$	U,SV	SV,P,OEN	Debug Reset	See Family Spec
SMU_ACCEN1	SMU_core Access Enable Register 1	$7F8_H$	U,SV	BE	Application Reset	See Family Spec
SMU_ACCEN0	SMU_core Access Enable Register 0	$7FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

SMU_stdby Specific Register Set

For SMU_stdby specific register set refer to the Power Management System chapter.

15.3 TC33xEXT Specific Registers

15.3.1 TC33xEXT Specific Registers

15.3.1.1 FPI slave interface

Alarm Configuration Register

SMU_AGiCFj (i=0-1;j=0-2)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**CF24**	**CF23**	**CF22**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	rw	rw	rw	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**CF14**	**CF13**	**CF12**	**CF11**	**CF10**	**CF9**	**CF8**	**CF7**	**CF6**	**CF5**	**CF4**	**0**	**CF2**	**CF1**	**CF0**
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-2,4-14,22-24)	z	rw	**Configuration flag x (x=0-2) for alarm z belonging to alarm group i.** The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiCFj (i=2-5;j=0-2)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiCFj (i=6;j=0-2)

Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**CF25**	**CF24**	**CF23**	**0**	**CF21**	**CF20**	**CF19**	**CF18**	**CF17**	**CF16**
r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**CF8**	**CF7**	**CF6**	**CF5**	**CF4**	**CF3**	**CF2**	**CF1**	**CF0**
r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-8,16-21,23-25)	z	rw	**Configuration flag x (x=0-2) for alarm z belonging to alarm group i.** The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1
0	31, 30, 29, 28, 27, 26, 22, 15, 14, 13, 12, 11, 10, 9	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiCFj (i=7;j=0-2)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF31	**CF30**	**CF29**	**CF28**	**CF27**	**CF26**	**CF25**	**CF24**	**CF23**	**CF22**	**CF21**	**CF20**	**0**	**0**	**CF17**	**CF16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	r	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	**CF14**	**CF13**	**CF12**	**0**	**0**	**0**	**CF8**	**CF7**	**CF6**	**CF5**	**CF4**	**CF3**	**CF2**	**CF1**	**CF0**
rw	rw	rw	rw	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-8,12-17,20-31)	z	rw	**Configuration flag x (x=0-2) for alarm z belonging to alarm group i.** The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1
0	19, 18, 11, 10, 9	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiCFj (i=8;j=0,2)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0001 $FC00_H$**
SMU_AGiCFj (i=8;j=1)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CF31	**CF30**	**CF29**	**CF28**	**CF27**	**CF26**	**CF25**	**0**	**CF23**	**CF22**	**CF21**	**CF20**	**CF19**	**CF18**	**CF17**	**CF16**
rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**CF11**	**CF10**	**CF9**	**CF8**	**CF7**	**CF6**	**CF5**	**CF4**	**CF3**	**CF2**	**CF1**	**CF0**
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-11,16-23,25-31)	z	rw	**Configuration flag x (x=0-2) for alarm z belonging to alarm group i.** The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1
0	24, 15, 14, 13, 12	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiCFj (i=9;j=0-2)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**CF30**	**0**	**CF28**	**0**	**0**	**0**	**0**	**0**	**CF22**	**CF21**	**CF20**	**0**	**0**	**CF17**	**CF16**
r	rw	r	rw	r	r	r	r	r	rw	rw	rw	r	r	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**CF5**	**0**	**CF3**	**0**	**CF1**	**CF0**
rw	r	r	r	r	r	r	r	r	r	rw	r	rw	r	rw	rw

Field	Bits	Type	Description
CFz (z=0-1,3,5,15-17,20-22,28,30)	z	rw	**Configuration flag x (x=0-2) for alarm z belonging to alarm group i.** The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1
0	31, 29, 27, 26, 25, 24, 23, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiCFj (i=10;j=0)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0000 0000_H**
SMU_AGiCFj (i=10;j=1-2)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0003 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**CF22**	**CF21**	**CF20**	**0**	**CF18**	**CF17**	**CF16**
r	r	r	r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF15	**CF14**	**CF13**	**CF12**	**CF11**	**CF10**	**CF9**	**CF8**	**CF7**	**CF6**	**CF5**	**CF4**	**CF3**	**CF2**	**CF1**	**CF0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-18,20-22)	z	rw	**Configuration flag x (x=0-2) for alarm z belonging to alarm group i.** The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiCFj (i=11;j=0-2)
Alarm Configuration Register **(100_H+i*12+j*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**CF13**	**CF12**	**0**	**0**	**CF9**	**0**	**CF7**	**CF6**	**CF5**	**CF4**	**CF3**	**CF2**	**CF1**	**CF0**
r	r	rw	rw	r	r	rw	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CFz (z=0-7,9,12-13)	z	rw	**Configuration flag x (x=0-2) for alarm z belonging to alarm group i.** The configuration flags 0, 1 and 2 must be used together to define the behavior of the SMU_core when a fault state is reported by the alarm n belonging to this group. 0_B Configuration flag x (x=0-2) is set to 0 1_B Configuration flag x (x=0-2) is set to 1
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 11, 10, 8	r	**Reserved** Read as 0; should be written with 0.

SMU_core FSP Configuration Register

SMU_AGiFSP (i=0-1)
SMU_core FSP Configuration Register **(190_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**FE24**	**FE23**	**FE22**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	rw	rw	rw	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**FE14**	**FE13**	**FE12**	**FE11**	**FE10**	**FE9**	**FE8**	**FE7**	**FE6**	**FE5**	**FE4**	**0**	**FE2**	**FE1**	**FE0**
r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-2,4-14,22-24)	z	rw	**Fault signaling configuration flag for alarm z belonging to alarm group i.** 0_B FSP disabled for this alarm event 1_B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiFSP (i=2-5)

SMU_core FSP Configuration Register **(190_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiFSP (i=6)

SMU_core FSP Configuration Register **(190_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**FE25**	**FE24**	**FE23**	**0**	**FE21**	**FE20**	**FE19**	**FE18**	**FE17**	**FE16**
r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**FE8**	**FE7**	**FE6**	**FE5**	**FE4**	**FE3**	**FE2**	**FE1**	**FE0**
r	r	r	r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-8,16-21,23-25)	z	rw	**Fault signaling configuration flag for alarm z belonging to alarm group i.** 0_B FSP disabled for this alarm event 1_B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 22, 15, 14, 13, 12, 11, 10, 9	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiFSP (i=7)

SMU_core FSP Configuration Register **(190_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FE31	**FE30**	**FE29**	**FE28**	**FE27**	**FE26**	**FE25**	**FE24**	**FE23**	**FE22**	**FE21**	**FE20**	**0**	**0**	**FE17**	**FE16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	r	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	**FE14**	**FE13**	**FE12**	**0**	**0**	**0**	**FE8**	**FE7**	**FE6**	**FE5**	**FE4**	**FE3**	**FE2**	**FE1**	**FE0**
rw	rw	rw	rw	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-8,12-17,20-31)	z	rw	**Fault signaling configuration flag for alarm z belonging to alarm group i.** 0_B FSP disabled for this alarm event 1_B FSP enabled for this alarm event
0	19, 18, 11, 10, 9	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiFSP (i=8)

SMU_core FSP Configuration Register **(190_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FE31	**FE30**	**FE29**	**FE28**	**FE27**	**FE26**	**FE25**	**0**	**FE23**	**FE22**	**FE21**	**FE20**	**FE19**	**FE18**	**FE17**	**FE16**
rw	rw	rw	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**FE11**	**FE10**	**FE9**	**FE8**	**FE7**	**FE6**	**FE5**	**FE4**	**FE3**	**FE2**	**FE1**	**FE0**
r	r	r	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-11,16-23,25-31)	z	rw	**Fault signaling configuration flag for alarm z belonging to alarm group i.** 0_B FSP disabled for this alarm event 1_B FSP enabled for this alarm event
0	24, 15, 14, 13, 12	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiFSP (i=9)

SMU_core FSP Configuration Register **(190_H+i*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**FE30**	**0**	**FE28**	**0**	**0**	**0**	**0**	**0**	**FE22**	**FE21**	**FE20**	**0**	**0**	**FE17**	**FE16**
r	rw	r	rw	r	r	r	r	r	rw	rw	rw	r	r	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**FE5**	**0**	**FE3**	**0**	**FE1**	**FE0**
rw	r	r	r	r	r	r	r	r	r	rw	r	rw	r	rw	rw

Field	Bits	Type	Description
FEz (z=0-1,3,5,15-17,20-22,28,30)	z	rw	**Fault signaling configuration flag for alarm z belonging to alarm group i.** 0_B FSP disabled for this alarm event 1_B FSP enabled for this alarm event
0	31, 29, 27, 26, 25, 24, 23, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiFSP (i=10)

SMU_core FSP Configuration Register **(190_H+i*4)** **Application Reset Value: 0003 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**FE22**	**FE21**	**FE20**	**0**	**FE18**	**FE17**	**FE16**
r	r	r	r	r	r	r	r	r	rw	rw	rw	r	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FE15	**FE14**	**FE13**	**FE12**	**FE11**	**FE10**	**FE9**	**FE8**	**FE7**	**FE6**	**FE5**	**FE4**	**FE3**	**FE2**	**FE1**	**FE0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-18,20-22)	z	rw	**Fault signaling configuration flag for alarm z belonging to alarm group i.** 0_B FSP disabled for this alarm event 1_B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	**Reserved** Read as 0; should be written with 0.

SMU_AGiFSP (i=11)

SMU_core FSP Configuration Register **(190_H+i*4)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**FE13**	**FE12**	**0**	**0**	**FE9**	**0**	**FE7**	**FE6**	**FE5**	**FE4**	**FE3**	**FE2**	**FE1**	**FE0**
r	r	rw	rw	r	r	rw	r	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FEz (z=0-7,9,12-13)	z	rw	**Fault signaling configuration flag for alarm z belonging to alarm group i.** 0_B FSP disabled for this alarm event 1_B FSP enabled for this alarm event
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 11, 10, 8	r	**Reserved** Read as 0; should be written with 0.

Alarm Status Register

Refer to Alarm Status Registers for the conditions to set and reset the status flag by software.

SMU_AGi (i=0-1)

Alarm Status Register **($1C0_H$+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**SF24**	**SF23**	**SF22**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	rwh	rwh	rwh	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**SF14**	**SF13**	**SF12**	**SF11**	**SF10**	**SF9**	**SF8**	**SF7**	**SF6**	**SF5**	**SF4**	**0**	**SF2**	**SF1**	**SF0**
r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-2,4-14,22-24)	z	rwh	**Status flag for alarm z belonging to alarm group i.** 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	**Reserved** Read as 0; should be written with 0.

SMU_AGi (i=2-5)

Alarm Status Register **($1C0_H$+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	r	**Reserved** Read as 0; should be written with 0.

SMU_AGi (i=6)

Alarm Status Register **($1C0_H$+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**SF25**	**SF24**	**SF23**	**0**	**SF21**	**SF20**	**SF19**	**SF18**	**SF17**	**SF16**
r	r	r	r	r	r	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**SF8**	**SF7**	**SF6**	**SF5**	**SF4**	**SF3**	**SF2**	**SF1**	**SF0**
r	r	r	r	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-8,16-21,23-25)	z	rwh	**Status flag for alarm z belonging to alarm group i.** 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 22, 15, 14, 13, 12, 11, 10, 9	r	**Reserved** Read as 0; should be written with 0.

SMU_AGi (i=7)

Alarm Status Register **($1C0_H$+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SF31	**SF30**	**SF29**	**SF28**	**SF27**	**SF26**	**SF25**	**SF24**	**SF23**	**SF22**	**SF21**	**SF20**	**0**	**0**	**SF17**	**SF16**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	r	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	**SF14**	**SF13**	**SF12**	**0**	**0**	**0**	**SF8**	**SF7**	**SF6**	**SF5**	**SF4**	**SF3**	**SF2**	**SF1**	**SF0**
rwh	rwh	rwh	rwh	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-8,12-17,20-31)	z	rwh	**Status flag for alarm z belonging to alarm group i.** 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	19, 18, 11, 10, 9	r	**Reserved** Read as 0; should be written with 0.

SMU_AGi (i=8)

Alarm Status Register **($1C0_H$+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SF31	**SF30**	**SF29**	**SF28**	**SF27**	**SF26**	**SF25**	**0**	**SF23**	**SF22**	**SF21**	**SF20**	**SF19**	**SF18**	**SF17**	**SF16**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**SF11**	**SF10**	**SF9**	**SF8**	**SF7**	**SF6**	**SF5**	**SF4**	**SF3**	**SF2**	**SF1**	**SF0**
r	r	r	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-11,16-23,25-31)	z	rwh	**Status flag for alarm z belonging to alarm group i.** 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	24, 15, 14, 13, 12	r	**Reserved** Read as 0; should be written with 0.

SMU_AGi (i=9)

Alarm Status Register **($1C0_H$+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**SF30**	**0**	**SF28**	**0**	**0**	**0**	**0**	**0**	**SF22**	**SF21**	**SF20**	**0**	**0**	**SF17**	**SF16**
r	rwh	r	rwh	r	r	r	r	r	rwh	rwh	rwh	r	r	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SF5**	**0**	**SF3**	**0**	**SF1**	**SF0**
rwh	r	r	r	r	r	r	r	r	r	rwh	r	rwh	r	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-1,3,5,15-17,20-22,28,30)	z	rwh	**Status flag for alarm z belonging to alarm group i.** 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 29, 27, 26, 25, 24, 23, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	**Reserved** Read as 0; should be written with 0.

SMU_AGi (i=10)

Alarm Status Register **($1C0_H$+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**SF22**	**SF21**	**SF20**	**0**	**SF18**	**SF17**	**SF16**
r	r	r	r	r	r	r	r	r	rwh	rwh	rwh	r	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SF15	**SF14**	**SF13**	**SF12**	**SF11**	**SF10**	**SF9**	**SF8**	**SF7**	**SF6**	**SF5**	**SF4**	**SF3**	**SF2**	**SF1**	**SF0**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-18,20-22)	z	rwh	**Status flag for alarm z belonging to alarm group i.** 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	**Reserved** Read as 0; should be written with 0.

SMU_AGi (i=11)

Alarm Status Register **($1C0_H$+i*4)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**SF13**	**SF12**	**0**	**0**	**SF9**	**0**	**SF7**	**SF6**	**SF5**	**SF4**	**SF3**	**SF2**	**SF1**	**SF0**
r	r	rwh	rwh	r	r	rwh	r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SFz (z=0-7,9,12-13)	z	rwh	**Status flag for alarm z belonging to alarm group i.** 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 11, 10, 8	r	**Reserved** Read as 0; should be written with 0.

Alarm Debug Register

Note: Writing to this register has no effect

SMU_ADi (i=0-1)
Alarm Debug Register **(200_H+i*4)** **PowerOn Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**DF24**	**DF23**	**DF22**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	rh	rh	rh	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**DF14**	**DF13**	**DF12**	**DF11**	**DF10**	**DF9**	**DF8**	**DF7**	**DF6**	**DF5**	**DF4**	**0**	**DF2**	**DF1**	**DF0**
r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	r	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-2,4-14,22-24)	z	rh	**Diagnosis flag for alarm z belonging to alarm group i.** The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 21, 20, 19, 18, 17, 16, 15, 3	r	**Reserved** Read as 0; should be written with 0.

SMU_ADi (i=2-5)
Alarm Debug Register **(200_H+i*4)** **PowerOn Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0	r	**Reserved** Read as 0; should be written with 0.

SMU_ADi (i=6)
Alarm Debug Register **(200_H+i*4)** **PowerOn Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**DF25**	**DF24**	**DF23**	**0**	**DF21**	**DF20**	**DF19**	**DF18**	**DF17**	**DF16**
r	r	r	r	r	r	rh	rh	rh	r	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**DF8**	**DF7**	**DF6**	**DF5**	**DF4**	**DF3**	**DF2**	**DF1**	**DF0**
r	r	r	r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-8,16-21,23-25)	z	rh	**Diagnosis flag for alarm z belonging to alarm group i.** The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 22, 15, 14, 13, 12, 11, 10, 9	r	**Reserved** Read as 0; should be written with 0.

SMU_ADi (i=7)
Alarm Debug Register **(200_H+i*4)** **PowerOn Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DF31	**DF30**	**DF29**	**DF28**	**DF27**	**DF26**	**DF25**	**DF24**	**DF23**	**DF22**	**DF21**	**DF20**	**0**	**0**	**DF17**	**DF16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	r	r	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	**DF14**	**DF13**	**DF12**	**0**	**0**	**0**	**DF8**	**DF7**	**DF6**	**DF5**	**DF4**	**DF3**	**DF2**	**DF1**	**DF0**
rh	rh	rh	rh	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-8,12-17,20-31)	z	rh	**Diagnosis flag for alarm z belonging to alarm group i.** The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	19, 18, 11, 10, 9	r	**Reserved** Read as 0; should be written with 0.

SMU_ADi (i=8)
Alarm Debug Register **(200_H+i*4)** **PowerOn Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DF31	**DF30**	**DF29**	**DF28**	**DF27**	**DF26**	**DF25**	**0**	**DF23**	**DF22**	**DF21**	**DF20**	**DF19**	**DF18**	**DF17**	**DF16**
rh	rh	rh	rh	rh	rh	rh	r	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**DF11**	**DF10**	**DF9**	**DF8**	**DF7**	**DF6**	**DF5**	**DF4**	**DF3**	**DF2**	**DF1**	**DF0**
r	r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-11,16-23,25-31)	z	rh	**Diagnosis flag for alarm z belonging to alarm group i.** The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	24, 15, 14, 13, 12	r	**Reserved** Read as 0; should be written with 0.

SMU_ADi (i=9)
Alarm Debug Register **(200_H+i*4)** **PowerOn Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**DF30**	**0**	**DF28**	**0**	**0**	**0**	**0**	**0**	**DF22**	**DF21**	**DF20**	**0**	**0**	**DF17**	**DF16**
r	rh	r	rh	r	r	r	r	r	rh	rh	rh	r	r	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**DF5**	**0**	**DF3**	**0**	**DF1**	**DF0**
rh	r	r	r	r	r	r	r	r	r	rh	r	rh	r	rh	rh

Field	Bits	Type	Description
DFz (z=0-1,3,5,15-17,20-22,28,30)	z	rh	**Diagnosis flag for alarm z belonging to alarm group i.** The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 29, 27, 26, 25, 24, 23, 19, 18, 14, 13, 12, 11, 10, 9, 8, 7, 6, 4, 2	r	**Reserved** Read as 0; should be written with 0.

SMU_ADi (i=10)
Alarm Debug Register **(200_H+i*4)** **PowerOn Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**DF22**	**DF21**	**DF20**	**0**	**DF18**	**DF17**	**DF16**
r	r	r	r	r	r	r	r	r	rh	rh	rh	r	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DF15	**DF14**	**DF13**	**DF12**	**DF11**	**DF10**	**DF9**	**DF8**	**DF7**	**DF6**	**DF5**	**DF4**	**DF3**	**DF2**	**DF1**	**DF0**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-18,20-22)	z	rh	**Diagnosis flag for alarm z belonging to alarm group i.** The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 19	r	**Reserved** Read as 0; should be written with 0.

SMU_ADi (i=11)
Alarm Debug Register **(200_H+i*4)** **PowerOn Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**DF13**	**DF12**	**0**	**0**	**DF9**	**0**	**DF7**	**DF6**	**DF5**	**DF4**	**DF3**	**DF2**	**DF1**	**DF0**
r	r	rh	rh	r	r	rh	r	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
DFz (z=0-7,9,12-13)	z	rh	**Diagnosis flag for alarm z belonging to alarm group i.** The diagnosis registers make a snapshot of the alarm group status registers when either the executed alarm action is a reset or a state machine transition to FAULT state takes place. 0_B Status flag z does not report a fault condition 1_B Status flag z reports a fault condition

Field	Bits	Type	Description
0	31, 30, 29, 28, 27, 26, 25, 24, 23, 22, 21, 20, 19, 18, 17, 16, 15, 14, 11, 10, 8	r	**Reserved** Read as 0; should be written with 0.

15.4 TC33xEXT Specific Alarm Mapping

This section defines the mapping between the alarm signals at the input of the SMU in the TC33xEXT and the alarm. For that purpose alarm groups are defined. There is a one-to-one relationship between an alarm group index ALM<n>[index] signal and the alarm configuration and status registers (AG<n>[index]). A group is made of up to 32 alarms; for convenience some entries may be reserved.

15.4.1 TC33xEXT Specific Pre-Alarms

There are situations where it is not necessary to implement configuration and status registers for every internal alarm event; a typical case is a module with multiple SRAMs. For that, alarm inputs, called pre-alarms, are combined together with a logical OR internally in SMU. The result is then connected to the alarm group.

MTU Pre-Alarm Mapping

Table 162 MTU Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
CPU0.DMEM - Correctable error CPU0.DLMU - Correctable error CPU0.DMEM1 - Correctable error	OR	**ALM0[9]**
CPU0.DMEM - Uncorrectable Critical error CPU0.DLMU - Uncorrectable Critical error CPU0.DMEM1 - Uncorrectable Critical error	OR	**ALM0[10]**
CPU0.DMEM - Miscellaneous error CPU0.DLMU - Miscellaneous error CPU0.DMEM1 - Miscellaneous error	OR	**ALM0[11]**
CPU1.DMEM - Correctable error CPU1.DLMU - Correctable error	OR	**ALM1[9]**
CPU1.DMEM - Uncorrectable Critical error CPU1.DLMU - Uncorrectable Critical error	OR	**ALM1[10]**
CPU1.DMEM - Miscellaneous error CPU1.DLMU - Miscellaneous error	OR	**ALM1[11]**
DMA - Correctable error MCDS - Correctable error SCR.XRAM - Correctable error SCR.RAMINT - Correctable error GIGETHERNET.RX0 - Correctable error GIGETHERNET.TX0 - Correctable error SDMMC - Correctable error	OR	**ALM6[19]**

Table 162 MTU Pre-Alarm Mapping (cont'd)

Alarm Source	Logic	Alarm Index
DMA - Uncorrectable Critical error MCDS - Uncorrectable Critical error SCR.XRAM - Uncorrectable critical error SCR.RAMINT - Uncorrectable Critical error GIGETHERNET.RX0 - Uncorrectable Critical error GIGETHERNET.TX0 - Uncorrectable Critical error SDMMC - Uncorrectable Critical error	OR	**ALM6[20]**
DMA - Miscellaneous error MCDS - Miscellaneous error SCR.XRAM - Miscellaneous error SCR.RAMINT - Miscellaneous error GIGETHERNET.RX0 - Miscellaneous error GIGETHERNET.TX0 - Miscellaneous error SDMMC - Miscellaneous error	OR	**ALM6[21]**
EMEM0 - Correctable error EMEM_XTM - Correctable error	OR	**ALM7[3]**
EMEM0 - Uncorrectable Critical error EMEM_XTM - Uncorrectable Critical error	OR	**ALM7[4]**
EMEM0 - Miscellaneous error EMEM_XTM - Miscellaneous error	OR	**ALM7[5]**
SPU_BUFFER0 - Correctable error SPU_CONFIG0 - Correctable error HSDPM - Correctable error SPU_FFT_RAM0 - Correctable error SPU_FFT_RAM1 - Correctable error SPU_FFT_RAM2 - Correctable error SPU_FFT_RAM3 - Correctable error	OR	**ALM7[6]**
SPU_BUFFER0 - Uncorrectable Critical error SPU_CONFIG0 - Uncorrectable Critical error HSDPM - Uncorrectable Critical error SPU_FFT_RAM0 - Uncorrectable Critical error SPU_FFT_RAM1 - Uncorrectable Critical error SPU_FFT_RAM2 - Uncorrectable Critical error SPU_FFT_RAM3 - Uncorrectable Critical error	OR	**ALM7[7]**
SPU_BUFFER0 - Miscellaneous error SPU_CONFIG0 - Miscellaneous error HSDPM - Miscellaneous error SPU_FFT_RAM0 - Miscellaneous error SPU_FFT_RAM1 - Miscellaneous error SPU_FFT_RAM2 - Miscellaneous error SPU_FFT_RAM3 - Miscellaneous error	OR	**ALM7[8]**

Safety Flip-flop Pre-Alarm Mapping

Table 163 Safety Flip-flop Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
MTU - Safety flip-flop uncorrectable error IOM - Safety flip-flop uncorrectable error EMEM - Safety flip-flop uncorrectable error IR - Safety flip-flop uncorrectable error SCU - Safety flip-flop uncorrectable error PMS - Safety flip-flop uncorrectable error DMA - Safety flip-flop uncorrectable error SYS_PLL.PER_PLL - Safety flip-flop uncorrectable error CERBERUS - Safety flip-flop uncorrectable error CCU - Safety flip-flop uncorrectable error SMU_core - Safety flip-flop uncorrectable error	OR	ALM10[21]

XBAR Pre-Alarm Mapping

Table 164 XBAR Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
XBAR.XBAR0 - Address Phase error XBAR.XBAR2 - Address Phase error	OR	ALM11[2]
XBAR.XBAR0 - Write Phase error XBAR.XBAR2 - Write Phase error	OR	ALM11[3]
XBAR.XBAR0 - Sota Swap error XBAR.XBAR2 - Sota Swap error	OR	ALM11[13]

Module Access Enable Pre-Alarm Mapping

Table 165 Module Access Enable Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
IR - Access Enable error HSM - Access Enable error	OR	ALM10[22]

PMS Pre-Alarm Mapping

Table 166 PMS Pre-Alarm Mapping

Alarm Source	Logic	Alarm Index
PMS - Uncorrectable error SMU.SMU_stdby - Safety flip-flop Uncorrectable error	OR	ALM21[7]
HSM.VDD - Under Voltage HSM.VDDP3 - Under Voltage HSM.VEXT - Under Voltage	OR	ALM9[17]
HSM.VDD - Over Voltage HSM.VDDP3 - Over Voltage HSM.VEXT - Over Voltage	OR	ALM9[16]

Table 166 PMS Pre-Alarm Mapping (cont'd)

Alarm Source	Logic	Alarm Index
PMS.VDD - Over voltage PMS.VDDPD - Over voltage PMS.VDDP3 - Over voltage PMS.VDDM - Over voltage PMS.VEXT - Over voltage PMS.VEVRSB - Over voltage	OR	**ALM9[3]**
PMS.VDD - Under voltage PMS.VDDPD - Under voltage PMS.VDDP3 - Under voltage PMS.VDDM - Under voltage PMS.VEXT - Under voltage PMS.VEVRSB - Under voltage	OR	**ALM9[5]**
PMS.EVRC - Short to Low PMS.EVRC - Short to High PMS.EVR33 - Short to Low PMS.EVR33 - Short to High	OR	**ALM9[15]**

15.4.2 TC33xEXT Specific Alarms

The following tables fully specify the mapping between the alarms provided by the safety mechanisms implemented by the microcontroller and the alarm groups.

In the following tables the column "Safety Mechanism & Error Indication" indicates to which safety mechanism the alarm is related. If multiple safety mechanisms are indicated, the alarm corresponds to the detection of an error by one of the listed safety mechanisms.

For some safety mechanisms different terms are used in the microcontroller documents; the following list provides a guideline between the term used in the alarm tables and the other definitions, in bold the definition used in the alarm tables.

- Register Access Protection or alternatively called Safety Register Protection
  - Purpose: Monitors the master identifier of a given bus-master during a write access to a configuration register. The master identifier is a hard-coded information that is provided during any bus access. If the master identifier is not enabled by the Register Access Protection configuration registers (ACCEN0) the write is aborted. Most of the modules do not provide a dedicated alarm for this event and instead will generate a bus error. Therefore the Register Access Protection is only documented where a dedicated alarm is available.
  - Note: for peripherals that implement memory-mapped SRAMs, the write accesses to the memories are monitored as well.
- Bus-level Memory Protection Unit (MPU) or alternatively called Safety Memory Protection
  - Purpose: Monitors the master identifier and the address of a given bus-master during a write access to a local SRAM. The master identifier is a hard-coded information that is provided during any bus access. If the master identifier is enabled by the Bus-level MPU configuration registers and the address is within the valid address range the write is accepted, otherwise the write is aborted and a Bus-level MPU alarm is issued.
  - The SRAMs monitored are the {PSPR, DSPR, DLMU} SRAMs of each CPU and the LMU SRAMs when available in the product.

Alarm Mapping related to ALM0 group

Table 167 Alarm Mapping related to ALM0 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM0[0]	cpu_pfi_pfrwb_0	Safety Mechanism: Lockstep CPU Alarm: CPU0 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM0[1]	cpu_pfi_pfrwb_0	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU0 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse
ALM0[2]	cpu_pfi_pfrwb_0	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU0 PFLASH0 Read Path Error Alarm Type: Pulse
ALM0[3]	Reserved	Reserved
ALM0[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM0[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM0[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM0[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level
ALM0[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM0[9]	**Page 22**	Safety Mechanism: SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM0[10]	**Page 22**	Safety Mechanism: SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level
ALM0[11]	**Page 22**	Safety Mechanism(s): SRAM Monitor Alarm: CPU0 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level

Table 167 Alarm Mapping related to ALM0 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM0[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Single bit error correction Alarm Type: Level
ALM0[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM0[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU0 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM0[21:15]	Reserved	Reserved
ALM0[22]	cpu_pfi_pfrwb_0	Safety Mechanism: SRI End-to-End EDC Alarm: CPU0 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM0[23]	cpu_pfi_pfrwb_0	Safety Mechanism: SRI End-to-End EDC Alarm: CPU0 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM0[24]	cpu_pfi_pfrwb_0	Safety Mechanism: Exception Monitor Alarm: CPU0 exception (interrupt/trap) Alarm Type: Pulse
ALM0[31:25]	Reserved	Reserved

Alarm Mapping related to ALM1 group

Table 168 Alarm Mapping related to ALM1 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM1[0]	cpu_1	Safety Mechanism: Lockstep CPU Alarm: CPU1 Lockstep Comparator Error Alarm Type: Pulse Note: For non-Lockstep CPUs (CPUs where no lockstep is implemented or where the lockstep is disabled by the user), this alarm only covers faults that might happen on the access path to the CPU side PFLASH bank. Moreover If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting LCL1 bitfield in SCU_LCLTEST Register. For more details about the CPU lockstep alarm, please refer to the CPU chapter.
ALM1[1]	cpu_1	Safety Mechanism: Bus-level Memory Protection Unit / Register Access Protection Alarm: CPU1 Bus-level MPU violation / Access Protection violation Alarm Type: Pulse

Table 168 Alarm Mapping related to ALM1 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM1[2]	cpu_1	Safety Mechanism: PFLASH Read Path Monitor Alarm: CPU1 PFLASH1 Read Path Error Alarm Type: Pulse Note: If the CPU side PFLASH bank does not exist, PFLASH read path lockstep still exist. The alarm can be triggered by setting PLCLT1 bitfield in SCU_LCLTEST Register.
ALM1[3]	Reserved	Reserved
ALM1[4]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM1[5]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM1[6]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Single bit error correction Alarm Type: Level
ALM1[7]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Uncorrectable critical error detection Alarm Type: Level
ALM1[8]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 PSPR/PCACHE Miscellaneous critical error detection Alarm Type: Level
ALM1[9]	**Page 22**	Safety Mechanism: SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Single bit error correction Alarm Type: Level
ALM1[10]	**Page 22**	Safety Mechanism: SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Uncorrectable critical error detection Alarm Type: Level
ALM1[11]	**Page 22**	Safety Mechanism(s): SRAM Monitor Alarm: CPU1 DSPR/DCACHE/DLMU Miscellaneous error detection Alarm Type: Level
ALM1[12]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Single bit error correction Alarm Type: Level
ALM1[13]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Uncorrectable critical error detection Alarm Type: Level
ALM1[14]	MTU	Safety Mechanism: SRAM Monitor Alarm: CPU1 DCACHE TAG Miscellaneous error detection Alarm Type: Level
ALM1[21:15]	Reserved	Reserved

Table 168 Alarm Mapping related to ALM1 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM1[22]	cpu_1	Safety Mechanism: SRI End-to-End EDC Alarm: CPU1 Instruction Fetch SRI Interface EDC Error Alarm Type: Pulse
ALM1[23]	cpu_1	Safety Mechanism: SRI End-to-End EDC Alarm: CPU1 Data SRI Interface (Load/Store) EDC Error Alarm Type: Pulse
ALM1[24]	cpu_1	Safety Mechanism: Exception Monitor Alarm: CPU1 exception (interrupt/trap) Alarm Type: Pulse
ALM1[31:25]	Reserved	Reserved

Alarm Mapping related to ALM2 group

Table 169 Alarm Mapping related to ALM2 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM2[0]	Reserved	Reserved
ALM2[1]	Reserved	Reserved
ALM2[2]	Reserved	Reserved
ALM2[3]	Reserved	Reserved
ALM2[14:4]	Reserved	Reserved
ALM2[21:15]	Reserved	Reserved
ALM2[24:22]	Reserved	Reserved
ALM2[31:25]	Reserved	Reserved

Alarm Mapping related to ALM3 group

Table 170 Alarm Mapping related to ALM3 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM3[0]	Reserved	Reserved
ALM3[1]	Reserved	Reserved
ALM3[2]	Reserved	Reserved
ALM3[3]	Reserved	Reserved
ALM3[14:4]	Reserved	Reserved
ALM3[21:15]	Reserved	Reserved
ALM3[24:22]	Reserved	Reserved
ALM3[31:25]	Reserved	Reserved

Alarm Mapping related to ALM4 group

Table 171 Alarm Mapping related to ALM4 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM4[2:0]	Reserved	Reserved
ALM4[3]	Reserved	Reserved
ALM4[14:4]	Reserved	Reserved
ALM4[21:15]	Reserved	Reserved
ALM4[24:22]	Reserved	Reserved
ALM4[31:25]	Reserved	Reserved

Alarm Mapping related to ALM5 group

Table 172 Alarm Mapping related to ALM5 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM5[2:0]	Reserved	Reserved
ALM5[3]	Reserved	Reserved
ALM5[14:4]	Reserved	Reserved
ALM5[21:15]	Reserved	Reserved
ALM5[24:22]	Reserved	Reserved
ALM5[31:25]	Reserved	Reserved

Alarm Mapping related to ALM6 group

Table 173 Alarm Mapping related to ALM6 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM6[0]	MTU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[1]	iom	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[2]	INT	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[3]	EMEMWRAPPER	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[4]	SCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[5]	PMS	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level

Table 173 Alarm Mapping related to ALM6 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM6[6]	DMA	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[7]	SMU_CORE	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[8]	CCU	Safety Mechanism: Safety Flip-flop Alarm: SYS_PLL.PER_PLL - Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[9]	Reserved	Reserved
ALM6[12:10]	Reserved	Reserved
ALM6[15:13]	Reserved	Reserved
ALM6[16]	MTU	Safety Mechanism: SRAM Monitor Alarm: CAN Single bit error correction Alarm Type: Level
ALM6[17]	MTU	Safety Mechanism: SRAM Monitor Alarm: CAN Uncorrectable critical error detection Alarm Type: Level
ALM6[18]	MTU	Safety Mechanism: SRAM Monitor Alarm: CAN Miscellaneous error detection Alarm Type: Level
ALM6[19]	**Page 22**	Safety Mechanism: SRAM Monitor Alarm: MISC Single bit error correction Alarm Type: Level
ALM6[20]	**Page 23**	Safety Mechanism: SRAM Monitor Alarm: MISC Uncorrectable critical error detection Alarm Type: Level
ALM6[21]	**Page 23**	Safety Mechanism: SRAM Monitor Alarm: MISC Miscellaneous error detection Alarm Type: Level
ALM6[22]	Reserved	Reserved
ALM6[23]	CBS	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[24]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop correctable error detected Alarm Type: Level
ALM6[25]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM6[31:26]	Reserved	Reserved

Alarm Mapping related to ALM7 group

Table 174 Alarm Mapping related to ALM7 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM7[0]	MTU	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Single bit error correction Alarm Type: Level
ALM7[1]	MTU	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Uncorrectable critical error detection Alarm Type: Level
ALM7[2]	MTU	Safety Mechanism: SRAM Monitor Alarm: LMU/FSI_RAM Miscellaneous error detection Alarm Type: Level
ALM7[3]	**Page 23**	Safety Mechanism: SRAM Monitor Alarm: EMEM Single bit error correction Alarm Type: Level
ALM7[4]	**Page 23**	Safety Mechanism: SRAM Monitor Alarm: EMEM Uncorrectable critical error detection Alarm Type: Level
ALM7[5]	**Page 23**	Safety Mechanism: SRAM Monitor Alarm: EMEM Miscellaneous error detection Alarm Type: Level
ALM7[6]	**Page 23**	Safety Mechanism: SRAM Monitor Alarm: SPU/CIF Single bit error correction Alarm Type: Level
ALM7[7]	**Page 23**	Safety Mechanism: SRAM Monitor Alarm: SPU/CIF Uncorrectable critical error detection Alarm Type: Level
ALM7[8]	**Page 23**	Safety Mechanism: SRAM Monitor Alarm: SPU/CIF Miscellaneous error detection Alarm Type: Level
ALM7[11:9]	Reserved	Reserved
ALM7[12]	EMEMWRAPPER	Safety Mechanism: LMU Lockstep Alarm: Lockstep Comparator Error Alarm Type: Pulse
ALM7[13]	EMEMWRAPPER	Safety Mechanism: LMU Lockstep Alarm: Lockstep Control Error Alarm Type: Pulse
ALM7[14]	EMEMWRAPPER	Safety Mechanism: SRAM ECC Monitor Alarm: ECC Error Alarm Type: Pulse
ALM7[15]	EMEMWRAPPER	Safety Mechanism: Bus-level MPU Alarm: Bus-level MPU error Alarm Type: Pulse

Table 174 Alarm Mapping related to ALM7 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM7[16]	EMEMWRAPPER	Safety Mechanism: LMU Error Detection Code (EDC) Alarm: EDC Read Phase Error Alarm Type: Pulse
ALM7[17]	SRI	Safety Mechanism: Built-in SRI Error Detection Alarm: XBAR0 Bus Error Event Alarm Type: Pulse
ALM7[18]	Reserved	Reserved
ALM7[19]	Reserved	Reserved
ALM7[20]	SBCU	Safety Mechanism: Built-in SPB Error Detection Alarm: SPB Bus Error Event Alarm Type: Pulse
ALM7[21]	EBCU	Safety Mechanism: Built-in BBB Error Detection Alarm: BBB Bus Error Event Alarm Type: Pulse
ALM7[22]	FSI	Safety Mechanism: PFlash ECC Alarm: PFlash Single Bit Error Alarm Type: Level
ALM7[23]	FSI	Safety Mechanism: PFlash ECC Alarm: PFlash Double Bit Error Alarm Type: Level
ALM7[24]	FSI	Safety Mechanism: PFlash ECC Alarm: Single Bit Correction Tracking Buffer Full Alarm Type: Level
ALM7[25]	FSI	Safety Mechanism: PFlash ECC Alarm: Double Bit Correction Tracking Buffer Full Alarm Type: Level
ALM7[26]	FSI	Safety Mechanism: PFlash ECC Alarm: Multiple Bit Error Detection Tracking Buffer Full Alarm Type: Level
ALM7[27]	FSI	Safety Mechanism: PFlash ECC Alarm: Zero Bit Error Tracking Buffer Full Alarm Type: Level
ALM7[28]	FSI	Safety Mechanism: PFlash ECC Monitor Alarm: PFlash ECC Error Alarm Type: Level
ALM7[29]	FSI	Safety Mechanism: PFlash EDC Monitor Alarm: PFlash EDC Error Alarm Type: Level

Table 174 Alarm Mapping related to ALM7 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM7[30]	FSI	Safety Mechanism: PFlash Configuration Monitor Alarm: CPU FLASHCON Configuration Error Alarm Type: Level
ALM7[31]	FSI	Safety Mechanism: PFlash Configuration Monitor Alarm: Flash Stored Configuration Error Alarm Type: Level

Alarm Mapping related to ALM8 group

Table 175 Alarm Mapping related to ALM8 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM8[0]	SCU	Safety Mechanism: Clock Monitor Alarm: OSC clock frequency out of range Alarm Type: Pulse
ALM8[1]	CCU	Safety Mechanism: Clock Monitor Alarm: Back-up clock out-of-range alarm Alarm Type: Level
ALM8[2]	CCU	Safety Mechanism: Clock Alive Monitor Alarm: Back-up clock alive alarm Alarm Type: Level
ALM8[3]	SCU	Safety Mechanism: PLL loss of lock detection Alarm: System PLL DCO loss of lock event Alarm Type: Pulse
ALM8[4]	SCU	Safety Mechanism: PLL loss of lock detection Alarm: Peripheral PLL DCO loss of lock event Alarm Type: Pulse
ALM8[5]	SCU	Safety Mechanism: LBIST Safe Reset State Alarm: LBIST Alarm Alarm Type: Level
ALM8[6]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 0 Alarm Type: Pulse
ALM8[7]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 1 Alarm Type: Pulse
ALM8[8]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 2 Alarm Type: Pulse
ALM8[9]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 3 Alarm Type: Pulse
ALM8[10]	SCU	Safety Mechanism: Watchdog Alarm: CPU0 Watchdog Time-out Alarm Type: Pulse

Table 175 Alarm Mapping related to ALM8 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM8[11]	SCU	Safety Mechanism: Watchdog Alarm: CPU1 Watchdog Time-out Alarm Type: Pulse
ALM8[12]	Reserved	Reserved
ALM8[13]	Reserved	Reserved
ALM8[15:14]	Reserved	Reserved
ALM8[16]	SCU	Safety Mechanism: Watchdog Alarm: Safety Watchdog Time-out Alarm Type: Pulse
ALM8[17]	SCU	Safety Mechanism: All Watchdogs Alarm: Watchdog Time-out. This alarm is a logical OR over all watchdog time-out alarms Alarm Type: Pulse
ALM8[18]	SCU	Safety Mechanism: Lockstep Dual Rail Monitor Alarm: Dual Rail Error Alarm Type: Pulse
ALM8[19]	SCU	Safety Mechanism: Emergency Stop Alarm: External Emergency Stop Signal Event Alarm Type: Pulse
ALM8[20]	SCU	Safety Mechanism: Pad Monitor Alarm: Pad Heating Alarm Alarm Type: Pulse Note: This alarm is triggered by the pad-heating enable signal of all core supply-pads. It will also be triggered by the enable signal for initialisation of security sensitive RAMs and TCU test enable signals
ALM8[21]	SCU	Safety Mechanism: LBIST Test Mode Alarm: LBIST Test Mode Alarm Alarm Type: Level Note: This alarm is also set if TCU related signals are activated in the SCU causing it to fail
ALM8[22]	INT	Safety Mechanism: Interrupt Monitor Alarm: EDC Configuration and Data Path Error Alarm Type: Pulse
ALM8[23]	DMA	Safety Mechanism: DMA SRI ECC Alarm: DMA SRI ECC Error Alarm Type: Pulse
ALM8[24]	Reserved	Reserved
ALM8[25]	iom	Safety Mechanism: External Alarm Alarm: Pin Mismatch Indication Alarm Type: Level
ALM8[26]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 4 Alarm Type: Pulse

Table 175 Alarm Mapping related to ALM8 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM8[27]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 5 Alarm Type: Pulse
ALM8[28]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 6 Alarm Type: Pulse
ALM8[29]	SCU	Safety Mechanism: External Alarm Alarm: External Request Unit Alarm 7 Alarm Type: Pulse
ALM8[30]	SCU	Safety Mechanism: Core Domain Die Temperature Sensor Alarm: Under Temperature Alarm Alarm Type: Level
ALM8[31]	SCU	Safety Mechanism: Core Domain Die Temperature Sensor Alarm: Over Temperature Alarm Alarm Type: Level

Alarm Mapping related to ALM9 group

Table 176 Alarm Mapping related to ALM9 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM9[0]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature Overflow Alarm Type: Level
ALM9[1]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature Underflow Alarm Type: Level
ALM9[2]	Reserved	Reserved
ALM9[3]	**Page 25**	Safety Mechanism: Voltage Monitor Alarm: Over-voltage Alarm Alarm Type: Level
ALM9[4]	Reserved	Reserved
ALM9[5]	**Page 25**	Safety Mechanism: Voltage Monitor Alarm: Under-voltage Alarm Alarm Type: Level
ALM9[14:6]	Reserved	Reserved
ALM9[15]	**Page 25**	Safety Mechanism: Voltage Monitor Alarm: Short to Low/High Alarm Alarm Type: Level
ALM9[16]	**Page 24**	Safety Mechanism: Voltage Monitor Alarm: Over-voltage Alarm Alarm Type: Level

Table 176 Alarm Mapping related to ALM9 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM9[17]	Page 24	Safety Mechanism: Voltage Monitor Alarm: Under-voltage Alarm Alarm Type: Level
ALM9[19:18]	Reserved	Reserved
ALM9[20]	EMEMWRAPPER	Safety Mechanism: EMEM Monitor Alarm: Unexpected Write to EMEM Alarm Alarm Type: Pulse
ALM9[21]	EMEMWRAPPER	Safety Mechanism: SEP Control Logic Monitor Alarm: SEP Control Logic Alarm Alarm Type: Pulse
ALM9[22]	EMEMWRAPPER	Safety Mechanism: SPU Lockstep Control Logic Input Monitor Alarm: SPU Configuration Error Alarm Alarm Type: Pulse
ALM9[23]	Reserved	Reserved
ALM9[26:24]	Reserved	Reserved
ALM9[27]	Reserved	Reserved
ALM9[28]	SPU0	Safety Mechanism: SPU Safety Monitor Alarm: SPU0 Safety Alarm Alarm Type: Pulse
ALM9[29]	Reserved	Reserved
ALM9[30]	RIF0	Safety Mechanism: RIF Safety Monitor Alarm: RIF0 Safety Alarm Alarm Type: Pulse
ALM9[31]	Reserved	Reserved

Alarm Mapping related to ALM10 group

Table 177 Alarm Mapping related to ALM10 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM10[0]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 0 Alarm Type: Pulse
ALM10[1]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 1 Alarm Type: Pulse
ALM10[2]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 2 Alarm Type: Pulse
ALM10[3]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 3 Alarm Type: Pulse

Table 177 Alarm Mapping related to ALM10 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM10[4]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 4 Alarm Type: Pulse
ALM10[5]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 5 Alarm Type: Pulse
ALM10[6]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 6 Alarm Type: Pulse
ALM10[7]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 7 Alarm Type: Pulse
ALM10[8]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 8 Alarm Type: Pulse
ALM10[9]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 9 Alarm Type: Pulse
ALM10[10]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 10 Alarm Type: Pulse
ALM10[11]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 11 Alarm Type: Pulse
ALM10[12]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 12 Alarm Type: Pulse
ALM10[13]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 13 Alarm Type: Pulse
ALM10[14]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 14 Alarm Type: Pulse
ALM10[15]	Software	Safety Mechanism: Software Monitor Alarm: Software Alarm 15 Alarm Type: Pulse
ALM10[16]	SMU_CORE	Safety Mechanism: Recovery Timer 0 Alarm: Timer Time-out Alarm Type: Pulse
ALM10[17]	SMU_CORE	Safety Mechanism: Recovery Timer 1 Alarm: Timer Time-out Alarm Type: Pulse

Table 177 Alarm Mapping related to ALM10 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM10[18]	FSP	Safety Mechanism: ErrorPin Alarm: ErrorPin Fault State Activation Alarm Type: Pulse
ALM10[19]	Reserved	Reserved
ALM10[20]	CCU	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop correctable error detected Alarm Type: Level
ALM10[21]	**Page 24**	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM10[22]	**Page 24**	Safety Mechanism: Access Enable Protection Alarm: Access Enable error Alarm Type: Pulse
ALM10[31:23]	Reserved	Reserved

Alarm Mapping related to ALM11 group

Table 178 Alarm Mapping related to ALM11 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM11[0]	EMEMWRAPPER	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[1]	EMEMWRAPPER	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[2]	**Page 24**	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[3]	**Page 24**	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[4]	DMU	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[5]	DMU	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse
ALM11[6]	SFIBRIDGE2	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Address Phase Error Alarm Type: Pulse
ALM11[7]	SFIBRIDGE2	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Write Phase Error Alarm Type: Pulse

Table 178 Alarm Mapping related to ALM11 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM11[8]	Reserved	Reserved
ALM11[9]	SFIBRIDGE1	Safety Mechanism: SRI Error Detection Code (EDC) Alarm: EDC Read Phase Error Alarm Type: Pulse
ALM11[10]	Reserved	Reserved
ALM11[11]	Reserved	Reserved
ALM11[12]	converter_0	Safety Mechanism: Converter Alarm: Phase Synchronizer Error Alarm Type: Level
ALM11[13]	**Page 24**	Safety Mechanism: SRI SOTA Monitor Alarm: SOTA Swap Error Alarm Type: Pulse
ALM11[31:14]	Reserved	Reserved

Alarm Mapping related to ALM20 group

Table 179 Alarm Mapping related to ALM20 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM20[3:0]	Reserved	Resreved
ALM20[4]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDD Over-voltage Alarm Alarm Type: Level
ALM20[5]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDPD Over-voltage Alarm Alarm Type: Level
ALM20[6]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Over-voltage Alarm Alarm Type: Level
ALM20[7]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDM Over-voltage Alarm Alarm Type: Level
ALM20[8]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEXT Over-voltage Alarm Alarm Type: Level
ALM20[9]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEVRSB Over-voltage Alarm Alarm Type: Level
ALM20[10]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDD Under-voltage Alarm Alarm Type: Level
ALM20[11]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDPD Under-voltage Alarm Alarm Type: Level

Table 179 Alarm Mapping related to ALM20 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM20[12]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Under-voltage Alarm Alarm Type: Level
ALM20[13]	PMS	Safety Mechanism: Voltage Monitor Alarm: VDDM Under-voltage Alarm Alarm Type: Level
ALM20[14]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEXT Under-voltage Alarm Alarm Type: Level
ALM20[15]	PMS	Safety Mechanism: Voltage Monitor Alarm: VEVRSB Under-voltage Alarm Alarm Type: Level
ALM20[31:16]	Reserved	Reserved

Alarm Mapping related to ALM21 group

Table 180 Alarm Mapping related to ALM21 group

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM21[0]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDD Under-voltage Alarm Alarm Type: Level
ALM21[1]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDDP3 Under-voltage Alarm Alarm Type: Level
ALM21[2]	hsm	Safety Mechanism: Voltage Monitor Alarm: VEXT Under-voltage Alarm Alarm Type: Level
ALM21[3]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDD Over-voltage Alarm Alarm Type: Level
ALM21[4]	hsm	Safety Mechanism: Voltage Monitor Alarm: VDDP3 over-voltage Alarm Alarm Type: Level
ALM21[5]	hsm	Safety Mechanism: Voltage Monitor Alarm: VEXT over-voltage Alarm Alarm Type: Level
ALM21[6]	Reserved	Reserved
ALM21[7]	**Page 24**	Safety Mechanism: Safety Flip-flop Alarm: Safety flip-flop uncorrectable error detected Alarm Type: Level
ALM21[8]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature underflow Alarm Type: Level

Table 180 Alarm Mapping related to ALM21 group (cont'd)

Alarm Index	Module	Safety Mechanism & Alarm Indication
ALM21[9]	PMS	Safety Mechanism: Die Temperature Sensor Alarm: Temperature overflow Alarm Type: Level
ALM21[10]	PMS	Safety Mechanism: Register Access Protection Alarm: Access Protection violation Alarm Type: Pulse
ALM21[11]	PMS	Safety Mechanism: Voltage Monitor Alarm: EVRC Short to Low Alarm Alarm Type: Level
ALM21[12]	PMS	Safety Mechanism: Voltage Monitor Alarm: EVRC Short to High Alarm Alarm Type: Level
ALM21[13]	PMS	Safety Mechanism: Voltage Monitor Alarm: EV33 Short to Low Alarm Alarm Type: Level
ALM21[14]	PMS	Safety Mechanism: Voltage Monitor Alarm: EV33 Short to High Alarm Alarm Type: Level
ALM21[15]	CCU	Safety Mechanism: Clock Alive Monitor Alarm: PLLx/fSPB Alive Alarm (provided on fBACK clock with x = 0..2) Alarm Type: Level Note: This alarm is also set if TCU related signals are activated in the CCU causing the clocks to fail
ALM21[16]	SMU_CORE	Safety Mechanism: SMU_core Alive Monitor Alarm: SMU_core Alive Alarm Alarm Type: Pulse
ALM21[31:17]	Reserved	Reserved

15.5 Connectivity

Table 181 Connections of SMU

Interface Signals	connects		Description
SMU:FSP(0)	to	P33.8:HWOUT(0)	FSP[1..0] Output Signals - Generated by SMU_core
SMU:FSP(1)	to	P33.10:HWOUT(0)	FSP[1..0] Output Signals - Generated by SMU_core
SMU:FSP_STS(0)	from	P33.8:IN	FSP Status Input - Shows the actual state of the FSP ErroPin
SMU:FSP_STS(1)	from	P33.10:IN	FSP Status Input - Shows the actual state of the FSP ErroPin
SMU:RUNSTATE	to	SCU:smu_wdt_run	SMU_core RUN state indication
SMU:INT(2:0)	to	INT:smu.INT(2:0)	SMU Service Request

15.6 Revision History

Table 182 Revision History

Reference	Change to Previous Version	Comment
V4.0.17		
	First release	
V4.0.18		
Page 41	Updated description of ALM21[0] and ALM21[3]	
Page 41	Added description for ALM21[6]	
Page 34	Updated description for ALM8[20]	
Page 1	Missing blank fixed	
V4.0.19		
Page 22, **Page 32**	Added FSI_RAM Alarms ALM7[0:2] which were not documented in the previous version	
Page 26	Added Alarm Types in Alarm Mapping Tables	
Page 2	Typo fixed, no functional change	
Page 43	Revision History updated	
V4.0.20		
Page 22	Updated description of ALM7[6:8] for SPU_FFT_RAM instances	
Page 22	Updated description of ALM6[16:18] for MCAN instances	
Page 22, **Page 30**, **Page 6**	Removed ALM6[13:15] as they don’t exist in this device	
V4.0.21		
-	No functional changes	
V4.0.22		
Page 30, **Page 6**	Removed ALM6[10:12] as they don’t exist in this device	
Page 32, **Page 7**	Removed ALM7[19] as they don’t exist in this device	
Page 27	Updated description of ALM1[0] and ALM1[2]	
V4.0.23		
Page 30	Updated description of ALM6[8]	
Page 22	Added CPU0.DMEM1 Alarms ALM0[9:11] which were not documented in the previous version. Removed CPU1.DMEM1 ALM1[9:11] as they don’t exist in this device	
Page 22	Added DMA Alarms ALM6[19:21] which were not documented in the previous version.	

16 Interrupt Router (IR)

This chapter supplements the family documentation whith device specific information for TC33xEXT.

The Interrupt Router allocates two address ranges

- Interrupt Router System and OTGM register address range: 2 * 256 byte address range covering the Interrupt Router system registers, ICU control registers and OTGM registers (**Chapter 16.2**)
- SRC register address range: 8 KByte address range covering the Service Request Control registers (**Chapter 16.4**)

16.1 TC33xEXT Specific Interrupt Router Configuration

Table 183 TC33xEXT specific configuration of INT

Parameter	INT
Number of Interrupt Service Providers	3
Number of SRB groups	2

Table 184 TC33xEXT specific configuration of SRC

Parameter	SRC
Number of Service Request Nodes	1024

16.2 TC33xEXT Specific Control Registers

This chapter describes the TC33xEXT specific Interrupt Router system, OTGM and ICU registers

List of used Access Protection Register abbreviations

- P0 -> ACCEN_SRBx, write protection of the related SRBx register. Number of Service Request Broadcast registers (SRB) and the related ACCEN_SRB registers is equal to the number of implemented TriCore CPUs.
- P1 -> ACCEN_CONFIG, write protection of all SRCx[15:0] and ICUx Error Capture registers (ECRx)
- P2 -> ACCEN_SRC_TOSx, write protects bits [31:16] of all SRCs that are mapped to TOSx (SCR.TOS=x). For each implemented Interrupt Control Unit, one ACCEN_SRC_TOSx register is implemented.

Note: A violation of the access protection will not be executed (e.g. a write to a ´Px´/ACCEN protected register by an SPB access with a disabled Master TAG-ID). In this case an access protection error is signaled to the SMU. Beside this signaling to the SMU, no other error, interrupt or trap is generated.

Interrupt Router Module Registers

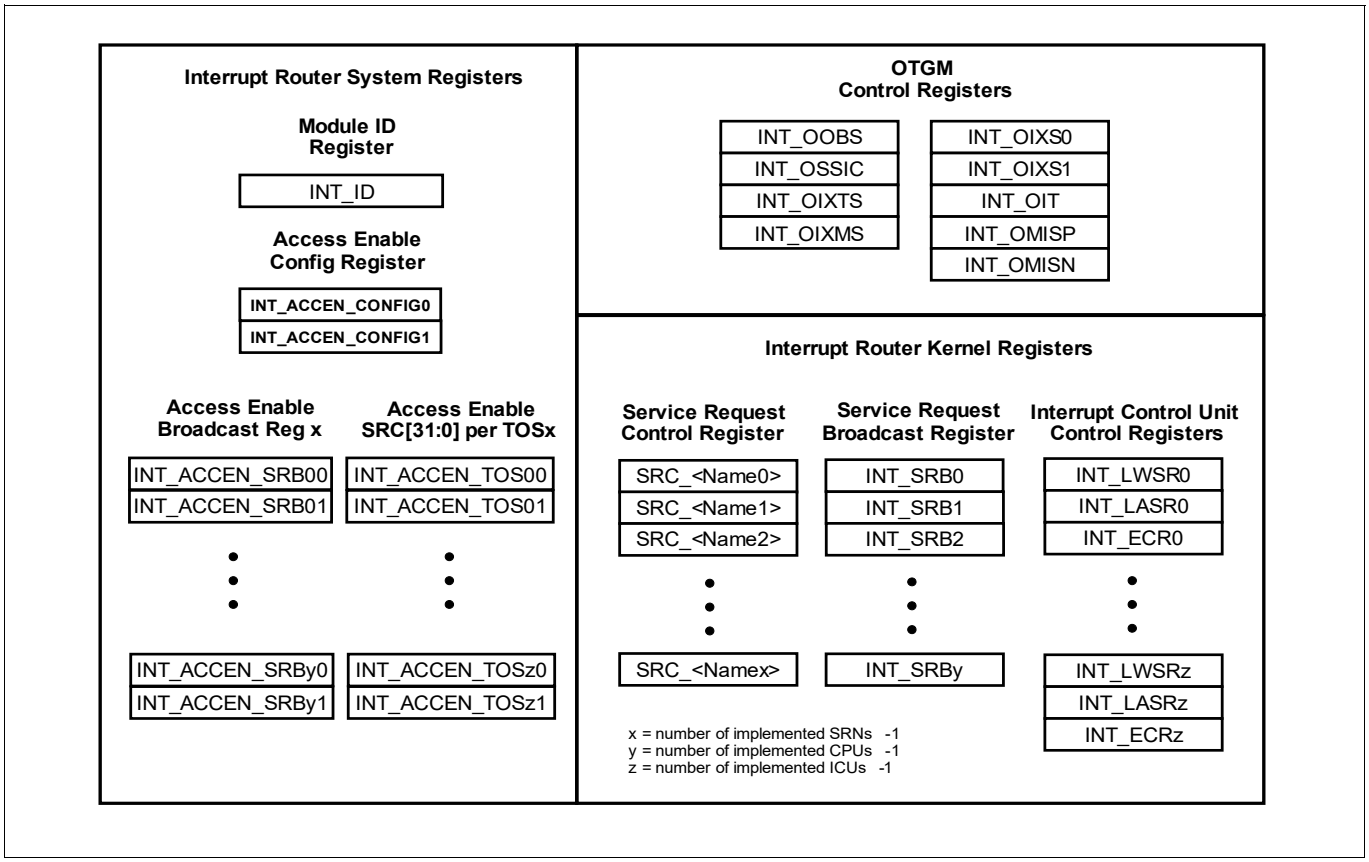


Figure 5 Interrupt Router module registers (SRC registers are described in Chapter 16.4)

Table 185 Register Address Space - INT

Module	Base Address	End Address	Note
INT	$F0037000_H$	$F0037FFF_H$	IR Status and Control Registers

Table 186 Register Overview - INT (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
INT_ID	Module Identification Register	0008_H	U,SV	nBE	Application Reset	See Family Spec
INT_SRBx (x=0-1)	Service Request Broadcast Register x	0010_H+x *4	U,SV	SV,P0	Application Reset	See Family Spec
INT_OOBS	OTGM OTGB0/1 Status	0080_H	U,SV	nBE	Application Reset	See Family Spec
INT_OSSIC	OTGM SSI Control	0084_H	U,SV	SV	Application Reset	See Family Spec
INT_OIXTS	OTGM IRQ MUX Trigger Set Select	0088_H	U,SV	SV	Application Reset	See Family Spec
INT_OIXMS	OTGM IRQ MUX Missed IRQ Select	$008C_H$	U,SV	SV	Application Reset	See Family Spec
INT_OIXS0	OTGM IRQ MUX Select 0	0090_H	U,SV	SV	Application Reset	See Family Spec
INT_OIXS1	OTGM IRQ MUX Select 1	0094_H	U,SV	SV	Application Reset	See Family Spec
INT_OIT	OTGM IRQ Trace	$00A0_H$	U,SV	SV	Application Reset	See Family Spec
INT_OMISP	OTGM MCDS I/F Sensitivity Posedge	$00A4_H$	U,SV	SV	Application Reset	See Family Spec
INT_OMISN	OTGM MCDS I/F Sensitivity Negedge	$00A8_H$	U,SV	SV	Application Reset	See Family Spec
INT_ACCEN_CONFIG0	Access Enable covering all INT_ECRx and all SRCy[15:0], Register 0	$00F0_H$	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_CONFIG1	Access Enable covering all INT_ECRx and all SRCy[15:0], Register 1	$00F4_H$	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRBx0 (x=0-1)	Access Enable covering SRBx, Register 0	0100_H+x *8	U,SV	SV,SE	Application Reset	See Family Spec

Table 186 Register Overview - INT (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
INT_ACCEN_SRBx1 (x=0-1)	Access Enable covering SRBx, Register 1	0104_H+x*8	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRC_TOSx0 (x=0-2)	Access Enable covering all SRCx[31:16] mapped to ICUx, Register 0	0180_H+x*8	U,SV	SV,SE	Application Reset	See Family Spec
INT_ACCEN_SRC_TOSx1 (x=0-2)	Access Enable covering all SRCx[31:16] mapped to ICUx, Register 1	0184_H+x*8	U,SV	SV,SE	Application Reset	See Family Spec
INT_LWSRx (x=0-2)	Latest Winning Service Request Register x, related to ICUx	0200_H+x*10_H	U,SV	nBE	Application Reset	See Family Spec
INT_LASRx (x=0-2)	Last Acknowledged Service Request Register x, related to ICUx	0204_H+x*10_H	U,SV	nBE	Application Reset	See Family Spec
INT_ECRx (x=0-2)	Error Capture Register x, related to ICUx	0208_H+x*10_H	U,SV	SV,P1	Application Reset	See Family Spec

16.3 TC33xEXT Specific Registers

No deviations from the Family Spec

16.4 TC33xEXT Specific Service Request Control (SRC) registers

This chapter describes the TC33xEXT Service Request Control (SRC) registers.

Table 188 shows all registers associated with the Interrupt Router module in the device. This chapter describes the Service Request Control registers including:

- Mapping of Aurix module interrupt triggers to SRC
- SRC offsets
- The index number of an SRC can be calculated with the SRC Offset: Index(SRC) = <SRC Address Offset> / 4

List of used Access Protection Register abbreviations

- P0 -> ACCEN_SRBx, write protection of the related SRBx register. Number of Service Request Broadcast registers (SRB) and the related ACCEN_SRB registers is equal to the number of implemented TriCore CPUs.
- P1 -> ACCEN_CONFIG, write protection of all SRCx[15:0] and ICUx Error Capture registers (ECRx)
- P2 -> ACCEN_SRC_TOSx, write protects bits [31:16] of all SRCs that are mapped to TOSx (SCR.TOS=x). For each implemented Interrupt Control Unit, one ACCEN_SRC_TOSx register is implemented.

Note: A violation of the access protection will not be executed (e.g. a write to a ´Px´/ACCEN protected register from a disabled master). In this case an access protection error is signaled to the SMU. Beside this signaling to the SMU, no other error, interrupt or trap is generated.

Table 187 Register Address Space - SRC

Module	Base Address	End Address	Note
SRC	$F0038000_H$	$F0039FFF_H$	IR Service Request Control Registers (SRC)

Table 188 Register Overview - SRC (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_CPUxSB (x=0-1)	CPUx Software Breakpoint Service Request	00000_H+ x*4	U,SV	SV,P1,P2	Debug Reset	9
SRC_BCUSPB	SBCU Service Request (SPB Bus Control Unit)	00020_H	U,SV	SV,P1,P2	Debug Reset	9
SRC_BCUBBB	EBCU Service Request (BBB Bus Control Unit, on ED and ADAS devices only)	00024_H	U,SV	SV,P1,P2	Debug Reset	9
SRC_AGBT	AGBT Service Request (on ED devices only)	$0002C_H$	U,SV	SV,P1,P2	Debug Reset	9
SRC_XBAR0	SRI Domain 0 Service Request	00030_H	U,SV	SV,P1,P2	Debug Reset	9
SRC_CERBERUSy (y=0-1)	Cerberus Service Request y	00040_H+ y*4	U,SV	SV,P1,P2	Debug Reset	9
SRC_ASCLINxTX (x=0-5)	ASCLINx Transmit Service Request	00050_H+ x*12	U,SV	SV,P1,P2	Application Reset	9
SRC_ASCLINxRX (x=0-5)	ASCLINx Receive Service Request	00054_H+ x*12	U,SV	SV,P1,P2	Application Reset	9

Table 188 Register Overview - SRC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_ASCLINxERR (x=0-5)	ASCLINx Error Service Request	00058_H+x*12	U,SV	SV,P1,P2	Application Reset	9
SRC_MTUDONE	MTU Done Service Request	$000EC_H$	U,SV	SV,P1,P2	Application Reset	9
SRC_QSPIxTX (x=0-3)	QSPIx Transmit Service Request	$000F0_H$+x*14_H	U,SV	SV,P1,P2	Application Reset	12
SRC_QSPIxRX (x=0-3)	QSPIx Receive Service Request	$000F4_H$+x*14_H	U,SV	SV,P1,P2	Application Reset	12
SRC_QSPIxERR (x=0-3)	QSPIx Error Service Request	$000F8_H$+x*14_H	U,SV	SV,P1,P2	Application Reset	12
SRC_QSPIxPT (x=0-3)	QSPIx Phase Transition Service Request	$000FC_H$+x*14_H	U,SV	SV,P1,P2	Application Reset	12
SRC_QSPIxU (x=0-3)	QSPIx User Defined Service Request	00100_H+x*14_H	U,SV	SV,P1,P2	Application Reset	12
SRC_QSPI2HC	QSPI2 High Speed Capture Service Request	00178_H	U,SV	SV,P1,P2	Application Reset	12
SRC_QSPI3HC	QSPI3 High Speed Capture Service Request	$0017C_H$	U,SV	SV,P1,P2	Application Reset	12
SRC_SENTx (x=0-9)	SENT TRIGx Service Request	00240_H+x*4	U,SV	SV,P1,P2	Application Reset	12
SRC_CCU6xSRy (x=0-1;y=0-3)	CCUx Service Request y	$002C0_H$+x*10_H+y*4	U,SV	SV,P1,P2	Application Reset	12
SRC_GPT120CIRQ	GPT120 CAPREL Service Request	$002E0_H$	U,SV	SV,P1,P2	Application Reset	12
SRC_GPT120T2	GPT120 Timer 2 Service Request	$002E4_H$	U,SV	SV,P1,P2	Application Reset	14
SRC_GPT120T3	GPT120 Timer 3 Service Request	$002E8_H$	U,SV	SV,P1,P2	Application Reset	14
SRC_GPT120T4	GPT120 Timer 4 Service Request	$002EC_H$	U,SV	SV,P1,P2	Application Reset	14
SRC_GPT120T5	GPT120 Timer 5 Service Request	$002F0_H$	U,SV	SV,P1,P2	Application Reset	14
SRC_GPT120T6	GPT120 Timer 6 Service Request	$002F4_H$	U,SV	SV,P1,P2	Application Reset	14
SRC_STMxSRy (x=0-1;y=0-1)	System Timer x Service Request y	00300_H+x*8+y*4	U,SV	SV,P1,P2	Application Reset	14
SRC_FCE0	FCE0 Error Service Request	00330_H	U,SV	SV,P1,P2	Application Reset	14

Table 188 Register Overview - SRC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_DMAERRy (y=0-3)	DMA Error Service Request y	00340_H+ y*4	U,SV	SV,P1,P2	Application Reset	14
SRC_DMACHy (y=0-63)	DMA Channel y Service Request	00370_H+ y*4	U,SV	SV,P1,P2	Application Reset	14
SRC_SDMMCERR	SDMMC Error Service Request	00570_H	U,SV	SV,P1,P2	Application Reset	14
SRC_SDMMCDMA	SDMMC DMA Ready Service Request	00574_H	U,SV	SV,P1,P2	Application Reset	17
SRC_GETHy (y=0-9)	GETH Service Request y	00580_H+ y*4	U,SV	SV,P1,P2	Application Reset	17
SRC_CANxINTy (x=0;y=0-15)	CANx Service Request y	$005B0_H$+ y*4	U,SV	SV,P1,P2	Application Reset	17
SRC_VADCGxSRy (x=0-5;y=0-3)	EVADC Group x Service Request y	00670_H+ x*10_H+y* 4	U,SV	SV,P1,P2	Application Reset	17
SRC_VADCCGxSRy (x=0-1;y=0-3)	EVADC Common Group x Service Request y	00750_H+ x*10_H+y* 4	U,SV	SV,P1,P2	Application Reset	17
SRC_DMUHOST	DMU Host Service Request	00860_H	U,SV	SV,P1,P2	Application Reset	17
SRC_DMUFSI	DMU FSI Service Request	00864_H	U,SV	SV,P1,P2	Application Reset	17
SRC_HSMy (y=0-1)	HSM Service Request y	00870_H+ y*4	U,SV	SV,P1,P2	Application Reset	17
SRC_SCUERUx (x=0-3)	SCU ERU Service Request x	00880_H+ x*4	U,SV	SV,P1,P2	Application Reset	17
SRC_PMSDTS	PMS DTS Service Request	$008AC_H$	U,SV	SV,P1,P2	Application Reset	17
SRC_PMSx (x=0-3)	Power Management System Service Request x	$008B0_H$+ x*4	U,SV	SV,P1,P2	Application Reset	19
SRC_SCR	Stand By Controller Service Request	$008C0_H$	U,SV	SV,P1,P2	Application Reset	19
SRC_SMUy (y=0-2)	SMU Service Request y	$008D0_H$+ y*4	U,SV	SV,P1,P2	Application Reset	19
SRC_HSPDM0BFR	HSPDM0 Buffer Service Request	00900_H	U,SV	SV,P1,P2	Application Reset	19
SRC_HSPDM0RAMP	HSPDM0 RAMP Events Service Request	00904_H	U,SV	SV,P1,P2	Application Reset	19
SRC_HSPDM0ERR	HSPDM0 Error / RAM Overflow Service Request	00908_H	U,SV	SV,P1,P2	Application Reset	19

Table 188 Register Overview - SRC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
SRC_RIFxERR (x=0)	Radar Interface x Error Service Request	00970_H	U,SV	SV,P1,P2	Application Reset	19
SRC_RIFxINT (x=0)	Radar Interface x Service Request	00974_H	U,SV	SV,P1,P2	Application Reset	19
SRC_SPUxINT (x=0)	SPU x Service Request	00980_H	U,SV	SV,P1,P2	Application Reset	19
SRC_SPUxERR (x=0)	SPU x Error Service Request	00984_H	U,SV	SV,P1,P2	Application Reset	19
SRC_GPSRxy (x=0-1;y=0-7)	General Purpose Group x Service Request y	00990_H+ x*20_H+y* 4	U,SV	SV,P1,P2	Application Reset	21

16.5 TC33xEXT Specific Registers

16.5.1 IR Service Request Control Registers (SRC)

CPUx Software Breakpoint Service Request

SRC_CPUxSB (x=0-1)
CPUx Software Breakpoint Service Request (00000$_H$ + x*4) Debug Reset Value: 0000 0000$_H$
SRC_BCUSPB
SBCU Service Request [SPB Bus Control Unit) (00020$_H$) Debug Reset Value: 0000 0000$_H$
SRC_BCUBBB
EBCU Service Request [BBB Bus Control Unit, on ED and ADAS devices only)(00024$_H$) Debug Reset Value: 0000 0000$_H$
SRC_AGBT
AGBT Service Request [on ED devices only) (0002C$_H$) Debug Reset Value: 0000 0000$_H$
SRC_XBAR0
SRI Domain 0 Service Request (00030$_H$) Debug Reset Value: 0000 0000$_H$
SRC_CERBERUSy (y=0-1)
Cerberus Service Request y (00040$_H$+y*4) Debug Reset Value: 0000 0000$_H$
SRC_ASCLINxTX (x=0-5)
ASCLINx Transmit Service Request (00050$_H$+x*12) Application Reset Value: 0000 0000$_H$
SRC_ASCLINxRX (x=0-5)
ASCLINx Receive Service Request (00054$_H$+x*12) Application Reset Value: 0000 0000$_H$
SRC_ASCLINxERR (x=0-5)
ASCLINx Error Service Request (00058$_H$+x*12) Application Reset Value: 0000 0000$_H$
SRC_MTUDONE
MTU Done Service Request (000EC$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSCLR	SWS	IOVCLR	IOV	SETR	CLRR	SRR	0			ECC				
r	w	rh	w	rh	w	w	rh	r			rwh				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS			SRE	0		SRPN							
r		rw			rw	r		rw							

Field	Bits	Type	Description
SRPN	7:0	rw	**Service Request Priority Number** The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration): 00_H -> Service request is on lowest priority ... FF_H -> Service request is on highest priority **Notes** 1. *For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0.* 2. *For DMA, SRPN must not be greater than the highest implemented DMA channel number.*
SRE	10	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled
TOS	13:11	rw	**Type of Service Control** The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000_B CPU0 service is initiated 001_B DMA service is initiated 010_B CPU1 service is initiated **Others**, Reserved (no action)
ECC	20:16	rwh	**Error Correction Code** The ECC bit field will be updated by the SRN under the following conditions: • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	**Service Request Flag** The SRR bit shows the status of the Service Request. 0_B No service request is pending 1_B A service request is pending
CLRR	25	w	**Request Clear Bit** The CLRR bit is required to reset **SRR**. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	**Request Set Bit** The SETR bit is required to set **SRR**. 0_B No action 1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.

Field	Bits	Type	Description
IOV	27	rh	**Interrupt Trigger Overflow Bit** The IOV bit is set by HW if a new service request was triggered via interrupt trigger or **SETR** bit while the SRN has still an pending service request. 0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.
IOVCLR	28	w	**Interrupt Trigger Overflow Clear Bit** IOVCLR is required to reset **IOV**. 0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	**SW Sticky Bit** The Software Sticky Bit is set when the **SRR** bit has been set via the **SETR** bit. This bit can be cleared by writing with 1 to **SWSCLR**. Writing to SWS has no effect. 0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR
SWSCLR	30	w	**SW Sticky Clear Bit** SWSCLR is required to reset **SWS**. 0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	**Reserved** Read as 0; should be written with 0.

SRC_QSPIxTX (x=0-3)
QSPIx Transmit Service Request **($000F0_H$+x*14_H)** **Application Reset Value: 0000 0000_H**
SRC_QSPIxRX (x=0-3)
QSPIx Receive Service Request **($000F4_H$+x*14_H)** **Application Reset Value: 0000 0000_H**
SRC_QSPIxERR (x=0-3)
QSPIx Error Service Request **($000F8_H$+x*14_H)** **Application Reset Value: 0000 0000_H**
SRC_QSPIxPT (x=0-3)
QSPIx Phase Transition Service Request **($000FC_H$+x*14_H)** **Application Reset Value: 0000 0000_H**
SRC_QSPIxU (x=0-3)
QSPIx User Defined Service Request **(00100_H+x*14_H)** **Application Reset Value: 0000 0000_H**
SRC_QSPI2HC
QSPI2 High Speed Capture Service Request **(00178_H)** **Application Reset Value: 0000 0000_H**
SRC_QSPI3HC
QSPI3 High Speed Capture Service Request **($0017C_H$)** **Application Reset Value: 0000 0000_H**
SRC_SENTx (x=0-9)
SENT TRIGx Service Request **(00240_H+x*4)** **Application Reset Value: 0000 0000_H**
SRC_CCU6xSRy (x=0-1;y=0-3)
CCUx Service Request y **($002C0_H$+x*10_H+y*4)** **Application Reset Value: 0000 0000_H**
SRC_GPT120CIRQ
GPT120 CAPREL Service Request **($002E0_H$)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**SWSCLR**	**SWS**	**IOVCLR**	**IOV**	**SETR**	**CLRR**	**SRR**	**0**			**ECC**				
r	w	rh	w	rh	w	w	rh	r			rwh				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**TOS**			**SRE**	**0**		**SRPN**							
r		rw			rw	r		rw							

Field	Bits	Type	Description
SRPN	7:0	rw	**Service Request Priority Number** The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration): 00_H -> Service request is on lowest priority ... FF_H -> Service request is on highest priority **Notes** 1. *For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0.* 2. *For DMA, SRPN must not be greater than the highest implemented DMA channel number.*
SRE	10	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled

Field	Bits	Type	Description
TOS	13:11	rw	**Type of Service Control** The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000_B CPU0 service is initiated 001_B DMA service is initiated 010_B CPU1 service is initiated **Others**, Reserved (no action)
ECC	20:16	rwh	**Error Correction Code** The ECC bit field will be updated by the SRN under the following conditions: • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	**Service Request Flag** The SRR bit shows the status of the Service Request. 0_B No service request is pending 1_B A service request is pending
CLRR	25	w	**Request Clear Bit** The CLRR bit is required to reset **SRR**. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	**Request Set Bit** The SETR bit is required to set **SRR**. 0_B No action 1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.
IOV	27	rh	**Interrupt Trigger Overflow Bit** The IOV bit is set by HW if a new service request was triggered via interrupt trigger or **SETR** bit while the SRN has still an pending service request. 0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.
IOVCLR	28	w	**Interrupt Trigger Overflow Clear Bit** IOVCLR is required to reset **IOV**. 0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	**SW Sticky Bit** The Software Sticky Bit is set when the **SRR** bit has been set via the **SETR** bit. This bit can be cleared by writing with 1 to **SWSCLR**. Writing to SWS has no effect. 0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR

Field	Bits	Type	Description
SWSCLR	30	w	**SW Sticky Clear Bit** SWSCLR is required to reset **SWS**. 0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	**Reserved** Read as 0; should be written with 0.

SRC_GPT120T2
GPT120 Timer 2 Service Request **($002E4_H$)** **Application Reset Value: $0000\ 0000_H$**
SRC_GPT120T3
GPT120 Timer 3 Service Request **($002E8_H$)** **Application Reset Value: $0000\ 0000_H$**
SRC_GPT120T4
GPT120 Timer 4 Service Request **($002EC_H$)** **Application Reset Value: $0000\ 0000_H$**
SRC_GPT120T5
GPT120 Timer 5 Service Request **($002F0_H$)** **Application Reset Value: $0000\ 0000_H$**
SRC_GPT120T6
GPT120 Timer 6 Service Request **($002F4_H$)** **Application Reset Value: $0000\ 0000_H$**
SRC_STMxSRy (x=0-1;y=0-1)
System Timer x Service Request y **(00300_H+x*8+y*4)** **Application Reset Value: $0000\ 0000_H$**
SRC_FCE0
FCE0 Error Service Request **(00330_H)** **Application Reset Value: $0000\ 0000_H$**
SRC_DMAERRy (y=0-3)
DMA Error Service Request y **(00340_H+y*4)** **Application Reset Value: $0000\ 0000_H$**
SRC_DMACHy (y=0-63)
DMA Channel y Service Request **(00370_H+y*4)** **Application Reset Value: $0000\ 0000_H$**
SRC_SDMMCERR
SDMMC Error Service Request **(00570_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**SWSCLR**	**SWS**	**IOVCLR**	**IOV**	**SETR**	**CLRR**	**SRR**	**0**			**ECC**				
r	w	rh	w	rh	w	w	rh	r			rwh				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**TOS**			**SRE**	**0**		**SRPN**							
r		rw			rw	r		rw							

Field	Bits	Type	Description
SRPN	7:0	rw	**Service Request Priority Number** The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration): 00_H -> Service request is on lowest priority ... FF_H -> Service request is on highest priority **Notes** 1. *For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0.* 2. *For DMA, SRPN must not be greater than the highest implemented DMA channel number.*
SRE	10	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled
TOS	13:11	rw	**Type of Service Control** The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000_B CPU0 service is initiated 001_B DMA service is initiated 010_B CPU1 service is initiated **Others**, Reserved (no action)
ECC	20:16	rwh	**Error Correction Code** The ECC bit field will be updated by the SRN under the following conditions: • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	**Service Request Flag** The SRR bit shows the status of the Service Request. 0_B No service request is pending 1_B A service request is pending
CLRR	25	w	**Request Clear Bit** The CLRR bit is required to reset **SRR**. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	**Request Set Bit** The SETR bit is required to set **SRR**. 0_B No action 1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.

Field	Bits	Type	Description
IOV	27	rh	**Interrupt Trigger Overflow Bit** The IOV bit is set by HW if a new service request was triggered via interrupt trigger or **SETR** bit while the SRN has still an pending service request. 0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.
IOVCLR	28	w	**Interrupt Trigger Overflow Clear Bit** IOVCLR is required to reset **IOV**. 0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	**SW Sticky Bit** The Software Sticky Bit is set when the **SRR** bit has been set via the **SETR** bit. This bit can be cleared by writing with 1 to **SWSCLR**. Writing to SWS has no effect. 0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR
SWSCLR	30	w	**SW Sticky Clear Bit** SWSCLR is required to reset **SWS**. 0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	**Reserved** Read as 0; should be written with 0.

SRC_SDMMCDMA
SDMMC DMA Ready Service Request **(00574_H)** **Application Reset Value: 0000 0000$_H$**
SRC_GETHy (y=0-9)
GETH Service Request y **(00580_H+y*4)** **Application Reset Value: 0000 0000$_H$**
SRC_CAN0INTy (y=0-15)
CAN0 Service Request y **($005B0_H$+y*4)** **Application Reset Value: 0000 0000$_H$**
SRC_VADCGxSRy (x=0-5;y=0-3)
EVADC Group x Service Request y **(00670_H+x*10_H+y*4)** **Application Reset Value: 0000 0000$_H$**
SRC_VADCCGxSRy (x=0-1;y=0-3)
EVADC Common Group x Service Request y **(00750_H+x*10_H+y*4)** **Application Reset Value: 0000 0000$_H$**
SRC_DMUHOST
DMU Host Service Request **(00860_H)** **Application Reset Value: 0000 0000$_H$**
SRC_DMUFSI
DMU FSI Service Request **(00864_H)** **Application Reset Value: 0000 0000$_H$**
SRC_HSMy (y=0-1)
HSM Service Request y **(00870_H+y*4)** **Application Reset Value: 0000 0000$_H$**
SRC_SCUERUx (x=0-3)
SCU ERU Service Request x **(00880_H+x*4)** **Application Reset Value: 0000 0000$_H$**
SRC_PMSDTS
PMS DTS Service Request **($008AC_H$)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SWSCLR	SWS	IOVCLR	IOV	SETR	CLRR	SRR	0			ECC				
r	w	rh	w	rh	w	w	rh	r			rwh				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		TOS			SRE	0		SRPN							
r		rw			rw	r		rw							

Field	Bits	Type	Description
SRPN	7:0	rw	**Service Request Priority Number** The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration): 00_H -> Service request is on lowest priority ... FF_H -> Service request is on highest priority **Notes** 1. *For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0.* 2. *For DMA, SRPN must not be greater than the highest implemented DMA channel number.*
SRE	10	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled

Field	Bits	Type	Description
TOS	13:11	rw	**Type of Service Control** The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000_B CPU0 service is initiated 001_B DMA service is initiated 010_B CPU1 service is initiated **Others**, Reserved (no action)
ECC	20:16	rwh	**Error Correction Code** The ECC bit field will be updated by the SRN under the following conditions: • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	**Service Request Flag** The SRR bit shows the status of the Service Request. 0_B No service request is pending 1_B A service request is pending
CLRR	25	w	**Request Clear Bit** The CLRR bit is required to reset **SRR**. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	**Request Set Bit** The SETR bit is required to set **SRR**. 0_B No action 1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.
IOV	27	rh	**Interrupt Trigger Overflow Bit** The IOV bit is set by HW if a new service request was triggered via interrupt trigger or **SETR** bit while the SRN has still an pending service request. 0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.
IOVCLR	28	w	**Interrupt Trigger Overflow Clear Bit** IOVCLR is required to reset **IOV**. 0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	**SW Sticky Bit** The Software Sticky Bit is set when the **SRR** bit has been set via the **SETR** bit. This bit can be cleared by writing with 1 to **SWSCLR**. Writing to SWS has no effect. 0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR

Field	Bits	Type	Description
SWSCLR	30	w	**SW Sticky Clear Bit** SWSCLR is required to reset **SWS**. 0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	**Reserved** Read as 0; should be written with 0.

SRC_PMSx (x=0-3)
Power Management System Service Request x($008B0_H$+x*4) **Application Reset Value: 0000 0000$_H$**
SRC_SCR
Stand By Controller Service Request ($008C0_H$) **Application Reset Value: 0000 0000$_H$**
SRC_SMUy (y=0-2)
SMU Service Request y ($008D0_H$+y*4) **Application Reset Value: 0000 0000$_H$**
SRC_HSPDM0BFR
HSPDM0 Buffer Service Request (00900_H) **Application Reset Value: 0000 0000$_H$**
SRC_HSPDM0RAMP
HSPDM0 RAMP Events Service Request (00904_H) **Application Reset Value: 0000 0000$_H$**
SRC_HSPDM0ERR
HSPDM0 Error / RAM Overflow Service Request (00908_H) **Application Reset Value: 0000 0000$_H$**
SRC_RIF0ERR
Radar Interface 0 Error Service Request (00970_H) **Application Reset Value: 0000 0000$_H$**
SRC_RIF0INT
Radar Interface 0 Service Request (00974_H) **Application Reset Value: 0000 0000$_H$**
SRC_SPU0INT
SPU 0 Service Request (00980_H) **Application Reset Value: 0000 0000$_H$**
SRC_SPU0ERR
SPU 0 Error Service Request (00984_H) **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**SWSCLR**	**SWS**	**IOVCLR**	**IOV**	**SETR**	**CLRR**	**SRR**	**0**			**ECC**				
r	w	rh	w	rh	w	w	rh	r			rwh				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**TOS**			**SRE**	**0**		**SRPN**							
r		rw			rw	r		rw							

Field	Bits	Type	Description
SRPN	7:0	rw	**Service Request Priority Number** The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration): 00_H -> Service request is on lowest priority ... FF_H -> Service request is on highest priority **Notes** 1. *For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0.* 2. *For DMA, SRPN must not be greater than the highest implemented DMA channel number.*
SRE	10	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled
TOS	13:11	rw	**Type of Service Control** The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000_B CPU0 service is initiated 001_B DMA service is initiated 010_B CPU1 service is initiated **Others**, Reserved (no action)
ECC	20:16	rwh	**Error Correction Code** The ECC bit field will be updated by the SRN under the following conditions: • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	**Service Request Flag** The SRR bit shows the status of the Service Request. 0_B No service request is pending 1_B A service request is pending
CLRR	25	w	**Request Clear Bit** The CLRR bit is required to reset **SRR**. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	**Request Set Bit** The SETR bit is required to set **SRR**. 0_B No action 1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.

Field	Bits	Type	Description
IOV	27	rh	**Interrupt Trigger Overflow Bit** The IOV bit is set by HW if a new service request was triggered via interrupt trigger or **SETR** bit while the SRN has still an pending service request. 0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.
IOVCLR	28	w	**Interrupt Trigger Overflow Clear Bit** IOVCLR is required to reset **IOV**. 0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	**SW Sticky Bit** The Software Sticky Bit is set when the **SRR** bit has been set via the **SETR** bit. This bit can be cleared by writing with 1 to **SWSCLR**. Writing to SWS has no effect. 0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR
SWSCLR	30	w	**SW Sticky Clear Bit** SWSCLR is required to reset **SWS**. 0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	**Reserved** Read as 0; should be written with 0.

SRC_GPSRxy (x=0-1;y=0-7)

General Purpose Group x Service Request y(00990_H+x*20_H+y*4) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**SWSCLR**	**SWS**	**IOVCLR**	**IOV**	**SETR**	**CLRR**	**SRR**	**0**			**ECC**				
r	w	rh	w	rh	w	w	rh	r			rwh				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**TOS**			**SRE**	**0**		**SRPN**							
r		rw			rw	r		rw							

Field	Bits	Type	Description
SRPN	7:0	rw	**Service Request Priority Number** The SRPN bit field defines the priority of a service request with respect to service requests with to the same service provider (same SRC.TOS configuration): 00_H -> Service request is on lowest priority ... FF_H -> Service request is on highest priority **Notes** 1. *For a CPU 01_H is the lowest priority as 00_H is never serviced. For a DMA 00_H triggers channel 0.* 2. *For DMA, SRPN must not be greater than the highest implemented DMA channel number.*
SRE	10	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled
TOS	13:11	rw	**Type of Service Control** The TOS bit field configuration maps a Service Request to an Interrupt Service Provider: 000_B CPU0 service is initiated 001_B DMA service is initiated 010_B CPU1 service is initiated **Others**, Reserved (no action)
ECC	20:16	rwh	**Error Correction Code** The ECC bit field will be updated by the SRN under the following conditions: • Write or Read-Modify-Write to SRC[31:0] • Write to SRC[15:0] (16-bit write) • Write to SRC[15:8] or write to SRC[7:0] (byte write)
SRR	24	rh	**Service Request Flag** The SRR bit shows the status of the Service Request. 0_B No service request is pending 1_B A service request is pending
CLRR	25	w	**Request Clear Bit** The CLRR bit is required to reset **SRR**. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set in parallel.
SETR	26	w	**Request Set Bit** The SETR bit is required to set **SRR**. 0_B No action 1_B Set SRR and SWS; SRR bit value is not stored; read always returns 0; no action if CLRR is set in parallel.

Field	Bits	Type	Description
IOV	27	rh	**Interrupt Trigger Overflow Bit** The IOV bit is set by HW if a new service request was triggered via interrupt trigger or **SETR** bit while the SRN has still an pending service request. 0_B No Interrupt Trigger Overflow detected 1_B Interrupt Overflow Detected.
IOVCLR	28	w	**Interrupt Trigger Overflow Clear Bit** IOVCLR is required to reset **IOV**. 0_B No action 1_B Clear IOV; bit value is not stored; read always returns 0.
SWS	29	rh	**SW Sticky Bit** The Software Sticky Bit is set when the **SRR** bit has been set via the **SETR** bit. This bit can be cleared by writing with 1 to **SWSCLR**. Writing to SWS has no effect. 0_B No interrupt was initiated via SETR 1_B Interrupt was initiated via SETR
SWSCLR	30	w	**SW Sticky Clear Bit** SWSCLR is required to reset **SWS**. 0_B No action 1_B Clear SWS; bit value is not stored; read always returns 0.
0	9:8, 15:14, 23:21, 31	r	**Reserved** Read as 0; should be written with 0.

16.6 Revision History

Table 189 Revision History

Reference	Change to Previous Version	Comment
V1.2.6		
Page 9	Removed GTM related SRC registers	
Page 9	Increased DMA channel SRC registers from 16 to 64	
Page 9	Removed ERAY related SRC registers	
Page 9	Removed CAN1 related SRC registers	
Page 9	Removed all ASCLINx related SRC registers for x>5	
V1.2.7		
Page 9	Changed SRC_VADCGxSR configuration to (x=0-5)	
Page 9	Removed SRC_VADCG8SR and SRC_VADCG9SR	
V1.2.8		
	Removed connection table.	
V1.2.9		

Table 189 Revision History (cont'd)

Reference	Change to Previous Version	Comment
	No changes.	
V1.2.10		
–	No functional changes.	
V1.2.11		
Page 5	Updated bullet list item.	

17 Flexible CRC Engine (FCE)

For the general description of the module and the registers, please refer to the family spec.

17.1 TC33xEXT Specific IP Configuration

There are no device specific IP configurations.

17.2 TC33xEXT Specific Register Set

Table 190 Register Address Space - FCE

Module	Base Address	End Address	Note
FCE	$F0000000_H$	$F00001FF_H$	FPI slave interface

Table 191 Register Overview - FCE (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FCE_CLC	Clock Control Register	000_H	U,SV	E,SV,P	Application Reset	See Family Spec
FCE_ID	Module Identification Register	008_H	U,SV	BE	Application Reset	See Family Spec
FCE_CHSTS	Channels Status Register	020_H	U,SV	BE	Application Reset	See Family Spec
FCE_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_KRST1	Kernel Reset Register 1	$0F0_H$	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_KRST0	Kernel Reset Register 0	$0F4_H$	U,SV	SV,E,P	Application Reset	See Family Spec
FCE_ACCEN1	Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	See Family Spec
FCE_ACCEN0	Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	See Family Spec
FCE_IRi (i=0-7)	Input Register i	100_H+i*20$_H$	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_RESi (i=0-7)	CRC Result Register i	104_H+i*20$_H$	U,SV	BE	Application Reset	See Family Spec
FCE_CFGi (i=0-7)	CRC Configuration Register i	108_H+i*20$_H$	U,SV	P,E,SV	Application Reset	See Family Spec
FCE_STSi (i=0-7)	CRC Status Register i	$10C_H$+i*20$_H$	U,SV	P,U,SV	Application Reset	See Family Spec

Table 191 Register Overview - FCE (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FCE_LENGTHi (i=0-7)	CRC Length Register i	110_H+i*20$_H$	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CHECKi (i=0-7)	CRC Check Register i	114_H+i*20$_H$	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CRCi (i=0-7)	CRC Regsister i	118_H+i*20$_H$	U,SV	P,U,SV	Application Reset	See Family Spec
FCE_CTRi (i=0-7)	CRC Test Register i	$11C_H$+i*20$_H$	U,SV	P,U,SV	Application Reset	See Family Spec

17.3 TC33xEXT Specific Registers

No deviations from the Family Spec

17.4 Connectivity

Table 192 Connections of FCE

Interface Signals	connects		Description
FCE:SRC_FCE	to	INT:fce0.SRC_FCE	FCE Service Request

17.5 Revision History

Table 193 Revision History

Reference	Change to Previous Version	Comment
V4.2.9		
	Initial version of TC33X.	

18 Direct Memory Access (DMA)

This is the TC33xEXT specific information related to the DMA module of the AURIXTC3XX product family.

18.1 TC33xEXT Specific IP Configuration

The TC33xEXT DMA contains 64 DMA channels.

18.2 TC33xEXT Specific Register Set

Table 194 Register Address Space - DMA

Module	Base Address	End Address	Note
DMA	$F0010000_H$	$F0013FFF_H$	FPI slave interface

Table 195 Register Overview - DMA (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_CLC	DMA Clock Control Register	0000_H	U,SV	SV,E,P00,P01	Application Reset	See Family Spec
DMA_ID	DMA Identification Register	0008_H	U,SV	BE	Application Reset	See Family Spec
DMA_ACCENr0 (r=0-3)	RP r Access Enable Register 0	0040_H+r*8	U,SV	SV,SE	Application Reset	See Family Spec
DMA_ACCENr1 (r=0-3)	RP r Access Enable Register 1	0044_H+r*8	U,SV	nBE	Application Reset	See Family Spec
DMA_EERm (m=0-1)	ME m Enable Error Register	0120_H+m*1000_H	U,SV	SV	Application Reset	See Family Spec
DMA_ERRSRm (m=0-1)	ME m Error Status Register	0124_H+m*1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_CLREm (m=0-1)	ME m Clear Error Register	0128_H+m*1000_H	U,SV	SV	Application Reset	See Family Spec
DMA_MEmSR (m=0-1)	ME m Status Register	0130_H+m*1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm0R (m=0-1)	ME m Read Register 0	0140_H+m*1000_H	U,SV	BE	Application Reset	See Family Spec

Table 195 Register Overview - DMA (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_MEm1R (m=0-1)	ME m Read Register 1	0144_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm2R (m=0-1)	ME m Read Register 2	0148_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm3R (m=0-1)	ME m Read Register 3	$014C_H$+ m*1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm4R (m=0-1)	ME m Read Register 4	0150_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm5R (m=0-1)	ME m Read Register 5	0154_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm6R (m=0-1)	ME m Read Register 6	0158_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEm7R (m=0-1)	ME m Read Register 7	$015C_H$+ m*1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmRDCRC (m=0-1)	ME m Channel Read Data CRC Register	0180_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSDCRC (m=0-1)	ME m Channel Source and Destination Address CRC Register	0184_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSADR (m=0-1)	ME m Channel Source Address Register	0188_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmDADR (m=0-1)	ME m Channel Destination Address Register	$018C_H$+ m*1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmADICR (m=0-1)	ME m Channel Address and Interrupt Control Register	0190_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmCHCR (m=0-1)	ME m Channel Control Register	0194_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_MEmSHADR (m=0-1)	ME m Channel Shadow Address Register	0198_H+m *1000_H	U,SV	BE	Application Reset	See Family Spec

Table 195 Register Overview - DMA (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_MEmCHSR (m=0-1)	ME m Channel Status Register	$019C_H$+ m*1000_H	U,SV	BE	Application Reset	See Family Spec
DMA_OTSS	DMA OCDS Trigger Set Select	1200_H	U,SV	SV	See Family Spec	See Family Spec
DMA_PRR0	DMA Pattern Read Register 0	1208_H	U,SV	SV	Application Reset	See Family Spec
DMA_PRR1	DMA Pattern Read Register 1	$120C_H$	U,SV	SV	Application Reset	See Family Spec
DMA_TIME	DMA Time Register	1210_H	U,SV	BE	Application Reset	See Family Spec
DMA_MODEr (r=0-3)	RP r Mode Register	1300_H+r* 4	U,SV	SV,SE,P00, P01	Application Reset	See Family Spec
DMA_ERRINTRr (r=0-3)	RP r Error Interrupt Set Register	1320_H+r* 4	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_HRRc (c=000-63)	DMA Channel c Resource Partition Register	1800_H+c *4	U,SV	SV,SE,P00, P01	Application Reset	See Family Spec
DMA_SUSENRc (c=000-63)	DMA Channel c Suspend Enable Register	$1A00_H$+c *4	U,SV	SV,E,Pr	See Family Spec	See Family Spec
DMA_SUSACRc (c=000-63)	DMA Channel c Suspend Acknowledge Register	$1C00_H$+c *4	U,SV	BE	See Family Spec	See Family Spec
DMA_TSRc (c=000-63)	DMA Channel c Transaction State Register	$1E00_H$+c *4	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_RDCRCRc (c=000-63)	DMARAM Channel c Read Data CRC Register	2000_H+c *20_H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SDCRCRc (c=000-63)	DMARAM Channel c Source and Destination Address CRC Register	2004_H+c *20_H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SADRc (c=000-63)	DMARAM Channel c Source Address Register	2008_H+c *20_H	U,SV	SV,Pr	Application Reset	See Family Spec

Table 195 Register Overview - DMA (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
DMA_DADRc (c=000-63)	DMARAM Channel c Destination Address Register	$200C_H$+c *20_H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_ADICRc (c=000-63)	DMARAM Channel c Address and Interrupt Control Register	2010_H+c *20_H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_CHCFGRc (c=000-63)	DMARAM Channel c Configuration Register	2014_H+c *20_H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_SHADRc (c=000-63)	DMARAM Channel c Shadow Address Register	2018_H+c *20_H	U,SV	SV,Pr	Application Reset	See Family Spec
DMA_CHCSRc (c=000-63)	DMARAM Channel c Control and Status Register	$201C_H$+c *20_H	U,SV	SV,Pr	Application Reset	See Family Spec

18.3 TC33xEXT Specific Registers

No deviations from the Family Spec

18.4 Connectivity

Table 196 Connections of DMA

Interface Signals	connects		Description
DMA:fpi0_sleep_n	from	SCU:scu_syst_sleep_n	Sleep Control
DMA:ERR_INT(3:0)	to	INT:dma.ERR_INT(3:0)	DMA Error Service Request
DMA:CH_INT(127:0)	to	INT:dma.CH_INT(127:0)	DMA Channel Service Request

18.5 Revision History

Table 197 Revision History

Reference	Change to Previous Version	Comment
V0.1.15		
–	Initial version for TC33x.	
V0.1.16		
Page 1	Updated number of DMA channels.	
V0.1.17		
–	No functional changes.	
V0.1.18		
–	No functional changes.	

19 Signal Processing Unit (SPU)

This is the device specific information related to the AURIX™ TC33xEXT version of the SPU.

19.1 TC33xEXT Specific IP Configuration

There is no specific configuration of the SPU for this device

19.2 TC33xEXT Specific Register Set

Table 198 Register Address Space - SPU

Module	Base Address	End Address	Note
SPU0	$FA800000_H$	$FA8007FF_H$	BBB Slave Interface to the SPU Special Function Registers
(SPU0)	$FAA00000_H$	$FAA0FFFF_H$	BBB Slave Interface for Accessing the SPU Config RAM

Table 199 Register Overview - SPU0 (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
SPU0_CLC	Clock Control	00000_H	See Family Spec
SPU0_MODID	Module Identification Register	00004_H	See Family Spec
SPU0_STAT	Status and Reporting	00008_H	See Family Spec
SPU0_ID_CONF	Input DMA Configuration	00030_H	See Family Spec
SPU0_ID_CONF2	Input DMA Configuration 2	00034_H	See Family Spec
SPU0_ID_RM_CONF	Input DMA Configuration: Radar Memory	00038_H	See Family Spec
SPU0_ID_RM_ILO	Inner Loop Address Offset	$0003C_H$	See Family Spec
SPU0_ID_RM_OLO	Outer Loop Address Offset	00040_H	See Family Spec
SPU0_ID_RM_BLO	Bin Offset Address Configuration	00044_H	See Family Spec

Table 199 Register Overview - SPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
SPU0_ID_RM_IOLR	Inner and Outer Loop Repeat	00048_H	See Family Spec
SPU0_ID_RM_BLR	Bin Loop Repeat	$0004C_H$	See Family Spec
SPU0_ID_RM_ACFG0	Spare Configuration Register	00050_H	See Family Spec
SPU0_ID_RM_ACFG1	Spare Configuration Register	00054_H	See Family Spec
SPU0_PACTR	Partial-Acquisition Counter	00058_H	See Family Spec
SPU0_DPASS_CONF	Double Pass Configuration	$0005C_H$	See Family Spec
SPU0_BEx_LDR_CONF (x=0-1)	Loader Configuration	00060_H+x*40_H	See Family Spec
SPU0_BEx_LDR_CONF2 (x=0-1)	Loader Configuration Extended	00064_H+x*40_H	See Family Spec
SPU0_BEx_Aj_ANTOFST (j=0-3;x=0-1)	Antenna Offset	00068_H+x*40_H+j*4	See Family Spec
SPU0_BEx_UNLDR_CONF (x=0-1)	Unloader Configuration	00078_H+x*40_H	See Family Spec
SPU0_BEx_UNLDR_CONF2 (x=0-1)	Unloader Configuration 2	$0007C_H+x*40_H$	See Family Spec
SPU0_BEx_UNLDR_ACFG (x=0-1)	Spare Configuration Register	00080_H+x*40_H	See Family Spec
SPU0_BEx_ODP_CONF (x=0-1)	Output Data Processor Configuration	00084_H+x*40_H	See Family Spec
SPU0_BEx_NCICTRL (x=0-1)	NCI Control	00088_H+x*40_H	See Family Spec

Table 199 Register Overview - SPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
SPU0_BEx_SUMCTRL (x=0-1)	Summation Unit Control	$0008C_H$+x*40_H	See Family Spec
SPU0_BEx_PWRSUM (x=0-1)	Power Summation	00090_H+x*40_H	See Family Spec
SPU0_BEx_PWRCTRL (x=0-1)	Power Information Channel Control	00094_H+x*40_H	See Family Spec
SPU0_BEx_CFARCTRL (x=0-1)	CFAR Module Control	00098_H+x*40_H	See Family Spec
SPU0_BEx_SBCTRL (x=0-1)	Sideband Control	$0009C_H$+x*40_H	See Family Spec
SPU0_BINm_REJ (m=0-63)	Bin Rejection Mask	$000E0_H$+m*4	See Family Spec
SPU0_MAGAPPROX	Magnitude Approximation Constants	$001E0_H$	See Family Spec
SPU0_NCISCALAR0	NCI Antennae Scaling Factor	$001E4_H$	See Family Spec
SPU0_NCISCALAR1	NCI Antennae Scaling Factor	$001E8_H$	See Family Spec
SPU0_NCISCALAR2	NCI Antennae Scaling Factor	$001EC_H$	See Family Spec
SPU0_NCISCALAR3	NCI Antennae Scaling Factor	$001F0_H$	See Family Spec
SPU0_CFARCFG	CFAR Configuration	$001F4_H$	See Family Spec
SPU0_CFARCFG2	CFAR Configuration 2	$001F8_H$	See Family Spec
SPU0_CFARCFG3	CFAR Configuration 3	$001FC_H$	See Family Spec

Table 199 Register Overview - SPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
SPU0_SCALARADD	Scalar Addition Operand	00200_H	See Family Spec
SPU0_SCALARMULT	Scalar Multiplication Operand	00204_H	See Family Spec
SPU0_BINREJCTRL	Bin Rejection Unit Control	00208_H	See Family Spec
SPU0_LCLMAX	Local Maximum Control	$0020C_H$	See Family Spec
SPU0_ACFG2	Spare Configuration Register	00210_H	See Family Spec
SPU0_REGCRC	Register CRC	00218_H	See Family Spec
SPU0_CTRL	SPU Control	$0021C_H$	See Family Spec
SPU0_MDq_METADATA (q=0-1)	Dataset Metadata	00220_H+q*88_H	See Family Spec
SPU0_MDq_BINCOUNT (q=0-1)	Bin Rejection Unit Tracking	00224_H+q*88_H	See Family Spec
SPU0_MDq_MASKm_ACCEPT (m=0-31;q=0-1)	Bin Acceptance Mask	00228_H+q*88_H +m*4	See Family Spec
SPU0_IDMCNT	Input DMA Count	00330_H	See Family Spec
SPU0_IBMCNT	Input Buffer Memory Count	00334_H	See Family Spec
SPU0_LDRCNT	Input Buffer Memory Read Count	00338_H	See Family Spec
SPU0_FFTWCNT	FFT Load Count	$0033C_H$	See Family Spec

Table 199 Register Overview - SPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
SPU0_FFTRCNT	FFT Unload Count	00340_H	See Family Spec
SPU0_ULDRCNT	Output Buffer Memory Write Count	00344_H	See Family Spec
SPU0_ODMCNT	Output Buffer Memory Read Count	00348_H	See Family Spec
SPU0_BRCNT	Bin Rejection Unit Load Count	$0034C_H$	See Family Spec
SPU0_CFARCNT	CFAR Unit Load Count	00350_H	See Family Spec
SPU0_ODMACNTp (p=0-7)	Output DMA Port Write Count	00354_H+p*4	See Family Spec
SPU0_CNTCLR	Safety Counter Clear	00374_H	See Family Spec
SPU0_MONITOR	SPU Monitor	00378_H	See Family Spec
SPU0_SMCTRL	Safety Mechanism Control Functions	$0037C_H$	See Family Spec
SPU0_SMSTAT	Safety Mechanism Status	00380_H	See Family Spec
SPU0_SMUSER	Safety Mechanism Control Functions (User)	00384_H	See Family Spec
SPU0_DATAd_CRC (d=0-85)	Monitor CRC Register	00388_H+d*4	See Family Spec
SPU0_CTRLe_CRC (e=0-24)	Monitor CRC Register	00500_H+e*4	See Family Spec
SPU0_USROTC	User OCDS Trace Control	$007E0_H$	See Family Spec

Table 199 Register Overview - SPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
SPU0_ACCEN0	Access Enable Register 0	$007E4_H$	See Family Spec
SPU0_ACCEN1	Access Enable Register 1	$007E8_H$	See Family Spec
SPU0_OCS	OCDS Control and Status	$007EC_H$	See Family Spec
SPU0_ODA	OCDS Debug Access Register	$007F0_H$	See Family Spec
SPU0_KRST0	Kernel Reset Register 0	$007F4_H$	See Family Spec
SPU0_KRST1	Kernel Reset Register 1	$007F8_H$	See Family Spec
SPU0_KRSTCLR	Kernel Reset Clear	$007FC_H$	See Family Spec

19.3 TC33xEXT Specific Registers

No deviations from the Family Spec

19.4 Connectivity

Connectivity of the SPUs in the AURIX™ TC33xEXT is as follows

Table 200 Connections of SPU0

Interface Signals	connects		Description
SPU0:RIFDV0	from	RIF0:spu_data_valid	Radar Data Valid from RIF0
SPU0:SD	to	SPU0:SDI0	SPU Done Output
SPU0:SDI0	from	SPU0:SD	Done indication from SPU0
SPU0:safety_alarm	to	SMU:safety_alarm=spu.spu0_safety_alarm.safety_alarm	SPU Alarm
SPU0:INT	to	INT:spu0.INT	SPU Service Request
SPU0:ERR		INT:spu0.ERR	

19.5 Revision History

Table 201 Revision History

Reference	Change to Previous Version	Comment
V1.1.20		
Page 7	Previous versions removed from revision history.	
V1.1.21		
All	Text Insets updated for new tools and source versions. All tables updated.	
V1.1.22		
All	Text Insets updated as part of document generation flow. All tables updated. No functional changes.	
V1.1.23		
Page 6	**Section 19.4** Tables updated to fix formatting error in interrupt connections	
V1.1.24		
All	Text Insets updated as part of document generation flow. All tables updated. No functional changes.	
V1.1.25		
All	Text Insets updated as part of document generation flow. All tables updated. No functional changes.	

20 SPU Lockstep Comparator (SPULCKSTP)

This device doesn’t contain a SPULCKSTP module.

21 Extended Memory (EMEM)

This is the TC33xEXT specific information related to the EMEM module of the AURIXTC3XX product family.

21.1 TC33xEXT Specific IP Configuration

The TC33xEXT EMEM contains 1 Mbyte of extension memory in one instance of the EMEM module.

21.2 TC33xEXT Specific Register Set

Table 202 Register Address Space - EMEM

Module	Base Address	End Address	Note
EMEM	$FA006000_H$	$FA0060FF_H$	BPI SFF (access to EMEM core registers)

Table 203 Register Address Space - EMEM_MPU

Module	Base Address	End Address	Note
EMEMMPU0	$FB000000_H$	$FB00FFFF_H$	SRI slave interface 0 (access to EMEM module registers)

Table 204 Register Address Space - EMEM_RAM

Module	Base Address	End Address	Note
(EMEMRAM0)	99000000_H	$990FFFFF_H$	BBB slave interface 0 (access to EMEM module RAM, cached segment)
	99000000_H	$990FFFFF_H$	SRI slave interface 0 (access to EMEM module RAM, cached segment)
	$B9000000_H$	$B90FFFFF_H$	BBB slave interface 0 (access to EMEM module RAM, non-cached segment)
	$B9000000_H$	$B90FFFFF_H$	SRI slave interface 0 (access to EMEM module RAM, non-cached segment)

Table 205 Register Address Space - XTM

Module	Base Address	End Address	Note
(XTM)	$B9400000_H$	$B947FFFF_H$	XTM FPI slave interface

Table 206 Register Overview - EMEM (ascending Offset Address)

Short Name	Description	Offset Address	Access Mode		Page Number
			Read	Write	
EMEM_CLC	EMEM Core Clock Control Register	0000_H	U,SV	SV,E,P	See Family Spec
EMEM_ID	EMEM Core Module Identification Register	0008_H	U,SV	BE	See Family Spec
EMEM_TILECONFIG	EMEM Core Tile Configuration Register	0020_H	U,SV	U,SV,P	See Family Spec
EMEM_TILECC	EMEM Core Tile Control Common Memory Register	0024_H	U,SV	U,SV,P	See Family Spec
EMEM_TILECT	EMEM Core Tile Control Trace Memory Register	0028_H	U,SV	U,SV,P	See Family Spec
EMEM_TILESTATE	EMEM Core Tile Status Register	$002C_H$	U,SV	BE	See Family Spec
EMEM_SBRCTR	EMEM Core Standby RAM Control Register	0034_H	U,SV	U,SV,P	See Family Spec
EMEM_ACCEN1	EMEM Core Access Enable Register 1	$00F8_H$	U,SV	BE	See Family Spec
EMEM_ACCEN0	EMEM Core Access Enable Register 0	$00FC_H$	U,SV	SV,SE	See Family Spec

Table 207 Register Overview - EMEMMPU0 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
EMEMMPU0_CLC	EMEM Module Clock Control Register	00000_H	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU0_MODID	EMEM Module ID Register	00008_H	SV	R	Application Reset	See Family Spec
EMEMMPU0_ACCEN0	EMEM Module Access Enable Register 0	00010_H	SV	SV,SE	Application Reset	See Family Spec

Table 207 Register Overview - EMEMMPU0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
EMEMMPU0_ACCEN1	EMEM Module Access Enable Register 1	00014_H	SV	SV,SE	Application Reset	See Family Spec
EMEMMPU0_MEMCON	EMEM Module Memory Control Register	00020_H	SV	SV,E,P	Application Reset	See Family Spec
EMEMMPU0_SCTRL	EMEM Module Safety Control Register	00024_H	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGNLAi (i=0-7)	EMEM Module Region i Lower Address Register	00050_H+i *10_H	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGNUAi (i=0-7)	EMEM Module Region i Upper Address Register	00054_H+i *10_H	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGNACCENWAi (i=0-7)	EMEM Module Region i Write Access Enable Register 0	00058_H+i *10_H	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGNACCENWBi (i=0-7)	EMEM Module Region i Write Access Enable Register 1	$0005C_H$+i *10_H	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGNACCENRAi (i=0-7)	EMEM Module Region i Read Access Enable Register 0	$000D8_H$+ i*10_H	SV	SV,SE,P	Application Reset	See Family Spec
EMEMMPU0_RGNACCENRBi (i=0-7)	EMEM Module Region i Read Access Enable Register 1	$000DC_H$+ i*10_H	SV	SV,SE,P	Application Reset	See Family Spec

21.3 TC33xEXT Specific Registers

There are no TC33xEXT specific registers in the EMEM.

21.4 Connectivity

Nothing included at this release

21.5 Revision History

Table 208 Revision History

Reference	Change to Previous Version	Comment
V1.3.13		
	Initial version for TC33X.	
V1.3.14		
Page 1	Correction of configuration size in chapter 1.1	
V1.4.1		
Page 2	Add extra registers TILESTATE1 and TILECONFIG1 to support increased memory size.	
V1.4.2		
–	No functional changes.	
V1.4.3		
–	No functional changes.	
V1.4.4		
–	No functional changes.	

22 Radar Interface (RIF)

This chapter describes the Radar Interface (RIF) module of the TC33xEXT.

22.1 TC33xEXT Specific IP Configuration

See features in the family spec.

Table 209 TC33xEXT specific configuration of RIF

Parameter	RIF0
Software Triggered Reset of the Module Kernel This reset does not affect the bus interfaces and therefore cannot cause a protocol violation. Other outputs are synchronously forced to the idle state	Kernel Reset (software controlled by KRST0-1 registers)

22.2 TC33xEXT Specific Register Set

22.2.1 Address Map

Table 210 Register Address Space - RIF

Module	Base Address	End Address	Note
RIF0	$FA040000_H$	$FA0401FF_H$	FPI slave interface

Note: The absolute register address is calculated as follows: Module Base Address + Offset Address

A register is addressed word wise.

22.3 TC33xEXT Specific Registers

No deviations from the Family Spec

22.4 Connectivity

Table 211 Connections of RIF0

Interface Signals	connects		Description
RIF0:RAMP1B	from	P02.6:IN	External RAMP B input
RIF0:safety_alarm	to	SMU:rif0_safety_alarm	RIF Alarm
RIF0:ERR	to	INT:rif0.ERR	Radar Interface Service Request
RIF0:INT		INT:rif0.INT	

Table 212 Connections of RIF0

Interface Signals	connects		Description
RIF0:CLKN	from	TC33xEXT:P50.4	LVDS RX Input (inverted Serial Clock)
RIF0:CLKP	from	TC33xEXT:P50.5	LVDS RX Input (Serial Clock)

Table 212 Connections of RIF0 (cont'd)

Interface Signals	connects		Description
RIF0:D1N	from	TC33xEXT:P50.0	LVDS RX Input (inverted Data Bits of Channel #0)
RIF0:D2N	from	TC33xEXT:P50.2	LVDS RX Input (inverted Data Bits of Channel #1)
RIF0:D3N	from	TC33xEXT:P50.8	LVDS RX Input (inverted Data Bits of Channel #2)
RIF0:D4N	from	TC33xEXT:P50.10	LVDS RX Input (inverted Data Bits of Channel #3)
RIF0:D1P	from	TC33xEXT:P50.1	LVDS RX Input (Data Bits of Channel #0)
RIF0:D2P	from	TC33xEXT:P50.3	LVDS RX Input (Data Bits of Channel #1)
RIF0:D3P	from	TC33xEXT:P50.9	LVDS RX Input (Data Bits of Channel #2)
RIF0:D4P	from	TC33xEXT:P50.11	LVDS RX Input (Data Bits of Channel #3)
RIF0:FRN	from	TC33xEXT:P50.6	LVDS RX Input (inverted FrameClock)
RIF0:FRP	from	TC33xEXT:P50.7	LVDS RX Input (FrameClock)

22.5 Revision History

Table 213 Revision History

Reference	Change to Previous Version	Comment
V1.0.36		
All	Initial Version TC33x.	
V1.0.37		
–	No functional changes.	–
V1.0.38		
–	No functional changes.	–
V1.0.39		
–	Device specific registers (RIF0_FLM, RIF0_INTCON, RIF0_FLAGSSET) are moved from the family spec to the appendix. No functional changes.	–
V1.0.40		
–	For registers from ESI to REGCRC, Kernel reset values are added for clarification. Device specific register, RIF0_FLAGSCL is moved from the family spec to the appendix.	
–	Device specific registers (RIF0_DBGDLY0, RIF0_DBGDLY1) are moved from the family spec to the appendix.	

Table 213 Revision History

Reference	Change to Previous Version	Comment
–	Device specific register, RIF0_ESI is moved from the family spec to the appendix.	
–	No functional changes.	–
V1.0.41		
–	No functional changes.	–
V1.0.42		
–	No functional changes.	–
V1.0.43		
–	References to TC3Ax are removed	

23 High Speed Pulse Density Modulation Module (HSPDM)

Text with reference to family spec.

23.1 TC33xEXT Specific IP Configuration

See features in the family spec.

Table 214 TC33xEXT specific configuration of HSPDM

Parameter	HSPDM
HSPDM ram	$F0280000_H$
HSPDM ram size	2000_H
HSPDM BPI registers	$F0282000_H$
HSPDM BPI registers size	100_H
SRAM size in byte	8192

23.2 TC33xEXT Specific Register Set

There are no specific register set.

23.2.1 Address Map

Table 215 Register Address Space - HSPDM

Module	Base Address	End Address	Note
(HSPDM)	$F0280000_H$	$F0281FFF_H$	FPI slave interface for SRAM access
HSPDM	$F0282000_H$	$F02820FF_H$	FPI slave interface for BPI registers access

Note: The absolute register address is calculated as follows: Module Base Address + Offset Address

A register is addressed word wise.

HSPDM RAM takes 8KBytes address space starting from 0xF028 0000 to 0xF028 1FFF.

23.3 TC33xEXT Specific Registers

There are no device specific registers for HSPDM in TC33xEXT.

23.4 Connectivity

There will be connections to the VADC.

23.4.1 Connections Regarding Hardware Run Feature

HSPDM module can be started by a CAN message. The reception (or transmision) of CAN messsage can trigger an interrupt. The interrupt signal can be delayed by a CCU6 timer module for a programmable time interval. The delayed interrupt signal can be used for starting the HSPDM module.

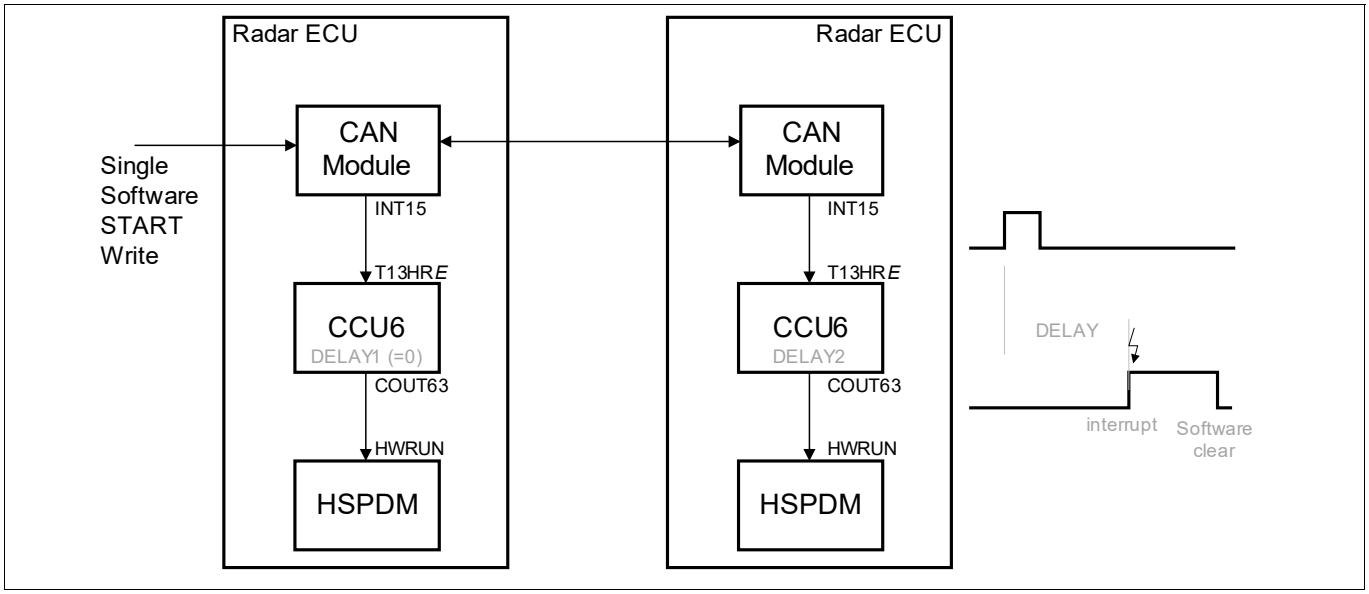


Figure 6 Hardware Run Connections

23.4.2 Pinning and Layout

The output signals of the HSPDM module are connected to the following pads:

- P22.3 - MUTE
- P22.4 - BS0
- P22.5 - BS1

23.5 Revision History

Table 216 Revision History

Reference	Change to Previous Version	Comment
V0.7.9		
Page 2	Typo “Histrory” fixed.	

24 Camera and ADC Interface (CIF)

This device doesn’t contain a CIF module.

25 System Timer (STM)

This chapter describes the device specific details in TC33xEXT.

25.1 TC33xEXT Specific IP Configuration

See features in family spec

25.2 TC33xEXT Specific Register Set

Register Address Space Table

The address space for the module registers is defined below

Table 217 Register Address Space - STM

Module	Base Address	End Address	Note
STM0	$F0001000_H$	$F00010FF_H$	FPI slave interface
STM1	$F0001100_H$	$F00011FF_H$	FPI slave interface

Register Overview Table

There are no product specific register for this module.

25.3 TC33xEXT Specific Registers

There are no product specific register for this module.

25.4 Connectivity

The tables below list all the connections of STM instances.

Table 218 Connections of STM0

Interface Signals	connects		Description
STM0:SR0_INT	to	INT:stm0.SR0_INT	System Timer Service Request 0
		CAN0:STM0.SR0_INT	
STM0:SR1_INT	to	INT:stm0.SR1_INT	System Timer Service Request 1
		CAN0:STM0.SR1_INT	

Table 219 Connections of STM1

Interface Signals	connects		Description
STM1:SR0_INT	to	INT:stm1.SR0_INT	System Timer Service Request 0
		CAN0:STM1.SR0_INT	
STM1:SR1_INT	to	INT:stm1.SR1_INT	System Timer Service Request 1
		CAN0:STM1.SR1_INT	

25.5 Revision History

Table 220 Revision History

Reference	Change to Previous Version	Comment
V9.2.3		
–	Initial version for TC33X.	
V9.2.4		
Page 1	Connection tables updated (no functional changes).	

26 Generic Timer Module (GTM)

This device doesn’t contain a GTM.

27 Capture/Compare Unit 6 (CCU6)

This chapter describes the specific properties of the product TC33xEXT, which is a member of the product family TC3XX.

The functionality of the CCU6 is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

27.1 TC33xEXT Specific Register Set

Table 221 Register Address Space - CCU6

Module	Base Address	End Address	Note
CCU60	$F0002A00_H$	$F0002AFF_H$	FPI slave interface
CCU61	$F0002B00_H$	$F0002BFF_H$	FPI slave interface

Note: Register MOSEL controls the trigger signals from both CCU6 kernels (CCU60 and CCU61) of the CCU6 module, and is only available in the address space of kernel CCU60.

Register Overview Tables of CCU6

Table 222 Register Overview - CCU60 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_CLC	Clock Control Register	0000_H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_MCFG	Module Configuration Register	0004_H	U,SV	U,SV,P	See Family Spec	See Family Spec
CCU60_ID	Module Identification Register	0008_H	U,SV	BE	See Family Spec	See Family Spec
CCU60_MOSEL	CCU60 Module Output Select Register	$000C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PISEL0	Port Input Select Register 0	0010_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PISEL2	Port Input Select Register 2	0014_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_KSCSR	Kernel State Control Sensitivity Register	$001C_H$	U,SV	U,SV,P,OEN	See Family Spec	See Family Spec
CCU60_T12	Timer T12 Counter Register	0020_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 222 Register Overview - CCU60 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_T12PR	Timer 12 Period Register	0024_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T12DTC	Dead-Time Control Register for Timer12	0028_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC6xR (x=0-2)	Capture/Compare Register for Channel CC6x	0030_H+x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC6xSR (x=0-2)	Capture/Compare Shadow Reg. for Channel CC6x	0040_H+x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T13	Timer T13 Counter Register	0050_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T13PR	Timer 13 Period Register	0054_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC63R	Compare Register for T13	0058_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CC63SR	Compare Shadow Register for T13	$005C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CMPSTAT	Compare State Register	0060_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_CMPMODIF	Compare State Modification Register	0064_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_T12MSEL	T12 Mode Select Register	0068_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR0	Timer Control Register 0	0070_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR2	Timer Control Register 2	0074_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TCTR4	Timer Control Register 4	0078_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 222 Register Overview - CCU60 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_MODCTR	Modulation Control Register	0080_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_TRPCTR	Trap Control Register	0084_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_PSLR	Passive State Level Register	0088_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMOUTS	Multi-Channel Mode Output Shadow Register	$008C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMOUT	Multi-Channel Mode Output Register	0090_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_MCMCTR	Multi-Channel Mode Control Register	0094_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IMON	Input Monitoring Register	0098_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_LI	Lost Indicator Register	$009C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IS	Interrupt Status Register	$00A0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_ISS	Interrupt Status Set Register	$00A4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_ISR	Interrupt Status Reset Register	$00A8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_INP	Interrupt Node Pointer Register	$00AC_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_IEN	Interrupt Enable Register	$00B0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU60_OCS	OCDS Control and Status Register	$00E8_H$	U,SV	SV,P,OEN	See Family Spec	See Family Spec

Table 222 Register Overview - CCU60 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU60_KRSTCLR	Kernel Reset Status Clear Register	$00EC_H$	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_KRST1	Kernel Reset Register 1	$00F0_H$	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_KRST0	Kernel Reset Register 0	$00F4_H$	U,SV	SV,E,P	Application Reset	See Family Spec
CCU60_ACCEN0	Access Enable Register 0	$00FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

Table 223 Register Overview - CCU61 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_CLC	Clock Control Register	0000_H	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_MCFG	Module Configuration Register	0004_H	U,SV	U,SV,P	See Family Spec	See Family Spec
CCU61_ID	Module Identification Register	0008_H	U,SV	BE	See Family Spec	See Family Spec
CCU61_PISEL0	Port Input Select Register 0	0010_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_PISEL2	Port Input Select Register 2	0014_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_KSCSR	Kernel State Control Sensitivity Register	$001C_H$	U,SV	U,SV,P,OEN	See Family Spec	See Family Spec
CCU61_T12	Timer T12 Counter Register	0020_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T12PR	Timer 12 Period Register	0024_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 223 Register Overview - CCU61 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_T12DTC	Dead-Time Control Register for Timer12	0028_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC6xR (x=0-2)	Capture/Compare Register for Channel CC6x	0030_H+x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC6xSR (x=0-2)	Capture/Compare Shadow Reg. for Channel CC6x	0040_H+x *4	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T13	Timer T13 Counter Register	0050_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T13PR	Timer 13 Period Register	0054_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC63R	Compare Register for T13	0058_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CC63SR	Compare Shadow Register for T13	$005C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CMPSTAT	Compare State Register	0060_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_CMPMODIF	Compare State Modification Register	0064_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_T12MSEL	T12 Mode Select Register	0068_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR0	Timer Control Register 0	0070_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR2	Timer Control Register 2	0074_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_TCTR4	Timer Control Register 4	0078_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MODCTR	Modulation Control Register	0080_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 223 Register Overview - CCU61 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_TRPCTR	Trap Control Register	0084_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_PSLR	Passive State Level Register	0088_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMOUTS	Multi-Channel Mode Output Shadow Register	$008C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMOUT	Multi-Channel Mode Output Register	0090_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_MCMCTR	Multi-Channel Mode Control Register	0094_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IMON	Input Monitoring Register	0098_H	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_LI	Lost Indicator Register	$009C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IS	Interrupt Status Register	$00A0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_ISS	Interrupt Status Set Register	$00A4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_ISR	Interrupt Status Reset Register	$00A8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_INP	Interrupt Node Pointer Register	$00AC_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_IEN	Interrupt Enable Register	$00B0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
CCU61_OCS	OCDS Control and Status Register	$00E8_H$	U,SV	SV,P,OEN	See Family Spec	See Family Spec
CCU61_KRSTCLR	Kernel Reset Status Clear Register	$00EC_H$	U,SV	SV,E,P	Application Reset	See Family Spec

Table 223 Register Overview - CCU61 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CCU61_KRST1	Kernel Reset Register 1	$00F0_H$	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_KRST0	Kernel Reset Register 0	$00F4_H$	U,SV	SV,E,P	Application Reset	See Family Spec
CCU61_ACCEN0	Access Enable Register 0	$00FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

27.2 TC33xEXT Specific Registers

No deviations from the Family Spec

27.3 Connectivity

Table 224 Connections of CCU60

Interface Signals	connects		Description
CCU60:CC60	to	P02.0:ALT(7)	T12 PWM channel 60
		P02.6:ALT(7)	
		P11.12:ALT(7)	
		P15.6:ALT(7)	
		P34.2:ALT(7)	
CCU60:CC61	to	P02.2:ALT(7)	T12 PWM channel 61
		P02.7:ALT(7)	
		P11.11:ALT(7)	
		P15.5:ALT(7)	
CCU60:CC62	to	P02.4:ALT(7)	T12 PWM channel 62
		P02.8:ALT(7)	
		P11.10:ALT(7)	
		P15.4:ALT(7)	
CCU60:CC60INA	from	P02.0:IN	T12 capture input 60
CCU60:CC61INA	from	P02.2:IN	T12 capture input 61
CCU60:CC62INA	from	P02.4:IN	T12 capture input 62
CCU60:CC60INB	from	P00.1:IN	T12 capture input 60
CCU60:CC61INB	from	P00.3:IN	T12 capture input 61
CCU60:CC62INB	from	P00.5:IN	T12 capture input 62
CCU60:CC60INC	from	P02.6:IN	T12 capture input 60
CCU60:CC61INC	from	P02.7:IN	T12 capture input 61
CCU60:CC62INC	from	P02.8:IN	T12 capture input 62

Table 224 Connections of CCU60 (cont'd)

Interface Signals	connects		Description
CCU60:CC60IND	from	PMS:pms_wut_underflow	T12 capture input 60
CCU60:CC62IND	from	SCU:E_PDOUT(4)	T12 capture input 62
CCU60:CCPOS0A	from	P02.6:IN	Hall capture input 0
CCU60:CCPOS1A	from	P02.7:IN	Hall capture input 1
CCU60:CCPOS2A	from	P02.8:IN	Hall capture input 2
CCU60:CCPOS0B	from	CCU61:SR(2)	Hall capture input 0
CCU60:CCPOS0C	from	P10.4:IN	Hall capture input 0
CCU60:CCPOS1C	from	P10.7:IN	Hall capture input 1
CCU60:CCPOS2C	from	P10.8:IN	Hall capture input 2
CCU60:COUT60	to	SCU:E_REQ0(1)	T12 PWM channel 60
		P02.1:ALT(7)	
		P11.9:ALT(7)	
		P15.7:ALT(7)	
		P34.3:ALT(7)	
CCU60:COUT61	to	P02.3:ALT(7)	T12 PWM channel 61
		P11.6:ALT(7)	
		P15.8:ALT(7)	
CCU60:COUT62	to	P02.5:ALT(7)	T12 PWM channel 62
		P11.3:ALT(7)	
		P14.0:ALT(7)	
CCU60:COUT63	to	P00.0:ALT(7)	T13 PWM channel 63
		P11.2:ALT(7)	
		P14.1:ALT(7)	
		P32.4:ALT(7)	
		P34.1:ALT(7)	
		PMS:dcdc_sync_ccu6	
CCU60:CTRAPB	from	CCU60:WHE_N	Trap input capture
CCU60:CTRAPD	from	SCU:E_PDOUT(0)	Trap input capture
CCU60:SR(0)	to	HSM:EXT_INT(10)	Service request
CCU60:SR(1)	to	CCU60:T13HRH	Service request
CCU60:SR(2)	to	CCU61:CCPOS0B	Service request
		CCU61:T12HRG	
		CCU61:T13HRG	

Table 224 Connections of CCU60 (cont'd)

Interface Signals	connects		Description
CCU60:SR(3)	to	EVADC:G0REQTRA	Service request
		EVADC:G1REQTRA	
		EVADC:G2REQTRA	
		EVADC:G3REQTRA	
		EVADC:G4REQTRA	
		EVADC:G5REQTRA	
CCU60:T12HRA	from	SCU:scu_cctrig0	External timer start 12
CCU60:T13HRA	from	SCU:scu_cctrig0	External timer start 13
CCU60:T12HRB	from	P00.7:IN	External timer start 12
CCU60:T13HRB	from	P00.8:IN	External timer start 13
CCU60:T12HRC	from	P00.9:IN	External timer start 12
CCU60:T13HRC	from	P00.9:IN	External timer start 13
CCU60:T12HRE	from	P00.0:IN	External timer start 12
CCU60:T12HRF	from	GPT120:T6OFL	External timer start 12
CCU60:T13HRF	from	GPT120:T6OFL	External timer start 13
CCU60:T12HRG	from	CCU61:SR(2)	External timer start 12
CCU60:T13HRG	from	CCU61:SR(2)	External timer start 13
CCU60:T12HRH	from	SCU:E_PDOUT(0)	External timer start 12
CCU60:T13HRH	from	CCU60:SR(1)	External timer start 13
CCU60:TRIG(0)	to	EVADC:G0REQGTC	Output select trigger
		EVADC:G1REQGTC	
		EVADC:G2REQGTC	
		EVADC:G3REQGTC	
		EVADC:G4REQGTC	
		EVADC:G5REQGTC	
CCU60:TRIG(1)	to	EVADC:G0REQGTD	Output select trigger
		EVADC:G1REQGTD	
		EVADC:G2REQGTD	
		EVADC:G3REQGTD	
		EVADC:G4REQGTD	
		EVADC:G5REQGTD	
CCU60:TRIG(2)	to	EVADC:G0REQGTE	Output select trigger
		EVADC:G1REQGTE	
		EVADC:G2REQGTE	
		EVADC:G3REQGTE	
		EVADC:G4REQGTE	
		EVADC:G5REQGTE	
CCU60:WHE_N	to	CCU60:CTRAPB	Set wrong hall event negative

Table 225 Connections of CCU61

Interface Signals	connects		Description
CCU61:CC60	to	P00.1:ALT(7)	T12 PWM channel 60
		P00.7:ALT(7)	
		P20.8:ALT(7)	
		P33.13:ALT(7)	
CCU61:CC61	to	P00.3:ALT(7)	T12 PWM channel 61
		P00.8:ALT(7)	
		P20.9:ALT(7)	
		P33.11:ALT(7)	
CCU61:CC62	to	P00.5:ALT(7)	T12 PWM channel 62
		P00.9:ALT(7)	
		P20.10:ALT(7)	
		P33.9:ALT(7)	
CCU61:CC60INA	from	P00.1:IN	T12 capture input 60
CCU61:CC61INA	from	P00.3:IN	T12 capture input 61
CCU61:CC62INA	from	P00.5:IN	T12 capture input 62
CCU61:CC60INB	from	P02.0:IN	T12 capture input 60
CCU61:CC61INB	from	P02.2:IN	T12 capture input 61
CCU61:CC62INB	from	P02.4:IN	T12 capture input 62
CCU61:CC60INC	from	P00.7:IN	T12 capture input 60
CCU61:CC61INC	from	P00.8:IN	T12 capture input 61
CCU61:CC62INC	from	P00.9:IN	T12 capture input 62
CCU61:CC60IND	from	PMS:pms_wut_underflow	T12 capture input 60
CCU61:CC61IND	from	CAN0:INT(12)	T12 capture input 61
CCU61:CC62IND	from	SCU:E_PDOUT(5)	T12 capture input 62
CCU61:CCPOS0A	from	P00.7:IN	Hall capture input 0
CCU61:CCPOS1A	from	P00.8:IN	Hall capture input 1
CCU61:CCPOS2A	from	P00.9:IN	Hall capture input 2
CCU61:CCPOS0B	from	CCU60:SR(2)	Hall capture input 0
CCU61:CCPOS0C	from	P33.7:IN	Hall capture input 0
CCU61:CCPOS1C	from	P33.6:IN	Hall capture input 1
CCU61:CCPOS2C	from	P33.5:IN	Hall capture input 2
CCU61:COUT60	to	SCU:E_REQ1(1)	T12 PWM channel 60
		P00.2:ALT(7)	
		P20.11:ALT(7)	
		P33.12:ALT(7)	

Table 225 Connections of CCU61 (cont'd)

Interface Signals	connects		Description
CCU61:COUT61	to	P00.4:ALT(7)	T12 PWM channel 61
		P20.12:ALT(7)	
		P33.10:ALT(7)	
CCU61:COUT62	to	P00.6:ALT(7)	T12 PWM channel 62
		P20.13:ALT(7)	
		P33.8:ALT(7)	
CCU61:COUT63	to	HSPDM:HWRUN(0)	T13 PWM channel 63
		P00.12:ALT(7)	
		P20.7:ALT(7)	
CCU61:CTRAPA	from	P00.0:IN	Trap input capture
CCU61:CTRAPB	from	CCU61:WHE_N	Trap input capture
CCU61:CTRAPC	from	P33.4:IN	Trap input capture
CCU61:CTRAPD	from	SCU:E_PDOUT(1)	Trap input capture
CCU61:SR(0)	to	HSM:EXT_INT(11)	Service request
CCU61:SR(1)	to	CCU61:T13HRH	Service request
CCU61:SR(2)	to	CCU60:CCPOS0B	Service request
		CCU60:T12HRG	
		CCU60:T13HRG	
CCU61:SR(3)	to	EVADC:G0REQTRB	Service request
		EVADC:G1REQTRB	
		EVADC:G2REQTRB	
		EVADC:G3REQTRB	
		EVADC:G4REQTRB	
		EVADC:G5REQTRB	
CCU61:T12HRA	from	SCU:scu_cctrig0	External timer start 12
CCU61:T13HRA	from	SCU:scu_cctrig0	External timer start 13
CCU61:T12HRB	from	P02.6:IN	External timer start 12
CCU61:T13HRB	from	P02.7:IN	External timer start 13
CCU61:T12HRC	from	P02.8:IN	External timer start 12
CCU61:T13HRC	from	P02.8:IN	External timer start 13
CCU61:T13HRE	from	CAN0:INT(15)	External timer start 13
CCU61:T12HRF	from	GPT120:T6OFL	External timer start 12
CCU61:T13HRF	from	GPT120:T6OFL	External timer start 13
CCU61:T12HRG	from	CCU60:SR(2)	External timer start 12
CCU61:T13HRG	from	CCU60:SR(2)	External timer start 13
CCU61:T12HRH	from	SCU:E_PDOUT(1)	External timer start 12
CCU61:T13HRH	from	CCU61:SR(1)	External timer start 13
CCU61:WHE_N	to	CCU61:CTRAPB	Set wrong hall event negative

27.4 Revision History

Table 226 Revision History

Reference	Change to Previous Version	Comment
V3.0.0		
	Initial release.	

28 General Purpose Timer Unit (GPT12)

This chapter describes the specific properties of the product TC33xEXT,
which is a member of the product family TC3XX.

The functionality of the GPT12 is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

28.1 TC33xEXT Specific Register Set

Table 227 Register Address Space - GPT12

Module	Base Address	End Address	Note
GPT120	$F0001800_H$	$F00018FF_H$	FPI slave interface

Register Overview Table

See corresponding AURIX™ TC3xx Platform family specification.

28.2 TC33xEXT Specific Registers

No deviations from the Family Spec

28.3 Connectivity

Table 228 Connections of GPT120

Interface Signals	connects		Description
GPT120:CAPINB	from	SCU:E_PDOUT(6)	Trigger input to capture value of timer T5 into CAPREL register
GPT120:T2EUDA	from	P00.8:IN	Count direction control input of timer T2
GPT120:T3EUDA	from	P02.7:IN	Count direction control input of core timer T3
GPT120:T4EUDA	from	P00.9:IN	Count direction control input of timer T4
GPT120:T5EUDA	from	P21.6:IN	Count direction control input of timer T5
GPT120:T6EUDA	from	P20.0:IN	Count direction control input of core timer T6
GPT120:T2EUDB	from	P33.6:IN	Count direction control input of timer T2
GPT120:T3EUDB	from	P10.7:IN	Count direction control input of core timer T3
GPT120:T4EUDB	from	P33.5:IN	Count direction control input of timer T4
GPT120:T5EUDB	from	P10.1:IN	Count direction control input of timer T5
GPT120:T6EUDB	from	P10.0:IN	Count direction control input of core timer T6
GPT120:T2INA	from	P00.7:IN	Trigger/gate input of timer T2
GPT120:T3INA	from	P02.6:IN	Trigger/gate input of core timer T3
GPT120:T4INA	from	P02.8:IN	Trigger/gate input of timer T4
GPT120:T5INA	from	P21.7:IN	Trigger/gate input of timer T5
GPT120:T6INA	from	P20.3:IN	Trigger/gate input of core timer T6
GPT120:T2INB	from	P33.7:IN	Trigger/gate input of timer T2
GPT120:T3INB	from	P10.4:IN	Trigger/gate input of core timer T3
GPT120:T4INB	from	P10.8:IN	Trigger/gate input of timer T4
GPT120:T5INB	from	P10.3:IN	Trigger/gate input of timer T5
GPT120:T6INB	from	P10.2:IN	Trigger/gate input of core timer T6
GPT120:T3INC	from	SCU:E_PDOUT(4)	Trigger/gate input of core timer T3
GPT120:T6OFL	to	CCU60:T12HRF	Overflow/underflow signal of timer T6
		CCU60:T13HRF	
		CCU61:T12HRF	
		CCU61:T13HRF	
GPT120:T3OUT	to	SCU:E_REQ4(2)	External output for overflow/underflow detection of core timer T3
		P10.6:ALT(4)	
		P21.6:ALT(7)	
GPT120:T6OUT	to	SCU:E_REQ5(2)	External output for overflow/underflow detection of core timer T6
		P10.5:ALT(5)	
		P21.7:ALT(7)	
GPT120:CIRQ_INT	to	INT:gpt120.CIRQ_INT	GPT120 CAPREL Service Request
GPT120:T2_INT	to	INT:gpt120.T2_INT	GPT120 T2 Overflow/Underflow Service Request

Table 228 Connections of GPT120 (cont'd)

Interface Signals	connects		Description
GPT120:T3_INT	to	INT:gpt120.T3_INT	GPT120 T3 Overflow/Underflow Service Request
GPT120:T4_INT	to	INT:gpt120.T4_INT	GPT120 T4 Overflow/Underflow Service Request
GPT120:T5_INT	to	INT:gpt120.T5_INT	GPT120 T5 Overflow/Underflow Service Request
GPT120:T6_INT	to	INT:gpt120.T6_INT	GPT120 T6 Overflow/Underflow Service Request

28.4 Revision History

Table 229 Revision History

Reference	Change to Previous Version	Comment
V3.0.0		
–	Initial version.	
V3.0.1		
Page 2	Signal GPT120:CAPINA removed from connections table.	
V3.0.2		
	Changes in Connection table and Revision History due to splitting of formerly identical content into separate appendices with different content for TC33xED and TC33xPD.	

29 Converter Control Block (CONVCTRL)

This chapter describes the specific properties of the product TC33xEXT,
which is a member of the product family TC3xx.

The functionality of the CONVCTRL is described in the TC3xx family documentation. The complete product description consists of the family documentation and this product-specific appendix.

29.1 TC33xEXT-Specific IP Configuration

The functional description describes the features and operating modes of the converter control block in a general way. This section summarizes the configuration that is available in a specific product.

Table 230 TC33xEXT specific configuration of CONVERTER

Parameter	CONVCTRL
FPI base address	$F0025000_H$
FPI address range	100_H
Application Reset and Kernel Reset	Application Reset
Name of the config sector value	CFS Value
CFS value for register VRCFG	$000000C3_H$

29.2 TC33xEXT Specific Register Set

Table 231 Register Address Space - CONVERTER

Module	Base Address	End Address	Note
CONVCTRL	$F0025000_H$	$F00250FF_H$	FPI slave interface

Register Overview Table

See main family chapter.

29.3 TC33xEXT Specific Registers

No deviations from the Family Spec

29.4 Connectivity

The CONVCTRL is connected to its environment through a number of input and output signals.

Table 232 Digital Connections for Product TC33xEXT

Signal	Dir.	Source/Destin.	Description
General			
PHSYNC	O	EVADC	Synchronization signal for analog clocks
CC_ALARM	O	SMU	Alarm signal from safety logic

Table 233 List of CONVERTER Interface Signals

Interface Signals	I/O	Description
PHSYNC	out	**Phase synchronization signal**
CC_ALARM	out	**Safety Alarm Signal**

29.5 Revision History

Table 234 Revision History for the Appendix

Reference	Change to Previous Version	
V3.0.0		
	Initial version for TC33X.	
V3.0.1		
Page 2	EDSADC removed from digital connections table because TC33xEXT has no EDSADC.	

30 Enhanced Versatile Analog-to-Digital Converter (EVADC)

This chapter describes the specific properties of the product TC33xEXT,
which is a member of the product family TC3XX.

The functionality of the EVADC is described in the TC3XX family documentation. The complete product description consists of the family documentation and this product-specific appendix.

30.1 TC33xEXT-Specific IP Configuration

The functional description describes the features and operating modes of the A/D Converters in a general way. This section summarizes the configuration that is available in a specific product.

Each converter group is equipped with a separate analog converter module and a dedicated analog input multiplexer.

Table 235 General Converter Configuration TC33xEXT

Converter Group	Input Channels	Converter Cluster	Common Service Req. Group	Associated Standard Reference Pins
Primary Groups				
G0	CH0 … CH7	Primary	C0	V_{AREF1}, V_{AGND1}
G1	CH0 … CH7	Primary	C1	V_{AREF1}, V_{AGND1}
G2[1)]	CH0 … CH3	Primary	C0	V_{AREF1}, V_{AGND1}
G3[1)]	CH0 … CH3	Primary	C1	V_{AREF1}, V_{AGND1}
G4	CH0 … CH7	Primary	C0	V_{AREF1}, V_{AGND1}
G5	CH0 … CH7	Primary	C1	V_{AREF1}, V_{AGND1}

1) For EVADC G2 and EVADC G3 the bit-fields 4 … 7 of channel event flag register (G2CEFLAG, G3CEFLAG) and channel event flag clear register (G2CEFCLR, G3CEFCLR) can't be used.

Synchronization Groups

Up to 4 converter kernels can be connected to synchronization groups to achieve parallel conversion of several input channels.

Not all channels can be synchronized to each other, but certain groups can be formed.

Table 236 summarizes which kernels can be synchronized for parallel conversions.

Table 236 Synchronization Groups

ADC Kernel	Synchr. Group	Master selected by control input CIx[1)]			
		CI0[2)]	CI1	CI2	CI3
G0 (Prim.)	A	G0	G1	G2	G3
G1 (Prim.)	A	G1	G0	G2	G3
G2 (Prim.)	A	G2	G0	G1	G3
G3 (Prim.)	A	G3	G0	G1	G2
G4 (Prim.)	B	G4	G5	---	---
G5 (Prim.)	B	G5	G4	---	---

1) The control input is selected by bitfield STSEL in register GxSYNCTR.
Select the corresponding ready inputs accordingly by bits EVALRx.

2) Control input CI0 always selects the own control signals of the corresponding ADC kernel. This selection is meant for the synchronization master or for stand-alone operation.

Table 237 TC33xEXT specific configuration of EVADC

Parameter	EVADC
Number of available primary groups	6
Number of available secondary groups	0
Number of available Fast Compare channels	0
FPI base address	$F0020000_H$
FPI address range	4000_H

30.2 TC33xEXT Specific Register Set

Table 238 Register Address Space - EVADC

Module	Base Address	End Address	Note
EVADC	$F0020000_H$	$F0023FFF_H$	FPI slave interface

Register Overview Table

See main family chapter.

30.3 Connectivity

The EVADC is connected to its environment through a number of analog input signals and also digital input and output signals. These connections establish communication with other peripherals, with the system blocks, and with external components. The following tables list:

- **Analog Module Connections**
- **Digital Module Connections**

30.3.1 Analog Module Connections

The EVADC module accepts a number of analog input signals. The analog input multiplexers select the input channels to be converted from the signals available in this product.

Note: If an analog input channel is connected to an I/O port pin, make sure the output driver and/or pull devices and/or the digital input path are disabled during normal operation (Px_PDISC.PDISy = 1). For diagnostic functions (MD, PDD) ports must be configured differently (see family description).

The exact number of analog input channels and the available connection to port pins depend on the employed product type and package (refer to **Table 235** and to the corresponding Data Sheets).

A summary of channels can be found in the table below.

Note: Most analog input pins are also connected either to other channels of the EVADC. These connections are listed in column “Overlay”

Special Markings

- Input channels marked “PDD” provide a pull-down device for pull-down diagnostics.
- Input channels marked “MD” can activate the pullup and pulldown devices for multiplexer diagnostics.
- Input channels marked “AltRef” can be selected as an alternate reference voltage for conversions on channels of the same group.
- Input channels marked “FixRef” cannot select an alternate reference voltage, but only the corresponding standard reference voltage.

Table 239 Analog Input Connections for Product TC33xEXT

Signal	Source	Overlay	Description
Reference Inputs			
V_{AREF}	VAREF1	-	positive analog reference
V_{AGND}	VAGND1	-	negative analog reference
Analog Inputs for Group 0 (Primary)			
G0CH0 (AltRef)	AN0	-	analog input channel 0 of group 0
G0CH1 (MD)	AN1	-	analog input channel 1 of group 0
G0CH2 (MD)	AN2	-	analog input channel 2 of group 0
G0CH3	AN3	-	analog input channel 3 of group 0
G0CH4 (FixRef)	AN4	G5CH0	analog input channel 4 of group 0
G0CH5 (FixRef)	AN5	G5CH1	analog input channel 5 of group 0
G0CH6 (FixRef)	AN6	G5CH2	analog input channel 6 of group 0
G0CH7 (PDD, FixRef)	AN7	G5CH3	analog input channel 7 of group 0

Table 239 Analog Input Connections for Product TC33xEXT (cont'd)

Signal	Source	Overlay	Description
Analog Inputs for Group 1 (Primary)			
G1CH0 (AltRef)	AN8	G5CH4	analog input channel 0 of group 1
G1CH1 (MD)	AN9	G5CH5	analog input channel 1 of group 1
G1CH2 (MD)	AN10	G5CH6	analog input channel 2 of group 1
G1CH3 (PDD)	AN11	G5CH7	analog input channel 3 of group 1
G1CH4	AN12	G4CH0	analog input channel 4 of group 1
G1CH5	AN13	G4CH1	analog input channel 5 of group 1
G1CH6	AN14	G4CH2	analog input channel 6 of group 1
G1CH7	AN15	G4CH3	analog input channel 7 of group 1
Analog Inputs for Group 2 (Primary)			
G2CH0 (AltRef)	AN16	G4CH4	analog input channel 0 of group 2
G2CH1 (MD)	AN17	G4CH5	analog input channel 1 of group 2
G2CH2 (MD)	AN18	G4CH6	analog input channel 2 of group 2
G2CH3 (PDD)	AN19	G4CH7	analog input channel 3 of group 2
G2CH4	-	-	analog input channel 4 of group 2
G2CH5	-	-	analog input channel 5 of group 2
G2CH6	-	-	analog input channel 6 of group 2
G2CH7	-	-	analog input channel 7 of group 2
Analog Inputs for Group 3 (Primary)			
G3CH0 (AltRef)	AN20	-	analog input channel 0 of group 3
G3CH1 (MD)	AN21	-	analog input channel 1 of group 3
G3CH2 (MD)	AN22	-	analog input channel 2 of group 3
G3CH3 (PDD)	AN23	-	analog input channel 3 of group 3
G3CH4	-	-	analog input channel 4 of group 3
G3CH5	-	-	analog input channel 5 of group 3
G3CH6	-	-	analog input channel 6 of group 3
G3CH7	-	-	analog input channel 7 of group 3
Analog Inputs for Group 4 (Primary)			
G4CH0 (AltRef)	AN12	G1CH4	analog input channel 0 of group 4
G4CH1 (MD)	AN13	G1CH5	analog input channel 1 of group 4
G4CH2 (MD)	AN14	G1CH6	analog input channel 2 of group 4
G4CH3 (PDD)	AN15	G1CH7	analog input channel 3 of group 4
G4CH4	AN16	G2CH0	analog input channel 4 of group 4
G4CH5	AN17	G2CH1	analog input channel 5 of group 4
G4CH6	AN18	G2CH2	analog input channel 6 of group 4
G4CH7	AN19	G2CH3	analog input channel 7 of group 4
Analog Inputs for Group 5 (Primary)			
G5CH0 (AltRef)	AN4	G0CH4	analog input channel 0 of group 5

Table 239 Analog Input Connections for Product TC33xEXT (cont'd)

Signal	Source	Overlay	Description
G5CH1 (MD)	AN5	G0CH5	analog input channel 1 of group 5
G5CH2 (MD)	AN6	G0CH6	analog input channel 2 of group 5
G5CH3	AN7	G0CH7	analog input channel 3 of group 5
G5CH4	AN8	G1CH0	analog input channel 4 of group 5
G5CH5	AN9	G1CH1	analog input channel 5 of group 5
G5CH6	AN10	G1CH2	analog input channel 6 of group 5
G5CH7	AN11	G1CH3	analog input channel 7 of group 5
Common Input Signals (x = 0-5)			
GxCH28	$V_{ANACOMM}$	-	common reference signal, available to all converters, used for production testing, can be fed to the converters through pin AN11
GxCH29	V_{MTS}	-	module test signal, comparator supply voltage V_{DDK}
GxCH30	V_{AGND}	-	negative reference voltage
GxCH31	V_{AREF}	-	positive reference voltage

30.3.2 Digital Module Connections

The EVADC module accepts a number of digital input signals and generates a number of output signals. This section summarizes the connection of these signals to other on-chip modules or to external resources via port pins.

Table 240 Digital Connections for Product TC33xEXT

Signal	Dir.	Source/Destin.	Description
Gate Inputs for Primary Groups (x = 0-5, input line selected via bitfield GTSEL = [yyyy$_B$])			
GxREQGTA	I	-	[0000$_B$] Gating input A, group x
GxREQGTB	I	-	[0001$_B$] Gating input B, group x
GxREQGTC	I	CCU6061 TRIG0	[0010$_B$] CCU6061 trigger output 0
GxREQGTD	I	CCU6061 TRIG1	[0011$_B$] CCU6061 trigger output 1
GxREQGTE	I	CCU6061 TRIG2	[0100$_B$] CCU6061 trigger output 2
GxREQGTF	I	-	[0101$_B$] Gating input F, group x
GxREQGTG	I	-	[0110$_B$] Gating input G, group x
GxREQGTH	I	-	[0111$_B$] Gating input H, group x
GxREQGTI	I	-	[1000$_B$] Gating input I, group x
GxREQGTJ	I	-	[1001$_B$] Gating input J, group x
GxREQGTK	I	-	[1010$_B$] Gating input K, group x
GxREQGTL	I	-	[1011$_B$] Gating input L, group x
GxREQGTM	I	eru_pdout_x	[1100$_B$] ERU pattern detection output x
GxREQGTN	I	-	[1101$_B$] Gating input N, group x
GxREQGTO	I	-	[1110$_B$] Gating input O, group x
GxREQGTP	I	[internal]	[1111$_B$] Extend inputs to the selected internal trigger source (see GxTRCTR)
GxREQGTySEL	O	GxREQTRyP[1)]	Selected gating signal of the respective source
Trigger Inputs for Primary Groups (x = 0-5, input line selected via bitfield XTSEL = [yyyy$_B$])			
GxREQTRA	I	CCU60_SR3	[0000$_B$] CCU60 service request output 3
GxREQTRB	I	CCU61_SR3	[0001$_B$] CCU61 service request output 3
GxREQTRC	I	HSPDM_adc_trig	[0010$_B$] HSPDM chirp trigger
GxREQTRD	I	-	[0011$_B$] Trigger input D, group x
GxREQTRE	I	-	[0100$_B$] Trigger input E, group x
GxREQTRF	I	-	[0101$_B$] Trigger input F, group x
GxREQTRG	I	-	[0110$_B$] Trigger input G, group x
GxREQTRH	I	eru_iout_x	[0111$_B$] ERU interrupt output x
GxREQTRI	I	-	[1000$_B$] Trigger input I, group x
GxREQTRJ	I	-	[1001$_B$] Trigger input J, group x
GxREQTRK	I	-	[1010$_B$] Trigger input K, group x
GxREQTRL	I	-	[1011$_B$] Trigger input L, group x
GxREQTRM	I	vadc_gxsr1	[1100$_B$] Service request 1, group x
GxREQTRN	I	vadc_c0sr1	[1101$_B$] Service request 1, common group 0

Table 240 Digital Connections for Product TC33xEXT (cont'd)

Signal	Dir.	Source/Destin.	Description
GxREQTRO	I	vadc_c1sr1	[1110_B] Service request 1, common group 1
GxREQTRyP	I	GxREQGTySEL[1)]	[1111_B] Extend triggers to selected gating input of the respective source
GxREQTRySEL	O	-	Selected trigger signal of the respective source
Global Signals and Service Request Lines For Primary Groups: x = 0-5			
GxDATA[20:0]	O	RIF	Result values written to RES15
GxWR	O	RIF	Write signal for GxDATA
EMUX00	O	P02.6, P33.3	Control of external analog multiplexer interface 0
EMUX01	O	P02.7, P33.2	
EMUX02	O	P02.8, P33.1	
EMUX10	O	P00.6, P33.6	Control of external analog multiplexer interface 1
EMUX11	O	P00.7, P33.5	
EMUX12	O	P00.8, P33.4	
GxSR0	O	ICU	Service request 0 of group x
GxSR1	O	ICU	Service request 1of group x
GxSR2	O	ICU	Service request 2 of group x
GxSR3	O	ICU	Service request 3 of group x
C0SR0	O	ICU	Service request 0 of common block 0
C0SR1	O	ICU	Service request 1 of common block 0
C0SR2	O	ICU	Service request 2 of common block 0
C0SR3	O	ICU	Service request 3 of common block 0
C1SR0	O	ICU	Service request 0 of common block 1
C1SR1	O	ICU	Service request 1 of common block 1
C1SR2	O	ICU	Service request 2 of common block 1
C1SR3	O	ICU	Service request 3 of common block 1
System-Internal Connections (x = 0-5)			
PHSYNC	I	Phase synchronizer	Synchronization signal for analog clocks
otgb0[15:0]	O	OTGM	Alternate trigger buses for additional trace signals indicating the input signal sample phase (see OCS)
otgb1[15:0]	O	OTGM	

1) Internal signal connection.

30.4 Revision History

This is a summary of the modifications that have been applied to this chapter.

Table 241 Revision History

Reference	Change to Previous Version	Comment
V3.0.0		
–	Initial version.	–
V3.0.1		
Page 1	Footnote added to table **General Converter Configuration TC33xEXT** regarding limitation of converter group G2 and G3.	
Page 1	V_{AREF1} / V_{AGND1} corrected to $_{AREF0}$ / V_{AGND0} in table **General Converter Configuration TC33xEXT**.	
Page 3	VAREF2 / VAGND2 corrected to VAREF0 / VAGND0 in table **Analog Input Connections for Product TC33xEXT**.	
V3.0.2		
Page 1	V_{AREF1} / V_{AGND1} fixed in table **General Converter Configuration TC33xEXT**.	
Page 3	VAREF1 / VAGND1 fixed in table **Analog Input Connections for Product TC33xEXT**.	
V3.0.3		
–	No functional changes.	–
V3.0.4		
–	No functional changes.	–
V3.0.5		
–	No functional changes.	–

31 Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

This device doesn’t contain an EDSADC.

32 Inter-Integrated Circuit (I2C)

This device doesn’t contain an I2C.

33 High Speed Serial Link (HSSL)

This device doesn’t contain a HSSL.

34 Asynchronous Serial Interface (ASCLIN)

Text with reference to family spec.

34.1 TC33xEXT Specific IP Configuration

No product specific configuration for ASCLIN

34.2 TC33xEXT Specific Register Set

Register Address Space Table

Table 242 Register Address Space - ASCLIN

Module	Base Address	End Address	Note
ASCLIN0	$F0000600_H$	$F00006FF_H$	FPI slave interface
ASCLIN1	$F0000700_H$	$F00007FF_H$	FPI slave interface
ASCLIN2	$F0000800_H$	$F00008FF_H$	FPI slave interface
ASCLIN3	$F0000900_H$	$F00009FF_H$	FPI slave interface
ASCLIN4	$F0000A00_H$	$F0000AFF_H$	FPI slave interface
ASCLIN5	$F0000B00_H$	$F0000BFF_H$	FPI slave interface

Register Overview Table

Table 243 Register Overview - ASCLIN (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_CLC	Clock Control Register	000_H	See Family Spec
ASCLIN1_CLC	Clock Control Register	000_H	See Family Spec
ASCLIN2_CLC	Clock Control Register	000_H	See Family Spec
ASCLIN3_CLC	Clock Control Register	000_H	See Family Spec
ASCLIN4_CLC	Clock Control Register	000_H	See Family Spec
ASCLIN5_CLC	Clock Control Register	000_H	See Family Spec
ASCLIN0_IOCR	Input and Output Control Register	004_H	See Family Spec
ASCLIN1_IOCR	Input and Output Control Register	004_H	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_IOCR	Input and Output Control Register	004_H	See Family Spec
ASCLIN3_IOCR	Input and Output Control Register	004_H	See Family Spec
ASCLIN4_IOCR	Input and Output Control Register	004_H	See Family Spec
ASCLIN5_IOCR	Input and Output Control Register	004_H	See Family Spec
ASCLIN0_ID	Module Identification Register	008_H	See Family Spec
ASCLIN1_ID	Module Identification Register	008_H	See Family Spec
ASCLIN2_ID	Module Identification Register	008_H	See Family Spec
ASCLIN3_ID	Module Identification Register	008_H	See Family Spec
ASCLIN4_ID	Module Identification Register	008_H	See Family Spec
ASCLIN5_ID	Module Identification Register	008_H	See Family Spec
ASCLIN0_TXFIFOCON	TX FIFO Configuration Register	$00C_H$	See Family Spec
ASCLIN1_TXFIFOCON	TX FIFO Configuration Register	$00C_H$	See Family Spec
ASCLIN2_TXFIFOCON	TX FIFO Configuration Register	$00C_H$	See Family Spec
ASCLIN3_TXFIFOCON	TX FIFO Configuration Register	$00C_H$	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN4_TXFIFOCON	TX FIFO Configuration Register	$00C_H$	See Family Spec
ASCLIN5_TXFIFOCON	TX FIFO Configuration Register	$00C_H$	See Family Spec
ASCLIN0_RXFIFOCON	RX FIFO Configuration Register	010_H	See Family Spec
ASCLIN1_RXFIFOCON	RX FIFO Configuration Register	010_H	See Family Spec
ASCLIN2_RXFIFOCON	RX FIFO Configuration Register	010_H	See Family Spec
ASCLIN3_RXFIFOCON	RX FIFO Configuration Register	010_H	See Family Spec
ASCLIN4_RXFIFOCON	RX FIFO Configuration Register	010_H	See Family Spec
ASCLIN5_RXFIFOCON	RX FIFO Configuration Register	010_H	See Family Spec
ASCLIN0_BITCON	Bit Configuration Register	014_H	See Family Spec
ASCLIN1_BITCON	Bit Configuration Register	014_H	See Family Spec
ASCLIN2_BITCON	Bit Configuration Register	014_H	See Family Spec
ASCLIN3_BITCON	Bit Configuration Register	014_H	See Family Spec
ASCLIN4_BITCON	Bit Configuration Register	014_H	See Family Spec
ASCLIN5_BITCON	Bit Configuration Register	014_H	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_FRAMECON	Frame Control Register	018_H	See Family Spec
ASCLIN1_FRAMECON	Frame Control Register	018_H	See Family Spec
ASCLIN2_FRAMECON	Frame Control Register	018_H	See Family Spec
ASCLIN3_FRAMECON	Frame Control Register	018_H	See Family Spec
ASCLIN4_FRAMECON	Frame Control Register	018_H	See Family Spec
ASCLIN5_FRAMECON	Frame Control Register	018_H	See Family Spec
ASCLIN0_DATCON	Data Configuration Register	$01C_H$	See Family Spec
ASCLIN1_DATCON	Data Configuration Register	$01C_H$	See Family Spec
ASCLIN2_DATCON	Data Configuration Register	$01C_H$	See Family Spec
ASCLIN3_DATCON	Data Configuration Register	$01C_H$	See Family Spec
ASCLIN4_DATCON	Data Configuration Register	$01C_H$	See Family Spec
ASCLIN5_DATCON	Data Configuration Register	$01C_H$	See Family Spec
ASCLIN0_BRG	Baud Rate Generation Register	020_H	See Family Spec
ASCLIN1_BRG	Baud Rate Generation Register	020_H	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_BRG	Baud Rate Generation Register	020_H	See Family Spec
ASCLIN3_BRG	Baud Rate Generation Register	020_H	See Family Spec
ASCLIN4_BRG	Baud Rate Generation Register	020_H	See Family Spec
ASCLIN5_BRG	Baud Rate Generation Register	020_H	See Family Spec
ASCLIN0_BRD	Baud Rate Detection Register	024_H	See Family Spec
ASCLIN1_BRD	Baud Rate Detection Register	024_H	See Family Spec
ASCLIN2_BRD	Baud Rate Detection Register	024_H	See Family Spec
ASCLIN3_BRD	Baud Rate Detection Register	024_H	See Family Spec
ASCLIN4_BRD	Baud Rate Detection Register	024_H	See Family Spec
ASCLIN5_BRD	Baud Rate Detection Register	024_H	See Family Spec
ASCLIN0_LINCON	LIN Control Register	028_H	See Family Spec
ASCLIN1_LINCON	LIN Control Register	028_H	See Family Spec
ASCLIN2_LINCON	LIN Control Register	028_H	See Family Spec
ASCLIN3_LINCON	LIN Control Register	028_H	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN4_LINCON	LIN Control Register	028_H	See Family Spec
ASCLIN5_LINCON	LIN Control Register	028_H	See Family Spec
ASCLIN0_LINBTIMER	LIN Break Timer Register	$02C_H$	See Family Spec
ASCLIN1_LINBTIMER	LIN Break Timer Register	$02C_H$	See Family Spec
ASCLIN2_LINBTIMER	LIN Break Timer Register	$02C_H$	See Family Spec
ASCLIN3_LINBTIMER	LIN Break Timer Register	$02C_H$	See Family Spec
ASCLIN4_LINBTIMER	LIN Break Timer Register	$02C_H$	See Family Spec
ASCLIN5_LINBTIMER	LIN Break Timer Register	$02C_H$	See Family Spec
ASCLIN0_LINHTIMER	LIN Header Timer Register	030_H	See Family Spec
ASCLIN1_LINHTIMER	LIN Header Timer Register	030_H	See Family Spec
ASCLIN2_LINHTIMER	LIN Header Timer Register	030_H	See Family Spec
ASCLIN3_LINHTIMER	LIN Header Timer Register	030_H	See Family Spec
ASCLIN4_LINHTIMER	LIN Header Timer Register	030_H	See Family Spec
ASCLIN5_LINHTIMER	LIN Header Timer Register	030_H	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_FLAGS	Flags Register	034_H	See Family Spec
ASCLIN1_FLAGS	Flags Register	034_H	See Family Spec
ASCLIN2_FLAGS	Flags Register	034_H	See Family Spec
ASCLIN3_FLAGS	Flags Register	034_H	See Family Spec
ASCLIN4_FLAGS	Flags Register	034_H	See Family Spec
ASCLIN5_FLAGS	Flags Register	034_H	See Family Spec
ASCLIN0_FLAGSSET	Flags Set Register	038_H	See Family Spec
ASCLIN1_FLAGSSET	Flags Set Register	038_H	See Family Spec
ASCLIN2_FLAGSSET	Flags Set Register	038_H	See Family Spec
ASCLIN3_FLAGSSET	Flags Set Register	038_H	See Family Spec
ASCLIN4_FLAGSSET	Flags Set Register	038_H	See Family Spec
ASCLIN5_FLAGSSET	Flags Set Register	038_H	See Family Spec
ASCLIN0_FLAGSCLEAR	Flags Clear Register	$03C_H$	See Family Spec
ASCLIN1_FLAGSCLEAR	Flags Clear Register	$03C_H$	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_FLAGSCLEAR	Flags Clear Register	$03C_H$	See Family Spec
ASCLIN3_FLAGSCLEAR	Flags Clear Register	$03C_H$	See Family Spec
ASCLIN4_FLAGSCLEAR	Flags Clear Register	$03C_H$	See Family Spec
ASCLIN5_FLAGSCLEAR	Flags Clear Register	$03C_H$	See Family Spec
ASCLIN0_FLAGSENABLE	Flags Enable Register	040_H	See Family Spec
ASCLIN1_FLAGSENABLE	Flags Enable Register	040_H	See Family Spec
ASCLIN2_FLAGSENABLE	Flags Enable Register	040_H	See Family Spec
ASCLIN3_FLAGSENABLE	Flags Enable Register	040_H	See Family Spec
ASCLIN4_FLAGSENABLE	Flags Enable Register	040_H	See Family Spec
ASCLIN5_FLAGSENABLE	Flags Enable Register	040_H	See Family Spec
ASCLIN0_TXDATA	Transmit Data Register	044_H	See Family Spec
ASCLIN1_TXDATA	Transmit Data Register	044_H	See Family Spec
ASCLIN2_TXDATA	Transmit Data Register	044_H	See Family Spec
ASCLIN3_TXDATA	Transmit Data Register	044_H	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN4_TXDATA	Transmit Data Register	044_H	See Family Spec
ASCLIN5_TXDATA	Transmit Data Register	044_H	See Family Spec
ASCLIN0_RXDATA	Receive Data Register	048_H	See Family Spec
ASCLIN1_RXDATA	Receive Data Register	048_H	See Family Spec
ASCLIN2_RXDATA	Receive Data Register	048_H	See Family Spec
ASCLIN3_RXDATA	Receive Data Register	048_H	See Family Spec
ASCLIN4_RXDATA	Receive Data Register	048_H	See Family Spec
ASCLIN5_RXDATA	Receive Data Register	048_H	See Family Spec
ASCLIN0_CSR	Clock Selection Register	$04C_H$	See Family Spec
ASCLIN1_CSR	Clock Selection Register	$04C_H$	See Family Spec
ASCLIN2_CSR	Clock Selection Register	$04C_H$	See Family Spec
ASCLIN3_CSR	Clock Selection Register	$04C_H$	See Family Spec
ASCLIN4_CSR	Clock Selection Register	$04C_H$	See Family Spec
ASCLIN5_CSR	Clock Selection Register	$04C_H$	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN0_RXDATAD	Receive Data Debug Register	050_H	See Family Spec
ASCLIN1_RXDATAD	Receive Data Debug Register	050_H	See Family Spec
ASCLIN2_RXDATAD	Receive Data Debug Register	050_H	See Family Spec
ASCLIN3_RXDATAD	Receive Data Debug Register	050_H	See Family Spec
ASCLIN4_RXDATAD	Receive Data Debug Register	050_H	See Family Spec
ASCLIN5_RXDATAD	Receive Data Debug Register	050_H	See Family Spec
ASCLIN0_OCS	OCDS Control and Status	$0E8_H$	See Family Spec
ASCLIN1_OCS	OCDS Control and Status	$0E8_H$	See Family Spec
ASCLIN2_OCS	OCDS Control and Status	$0E8_H$	See Family Spec
ASCLIN3_OCS	OCDS Control and Status	$0E8_H$	See Family Spec
ASCLIN4_OCS	OCDS Control and Status	$0E8_H$	See Family Spec
ASCLIN5_OCS	OCDS Control and Status	$0E8_H$	See Family Spec
ASCLIN0_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	See Family Spec
ASCLIN1_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN2_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	See Family Spec
ASCLIN3_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	See Family Spec
ASCLIN4_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	See Family Spec
ASCLIN5_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	See Family Spec
ASCLIN0_KRST1	Kernel Reset Register 1	$0F0_H$	See Family Spec
ASCLIN1_KRST1	Kernel Reset Register 1	$0F0_H$	See Family Spec
ASCLIN2_KRST1	Kernel Reset Register 1	$0F0_H$	See Family Spec
ASCLIN3_KRST1	Kernel Reset Register 1	$0F0_H$	See Family Spec
ASCLIN4_KRST1	Kernel Reset Register 1	$0F0_H$	See Family Spec
ASCLIN5_KRST1	Kernel Reset Register 1	$0F0_H$	See Family Spec
ASCLIN0_KRST0	Kernel Reset Register 0	$0F4_H$	See Family Spec
ASCLIN1_KRST0	Kernel Reset Register 0	$0F4_H$	See Family Spec
ASCLIN2_KRST0	Kernel Reset Register 0	$0F4_H$	See Family Spec
ASCLIN3_KRST0	Kernel Reset Register 0	$0F4_H$	See Family Spec

Table 243 Register Overview - ASCLIN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
ASCLIN4_KRST0	Kernel Reset Register 0	$0F4_H$	See Family Spec
ASCLIN5_KRST0	Kernel Reset Register 0	$0F4_H$	See Family Spec
ASCLIN0_ACCEN1	Access Enable Register 1	$0F8_H$	See Family Spec
ASCLIN1_ACCEN1	Access Enable Register 1	$0F8_H$	See Family Spec
ASCLIN2_ACCEN1	Access Enable Register 1	$0F8_H$	See Family Spec
ASCLIN3_ACCEN1	Access Enable Register 1	$0F8_H$	See Family Spec
ASCLIN4_ACCEN1	Access Enable Register 1	$0F8_H$	See Family Spec
ASCLIN5_ACCEN1	Access Enable Register 1	$0F8_H$	See Family Spec
ASCLIN0_ACCEN0	Access Enable Register 0	$0FC_H$	See Family Spec
ASCLIN1_ACCEN0	Access Enable Register 0	$0FC_H$	See Family Spec
ASCLIN2_ACCEN0	Access Enable Register 0	$0FC_H$	See Family Spec
ASCLIN3_ACCEN0	Access Enable Register 0	$0FC_H$	See Family Spec
ASCLIN4_ACCEN0	Access Enable Register 0	$0FC_H$	See Family Spec
ASCLIN5_ACCEN0	Access Enable Register 0	$0FC_H$	See Family Spec

34.3 TC33xEXT Specific Registers

No deviations from the Family Spec

34.4 Connectivity

Table 244 Connections of ASCLIN0

Interface Signals	connects		Description
ASCLIN0:ACTSA	from	P14.9:IN	Clear to send input
ASCLIN0:ACTSD	from	ASCLIN0:ARTS	Clear to send input
ASCLIN0:ARTS	to	P14.7:ALT(2)	Ready to send output
		ASCLIN0:ACTSD	
ASCLIN0:ARXA	from	P14.1:IN	Receive input
ASCLIN0:ARXB	from	P15.3:IN	Receive input
ASCLIN0:ARXD	from	P33.10:IN	Receive input
ASCLIN0:ASCLK	to	P14.0:ALT(6)	Shift clock output
		P15.2:ALT(6)	
ASCLIN0:ATX	to	P14.0:ALT(2)	Transmit output
		P14.1:ALT(2)	
		P15.2:ALT(2)	
		P15.3:ALT(2)	
		P33.9:ALT(6)	
ASCLIN0:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN0:TX_INT	to	INT:asclin0.TX_INT	ASCLIN Transmit Service Request
ASCLIN0:RX_INT	to	INT:asclin0.RX_INT	ASCLIN Receive Service Request
ASCLIN0:ERR_INT	to	INT:asclin0.ERR_INT	ASCLIN Error Service Request

Table 245 Connections of ASCLIN1

Interface Signals	connects		Description
ASCLIN1:ACTSA	from	P20.7:IN	Clear to send input
ASCLIN1:ACTSB	from	P32.4:IN	Clear to send input
ASCLIN1:ACTSD	from	ASCLIN1:ARTS	Clear to send input
ASCLIN1:ARTS	to	P20.6:ALT(2)	Ready to send output
		P23.1:ALT(2)	
		ASCLIN1:ACTSD	
ASCLIN1:ARXA	from	P15.1:IN	Receive input
ASCLIN1:ARXB	from	P15.5:IN	Receive input
ASCLIN1:ARXC	from	P20.9:IN	Receive input
ASCLIN1:ARXD	from	P14.8:IN	Receive input
ASCLIN1:ARXE	from	P11.10:IN	Receive input

Table 245 Connections of ASCLIN1 (cont'd)

Interface Signals	connects		Description
ASCLIN1:ARXF	from	P33.13:IN	Receive input
ASCLIN1:ARXG	from	P02.3:IN	Receive input
ASCLIN1:ASCLK	to	P15.0:ALT(6)	Shift clock output
		P20.10:ALT(6)	
		P33.11:ALT(2)	
		P33.12:ALT(4)	
ASCLIN1:ASLSO	to	P14.3:ALT(4)	Slave select signal output
		P20.8:ALT(2)	
		P33.10:ALT(4)	
ASCLIN1:ATX	to	P02.2:ALT(2)	Transmit output
		P11.12:ALT(2)	
		P14.10:ALT(4)	
		P15.0:ALT(2)	
		P15.1:ALT(2)	
		P15.4:ALT(2)	
		P15.5:ALT(2)	
		P20.10:ALT(2)	
		P33.12:ALT(2)	
		P33.13:ALT(2)	
ASCLIN1:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN1:TX_INT	to	INT:asclin1.TX_INT	ASCLIN Transmit Service Request
ASCLIN1:RX_INT	to	INT:asclin1.RX_INT	ASCLIN Receive Service Request
ASCLIN1:ERR_INT	to	INT:asclin1.ERR_INT	ASCLIN Error Service Request

Table 246 Connections of ASCLIN2

Interface Signals	connects		Description
ASCLIN2:ACTSA	from	P10.7:IN	Clear to send input
ASCLIN2:ACTSB	from	P33.5:IN	Clear to send input
ASCLIN2:ACTSD	from	ASCLIN2:ARTS	Clear to send input
ASCLIN2:ARTS	to	P10.8:ALT(2)	Ready to send output
		P33.4:ALT(2)	
		ASCLIN2:ACTSD	
ASCLIN2:ARXA	from	P14.3:IN	Receive input
ASCLIN2:ARXB	from	P02.1:IN	Receive input
ASCLIN2:ARXD	from	P10.6:IN	Receive input
ASCLIN2:ARXE	from	P33.8:IN	Receive input
ASCLIN2:ARXG	from	P02.0:IN	Receive input

Table 246 Connections of ASCLIN2 (cont'd)

Interface Signals	connects		Description
ASCLIN2:ASCLK	to	P02.4:ALT(2)	Shift clock output
		P10.6:ALT(2)	
		P14.2:ALT(6)	
		P33.7:ALT(2)	
		P33.9:ALT(4)	
ASCLIN2:ASLSO	to	P02.3:ALT(2)	Slave select signal output
		P10.5:ALT(6)	
		P33.6:ALT(2)	
ASCLIN2:ATX	to	P02.0:ALT(2)	Transmit output
		P10.5:ALT(2)	
		P14.2:ALT(2)	
		P14.3:ALT(2)	
		P33.8:ALT(2)	
		P33.9:ALT(2)	
ASCLIN2:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN2:TX_INT	to	INT:asclin2.TX_INT	ASCLIN Transmit Service Request
ASCLIN2:RX_INT	to	INT:asclin2.RX_INT	ASCLIN Receive Service Request
ASCLIN2:ERR_INT	to	INT:asclin2.ERR_INT	ASCLIN Error Service Request

Table 247 Connections of ASCLIN3

Interface Signals	connects		Description
ASCLIN3:ACTSA	from	P00.12:IN	Clear to send input
ASCLIN3:ACTSD	from	ASCLIN3:ARTS	Clear to send input
ASCLIN3:ARTS	to	P00.9:ALT(3)	Ready to send output
		ASCLIN3:ACTSD	
ASCLIN3:ARXA	from	P15.7:IN	Receive input
ASCLIN3:ARXB	from	P11.0:IN	Receive input
ASCLIN3:ARXC	from	P20.3:IN	Receive input
ASCLIN3:ARXE	from	P00.1:IN	Receive input
ASCLIN3:ARXF	from	P21.6:IN	Receive input

Table 247 Connections of ASCLIN3 (cont'd)

Interface Signals	connects		Description
ASCLIN3:ASCLK	to	P00.0:ALT(2)	Shift clock output
		P00.2:ALT(2)	
		P11.1:ALT(2)	
		P11.4:ALT(2)	
		P15.6:ALT(6)	
		P15.8:ALT(6)	
		P20.0:ALT(3)	
		P21.5:ALT(2)	
		P21.7:ALT(3)	
		P33.2:ALT(2)	
ASCLIN3:ASLSO	to	P00.3:ALT(2)	Slave select signal output
		P12.1:ALT(2)	
		P14.3:ALT(5)	
		P21.2:ALT(2)	
		P21.6:ALT(2)	
		P33.1:ALT(2)	
ASCLIN3:ATX	to	P00.0:ALT(3)	Transmit output
		P00.1:ALT(2)	
		P11.0:ALT(2)	
		P11.1:ALT(3)	
		P15.6:ALT(2)	
		P15.7:ALT(2)	
		P20.0:ALT(2)	
		P20.3:ALT(2)	
		P21.7:ALT(2)	
ASCLIN3:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN3:TX_INT	to	INT:asclin3.TX_INT	ASCLIN Transmit Service Request
ASCLIN3:RX_INT	to	INT:asclin3.RX_INT	ASCLIN Receive Service Request
ASCLIN3:ERR_INT	to	INT:asclin3.ERR_INT	ASCLIN Error Service Request

Table 248 Connections of ASCLIN4

Interface Signals	connects		Description
ASCLIN4:ACTSD	from	ASCLIN4:ARTS	Clear to send input
ASCLIN4:ARTS	to	ASCLIN4:ACTSD	Ready to send output
ASCLIN4:ARXA	from	P00.12:IN	Receive input
ASCLIN4:ARXB	from	P34.2:IN	Receive input
ASCLIN4:ASCLK	to	P34.3:ALT(2)	Shift clock output
ASCLIN4:ASLSO	to	P22.4:ALT(2)	Slave select signal output

Table 248 Connections of ASCLIN4 (cont'd)

Interface Signals	connects		Description
ASCLIN4:ATX	to	P00.9:ALT(5)	Transmit output
		P22.5:ALT(2)	
		P34.1:ALT(2)	
ASCLIN4:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN4:TX_INT	to	INT:asclin4.TX_INT	ASCLIN Transmit Service Request
ASCLIN4:RX_INT	to	INT:asclin4.RX_INT	ASCLIN Receive Service Request
ASCLIN4:ERR_INT	to	INT:asclin4.ERR_INT	ASCLIN Error Service Request

Table 249 Connections of ASCLIN5

Interface Signals	connects		Description
ASCLIN5:ACTSD	from	ASCLIN5:ARTS	Clear to send input
ASCLIN5:ARTS	to	ASCLIN5:ACTSD	Ready to send output
ASCLIN5:ARXA	from	P00.6:IN	Receive input
ASCLIN5:ARXB	from	P33.4:IN	Receive input
ASCLIN5:ARXC	from	P22.3:IN	Receive input
ASCLIN5:ASCLK	to	P33.3:ALT(2)	Shift clock output
ASCLIN5:ASLSO	to	P14.8:ALT(2)	Slave select signal output
		P33.5:ALT(7)	
ASCLIN5:ATX	to	P00.7:ALT(2)	Transmit output
		P22.2:ALT(2)	
		P33.0:ALT(2)	
ASCLIN5:sleep_n	from	SCU:scu_syst_sleep_n	Negative turn-off request
ASCLIN5:TX_INT	to	INT:asclin5.TX_INT	ASCLIN Transmit Service Request
ASCLIN5:RX_INT	to	INT:asclin5.RX_INT	ASCLIN Receive Service Request
ASCLIN5:ERR_INT	to	INT:asclin5.ERR_INT	ASCLIN Error Service Request

34.5 Revision History

Table 250 Revision History

Reference	Change to Previous Version	Comment
V3.2.6		
–	Initial version for TC33x.	
V3.2.7		
–	No functional changes.	
V3.2.8		
–	No functional changes.	

35 Queued Synchronous Peripheral Interface (QSPI)

35.1 TC33xEXT Specific IP Configuration

Table 251 TC33xEXT specific configuration of QSPI

Parameter	QSPI0	QSPI1	QSPI2	QSPI3
QSPI module has HSIC			x	x

35.2 TC33xEXTSpecific Register Set

Register Address Space Table

Table 252 Register Address Space - QSPI

Module	Base Address	End Address	Note
QSPI0	$F0001C00_H$	$F0001CFF_H$	Register block QSPI0
QSPI1	$F0001D00_H$	$F0001DFF_H$	Register block QSPI1
QSPI2	$F0001E00_H$	$F0001EFF_H$	Register block QSPI2
QSPI3	$F0001F00_H$	$F0001FFF_H$	Register block QSPI3

Register Overview Tables of QSPI

Table 253 Register Overview - QSPI0 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI0_CLC	Clock Control Register	000_H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_PISEL	Port Input Select Register	004_H	U,SV	SV,P	Application Reset	10
QSPI0_ID	Module Identification Register	008_H	U,SV	BE	Application Reset	See Family Spec
QSPI0_GLOBALCON	Global Configuration Register	010_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_GLOBALCON1	Global Configuration Register 1	014_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_BACON	Basic Configuration Register	018_H	U,SV	BE	Application Reset	See Family Spec
QSPI0_ECONz (z=0-7)	Configuration Extension z	020_H+z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_STATUS	Status Register	040_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_STATUS1	Status Register 1	044_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 253 Register Overview - QSPI0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI0_SSOC	Slave Select Output Control Register	048_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI0_FLAGSCLEAR	Flags Clear Register	054_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_XXLCON	Extra Large Data Configuration Register	058_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_MIXENTRY	MIX_ENTRY Register	$05C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_BACONENTRY	BACON_ENTRY Register	060_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_DATAENTRYx (x=0-7)	DATA_ENTRY Register x	064_H+x* 4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_RXEXIT	RX_EXIT Register	090_H	U,SV	BE	Application Reset	See Family Spec
QSPI0_RXEXITD	RX_EXIT Debug Register	094_H	U,SV	BE	Application Reset	See Family Spec
QSPI0_MC	Move Counter Register	$0A4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_MCCON	Move Counter control Register	$0A8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI0_OCS	OCDS Control and Status	$0E8_H$	U,SV	SV,P	Debug Reset	See Family Spec
QSPI0_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_KRST1	Kernel Reset Register 1	$0F0_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI0_KRST0	Kernel Reset Register 0	$0F4_H$	U,SV	SV,E,P	Application Reset	See Family Spec

Table 253 Register Overview - QSPI0 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI0_ACCEN1	Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	See Family Spec
QSPI0_ACCEN0	Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

Table 254 Register Overview - QSPI1 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI1_CLC	Clock Control Register	000_H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_PISEL	Port Input Select Register	004_H	U,SV	SV,P	Application Reset	11
QSPI1_ID	Module Identification Register	008_H	U,SV	BE	Application Reset	See Family Spec
QSPI1_GLOBALCON	Global Configuration Register	010_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_GLOBALCON1	Global Configuration Register 1	014_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_BACON	Basic Configuration Register	018_H	U,SV	BE	Application Reset	See Family Spec
QSPI1_ECONz (z=0-7)	Configuration Extension z	020_H+z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_STATUS	Status Register	040_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_STATUS1	Status Register 1	044_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_SSOC	Slave Select Output Control Register	048_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI1_FLAGSCLEAR	Flags Clear Register	054_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 254 Register Overview - QSPI1 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI1_XXLCON	Extra Large Data Configuration Register	058_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_MIXENTRY	MIX_ENTRY Register	$05C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_BACONENTRY	BACON_ENTRY Register	060_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_DATAENTRYx (x=0-7)	DATA_ENTRY Register x	064_H+x* 4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_RXEXIT	RX_EXIT Register	090_H	U,SV	BE	Application Reset	See Family Spec
QSPI1_RXEXITD	RX_EXIT Debug Register	094_H	U,SV	BE	Application Reset	See Family Spec
QSPI1_MC	Move Counter Register	$0A4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_MCCON	Move Counter control Register	$0A8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI1_OCS	OCDS Control and Status	$0E8_H$	U,SV	SV,P	Debug Reset	See Family Spec
QSPI1_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_KRST1	Kernel Reset Register 1	$0F0_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_KRST0	Kernel Reset Register 0	$0F4_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI1_ACCEN1	Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	See Family Spec
QSPI1_ACCEN0	Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

Table 255 Register Overview - QSPI2 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI2_CLC	Clock Control Register	000_H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_PISEL	Port Input Select Register	004_H	U,SV	SV,P	Application Reset	12
QSPI2_ID	Module Identification Register	008_H	U,SV	BE	Application Reset	See Family Spec
QSPI2_GLOBALCON	Global Configuration Register	010_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_GLOBALCON1	Global Configuration Register 1	014_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_BACON	Basic Configuration Register	018_H	U,SV	BE	Application Reset	See Family Spec
QSPI2_ECONz (z=0-7)	Configuration Extension z	020_H+z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_STATUS	Status Register	040_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_STATUS1	Status Register 1	044_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_SSOC	Slave Select Output Control Register	048_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI2_FLAGSCLEAR	Flags Clear Register	054_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_XXLCON	Extra Large Data Configuration Register	058_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_MIXENTRY	MIX_ENTRY Register	$05C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_BACONENTRY	BACON_ENTRY Register	060_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 255 Register Overview - QSPI2 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI2_DATAENTRYx (x=0-7)	DATA_ENTRY Register x	064_H+x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_RXEXIT	RX_EXIT Register	090_H	U,SV	BE	Application Reset	See Family Spec
QSPI2_RXEXITD	RX_EXIT Debug Register	094_H	U,SV	BE	Application Reset	See Family Spec
QSPI2_CAPCON	Capture Control Register	$0A0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_MC	Move Counter Register	$0A4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_MCCON	Move Counter control Register	$0A8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI2_OCS	OCDS Control and Status	$0E8_H$	U,SV	SV,P	Debug Reset	See Family Spec
QSPI2_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_KRST1	Kernel Reset Register 1	$0F0_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_KRST0	Kernel Reset Register 0	$0F4_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI2_ACCEN1	Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	See Family Spec
QSPI2_ACCEN0	Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

Table 256 Register Overview - QSPI3 (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI3_CLC	Clock Control Register	000_H	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_PISEL	Port Input Select Register	004_H	U,SV	SV,P	Application Reset	13
QSPI3_ID	Module Identification Register	008_H	U,SV	BE	Application Reset	See Family Spec
QSPI3_GLOBALCON	Global Configuration Register	010_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_GLOBALCON1	Global Configuration Register 1	014_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_BACON	Basic Configuration Register	018_H	U,SV	BE	Application Reset	See Family Spec
QSPI3_ECONz (z=0-7)	Configuration Extension z	020_H+z*4	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_STATUS	Status Register	040_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_STATUS1	Status Register 1	044_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_SSOC	Slave Select Output Control Register	048_H	U,SV	SV,P	Application Reset	See Family Spec
QSPI3_FLAGSCLEAR	Flags Clear Register	054_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_XXLCON	Extra Large Data Configuration Register	058_H	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_MIXENTRY	MIX_ENTRY Register	$05C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_BACONENTRY	BACON_ENTRY Register	060_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 256 Register Overview - QSPI3 (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
QSPI3_DATAENTRYx (x=0-7)	DATA_ENTRY Register x	064_H+x*4	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_RXEXIT	RX_EXIT Register	090_H	U,SV	BE	Application Reset	See Family Spec
QSPI3_RXEXITD	RX_EXIT Debug Register	094_H	U,SV	BE	Application Reset	See Family Spec
QSPI3_CAPCON	Capture Control Register	$0A0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_MC	Move Counter Register	$0A4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_MCCON	Move Counter control Register	$0A8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
QSPI3_OCS	OCDS Control and Status	$0E8_H$	U,SV	SV,P	Debug Reset	See Family Spec
QSPI3_KRSTCLR	Kernel Reset Status Clear Register	$0EC_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_KRST1	Kernel Reset Register 1	$0F0_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_KRST0	Kernel Reset Register 0	$0F4_H$	U,SV	SV,E,P	Application Reset	See Family Spec
QSPI3_ACCEN1	Access Enable Register 1	$0F8_H$	U,SV	SV,SE	Application Reset	See Family Spec
QSPI3_ACCEN0	Access Enable Register 0	$0FC_H$	U,SV	SV,SE	Application Reset	See Family Spec

35.3 TC33xEXT Specific Registers

35.3.1 Register block QSPI

Port Input Select Register

The PISEL register controls the input signal selection of the SSC module.

QSPI0_PISEL

Port Input Select Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SLSIS			0	SCIS			0	SRIS			0	MRIS		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
MRIS	2:0	rw	**Master Mode Receive Input Select** MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P20.12_IN**,
SRIS	6:4	rw	**Slave Mode Receive Input Select** SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P20.14_IN**, 010_B **P22.5_IN**,
SCIS	10:8	rw	**Slave Mode Clock Input Select** SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P20.11_IN**,

Field	Bits	Type	Description
SLSIS	14:12	rw	**Slave Mode Slave Select Input Selection** The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) 000_B no input 001_B **P20.13_IN**, 010_B **P20.9_IN**,
0	3, 7, 11, 31:15	r	**Reserved** Read as 0; should be written with 0.

QSPI1_PISEL

Port Input Select Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**SLSIS**			**0**	**SCIS**			**0**	**SRIS**			**0**	**MRIS**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
MRIS	2:0	rw	**Master Mode Receive Input Select** MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P10.1_IN**, 001_B **P11.3_IN**,
SRIS	6:4	rw	**Slave Mode Receive Input Select** SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P10.3_IN**, 001_B **P11.9_IN**, 010_B **P10.4_IN**,

Field	Bits	Type	Description
SCIS	10:8	rw	**Slave Mode Clock Input Select** SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P10.2_IN**, 001_B **P11.6_IN**,
SLSIS	14:12	rw	**Slave Mode Slave Select Input Selection** The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) 000_B no input 001_B **P11.10_IN**,
0	3, 7, 11, 31:15	r	**Reserved** Read as 0; should be written with 0.

QSPI2_PISEL

Port Input Select Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**SLSIS**			**0**	**SCIS**			**0**	**SRIS**			**0**	**MRIS**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
MRIS	2:0	rw	**Master Mode Receive Input Select** MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P15.4_IN**, 001_B **P15.7_IN**, 100_B **P15.2_IN**,

Field	Bits	Type	Description
SRIS	6:4	rw	**Slave Mode Receive Input Select** SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P15.5_IN**, 001_B **P15.6_IN**,
SCIS	10:8	rw	**Slave Mode Clock Input Select** SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P15.3_IN**, 001_B **P15.8_IN**,
SLSIS	14:12	rw	**Slave Mode Slave Select Input Selection** The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) 000_B no input 001_B **P15.2_IN**, 010_B **P15.1_IN**,
0	3, 7, 11, 31:15	r	**Reserved** Read as 0; should be written with 0.

QSPI3_PISEL

Port Input Select Register **(004_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**SLSIS**			**0**	**SCIS**			**0**	**SRIS**			**0**	**MRIS**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
MRIS	2:0	rw	**Master Mode Receive Input Select** MRIS selects one out of eight MRST receive input lines, used in Master Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P02.5_IN**, 001_B **P10.7_IN**,
SRIS	6:4	rw	**Slave Mode Receive Input Select** SRIS selects one out of eight MTSR receive input lines, used in Slave Mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P02.6_IN**, 001_B **P10.6_IN**,
SCIS	10:8	rw	**Slave Mode Clock Input Select** SCIS selects one out of eight module kernel SCLK input lines that is used as clock input line in slave mode. Note that not all inputs are used in every device of the family. Selecting an unused input returns a continuous low value. The following signal sources are available in this product (if supported by the package!) 000_B **P02.7_IN**, 001_B **P10.8_IN**,
SLSIS	14:12	rw	**Slave Mode Slave Select Input Selection** The SLSIS must be programmed properly before the slave mode is set with GLOBALCON.MODE and the module is set to RUN mode. The following signal sources are available in this product (if supported by the package!) 000_B no input 001_B **P02.4_IN**,
0	3, 7, 11, 31:15	r	**Reserved** Read as 0; should be written with 0.

35.4 Connectivity

The tables below list all the connections of QSPI instances.

Table 257 Connections of QSPI0

Interface Signals	connects		Description
QSPI0:MRST	to	P20.12:ALT(3)	Slave SPI data output
QSPI0:MRSTA	from	P20.12:IN	Master SPI data input

Table 257 Connections of QSPI0 (cont'd)

Interface Signals	connects		Description
QSPI0:MTSR	to	P20.12:ALT(4)	Master SPI data output
		P20.14:ALT(3)	
		P22.5:ALT(4)	
QSPI0:MTSRA	from	P20.14:IN	Slave SPI data input
QSPI0:MTSRC	from	P22.5:IN	Slave SPI data input
QSPI0:SCLK	to	P20.11:ALT(3)	Master SPI clock output
		P20.13:ALT(5)	
QSPI0:SCLKA	from	P20.11:IN	Slave SPI clock inputs
QSPI0:SLSIA	from	P20.13:IN	Slave select input
QSPI0:SLSIB	from	P20.9:IN	Slave select input
QSPI0:SLSO(0)	to	P20.8:ALT(3)	Master slave select output
QSPI0:SLSO(1)	to	P20.9:ALT(3)	Master slave select output
QSPI0:SLSO(2)	to	P20.13:ALT(3)	Master slave select output
QSPI0:SLSO(3)	to	P11.10:ALT(3)	Master slave select output
QSPI0:SLSO(4)	to	P11.11:ALT(3)	Master slave select output
QSPI0:SLSO(5)	to	P11.2:ALT(3)	Master slave select output
QSPI0:SLSO(6)	to	P20.10:ALT(3)	Master slave select output
QSPI0:SLSO(7)	to	P33.5:ALT(2)	Master slave select output
QSPI0:SLSO(8)	to	P20.6:ALT(3)	Master slave select output
QSPI0:SLSO(9)	to	P20.3:ALT(3)	Master slave select output
QSPI0:SLSO(12)	to	P22.4:ALT(4)	Master slave select output
QSPI0:SLSO(13)	to	P15.0:ALT(3)	Master slave select output
QSPI0:TX_INT	to	INT:qspi0.TX_INT	QSPI Transmit Service Request
QSPI0:RX_INT	to	INT:qspi0.RX_INT	QSPI Receive Service Request
QSPI0:ERR_INT	to	INT:qspi0.ERR_INT	QSPI Error Service Request
QSPI0:PT_INT	to	INT:qspi0.PT_INT	QSPI Phase Transition Service Request
QSPI0:U_INT	to	INT:qspi0.U_INT	QSPI User Defined Service Request
QSPI0:HC_INT	to	INT:qspi0.HC_INT	QSPI High Speed Capture Service Request

Table 258 Connections of QSPI1

Interface Signals	connects		Description
QSPI1:MRST	to	P10.1:ALT(3)	Slave SPI data output
		P10.6:ALT(6)	
		P11.3:ALT(3)	
QSPI1:MRSTA	from	P10.1:IN	Master SPI data input
QSPI1:MRSTB	from	P11.3:IN	Master SPI data input

Table 258 Connections of QSPI1 (cont'd)

Interface Signals	connects		Description
QSPI1:MTSR	to	P10.1:ALT(2)	Master SPI data output
		P10.3:ALT(3)	
		P10.4:ALT(4)	
		P11.9:ALT(3)	
QSPI1:MTSRA	from	P10.3:IN	Slave SPI data input
QSPI1:MTSRB	from	P11.9:IN	Slave SPI data input
QSPI1:MTSRC	from	P10.4:IN	Slave SPI data input
QSPI1:SCLK	to	P10.2:ALT(3)	Master SPI clock output
		P11.6:ALT(3)	
QSPI1:SCLKA	from	P10.2:IN	Slave SPI clock inputs
QSPI1:SCLKB	from	P11.6:IN	Slave SPI clock inputs
QSPI1:SLSIA	from	P11.10:IN	Slave select input
QSPI1:SLSO(0)	to	P20.8:ALT(4)	Master slave select output
QSPI1:SLSO(1)	to	P20.9:ALT(4)	Master slave select output
QSPI1:SLSO(2)	to	P20.13:ALT(4)	Master slave select output
QSPI1:SLSO(3)	to	P11.10:ALT(4)	Master slave select output
QSPI1:SLSO(4)	to	P11.11:ALT(4)	Master slave select output
QSPI1:SLSO(5)	to	P11.2:ALT(4)	Master slave select output
QSPI1:SLSO(6)	to	P33.10:ALT(2)	Master slave select output
QSPI1:SLSO(7)	to	P33.5:ALT(3)	Master slave select output
QSPI1:SLSO(8)	to	P10.4:ALT(3)	Master slave select output
QSPI1:SLSO(9)	to	P10.5:ALT(4)	Master slave select output
QSPI1:SLSO(10)	to	P10.0:ALT(3)	Master slave select output
QSPI1:TX_INT	to	INT:qspi1.TX_INT	QSPI Transmit Service Request
QSPI1:RX_INT	to	INT:qspi1.RX_INT	QSPI Receive Service Request
QSPI1:ERR_INT	to	INT:qspi1.ERR_INT	QSPI Error Service Request
QSPI1:PT_INT	to	INT:qspi1.PT_INT	QSPI Phase Transition Service Request
QSPI1:U_INT	to	INT:qspi1.U_INT	QSPI User Defined Service Request
QSPI1:HC_INT	to	INT:qspi1.HC_INT	QSPI High Speed Capture Service Request

Table 259 Connections of QSPI2

Interface Signals	connects		Description
QSPI2:HSICINA	from	P15.2:IN	Highspeed capture channel
QSPI2:HSICINB	from	P15.3:IN	Highspeed capture channel
QSPI2:MRST	to	P15.4:ALT(3)	Slave SPI data output
		P15.7:ALT(3)	
QSPI2:MRSTA	from	P15.4:IN	Master SPI data input
QSPI2:MRSTB	from	P15.7:IN	Master SPI data input

Table 259 Connections of QSPI2 (cont'd)

Interface Signals	connects		Description
QSPI2:MRSTE	from	P15.2:IN	Master SPI data input
QSPI2:MTSR	to	P15.5:ALT(3)	Master SPI data output
		P15.6:ALT(3)	
QSPI2:MTSRA	from	P15.5:IN	Slave SPI data input
QSPI2:MTSRB	from	P15.6:IN	Slave SPI data input
QSPI2:SCLK	to	P15.3:ALT(3)	Master SPI clock output
		P15.6:ALT(5)	
		P15.8:ALT(3)	
		P33.1:ALT(3)	
QSPI2:SCLKA	from	P15.3:IN	Slave SPI clock inputs
QSPI2:SCLKB	from	P15.8:IN	Slave SPI clock inputs
QSPI2:SLSIA	from	P15.2:IN	Slave select input
QSPI2:SLSIB	from	P15.1:IN	Slave select input
QSPI2:SLSO(0)	to	P15.2:ALT(3)	Master slave select output
QSPI2:SLSO(1)	to	P14.2:ALT(3)	Master slave select output
QSPI2:SLSO(2)	to	P14.6:ALT(3)	Master slave select output
QSPI2:SLSO(3)	to	P14.3:ALT(3)	Master slave select output
QSPI2:SLSO(4)	to	P14.7:ALT(3)	Master slave select output
QSPI2:SLSO(5)	to	P15.1:ALT(3)	Master slave select output
QSPI2:SLSO(6)	to	P33.13:ALT(4)	Master slave select output
QSPI2:SLSO(7)	to	P20.10:ALT(4)	Master slave select output
QSPI2:SLSO(8)	to	P20.6:ALT(4)	Master slave select output
QSPI2:SLSO(9)	to	P20.3:ALT(4)	Master slave select output
QSPI2:SLSO(10)	to	P33.2:ALT(3)	Master slave select output
		P34.3:ALT(4)	
QSPI2:SLSO(11)	to	P33.6:ALT(3)	Master slave select output
QSPI2:SLSO(12)	to	P33.4:ALT(3)	Master slave select output
QSPI2:TX_INT	to	INT:qspi2.TX_INT	QSPI Transmit Service Request
QSPI2:RX_INT	to	INT:qspi2.RX_INT	QSPI Receive Service Request
QSPI2:ERR_INT	to	INT:qspi2.ERR_INT	QSPI Error Service Request
QSPI2:PT_INT	to	INT:qspi2.PT_INT	QSPI Phase Transition Service Request
QSPI2:U_INT	to	INT:qspi2.U_INT	QSPI User Defined Service Request
QSPI2:HC_INT	to	INT:qspi2.HC_INT	QSPI High Speed Capture Service Request

Table 260 Connections of QSPI3

Interface Signals	connects		Description
QSPI3:HSICINA	from	P33.9:IN	Highspeed capture channel
QSPI3:HSICINB	from	P33.10:IN	Highspeed capture channel

Table 260 Connections of QSPI3 (cont'd)

Interface Signals	connects		Description
QSPI3:MRST	to	P02.5:ALT(3)	Slave SPI data output
		P10.7:ALT(3)	
QSPI3:MRSTA	from	P02.5:IN	Master SPI data input
QSPI3:MRSTB	from	P10.7:IN	Master SPI data input
QSPI3:MTSR	to	P02.6:ALT(3)	Master SPI data output
		P10.6:ALT(3)	
QSPI3:MTSRA	from	P02.6:IN	Slave SPI data input
QSPI3:MTSRB	from	P10.6:IN	Slave SPI data input
QSPI3:SCLK	to	P02.7:ALT(3)	Master SPI clock output
		P10.8:ALT(3)	
QSPI3:SCLKA	from	P02.7:IN	Slave SPI clock inputs
QSPI3:SCLKB	from	P10.8:IN	Slave SPI clock inputs
QSPI3:SLSIA	from	P02.4:IN	Slave select input
QSPI3:SLSO(0)	to	P02.4:ALT(3)	Master slave select output
QSPI3:SLSO(1)	to	P02.0:ALT(3)	Master slave select output
QSPI3:SLSO(2)	to	P02.1:ALT(3)	Master slave select output
QSPI3:SLSO(3)	to	P00.5:ALT(3)	Master slave select output
		P02.2:ALT(3)	
QSPI3:SLSO(4)	to	P00.2:ALT(6)	Master slave select output
		P02.3:ALT(3)	
QSPI3:SLSO(5)	to	P02.8:ALT(2)	Master slave select output
QSPI3:SLSO(6)	to	P00.8:ALT(2)	Master slave select output
QSPI3:SLSO(7)	to	P00.9:ALT(2)	Master slave select output
QSPI3:SLSO(8)	to	P10.5:ALT(3)	Master slave select output
QSPI3:TX_INT	to	INT:qspi3.TX_INT	QSPI Transmit Service Request
QSPI3:RX_INT	to	INT:qspi3.RX_INT	QSPI Receive Service Request
QSPI3:ERR_INT	to	INT:qspi3.ERR_INT	QSPI Error Service Request
QSPI3:PT_INT	to	INT:qspi3.PT_INT	QSPI Phase Transition Service Request
QSPI3:U_INT	to	INT:qspi3.U_INT	QSPI User Defined Service Request
QSPI3:HC_INT	to	INT:qspi3.HC_INT	QSPI High Speed Capture Service Request

35.5 Revision History

Table 261 Revision History

Reference	Change to Previous Version	Comment
V3.0.20		
	Initial version TC33x	

36 Micro Second Channel (MSC)

This device doesn’t contain a MSC.

37 Single Edge Nibble Transmission (SENT)

This document describes the SENT Interface specific appendix for the product TC33xEXT.

37.1 TC33xEXT Specific IP Configuration

See features in family spec.

Table 262 TC33xEXT specific configuration of SENT

Parameter	SENT
Number of SENT channels for this device	6

37.2 TC33xEXT Specific Register Set

Register Address Space Table

The address space for the module registers is defined in **Register Address Space Table**.

Table 263 Register Address Space - SENT

Module	Base Address	End Address	Note
SENT	$F0003000_H$	$F0003AFF_H$	FPI slave interface

Register Overview Table

There are no product specific register for this module.

37.3 TC33xEXT Specific Registers

There are no product specific register for this module.

37.4 Connectivity

This section describes the connectivity of the SENT module.

37.4.1 Interrupt and DMA Controller Service Requests

The trigger outputs of the SENT module are connected via the Interrupt router. The request lines are connected as shown in **Connections of SENT**.

37.4.2 Trigger Inputs

The module has 8 Sent Channels and the same number of trigger inputs but not more than n+1 = 16. They can be randomly chosen by programming IOCRx.ETS. The trigger inputs (TRIG[n:0]) of the SENT module are connected to the GTM as shown in **Connections of SENT**.

37.4.3 Connections of SENT

The tables below list all the connections of SENT instances.

Table 264 Connections of SENT

Interface Signals	connects		Description
SENT:SENT0B	from	P00.1:IN	Receive input channel 0
SENT:SENT1B	from	P00.2:IN	Receive input channel 1
SENT:SENT2B	from	P00.3:IN	Receive input channel 2
SENT:SENT3B	from	P00.4:IN	Receive input channel 3
SENT:SENT4B	from	P00.5:IN	Receive input channel 4
SENT:SENT5B	from	P00.6:IN	Receive input channel 5
SENT:SENT0C	from	P02.8:IN	Receive input channel 0
SENT:SENT1C	from	P02.7:IN	Receive input channel 1
SENT:SENT2C	from	P02.6:IN	Receive input channel 2
SENT:SENT3C	from	P02.5:IN	Receive input channel 3

Table 264 Connections of SENT (cont'd)

Interface Signals	connects		Description
SENT:SENT4C	from	P33.6:IN	Receive input channel 4
SENT:SENT5C	from	P33.5:IN	Receive input channel 5
SENT:SPC(0)	to	P00.1:ALT(6)	Transmit output
SENT:SPC(1)	to	P02.7:ALT(6)	Transmit output
SENT:SPC(2)	to	P00.3:ALT(6)	Transmit output
SENT:SPC(3)	to	P00.4:ALT(6)	Transmit output
SENT:SPC(4)	to	P00.5:ALT(6)	Transmit output
SENT:SPC(5)	to	P00.6:ALT(6)	Transmit output
SENT:TRIGO(9:0)	to	INT:sent.TRIGO(9:0)	SENT TRIGO=m Service Request

37.5 Revision History

Table 265 Revision History

Reference	Change to Previous Version	Comment
V2.1.9		
	Initial version for TC33X.	
V2.1.10		
Page 1	Second sentence changed to internal audience only due to customer confusion. No functional change.	
Page 2	Minor notation update in connection table, no functional change.SAE J2716 042016	

38 CAN Interface (MCMCAN)

This section describes the MCMCAN Interface specific appendix for the product TC33xEXT.

38.1 TC33xEXT Specific IP Configuration

Table 266 TC33xEXT specific configuration of CAN

Parameter	CAN0
Node size in byte	1024
Number of CAN Nodes	4
RAM size in byte	32768
Maximum Number of Standard ID Filter Messages per node	128
Maximum Number of Extended ID Filter Messages per node	64
Maximum Number of RxFIFO structures per node	2
Maximum Number of Messages in a Rx buffer per node	64
Maximum Number of Tx Event Messages per node	32
Maximum Number of Tx Messages in a Tx Buffer per node	32

38.2 TC33xEXT Specific Register Set

Register Address Space Table

Table 267 Register Address Space - CAN

Module	Base Address	End Address	Note
CAN0	$F0200000_H$	$F0208FFF_H$	Bus Interface

Register Overview Table

Table 268 Register Overview - CAN (ascending Offset Address)

Short Name	Long Name	Offset Address	Page Number
CAN0_RAM	Embedded SRAM for messages (008000_H Byte)	000000_H	
CAN0_CLC	CAN Clock Control Register	008000_H	See Family Spec
CAN0_ID	Module Identification Register	008008_H	See Family Spec
CAN0_MCR	Module Control Register	008030_H	See Family Spec
CAN0_BUFADR	Buffer receive address and transmit address	008034_H	See Family Spec
CAN0_MECR	Measure Control Register	008040_H	See Family Spec
CAN0_MESTAT	Measure Status Register	008044_H	See Family Spec
CAN0_ACCENCTR0	Access Enable Register Control 0	$0080DC_H$	See Family Spec
CAN0_OCS	OCDS Control and Status	$0080E8_H$	See Family Spec
CAN0_KRSTCLR	Kernel Reset Status Clear Register	$0080EC_H$	See Family Spec

Table 268 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_KRST1	Kernel Reset Register 1	$0080F0_H$	See Family Spec
CAN0_KRST0	Kernel Reset Register 0	$0080F4_H$	See Family Spec
CAN0_ACCEN0	Access Enable Register 0	$0080FC_H$	See Family Spec
CAN0_ACCENNODEi0 (i=0-3)	Access Enable Register CAN Node i 0	008100_H+i*400 H	See Family Spec
CAN0_STARTADRi (i=0-3)	Start Address Node i	008108_H+i*400 H	See Family Spec
CAN0_ENDADRi (i=0-3)	End Address Node i	$00810C_H$+i*40 0_H	See Family Spec
CAN0_ISREGi (i=0-3)	Interrupt Signalling Register i	008110_H+i*400 H	See Family Spec
CAN0_GRINT1i (i=0-3)	Interrupt routing for Groups 1 i	008114_H+i*400 H	See Family Spec
CAN0_GRINT2i (i=0-3)	Interrupt routing for Groups 2 i	008118_H+i*400 H	See Family Spec
CAN0_NTCCRi (i=0-3)	Node i Timer Clock Control Register	008120_H+i*400 H	See Family Spec
CAN0_NTATTRi (i=0-3)	Node i Timer A Transmit Trigger Register	008124_H+i*400 H	See Family Spec
CAN0_NTBTTRi (i=0-3)	Node i Timer B Transmit Trigger Register	008128_H+i*400 H	See Family Spec
CAN0_NTCTTRi (i=0-3)	Node i Timer C Transmit Trigger Register	$00812C_H$+i*40 0_H	See Family Spec
CAN0_NTRTRi (i=0-3)	Node i Timer Receive Timeout Register	008130_H+i*400 H	See Family Spec

Table 268 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_NPCRi (i=0-3)	Node i Port Control Register	008140_H+i*400 H	See Family Spec
CAN0_CRELi (i=0-3)	Core Release Register i	008200_H+i*400 H	See Family Spec
CAN0_ENDNi (i=0-3)	Endian Register i	008204_H+i*400 H	See Family Spec
CAN0_DBTPi (i=0-3)	Data Bit Timing & Prescaler Register i	$00820C_H$+i*40 0_H	See Family Spec
CAN0_TESTi (i=0-3)	Test Register i	008210_H+i*400 H	See Family Spec
CAN0_RWDi (i=0-3)	RAM Watchdog i	008214_H+i*400 H	See Family Spec
CAN0_CCCRi (i=0-3)	CC Control Register i	008218_H+i*400 H	See Family Spec
CAN0_NBTPi (i=0-3)	Nominal Bit Timing & Prescaler Register i	$00821C_H$+i*40 0_H	See Family Spec
CAN0_TSCCi (i=0-3)	Timestamp Counter Configuration i	008220_H+i*400 H	See Family Spec
CAN0_TSCVi (i=0-3)	Timestamp Counter Value i	008224_H+i*400 H	See Family Spec
CAN0_TOCCi (i=0-3)	Timeout Counter Configuration i	008228_H+i*400 H	See Family Spec
CAN0_TOCVi (i=0-3)	Timeout Counter Value i	$00822C_H$+i*40 0_H	See Family Spec
CAN0_ECRi (i=0-3)	Error Counter Register i	008240_H+i*400 H	See Family Spec
CAN0_PSRi (i=0-3)	Protocol Status Register i	008244_H+i*400 H	See Family Spec

Table 268 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_TDCRi (i=0-3)	Transmitter Delay Compensation Register i	008248_H+i*400 H	See Family Spec
CAN0_IRi (i=0-3)	Interrupt Register i	008250_H+i*400 H	See Family Spec
CAN0_IEi (i=0-3)	Interrupt Enable i	008254_H+i*400 H	See Family Spec
CAN0_GFCi (i=0-3)	Global Filter Configuration i	008280_H+i*400 H	See Family Spec
CAN0_SIDFCi (i=0-3)	Standard ID Filter Configuration i	008284_H+i*400 H	See Family Spec
CAN0_XIDFCi (i=0-3)	Extended ID Filter Configuration i	008288_H+i*400 H	See Family Spec
CAN0_XIDAMi (i=0-3)	Extended ID AND Mask i	008290_H+i*400 H	See Family Spec
CAN0_HPMSi (i=0-3)	High Priority Message Status i	008294_H+i*400 H	See Family Spec
CAN0_NDAT1i (i=0-3)	New Data 1 i	008298_H+i*400 H	See Family Spec
CAN0_NDAT2i (i=0-3)	New Data 2 i	$00829C_H$+i*40 0_H	See Family Spec
CAN0_RXF0Ci (i=0-3)	Rx FIFO 0 Configuration i	$0082A0_H$+i*40 0_H	See Family Spec
CAN0_RXF0Si (i=0-3)	Rx FIFO 0 Status i	$0082A4_H$+i*40 0_H	See Family Spec
CAN0_RXF0Ai (i=0-3)	Rx FIFO 0 Acknowledge i	$0082A8_H$+i*40 0_H	See Family Spec
CAN0_RXBCi (i=0-3)	Rx Buffer Configuration i	$0082AC_H$+i*40 0_H	See Family Spec

Table 268 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_RXF1Ci (i=0-3)	Rx FIFO 1 Configuration i	$0082B0_H$+i*40 0_H	See Family Spec
CAN0_RXF1Si (i=0-3)	Rx FIFO 1 Status i	$0082B4_H$+i*40 0_H	See Family Spec
CAN0_RXF1Ai (i=0-3)	Rx FIFO 1 Acknowledge i	$0082B8_H$+i*40 0_H	See Family Spec
CAN0_RXESCi (i=0-3)	Rx Buffer/FIFO Element Size Configuration i	$0082BC_H$+i*40 0_H	See Family Spec
CAN0_TXBCi (i=0-3)	Tx Buffer Configuration i	$0082C0_H$+i*40 0_H	See Family Spec
CAN0_TXFQSi (i=0-3)	Tx FIFO/Queue Status i	$0082C4_H$+i*40 0_H	See Family Spec
CAN0_TXESCi (i=0-3)	Tx Buffer Element Size Configuration i	$0082C8_H$+i*40 0_H	See Family Spec
CAN0_TXBRPi (i=0-3)	Tx Buffer Request Pending i	$0082CC_H$+i*40 0_H	See Family Spec
CAN0_TXBARi (i=0-3)	Tx Buffer Add Request i	$0082D0_H$+i*40 0_H	See Family Spec
CAN0_TXBCRi (i=0-3)	Tx Buffer Cancellation Request i	$0082D4_H$+i*40 0_H	See Family Spec
CAN0_TXBTOi (i=0-3)	Tx Buffer Transmission Occurred i	$0082D8_H$+i*40 0_H	See Family Spec
CAN0_TXBCFi (i=0-3)	Tx Buffer Cancellation Finished i	$0082DC_H$+i*40 0_H	See Family Spec
CAN0_TXBTIEi (i=0-3)	Tx Buffer Transmission Interrupt Enable i	$0082E0_H$+i*40 0_H	See Family Spec
CAN0_TXBCIEi (i=0-3)	Tx Buffer Cancellation Finished Interrupt Enable i	$0082E4_H$+i*40 0_H	See Family Spec

Table 268 Register Overview - CAN (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Page Number
CAN0_TXEFCi (i=0-3)	Tx Event FIFO Configuration i	$0082F0_H$+i*400 H	See Family Spec
CAN0_TXEFSi (i=0-3)	Tx Event FIFO Status i	$0082F4_H$+i*400 H	See Family Spec
CAN0_TXEFAi (i=0-3)	Tx Event FIFO Acknowledge i	$0082F8_H$+i*400 H	See Family Spec

38.3 TC33xEXT Specific Registers

No deviations from the Family Spec

38.4 Connectivity

Table 269 Connections of CAN0

Interface Signals	connects		Description
CAN0:DSTDBG	from	DMU:SCU_ENTERED_DEST_DBG	Destructive Debug entered
CAN0:DXSCLK	to	TCU:dxs_clk	DXS Clock, DAP module clock
CAN0:INT(5:0)	to	HSM:EXT_INT(18:13)	CAN interrupt request
CAN0:INT(12)	to	CCU61:CC61IND	CAN interrupt request
CAN0:INT(15)	to	CCU61:T13HRE	CAN interrupt request
CAN0:STM0_SR0_INT	from	STM0:SR0_INT	System Timer Service Request 0
CAN0:STM0_SR1_INT	from	STM0:SR1_INT	System Timer Service Request 1
CAN0:STM1_SR0_INT	from	STM1:SR0_INT	System Timer Service Request 0
CAN0:STM1_SR1_INT	from	STM1:SR1_INT	System Timer Service Request 1
CAN0:INT(15:0)	to	INT:mcmcan0.INT(15:0)	CAN Service Request

Table 270 Connections of CAN00

Interface Signals	connects		Description
CAN00:RXDA	from	P02.1:IN	CAN receive input node 0
CAN00:RXDB	from	P20.7:IN	CAN receive input node 0
CAN00:RXDC	from	P12.0:IN	CAN receive input node 0
CAN00:RXDD	from	P33.12:IN	CAN receive input node 0
CAN00:RXDE	from	P33.7:IN	CAN receive input node 0
CAN00:RXDG	from	P34.2:IN	CAN receive input node 0

Table 270 Connections of CAN00 (cont'd)

Interface Signals	connects		Description
CAN00:TXD	to	P02.0:ALT(5)	CAN transmit output node 0
		P12.1:ALT(5)	
		P20.8:ALT(5)	
		P33.8:ALT(5)	
		P33.13:ALT(5)	
		P34.1:ALT(4)	

Table 271 Connections of CAN01

Interface Signals	connects		Description
CAN01:RXDA	from	P15.3:IN	CAN receive input node 1
CAN01:RXDB	from	P14.1:IN	CAN receive input node 1
CAN01:RXDD	from	P33.10:IN	CAN receive input node 1
CAN01:RXDE	from	P14.7:IN	CAN receive input node 1
CAN01:TXD	to	P14.0:ALT(5)	CAN transmit output node 1
		P14.9:ALT(4)	
		P15.2:ALT(5)	
		P33.9:ALT(5)	

Table 272 Connections of CAN02

Interface Signals	connects		Description
CAN02:RXDA	from	P15.1:IN	CAN receive input node 2
CAN02:RXDB	from	P02.3:IN	CAN receive input node 2
CAN02:RXDD	from	P14.8:IN	CAN receive input node 2
CAN02:RXDE	from	P10.2:IN	CAN receive input node 2
CAN02:RXDF	from	P14.7:IN	CAN receive input node 2
CAN02:TXD	to	P02.2:ALT(5)	CAN transmit output node 2
		P10.3:ALT(6)	
		P14.10:ALT(5)	
		P15.0:ALT(5)	

Table 273 Connections of CAN03

Interface Signals	connects		Description
CAN03:RXDA	from	P00.3:IN	CAN receive input node 3
CAN03:RXDC	from	P20.0:IN	CAN receive input node 3
CAN03:RXDD	from	P11.10:IN	CAN receive input node 3
CAN03:RXDE	from	P20.9:IN	CAN receive input node 3

Table 273 Connections of CAN03 (cont'd)

Interface Signals	connects		Description
CAN03:TXD	to	P00.2:ALT(5)	CAN transmit output node 3
		P11.12:ALT(5)	
		P20.3:ALT(5)	
		P20.10:ALT(5)	

Note: For the connectivity of the MCMCAN module to the STM module, please refer to the User Manual, chapter MCMCAN User Interface under CAN Transmit Trigger Inputs section.

38.5 Revision History

Table 274 Revision History

Reference	Change to Previous Version	Comment
V1.19.8		
-	First revision of MCMCAN Appendix for TC33xEXT devices.	
V1.19.9		
-	No changes.	
V1.19.10		
Page 7	Added connections CAN01:RXDE from P14.7 and CAN01:TXD to P14.9.	
Page 9	Added note at the end of connections tables.	
V1.19.11		
–	No functional changes.	
V1.19.12		
Page 1	Update of “specific configuration of CAN” table.	
V1.19.13		
–	No functional changes.	

39 FlexRay™ Protocol Controller (E-Ray)

This device doesn’t contain a FlexRay module.

40 Peripheral Sensor Interface (PSI5)

This device doesn’t contain a PSI5.

41 Peripheral Sensor Interface with Serial PHY Connection (PSI5-S)

This device doesn’t contain a PSI5.

42 Gigabit Ethernet MAC (GETH)

This document describes the GETH Interface specific appendix for the product TC33xEXT.

42.1 TC33xEXT Specific IP Configuration

No product specific configuration for GETH

42.2 TC33xEXT Specific Register Set

Register Address Space Table

The address space for the module registers is defined in **Register Address Space Table**.

Table 275 Register Address Space - GETH

Module	Base Address	End Address	Note
GETH	$F001D000_H$	$F001F0FF_H$	FPI bus interface

Register Overview Table

Table 276 Register Overview - GETH (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_CONFIGURATION	MAC Configuration Register	0000_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_EXT_CONFIGURATION	MAC Extended Configuration Register	0004_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PACKET_FILTER	MAC Packet Filter Register	0008_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_WATCHDOG_TIMEOUT	MAC Watchdog Timeout Register	$000C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_TAG_CTRL	MAC VLAN Tag Control Register	0050_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_TAG_DATA	MAC VLAN Tag Data Register	0054_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_TAG_FILTER_i (i=0-7)	MAC VLAN Tag Filter i Register	0054_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_VLAN_HASH_TABLE	MAC VLAN Hash Table Register	0058_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_INCL	MAC VLAN Tag Inclusion or Replacement Register	0060_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VLAN_INCL_Q_i (i=0-3)	MAC VLAN Tag Inclusion or Replacement Register per Queue	0060_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INNER_VLAN_INCL_i (i=0-3)	MAC Inner VLAN Tag Inclusion or Replacement Register	0064_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_Q0_TX_FLOW_CTRL	MAC Queue 0 TX Flow Control Register	0070_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_FLOW_CTRL	MAC Receive Flow Control Register	0090_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RXQ_CTRL4	MAC Receive Queue Control 4 register	0094_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RXQ_CTRL0	MAC Receive Queue Control 0 Register	$00A0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RXQ_CTRL1	MAC Receive Queue Control 1 Register	$00A4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RXQ_CTRL2	MAC Receive Queue Control 2 Register	$00A8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INTERRUPT_STATUS	MAC Interrupt Status Register	$00B0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_INTERRUPT_ENABLE	MAC Interrupt Enable Register	$00B4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_RX_TX_STATUS	MAC Receive Transmit Status Register	$00B8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PMT_CONTROL_STATUS	MAC PMT Control and Status Register	$00C0_H$	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_RWK_PACKET_FILTER	MAC Wake-up Packet Filter Register	$00C4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_COMMAND_0	MAC Wake-up Filter Command 0 Register	$00C4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_OFFSET_0	MAC Wake-up Filter Offset 0 Register	$00C4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_CRC_i (i=0-1)	MAC Wake-up Filter CRC i Register	$00C4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RWK_FILTER_BYTE_MASK_i (i=0-3)	MAC Wake-up i Filter Byte Mask register	$00C4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_CONTROL_STATUS	MAC LPI Control and Status Register	$00D0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_TIMERS_CONTROL	MAC LPI Timers Control Register	$00D4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_LPI_ENTRY_TIMER	MAC LPI Entry Timer Register	$00D8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_1US_TIC_COUNTER	MAC One Microsecond Tic Counter Register	$00DC_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PHYIF_CONTROL_STATUS	MAC PHY Interface Control and Status Register	$00F8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_VERSION	MAC Version Register	0110_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_DEBUG	MAC Debug Register	0114_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE0	MAC Hardware Feature Register 0	$011C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE1	MAC Hardware Feature Register 1	0120_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_HW_FEATURE2	MAC Hardware Feature Register 2	0124_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_HW_FEATURE3	MAC Hardware Feature Register 3	0128_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_MDIO_ADDRESS	MAC MDIO Address Register	0200_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_MDIO_DATA	MAC MDIO Data Register	0204_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_CSR_SW_CTRL	MAC CSR Software Controls Register	0230_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_EXT_CFG1	MAC Extended Configuration Register 1	0238_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADDRESS0_HIGH	MAC Address 0 High Register	0300_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADDRESS0_LOW	MAC Address 0 Low Register	0304_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADDRESSi_HIGH (i=1-31)	MAC Address i High Register	0308_H+(i-1)*8	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_ADDRESSi_LOW (i=1-31)	MAC Address i Low Register	$030C_H$+(i-1)*8	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_CONTROL	MMC Control Register	0700_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_RX_INTERRUPT	MMC Receive Interrupts Register	0704_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_TX_INTERRUPT	MMC Transmit Interrupts Register	0708_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_RX_INTERRUPT_MASK	MMC Receive Interrupts Mask Register	$070C_H$	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MMC_TX_INTERRUPT_MASK	MMC Transmit Interrupts Mask Register	0710_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OCTET_COUNT_GOOD_BAD	Good And Bad Transmitted Octet Count Register	0714_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_PACKET_COUNT_GOOD_BAD	Good And Bad Transmitted Packets Count Register	0718_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_BROADCAST_PACKETS_GOOD	Good Transmitted Broadcast Packets Count Register	$071C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTICAST_PACKETS_GOOD	Good Transmitted Multicast Packets Count Register	0720_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_64OCTETS_PACKETS_GOOD_BAD	Good And Bad 64 Octets Packets Transmitted Count Register	0724_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_65TO127OCTETS_PACKETS_GOOD_BAD	Good And Bad 65to127 Octets Packets Transmitted Count Register	0728_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_128TO255OCTETS_PACKETS_GOOD_BAD	Good And Bad 128to255 Octets Packets Transmitted Count Register	$072C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_256TO511OCTETS_PACKETS_GOOD_BAD	Good And Bad 256to511 Octets Packets Transmitted Count Register	0730_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_512TO1023OCTETS_PACKETS_GOOD_BAD	Good And Bad 512to1023 Octets Packets Transmitted Count Register	0734_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	Good And Bad 1024toMax Octets Packets Transmitted Count Register	0738_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_UNICAST_PACKETS_GOOD_BAD	Good Transmitted Unicat Packets Count Register	$073C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTICAST_PACKETS_GOOD_BAD	Good And Bad Transmitted Multicast Packets Count Register	0740_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_TX_BROADCAST_PACKETS_GOOD_BAD	Good And Bad Transmitted Broadcast Packets Count Register	0744_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_UNDERFLOW_ERROR_PACKETS	Transmitted Underflow Error Packets Count Register	0748_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_SINGLE_COLLISION_GOOD_PACKETS	Good Transmitted Single Collision Count Register	$074C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_MULTIPLE_COLLISION_GOOD_PACKETS	Transmitted Multiple Collision Count Register	0750_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_DEFERRED_PACKETS	Transmitted Deferred Packets Count Register	0754_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_LATE_COLLISION_PACKETS	Transmitted Late Collision Packets Count Register	0758_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_EXCESSIVE_COLLISION_PACKETS	Transmitted Excessive Collision Packets Count Register	$075C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_CARRIER_ERROR_PACKETS	Transmitted Carrier Error Packets Count Register	0760_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OCTET_COUNT_GOOD	Good Transmitted Octet Count Register	0764_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_PACKET_COUNT_GOOD	Good Transmitted Packet Count Register	0768_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_EXCESSIVE_DEFERRAL_ERROR	Transmitted Excessive Deferral Error Count Register	$076C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_PAUSE_PACKETS	Transmitted Pause Packets Count Register	0770_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_VLAN_PACKETS_GOOD	Good Transmitted VLAN Packets Count Register	0774_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_OSIZE_PACKETS_GOOD	Good Transmitted Osize Packets Count Register	0778_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_RX_PACKETS_COUNT_GOOD_BAD	Good And Bad Received Packets Count Register	0780_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OCTET_COUNT_GOOD_BAD	Good And Bad Received Octet Count Register	0784_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OCTET_COUNT_GOOD	Good Received Octet Count Register	0788_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_BROADCAST_PACKETS_GOOD	Good Received Broadcast Packets Count Register	$078C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_MULTICAST_PACKETS_GOOD	Good Received Multicast Packets Count Register	0790_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_CRC_ERROR_PACKETS	Received CRC Error Packets Count Register	0794_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_ALIGNMENT_ERROR_PACKETS	Received Alignment Error Count Register	0798_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_RUNT_ERROR_PACKETS	Received Runtime Error Count Register	$079C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_JABBER_ERROR_PACKETS	Received Jabber Error Count Register	$07A0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_UNDERSIZE_PACKETS_GOOD	Good Received Undersized Packets Count Register	$07A4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OVERSIZE_PACKETS_GOOD	Good Received Oversized Packets Count Register	$07A8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_64OCTETS_PACKETS_GOOD_BAD	Good And Bad 64 Octets Packets Received Count Register	$07AC_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_65TO127OCTETS_PACKETS_GOOD_BAD	Good And Bad 65to127 Octets Packets Received Count Register	$07B0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_128TO255OCTETS_PACKETS_GOOD_BAD	Good And Bad 128to255 Octets Packets Received Count Register	$07B4_H$	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_RX_256TO511OCTETS_PACKETS_GOOD_BAD	Good And Bad 256to511 Octets Packets Received Count Register	$07B8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_512TO1023OCTETS_PACKETS_GOOD_BAD	Good And Bad 512to1023 Octets Packets Received Count Register	$07BC_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_1024TOMAXOCTETS_PACKETS_GOOD_BAD	Good And Bad 1024toMax Octets Packets Received Count Register	$07C0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_UNICAST_PACKETS_GOOD	Good Received Unicat Packets Count Register	$07C4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_LENGTH_ERROR_PACKETS	Received Length Error Packets Count Register	$07C8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_OUT_OF_RANGE_TYPE_PACKETS	Received Out Of Range Type Count Register	$07CC_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_PAUSE_PACKETS	Received Pause Packets Count Register	$07D0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_FIFO_OVERFLOW_PACKETS	Received FIFO Overflow Count Register	$07D4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_VLAN_PACKETS_GOOD_BAD	Good And Bad Received VLAN Packets Count Registerv	$07D8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_WATCHDOG_ERROR_PACKETS	Received Watchdog Error Count Register	$07DC_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_RECEIVE_ERROR_PACKETS	Received Receive Error Count Register	$07E0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_CONTROL_PACKETS_GOOD	Good Received Control Packets Count Register	$07E4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_TX_LPI_USEC_CNTR	Transmitted LPI Microseconds Count Register	$07EC_H$	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_TX_LPI_TRAN_CNTR	Transmitted LPI Transition Count Register	$07F0_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_LPI_USEC_CNTR	Received Microseconds LPI Count Register	$07F4_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RX_LPI_TRAN_CNTR	Received LPI Transition Count Register	$07F8_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_IPC_RX_INTERRUPT_MASK	MMC IPC Receive Interrupts Mask Register	0800_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MMC_IPC_RX_INTERRUPT	MMC IPC Receive Interrupts Register	0808_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_GOOD_PACKETS	Good Received RxIPv4 Packets Count Register	0810_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_HEADER_ERROR_PACKETS	Received IPv4 Header Error Packets Count Register	0814_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_NO_PAYLOAD_PACKETS	Received IPv4 No Payload Packets Count Register	0818_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_FRAGMENTED_PACKETS	Received IPv4 Fragmented Packets Count Register	$081C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_UDP_CHECKSUM_DISABLED_PACKETS	Received IPv4 UPD Checksum Disabled Packets Count Register	0820_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_GOOD_PACKETS	Good Received RxIPv6 Packets Count Register	0824_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_HEADER_ERROR_PACKETS	Received IPv6 Header Error Packets Count Register	0828_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_NO_PAYLOAD_PACKETS	Received IPv6 No Payload Packets Count Register	$082C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXUDP_GOOD_PACKETS	Good Received UDP Packets Count Register	0830_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_RXUDP_ERROR_PACKETS	Received UDP Error Packets Count Register	0834_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_GOOD_PACKETS	Good Received TCP Packets Count Register	0838_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_ERROR_PACKETS	Received TCP Error Packets Count Register	$083C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_GOOD_PACKETS	Good Received ICMP Packets Count Register	0840_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_ERROR_PACKETS	Received ICMP Error Packets Count Register	0844_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_GOOD_OCTETS	Good Received IPV4 Octets Count Register	0850_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_HEADER_ERROR_OCTETS	Received IPV4 Header Error Octets Count Register	0854_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_NO_PAYLOAD_OCTETS	Received IPV4 No Payload Octets Count Register	0858_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_FRAGMENTED_OCTETS	Received IPV4 Fragmented Octets Count Register	$085C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV4_UDP_CHECKSUM_DISABLE_OCTETS	Received IPV4 UPD Checksum Disabled Octets Count Register	0860_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_GOOD_OCTETS	Good Received IPV6 Octets Count Register	0864_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_HEADER_ERROR_OCTETS	Received IPV6 Header Error Octets Count Register	0868_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXIPV6_NO_PAYLOAD_OCTETS	Received IPV6 No Payload Octets Count Register	$086C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXUDP_GOOD_OCTETS	Good Received UDP Octets Count Register	0870_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_RXUDP_ERROR_OCTETS	Received UDP Error Octets Count Register	0874_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_GOOD_OCTETS	Good Received TCP Octets Count Register	0878_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXTCP_ERROR_OCTETS	Received TCP Error Octets Count Register	$087C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_GOOD_OCTETS	Good Received ICMP Octets Count Register	0880_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_RXICMP_ERROR_OCTETS	Received ICMP Error Octets Count Register	0884_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIMESTAMP_CONTROL	MAC Timestamp Control Register	$0B00_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SUB_SECOND_INCREMENT	MAC Sub-Second Increment Register	$0B04_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_SECONDS	MAC System Time Seconds Register	$0B08_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_NANOSECONDS	MAC System Time Nanoseconds Register	$0B0C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_SECONDS_UPDATE	MAC System Time Seconds Update Register	$0B10_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_NANOSECONDS_UPDATE	MAC System Time Nanoseconds Update Register	$0B14_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIMESTAMP_ADDEND	MAC Timestamp Addend Register	$0B18_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_SYSTEM_TIME_HIGHER_WORD_SECONDS	MAC System Time Higher Word Seconds Register	$0B1C_H$	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_TIMESTAMP_STATUS	MAC Timestamp Status Register	$0B20_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TX_TIMESTAMP_STATUS_NANOSECONDS	MAC Transmit Timestamp Nanoseconds Status Register	$0B30_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TX_TIMESTAMP_STATUS_SECONDS	MAC Transmit Timestamp Seconds Status Register	$0B34_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIMESTAMP_INGRESS_ASYM_CORR	MAC Timestamp Ingress Asymmetry Correction Register	$0B50_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIMESTAMP_EGRESS_ASYM_CORR	MAC Timestamp Egress Asymmetry Correction Register	$0B54_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIMESTAMP_INGRESS_CORR_NANOSECOND	MAC Timestamp Ingress Correction Nanoseconds Register	$0B58_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIMESTAMP_EGRESS_CORR_NANOSECOND	MAC Timestamp Egress Correction Nanoseconds Register	$0B5C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIMESTAMP_INGRESS_CORR_SUBNANOSEC	MAC Timestamp Ingress Correction Subnanoseconds Register	$0B60_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_TIMESTAMP_EGRESS_CORR_SUBNANOSEC	MAC Timestamp Egress Correction Subnanoseconds Register	$0B64_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS_CONTROL	MAC PPS Control Register	$0B70_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS0_TARGET_TIME_SECONDS	MAC PPS 0 Target Time Seconds Register	$0B80_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS0_TARGET_TIME_NANOSECONDS	MAC PPS 0 Target Time Nanoeconds Register	$0B84_H$	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MAC_PPS0_INTERVAL	MAC PPS 0 Interval Register	$0B88_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MAC_PPS0_WIDTH	MAC PPS 0 Width Register	$0B8C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_OPERATION_MODE	MTL Operation Mode Register	$0C00_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_INTERRUPT_STATUS	MTL Interrupt Status Register	$0C20_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ_DMA_MAP0	MTL Receive Queue and DMA Channel Mapping 0 Register	$0C30_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_OPERATION_MODE	MTL Queue 0 Transmit Operation Mode Register	$0D00_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_UNDERFLOW	MTL Queue 0 Transmit Underflow Counter Register	$0D04_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_DEBUG	MTL Queue 0 Transmit Debug Register	$0D08_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_ETS_STATUS	MTL Queue 0 Transmit Status Register	$0D14_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQ0_QUANTUM_WEIGHT	MTL Queue 0 Transmit Quantum or Weights Register	$0D18_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_Q0_INTERRUPT_CONTROL_STATUS	MTL Queue 0 Interrupt Control Status Register	$0D2C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ0_OPERATION_MODE	MTL Queue 0 Receive Operation Mode Register	$0D30_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ0_MISSED_PACKET_OVERFLOW_CNT	MTL Queue 0 Receive Missed Packet and Overflow Counter Register	$0D34_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQ0_DEBUG	MTL Queue 0 Receive Debug Register	$0D38_H$	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MTL_RXQ0_CONTROL	MTL Queue 0 Receive Control Register	$0D3C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_OPERATION_MODE (i=1-3)	MTL Queue i Transmit Operation Mode Register	$0D40_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_UNDERFLOW (i=1-3)	MTL Queue i Transmit Underflow Counter Register	$0D44_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_DEBUG (i=1-3)	MTL Queue i Transmit Debug Register	$0D48_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_ETS_CONTROL (i=1-3)	MTL Queue i Transmit ETS Control Register	$0D50_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_ETS_STATUS (i=1-3)	MTL Queue i Transmit ETS Status Register	$0D54_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_QUANTUM_WEIGHT (i=1-3)	MTL Queue i Transmit Quantum or Weights Register	$0D58_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_SENDSLOPECREDIT (i=1-3)	MTL Queue i Transmit SendSlopeCredit Register	$0D5C_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_HICREDIT (i=1-3)	MTL Queue i Transmit HiCredit Register	$0D60_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_TXQi_LOCREDIT (i=1-3)	MTL Queue i Transmit LoCredit Register	$0D64_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_Qi_INTERRUPT_CONTROL_STATUS (i=1-3)	MTL Queue i Interrupt Status Register	$0D6C_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_OPERATION_MODE (i=1-3)	MTL Queue i Receive Operation Mode Register	$0D70_H+(i-1)*40_H$	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_MTL_RXQi_MISSED_PACKET_OVERFLOW_CNT (i=1-3)	MTL Queue i Receive Missed Packet and Overflow Counter Register	$0D74_H$+(i-1)*40_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_DEBUG (i=1-3)	MTL Queue i Receive Debug Register	$0D78_H$+(i-1)*40_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_MTL_RXQi_CONTROL (i=1-3)	MTL Queue i Receive Control Register	$0D7C_H$+(i-1)*40_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_MODE	DMA Bus Mode Register	1000_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_SYSBUS_MODE	DMA System Bus Mode Register	1004_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_INTERRUPT_STATUS	DMA Interrupt Status Register	1008_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_DEBUG_STATUS0	DMA Debug Status 0 Register	$100C_H$	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_DEBUG_STATUS1	DMA Debug Status 1 Register	1010_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CONTROL (i=0-3)	DMA Channel i Control Register	1100_H+i*80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_TX_CONTROL (i=0-3)	DMA Channel i Transmit Control Register	1104_H+i*80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RX_CONTROL (i=0-3)	DMA Channel i Receive Control Register	1108_H+i*80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_TXDESC_LIST_ADDRESS (i=0-3)	DMA Channel i Transmit Descriptor List Address Register	1114_H+i*80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RXDESC_LIST_ADDRESS (i=0-3)	DMA Channel i Receive Descriptor List Address Register	$111C_H$+i*80_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_DMA_CHi_TXDESC_TAIL_POINTER (i=0-3)	DMA Channel i Transmit Descriptor Tail Pointer Register	1120_H+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RXDESC_TAIL_POINTER (i=0-3)	DMA Channel i Recieve Descriptor Tail Pointer Register	1128_H+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_TXDESC_RING_LENGTH (i=0-3)	DMA Channel i Transmit Descriptor Ring Length Register	$112C_H$+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RXDESC_RING_LENGTH (i=0-3)	DMA Channel i Recieve Descriptor Ring Length Register	1130_H+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_INTERRUPT_ENABLE (i=0-3)	DMA Channel i Interrupt Enable Register	1134_H+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_RX_INTERRUPT_WATCHDOG_TIMER (i=0-3)	DMA Channel i Recieve Interrupt Watchdog Timer Register	1138_H+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_SLOT_FUNCTION_CONTROL_STATUS (i=0-3)	DMA Channel i Slot Function Control and Status Register	$113C_H$+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APP_TXDESC (i=0-3)	DMA Channel i Current Application Transmit Descriptor Register	1144_H+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APP_RXDESC (i=0-3)	DMA Channel i Current Application Receive Descriptor Register	$114C_H$+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_CURRENT_APP_TXBUFFER (i=0-3)	DMA Channel i Current Application Transmit Buffer Address Register	1154_H+i* 80_H	U,SV	U,SV,P	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_DMA_CHi_CURRENT_APP_RXBUFFER (i=0-3)	DMA Channel i Current Application Receive Buffer Address Register	$115C_H$+i*80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_STATUS (i=0-3)	DMA Channel i Status Register	1160_H+i*80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_DMA_CHi_MISS_FRAME_CNT (i=0-3)	DMA Channel i Missed Frames Count Register	1164_H+i*80_H	U,SV	U,SV,P	Application Reset	See Family Spec
GETH_CLC	Clock Control Register	2000_H	SV,U	SV,E,P	Application Reset	See Family Spec
GETH_ID	Module Identification Register	2004_H	SV,U	BE	Application Reset	See Family Spec
GETH_GPCTL	General Purpose Control Register	2008_H	SV,U	SV,P	Application Reset	See Family Spec
GETH_ACCEN0	Access Enable Register 0	$200C_H$	U,SV	SV,SE	Application Reset	See Family Spec
GETH_ACCEN1	Access Enable Register 1	2010_H	U,SV	SV,SE	Application Reset	See Family Spec
GETH_KRST0	Kernel Reset Register 0	2014_H	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_KRST1	Kernel Reset Register 1	2018_H	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_KRSTCLR	Kernel Reset Status Clear Register	$201C_H$	U,SV	SV,E,P	Application Reset	See Family Spec
GETH_ACCEN0Dx (x=0-3)	Access Enable Register 0 for DMAx	2020_H+x*8	U,SV	SV,SE	Application Reset	See Family Spec

Table 276 Register Overview - GETH (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
GETH_ACCEN1Dx (x=0-3)	Access Enable Register 1 for DMAx	2024_H+x *8	U,SV	SV,SE	Application Reset	See Family Spec
GETH_SKEWCTL	Skew Control Register	2040_H	SV,U	SV,P	Application Reset	See Family Spec

42.3 TC33xEXT Specific Registers

No deviations from the Family Spec

42.4 Connectivity

If for one product no signal is connected to an alternate input, it is connected to GND internally at module entity level. This allows to leave some signals unconnected in the application (i.e. RXER, CRS, COL) and save pins and external connection to GND. The tables below list all the connections of the instances.

Table 277 Connections of GETH

Interface Signals	connects		Description
GETH:COLA	from	P11.15:IN	Collision MII
GETH:CRSA	from	P11.14:IN	Carrier Sense MII
GETH:CRSB	from	P11.11:IN	Carrier Sense MII
GETH:CRSDVA	from	P11.11:IN	Carrier Sense / Data Valid combi-signal for RMII
GETH:CRSDVB	from	P11.14:IN	Carrier Sense / Data Valid combi-signal for RMII
GETH:GREFCLK	from	TC33xEXT:P11.5	Gigabit Reference Clock input for RGMII (125 MHz high precission)
GETH:MDC	to	P02.8:ALT(6)	MDIO clock
		P12.0:ALT(6)	
		P21.2:ALT(5)	
GETH:MDIO	to	P00.0:HWOUT(0)	MDIO Output
		P12.1:HWOUT(0)	
		P21.3:HWOUT(0)	
GETH:MDIOA	from	P00.0:IN	MDIO Input
GETH:MDIOC	from	P12.1:IN	MDIO Input
GETH:MDIOD	from	P21.3:IN	MDIO Input
GETH:PPS	to	P14.4:ALT(6)	Pulse Per Second
GETH:RCTLA	from	P11.11:IN	Receive Control for RGMII
GETH:REFCLKA	from	P11.12:IN	Reference Clock input for RMII (50 MHz)
GETH:RXCLKA	from	P11.12:IN	Receive Clock MII and RGMII

Table 277 Connections of GETH (cont'd)

Interface Signals	connects		Description
GETH:RXCLKB	from	P11.4:IN	Receive Clock MII and RGMII
GETH:RXCLKC	from	P12.0:IN	Receive Clock MII and RGMII
GETH:RXD0A	from	P11.10:IN	Receive Data 0 MII, RMII and RGMII (RGMII can use RXD0A only)
GETH:RXD1A	from	P11.9:IN	Receive Data 1 MII, RMII and RGMII (RGMII can use RXD1A only)
GETH:RXD2A	from	P11.8:IN	Receive Data 2 MII and RGMII (RGMII can use RXD2A only)
GETH:RXD3A	from	P11.7:IN	Receive Data 3 MII and RGMII (RGMII can use RXD3A only)
GETH:RXDVA	from	P11.11:IN	Receive Data Valid MII
GETH:RXDVB	from	P11.14:IN	Receive Data Valid MII
GETH:RXERA	from	P11.13:IN	Receive Error MII
GETH:RXERB	from	P21.7:IN	Receive Error MII
GETH:RXERC	from	P10.0:IN	Receive Error MII
GETH:TRIGO(9:0)	to	INT:eth.TRIGO(9:0)	Ethernet Service Request
GETH:TCTL	to	TC33xEXT:P11.6	Transmit Control for RGMII
GETH:TXCLK	to	TC33xEXT:P11.4	Transmit Clock Output for MII and RGMII
GETH:TXCLKA	from	P11.5:IN	Transmit Clock Input for MII
GETH:TXCLKB	from	P11.12:IN	Transmit Clock Input for MII
GETH:TXD(0)	to	TC33xEXT:P11.3	Transmit Data
GETH:TXD(1)	to	TC33xEXT:P11.2	Transmit Data
GETH:TXD(2)	to	TC33xEXT:P11.1	Transmit Data
GETH:TXD(3)	to	TC33xEXT:P11.0	Transmit Data
GETH:TXEN	to	TC33xEXT:P11.6	Transmit Enable MII and RMII
GETH:TXER	to	P11.4:ALT(6)	Transmit Error MII

42.5 DMA Burst Lengths Limitations by the System

Not all burst lengths of the IP are supported by the system.

The GETH / GETH1 kernel IP supports various burst length of 1 up to 32 beats as defined in DMA_CHi_TX_CONTROL.TxPBL and DMA_CHi_RX_CONTROL.RxPBL. They can be multiplied by 8 by setting DMA_CH(#i)_Control.PBLx8.

Other than specified in the IP only the following burst lengths are supported by the system: SINGLE, INCR4, INCR8. Note that DMA_CH(#i)_Control.PBLx8 must not be set with PBL values higher than 1.

42.6 Buffer and Descriptor Alignment

The GETH / GETH1 are implemented as a 32 bit peripherals. Nevertheless they are connected to 64 bit wide bus (SRI). To make full use of the possible performance of SRI and its bridges, the data buffers and the descriptors need to be aligned to 64 bit addresses.

42.7 Embedded FIFOs

Each GETH / GETH1 uses two embedded FIFOs. The TX FIFO has a size of 4 kByte, the RX FIFO has a size of 8 kByte.

42.8 Master TAG ID

Each module has 4 DMA Channels that share one master interface connecting them to the SRI bus. In order to distinguish the 4 DMAs from each other in the system, the master tag ID will dynamically be changed depending on the currently active DMA. **Table 278** details which ID is presented for each DMA.

Table 278 Master TAG IDs for the Gigabit Ethernet MACs

GETH_DMA	Master TAG ID
DMA0	$0x28_H$
DMA1	$0x29_H$
DMA2	$0x2A_H$
DMA3	$0x2B_H$

42.9 Interrupt Service Requests

Each module has 10 Service Request Nodes connecting it to the interrupt system. The interrupt request lines are connected to the interrupt controller as shown in **Table 279**.

Table 279 Service Request Lines of Ethernet MAC GETH

IR SRC	GETH IP signal	GETH IP function	Description
SRC_GETH0	GETH_TRIGO0	GETH_INTR	DMA functions (sbd_intr_o), this internal line is connected via OR gate to GETH.SR0 wake up on LAN (pmt_intr_o), this internal line is connected via OR gate to GETH.SR0 wake up on EEE - LPI (lpi_intr_o), this internal line is connected via OR gate to GETH.SR0
SRC_GETH1	GETH_TRIGO1	GETH_PPS	Pulse Per Second signal from Precision Time Protocol (ptp_pps_o)
SRC_GETH2	GETH_TRIGO2	GETH_TX_DMA0	TX interrupt from DMA 0 (sbd_perch_tx_intr_o[0])
SRC_GETH3	GETH_TRIGO3	GETH_TX_DMA1	TX interrupt from DMA 1(sbd_perch_tx_intr_o[1])
SRC_GETH4	GETH_TRIGO4	GETH_TX_DMA2	TX interrupt from DMA 2(sbd_perch_tx_intr_o[2])
SRC_GETH5	GETH_TRIGO4	GETH_TX_DMA3	TX interrupt from DMA 3(sbd_perch_tx_intr_o[3])
SRC_GETH6	GETH_TRIGO6	GETH_RX_DMA0	RX interrupt from DMA 0 (sbd_perch_rx_intr_o[0])
SRC_GETH7	GETH_TRIGO7	GETH_RX_DMA1	RX interrupt from DMA 1(sbd_perch_rx_intr_o[1])
SRC_GETH8	GETH_TRIGO8	GETH_RX_DMA2	RX interrupt from DMA 2(sbd_perch_rx_intr_o[2])
SRC_GETH9	GETH_TRIGO9	GETH_RX_DMA3	RX interrupt from DMA 3(sbd_perch_rx_intr_o[3])

42.10 Clocks

Each module has multiple clock inputs and outputs connecting it to the system. They are connected to the system as shown in **Table 280**.

If the application wants to use the IP in RGMII mode the appliction has to execute the following steps:

- Prior to the application reset the application must switch on (e.g. for f_{GETH} by configuring CCUCON5.GETHDIV)
- Attach an external 125 MHz clock to input GREFCLK
- Activate the application reset
- Wait for 10 µs

Table 280 Clock Lines of Ethernet MAC GETH

Clock Line	Connected to	Description
hclk_i / f_{AHB}	f_{GETH}	AHB master interface clock
clk_csr_i / f_{CSR}	f_{SPB}	AHB slave interface clock
clk_tx_i	GETH_TXCLK (port pin)	MII transmit clock Input from PHY (10/100 MBit/s) The external PHY or oscillator provides this transmission clock. TXD[3:0] is synchronous to this clock. This is 25 MHz in 100 Mbps mode and 2.5 MHz in 10 Mbps mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_gref_i	GETH_GREFCLK (port pin)	RGMII transmit clock **Reference Input** from PHY (1000 MBit/s). The external PHY or oscillator provides this clock as reference. TXD[3:0] is not neccessarily synchronous to this clock! This is always 125 MHz in 1000/100/10 MBit/s mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_tx_o	GETH_TXCLK (port pin)	RGMII transmission clock **Output** to PHY (1000 MBit/s) . TXD[3:0] is synchronous (DDR) to this 125 MHz clock to the PHY. If RGMII is downgraded to 100 MBit/s it is divided internally to 25 MHz and for 10 MBit/s to 2.5 MHz. In each case it is generated from clk_gref_i by respective division. This division is controlled automatically by evaluation of mac_speed_o[1:0] and phy_intf_sel_i[2:0]. TXCLK has the same on chip delay and output pad delay as the TXD signals and TCTL unless clock skew is selected in SKEW.
clk_rx_i	GETH_RXCLK (port pin)	Receive clock from Phy. The external PHY provides this receive clock for RGMII, GMII, MII, and RMII interfaces. This clock is 125 MHz in 1 Gbps mode, 25 MHz in 100 Mbps mode, 2.5 MHz in 10 Mbps mode. Needs a clock input during SW reset (GETH_BUS_MODE.SWR)
clk_rmii_i	GETH_REFCLK (port pin)	50-MHz clock used by the RMII from PHY. In 100 MBit/s Mode, it is divided internally to 25 MHz and provided to the internal MII interface. If RMII is downgraded to 10 MBit/s it is divided internally to 2,5 MHz. This division is controlled automatically by evaluation of mac_speed_o[1:0] and phy_intf_sel_i[2:0]. Needs a clock input during SW reset (GETH_BUS_MODE.SWR).
clk_ptp_ref_i	f_{GETH}	Reference Clock for the Time Stamp Update Logic

42.11 Revision History

Table 281 Revision History

Reference	Change to Previous Version	Comment
V1.3.10		
–	Initial version for TC33X	
V1.3.11		
Page 18	Incorrect presentation of registers GETH_MAC_EXT_CONFIGURATION, GETH_MAC_VERSION and GETH_DMA_MODE removed.	–
V1.3.12		
Page 21	f_{SRI} changed to f_{GETH} as connection of clk_ptp_ref_i.	
Page 20	Removed GETH1 in table Master TAG IDs.	
Page 20	Removed table Service Request Lines of Ethernet MAC GETH1 in section Interrupt Service Requests.	
Page 20	Removed table Clock Lines of Ethernet MAC GETH1 in section Clocks.	
Page 18	Updated connection of MII and RGMII in **Connectivity**.	
V1.3.13		
–	No functional changes.	
V1.3.14		
–	No functional changes.	
V1.3.15		
–	No functional changes.	–

43 External Bus Unit (EBU)

This device doesn’t contain an EBU module.

44 SD- and eMMC Interface (SDMMC)

This chapter describes the SDMMC.

44.1 TC33xEXT Specific Register Set

Register Address Space Table

Table 282 Register Address Space - SDMMC

Module	Base Address	End Address	Note
SDMMC0	$F02B0000_H$	$F02B0FFF_H$	FPI slave interface

Register Overview Table

There are no product specific register for this module.

44.2 TC33xEXT Specific Registers

There are no product specific register for this module.

44.3 Connectivity

Table 283 Connections of SDMMC0

Interface Signals	connects		Description
SDMMC0:CLK	to	P15.1:ALT(7)	card clock
SDMMC0:CMD	to	P15.3:HWOUT(0)	command out
SDMMC0:CMD_IN	from	P15.3:IN	command in
SDMMC0:DAT(0)	to	P20.7:HWOUT(0)	write data out
SDMMC0:DAT(1)	to	P20.8:HWOUT(0)	write data out
SDMMC0:DAT(2)	to	P20.10:HWOUT(0)	write data out
SDMMC0:DAT(3)	to	P20.11:HWOUT(0)	write data out
SDMMC0:DAT(4)	to	P20.12:HWOUT(0)	write data out
SDMMC0:DAT(5)	to	P20.13:HWOUT(0)	write data out
SDMMC0:DAT(6)	to	P20.14:HWOUT(0)	write data out
SDMMC0:DAT(7)	to	P15.0:HWOUT(0)	write data out
SDMMC0:DAT0_IN	from	P20.7:IN	read data in
SDMMC0:DAT1_IN	from	P20.8:IN	read data in
SDMMC0:DAT2_IN	from	P20.10:IN	read data in
SDMMC0:DAT3_IN	from	P20.11:IN	read data in
SDMMC0:DAT4_IN	from	P20.12:IN	read data in
SDMMC0:DAT5_IN	from	P20.13:IN	read data in
SDMMC0:DAT6_IN	from	P20.14:IN	read data in
SDMMC0:DAT7_IN	from	P15.0:IN	read data in

44.4 Revision History

Table 284 Revision History

Reference	Change to Previous Version	Comment
V1.0.17		
–	No functional changes.	
V1.0.18		
–	No functional changes.	

45 Hardware Security Module (HSM)

The HSM is a separate processor subsystem dedicated for security tasks. It is connected as master and slave to the SPB bus.

For security reasons this module is described in a separate documentation. Please contact your Infineon representative for further information.

46 Input Output Monitor (IOM)

This device doesn’t contain an IOM.

47 8-Bit Standby Controller (SCR)

The description of the SCR for all devices is covered by the family specification.

Revision history

Document version	Date of release	Description of changes
V2.0.0	2021-02	• Version comparison table updated. • For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.6.0	2020-08	• Version comparison table updated. • For further changes see respective revision history of each chapter. The version comparison table below gives an overview. • Removed device TC3Ax from set of documentation.
V1.5.0	2020-04	• Version comparison table updated. • For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.4.0	2019-12	• Added TC3Ax appendix as target specification. • Version comparison table updated. • For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.3.0	2019-09	• Added additional device TC3Ax to AURIX™ TC3xx set of documentation. • Version comparison table updated. • For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.2.0	2019-04	• Added additional device TC3Ex to AURIX™ TC3xx set of documentation. • Version comparison table updated. • For further changes see respective revision history of each chapter. The version comparison table below gives an overview.
V1.1.0	2019-01	• Power Management System for Low-End (PMSLE) added. • TC33x and TC33xED added. • Changes in connectivity tables. • Version comparison table new. • Detailed Revision History contained in each chapter.
V1.0.0	2018-08	• First revision of the User's Manual. • Detailed OCDS information not contained. Available under NDA. • Detailed Revision History contained in each chapter.

Version comparison table for AURIX™ TC33xEXT appendix

Chapter name	UM V1.6.0 chapter version	UM V2.0.0 chapter version	Content changes
Introduction	V1.0.0	V1.0.0	No
MEMMAP	V0.1.20	V0.1.21	**Yes, see chapter revision history**
FW	V1.1.0.1.17	V1.1.0.1.18	No functional changes
SRI Fabric	V1.1.16	V1.1.17	No functional changes

Chapter name	UM V1.6.0 chapter version	UM V2.0.0 chapter version	Content changes
• SBCU, EBCU	V1.2.8	V1.2.9	**Yes, see chapter revision history**
CPU	V1.1.20	V1.1.21	No functional changes
NVM Subsystem	V2.0.7	V2.0.7	No
• DMU	V2.0.11	V2.0.12	No functional changes
• NVM	V2.0.6	V2.0.6	No
LMU	n/a	n/a	–
DAM	n/a	n/a	–
SCU	V2.1.26	V2.1.27	No functional changes
CCU	see SCU	see SCU	–
PMS	V2.2.33	V2.2.34	No functional changes
PMSLE	n/a	n/a	–
MTU	V7.4.12	V7.4.13	**Yes, see chapter revision history**
PORTS	V1.8.21	V1.8.21	No
SMU	V4.0.22	V4.0.23	**Yes, see chapter revision history**
INT	V1.2.11	V1.2.11	No
FCE	V4.2.9	V4.2.9	No
DMA	V0.1.18	V0.1.18	No
SPU	V1.1.24	V1.1.25	No functional changes
SPU2	n/a	n/a	–
BITMGR	n/a	n/a	–
SPULCKSTP	n/a	n/a	–
EMEM	V1.4.4	V1.4.4	No
RIF	V1.0.40	V1.0.43	**Yes, see chapter revision history**
HSPDM	V0.7.9	V0.7.9	No
CIF	n/a	n/a	–
STM	V9.2.4	V9.2.4	No
GTM	n/a	n/a	–
CCU6	V3.0.0	V3.0.0	No
GPT12	V3.0.2	V3.0.2	No
CONVCTRL	V3.0.1	V3.0.1	No
EVADC	V3.0.4	V3.0.5	No functional changes
EDSADC	n/a	n/a	–
I2C	n/a	n/a	–
HSSL	n/a	n/a	–
ASCLIN	V3.2.8	V3.2.8	No
QSPI	V3.0.20	V3.0.20	No
MSC	n/a	n/a	–
SENT	V2.1.10	V2.1.10	No

Chapter name	UM V1.6.0 chapter version	UM V2.0.0 chapter version	Content changes
MCMCAN	V1.19.13	V1.19.13	No
E-Ray	n/a	n/a	–
PSI5	n/a	n/a	–
PSI5-S	n/a	n/a	–
GETH	V1.3.14	V1.3.15	No functional changes
EBU	n/a	n/a	–
SDMMC	V1.0.18	V1.0.18	No
HSM	n/a	n/a	–
IOM	n/a	n/a	–
SCR	n/a	n/a	–

Edition 2021-02
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about any aspect of this document?
Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie").

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.