System: Cortex® – M4 debug system

XMC™ microcontrollers

September 2016

Agenda

1. Data Watchpoint and Trace (DWT)
2. Breakpoint unit
3. Trace support
4. Debug connector pins

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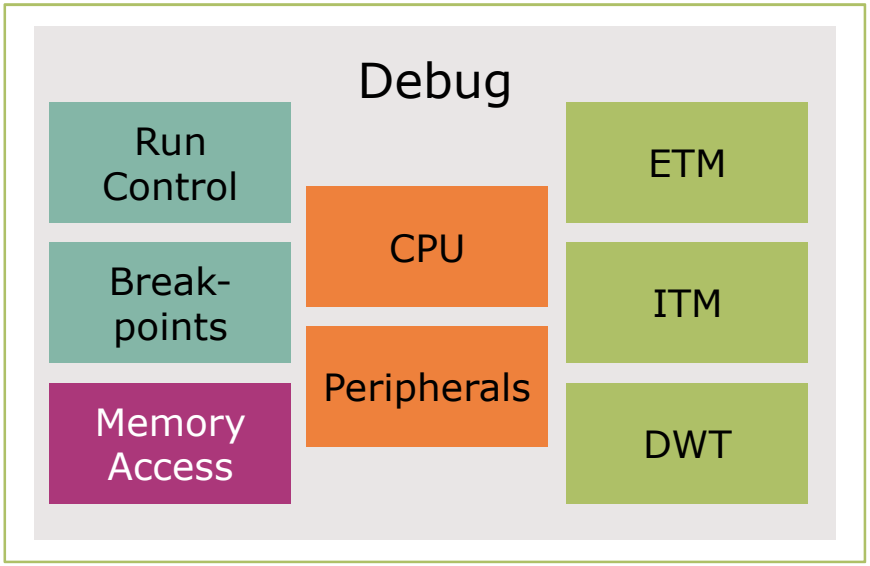
Debug system



Highlights

Cortex®- M4 debug system includes processor halt, single-step, processor core register access, vector catch and full system memory access.

8 hardware breakpoints and unlimited software breakpoints. 4 data watch points for address matching. Native JTAG and two pin SWD debug with full trace supported.

Key feature

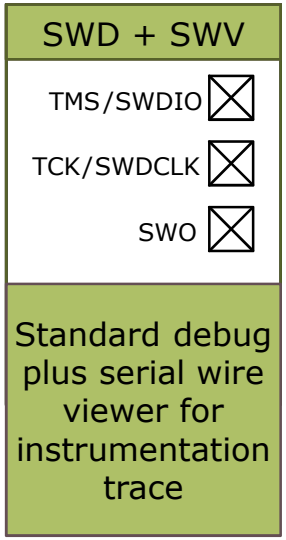
- Serial wire viewer and trace
- Halt after reset
- Peripheral suspend support

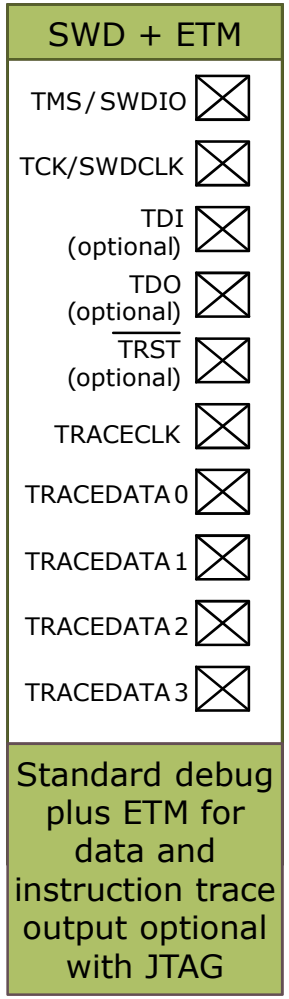
Customer benefits

- Data trace using serial wire interface or 4-bit parallel interface
- Halt CPU before user code starts (at 1st instruction of user code)
- Microcontroller critical state debugging by peripheral suspend on a CPU halt

Debug system
Serial wire viewer and trace

- Trace capability provided via
  - Serial Wire Viewer (SWV)
  - 4-bit Embedded Trace Macrocell (ETM) data port
- Serial wire viewer available via Serial Wire Output (SWO) connection when serial wire debug mode is used
- Data and instruction trace information is transmitted to the debugger for observation





Debug system
Halt after reset

- Halt after reset allows halting of the CPU at the first instruction of user code
- Cold reset (HAR)
  - After power on reset, a tool can register within a short time slot
  - On successful tool registration CPU halts at the end of the start-up software (SSW) otherwise code in flash will be executed
- Warm reset
  - Halt after system reset (warm reset) can be achieved by programming a break point at the first instruction of the application code
  - HOT PLUG capability is possible in this mode
- Security features
  - Debug access to CPU/system prevented before and during SSW is executed (tool registration is possible)
  - Debug access to flash prevented if flash protection is activated

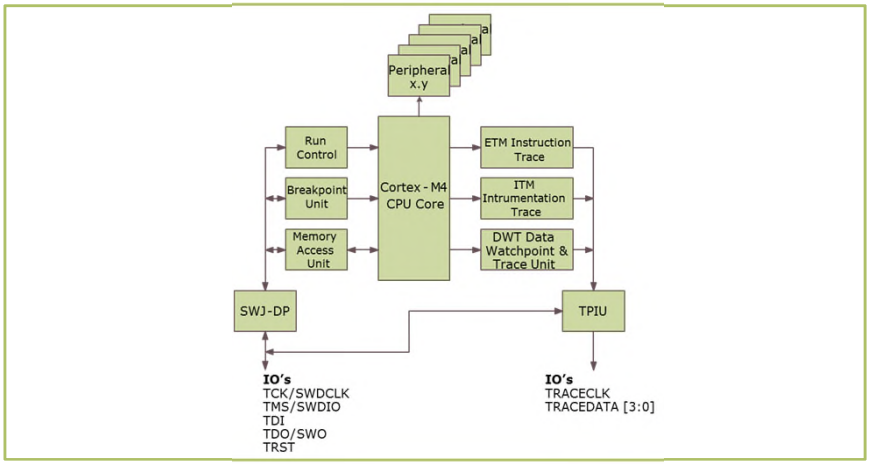
Debug system
Peripheral suspend support (1/2)

- Allows critical system state debugging
  - E.g. Debug watchdog behavior
- Suspend based on breakpoint or by setting the processor halt bit (C_HALT)
- Availability of hard and soft suspend capability
  - Hard suspend: Peripheral switched off immediately
  - Soft suspend: Peripheral can decide when to suspend. Usually at the end of the actual active transfer
    - E.g. Versatile Analog-to-Digital Converter (VADC) stops conversions after the current running one is completed and its result stored
  - Ensure correct suspend configuration to avoid system damage
- Suspend configuration can be performed in the user initialization code after reset

Debug system
Peripheral suspend support (2/2)

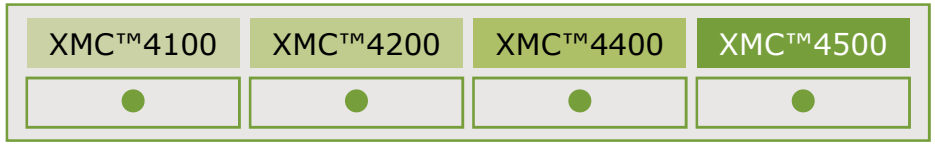
Peripheral suspend support					
Peripheral	Supported	Default mode	Hard suspend	Soft suspend	Suspend reset
RTC	No	-	-	-	-
WDT	Yes	Active	Yes	No	System reset
LEDTS	Yes	Not active	Yes	No	Debug reset
SDMMC	No	-	-	-	-
EBU	No	-	-	-	-
ETH	No	-	-	-	-
USB	No	-	-	-	-
USIC	Yes	Not active	No	Yes	Debug reset
MultiCAN	Yes	Not active	Yes	Yes	Debug reset
VADC	Yes	Not active	Yes	Yes	Debug reset
DSD	Yes	Not active	Yes	Yes	Debug reset
DAC	No	-	-	-	-
CCU4	Yes	Not active	Yes	Yes	System reset
CCU8	Yes	Not active	Yes	Yes	System reset
POSIF	Yes	Not active	Yes	Yes	System reset

Debug system
System integration



Debug system based on events

- Synchronous events
  - BKPT instruction execution
  - Match in Breakpoint Unit
  - Vector catch
  - Step debug events
- Asynchronous events
  - Watchpoint (including PC match)
  - Halt request
  - External Signal based request



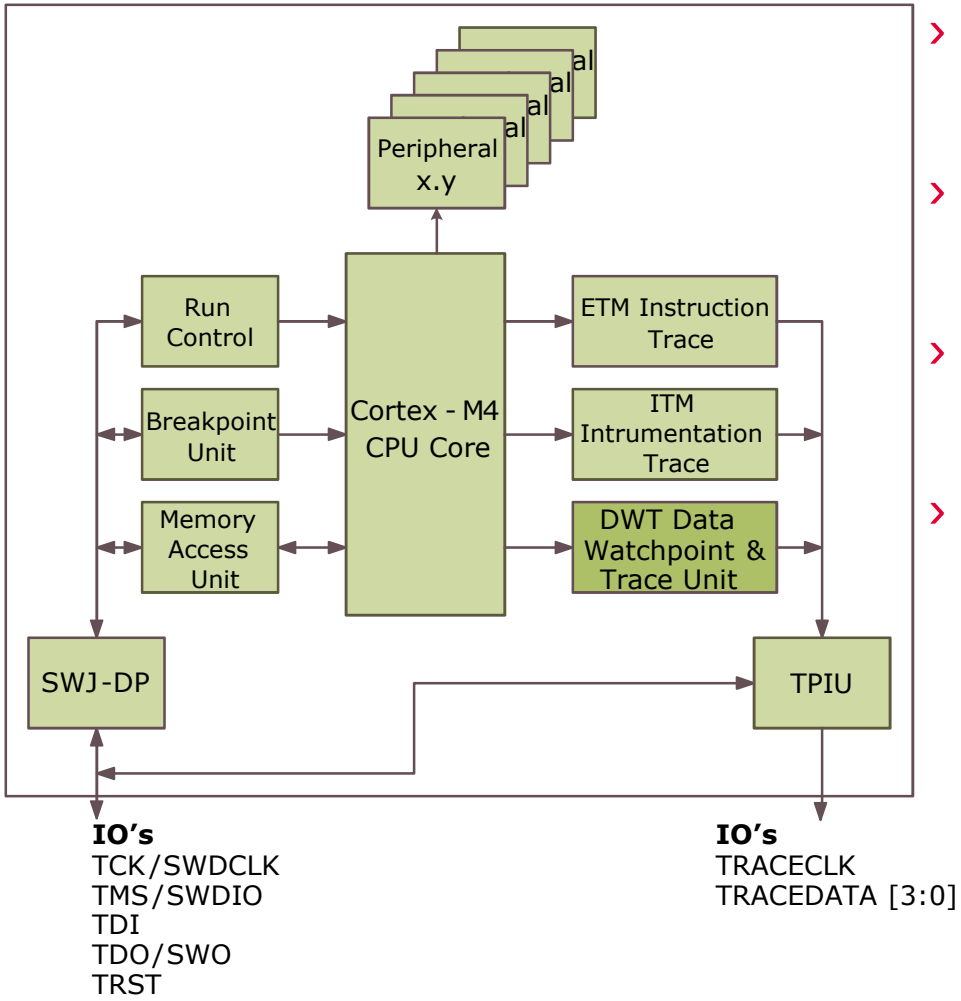
XMC™4000 product family provides debug and trace capability using ARM M4 Debug port JTAG or SWD

- JTAG Port – 5 interface, signal test Clock, test mode select, data in, data out and reset. Reset pin not available for low pin package.
- SWD Port – 2 interface, signal Clock and bidirectional data. Instrumentation trace provided via 3rd pin

TRST/TCK/TMS pin pull settings:

- TRST: Internal pull-down
- TMS/SWDIO: Internal pull-up
- TCK/SWCLK: Internal pull-down

Debug system
Data Watchpoint and Trace (DWT)



- Program Counter (PC) sampling capability
- 4 watch points for address matching
- PC watch points for instruction address matching
- Watch point events result in a processor halt and enters processor system into a debug state

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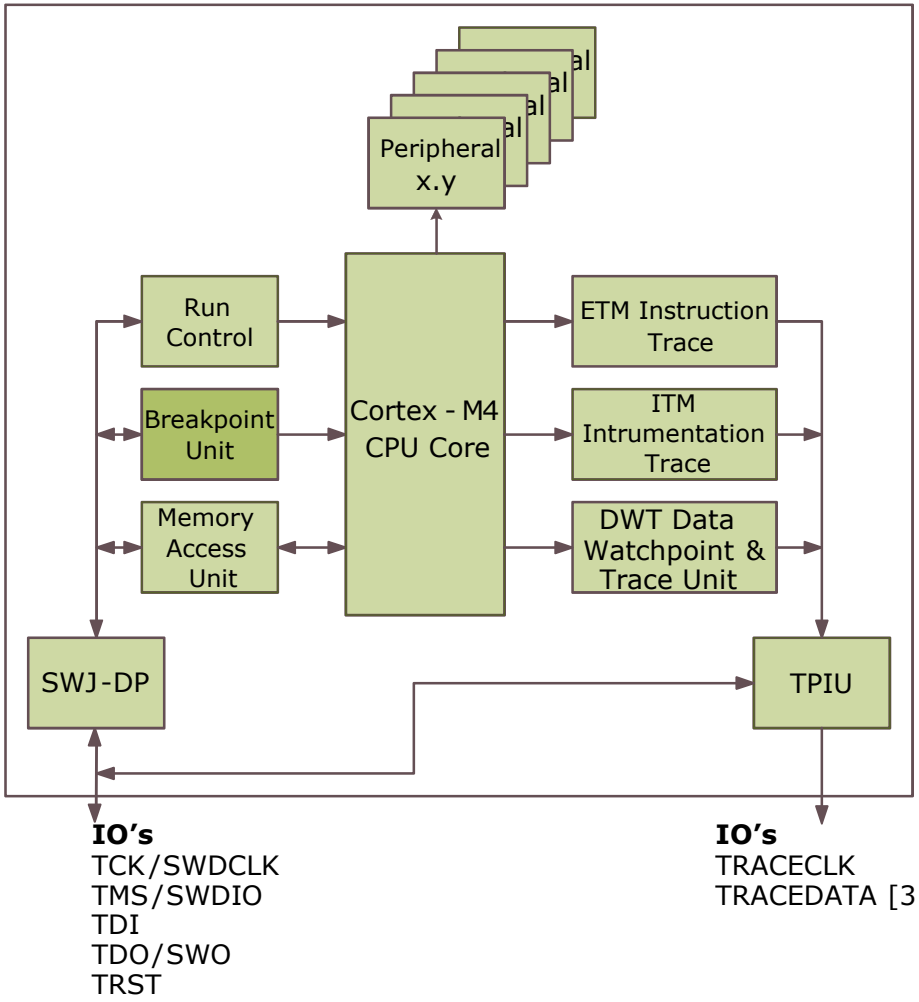
Debug system
Breakpoint unit



- Can cause a running system to halt
- Provides 8 hardware and unlimited software breakpoints
- A Breakpoint (BKPT) is caused by execution of a BKPT instruction or a match in Flash Patch and Breakpoint (FPB) unit
- A BKPT is a debug event and causes the processor to enter debug state
- Reason for a debug event: debug halt, BKPT, DWT trap and vector catch

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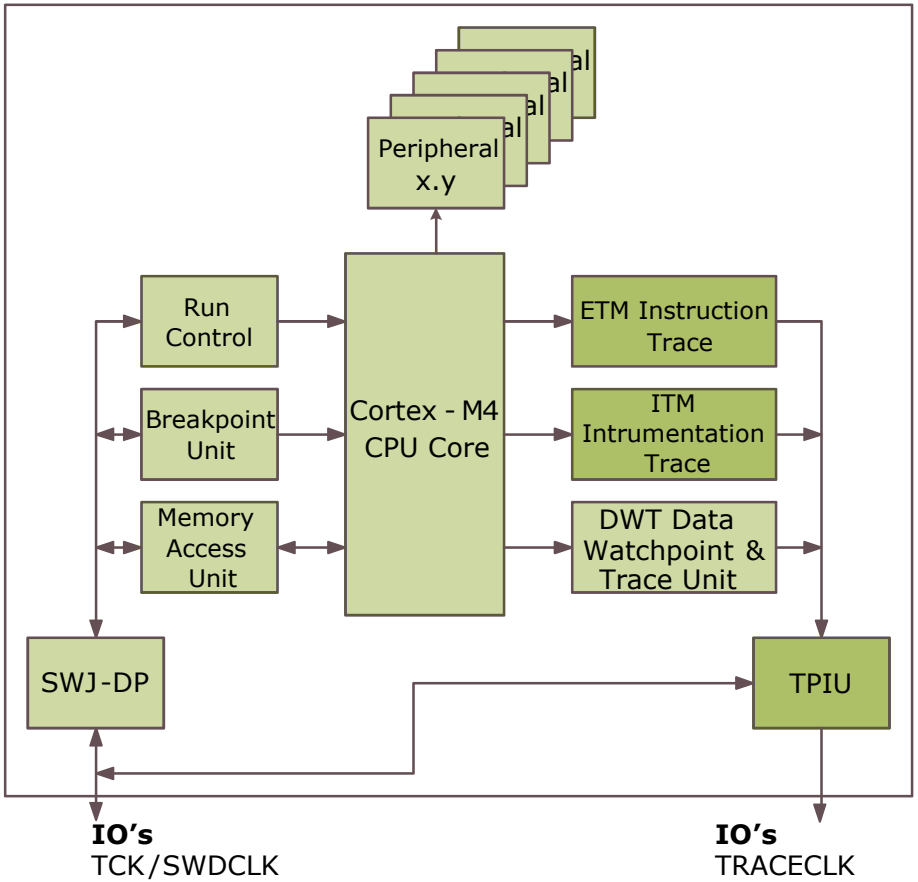
Trace support



- Embedded Trace Macrocell (ETM)
  - Instruction trace capabilities
  - Trigger source: DWT comparators
- Instrumentation Trace Macrocell (ITM)
  - Application driven trace source
  - Print style debugging
  - Supported sources: Software trace, hardware trace, time stamping
- Trace Port Interface Unit (TPIU)
  - Provides trace information from ITM and ETM to debugger
  - Serial wire viewer, 4 trace ports

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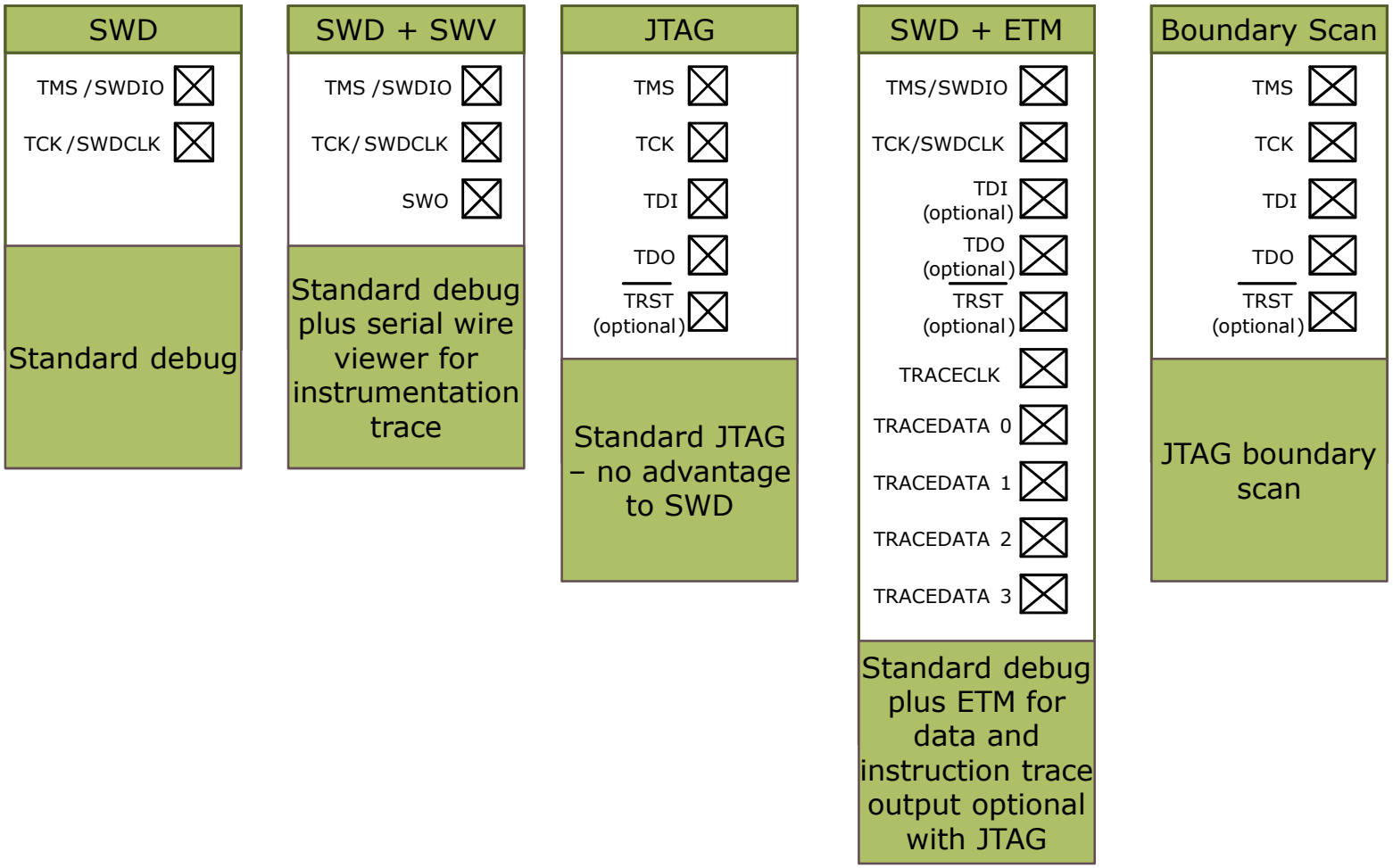

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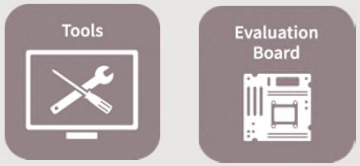
Technical Material 	– Application Notes – Technical Articles – Simulation Models – Datasheets, MCDS Files – PCB Design Data	– www.infineon.com/XMC – Kits and Boards – DAVE™ – Software and Tool Ecosystem
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