DEBUG

Cortex®-M0 Debug system

XMC™ microcontrollers

September 2016

Agenda

1. Debug system – introduction
2. Data Watchpoint and Trace (DWT)
3. Breakpoint Unit (BPU)
4. ROM table
5. Debug tool access
6. Debug connector pins
7. Support material

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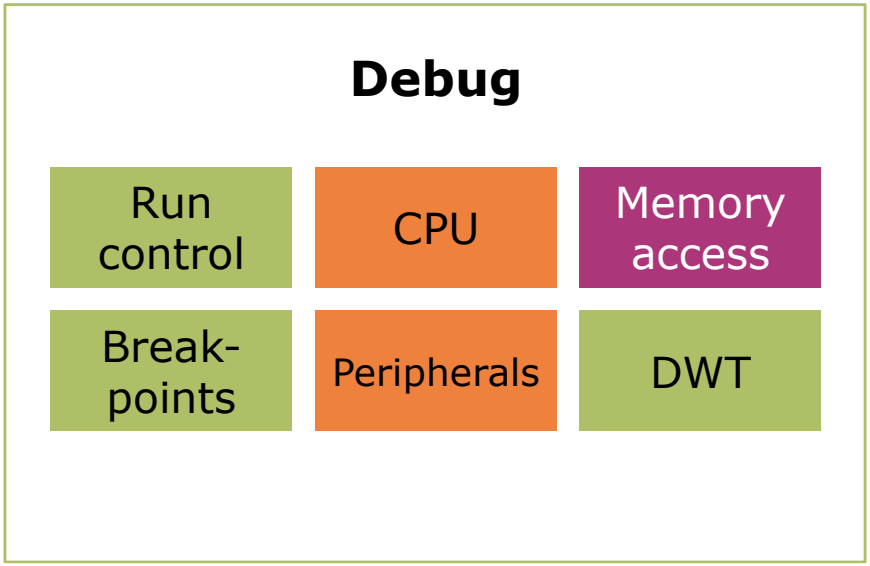
Debug system



Highlights

Cortex®-M0 Debug System includes processor halt, single step, full system memory access, processor core register access, reset and "HardFault" Vector Catch.

4 hardware breakpoints and unlimited software breakpoints. 2 Data watch points for address matching. Two-pin SWD debug and single-pin SPD debug supported. No trace capability.

Key feature

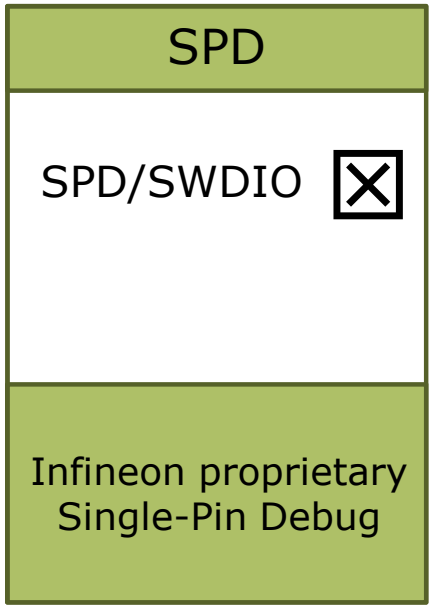
- Single Pin Debug (SPD)
- Halt After Reset (HAR)
- Peripheral suspend support

Customer benefits

- Low pin count debug interface
- Halt CPU before user code starts (at 1st instruction of user code)
- Microcontroller critical state debugging by peripheral suspend on a CPU halt

Debug system
Single-Pin Debug (SPD)

- Infineon proprietary Single-Pin Debug (SPD)
  - Provides debug capability via 1 pin, bidirectional data
  - Two Single-Pin Debug ports SPD_0 and SPD_1 available
  - Selection of Single-Pin Debug ports via Boot Mode Index (BMI)
  - Overlay of Single-Pin debug with Serial Wire Debug Data IO (SWDIO) pin



Debug system
Halt After Reset

- Halt After Reset allows halting of the CPU at the first instruction of user code
- Cold Reset (HAR)
  - Boot Mode Index has to be set to “UMHAR” to allow debug and HAR
  - In UMHAR mode after master reset (includes power on reset) startup software (SSW) waits for a tool to register
  - On successful tool registration CPU halts at first instruction of user code
- Warm Reset
  - Halt After System Reset is based on break point configuration
  - HOT PLUG capability is possible in this mode
- Security features
  - Debug access to CPU/system prevented before and during SSW is executed

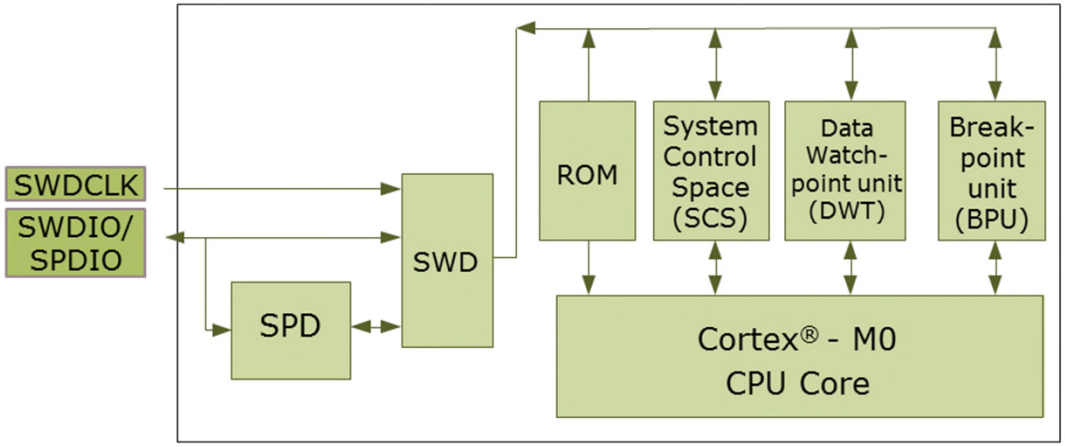
Debug system
Peripheral suspend support (1/2)

- Allows critical system state debugging
  - E.g. Debug watchdog behavior
- Suspend based on breakpoint or by setting the processor halt bit (C_HALT)
- Availability of hard and soft suspend capability
  - Hard suspend: Clock at peripheral gated immediately
  - Soft suspend: Peripheral can decide when to suspend. Usually at the end of the actual active transfer
    - E.g. Versatile Analog-to-Digital Converter (VADC) stops conversions after the current running one is completed and its result stored
  - Ensure correct suspend configuration to avoid system damage
- Suspend configuration can be performed in the user initialization code after reset

Debug system
Peripheral suspend support (2/2)

Peripheral suspend support				
Peripheral	Supported	Default mode	Hard Suspend	Soft Suspend
RTC	Yes	Not active	Yes	No
USIC	Yes	Not active	No	Yes
CCU4	Yes	Not active	Yes	Yes
CCU8	Yes	Not active	Yes	Yes
POSIF	Yes	Not active	Yes	Yes
BCCU	Yes	Not active	Yes	No
WDT	Yes	Active	Yes	No
ADC	Yes	Not active	Yes	Yes
VADC	Yes	Not active	Yes	Yes
LEDTS	Yes	Not active	Yes	No
MATH	Yes	Not active	Yes	Yes
PRNG	No	-	-	-

Debug system
System integration



XMC1100	XMC1200	XMC1300
●	●	●

Debug system based on events

- Synchronous events
  - BKPT instruction execution
  - Match in the BPU (Break Point Unit)
  - Vector catch
  - Step debug events
- Asynchronous events
  - Watchpoint (including PC match)
  - Halt request
  - External signal based request

XMC1000 product family provides debug capability using ARM M0 Debug port SWD or Infineon proprietary SPD

- SWD port - 2 interface, signal clock and bidirectional data)
- SPD port - one Interface signal (SPDIO – bidirectional data, overlay of SWD Interface SWDIO pin)

SWD/SPD pin pull settings:

- SWDIO/SPD: Internal pull-up
- SWCLK: Internal pull-down

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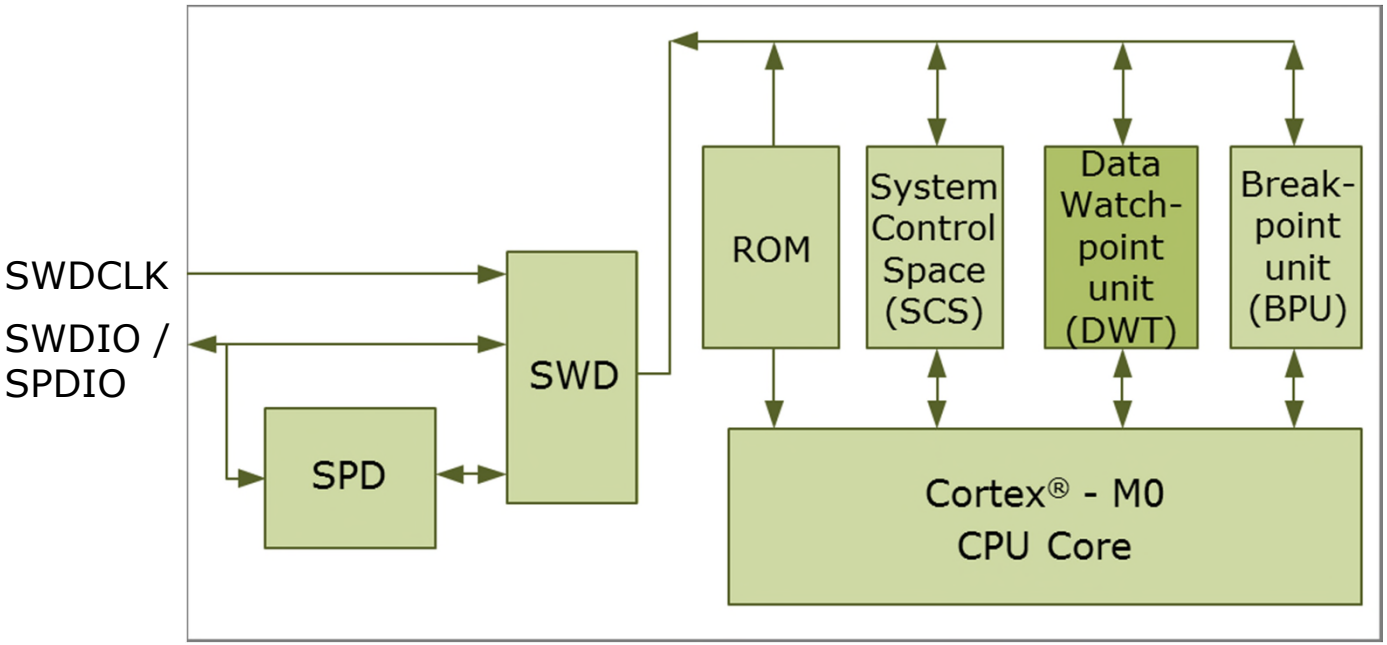
Debug system
Data Watchpoint and Trace (DWT)

- Program Counter (PC) sampling capability
- 2 watchpoints for address matching
- PC watchpoints for instruction address matching
- Watchpoint events result in a processor halt and enters processor system into a debug state.



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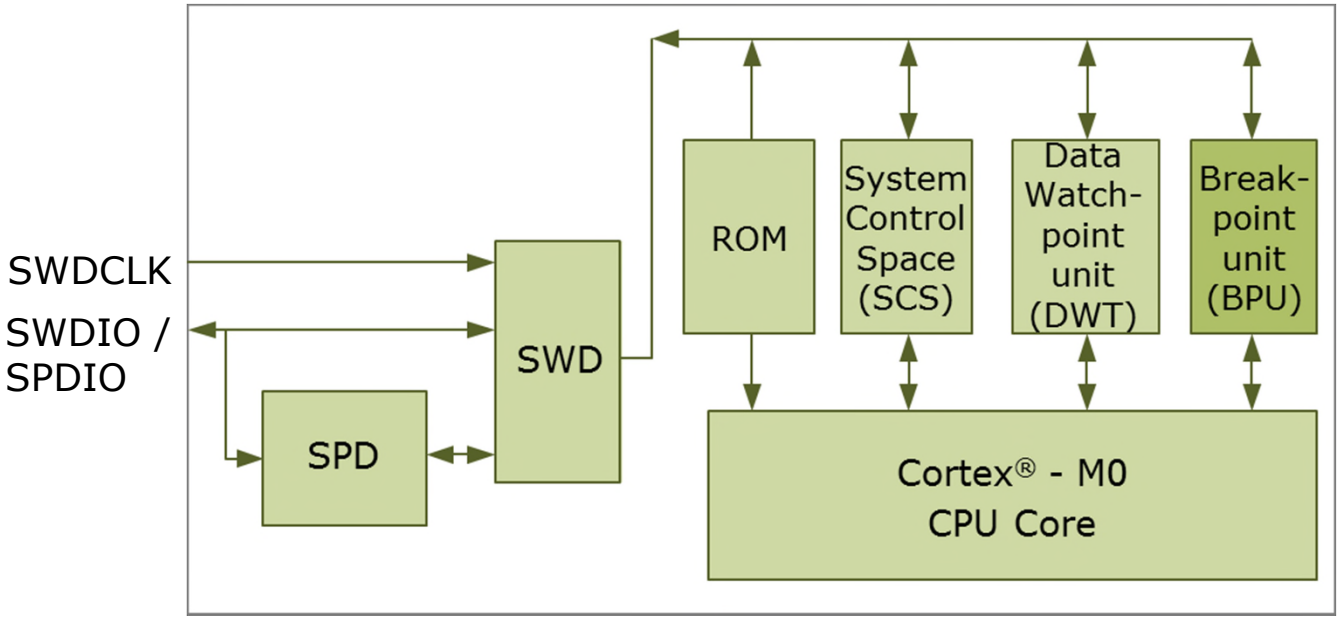
Debug system
Breakpoint Unit (BPU)

- Can cause a running system to halt
- Provides 4 hardware and unlimited software breakpoints
- A Breakpoint (BKPT) is caused by execution of a BKPT instruction or a match in BPU
- A BKPT is a debug event and causes the processor to enter debug state
- Reason for a debug event: debug halt, BKPT, DWT trap and Vector Catch



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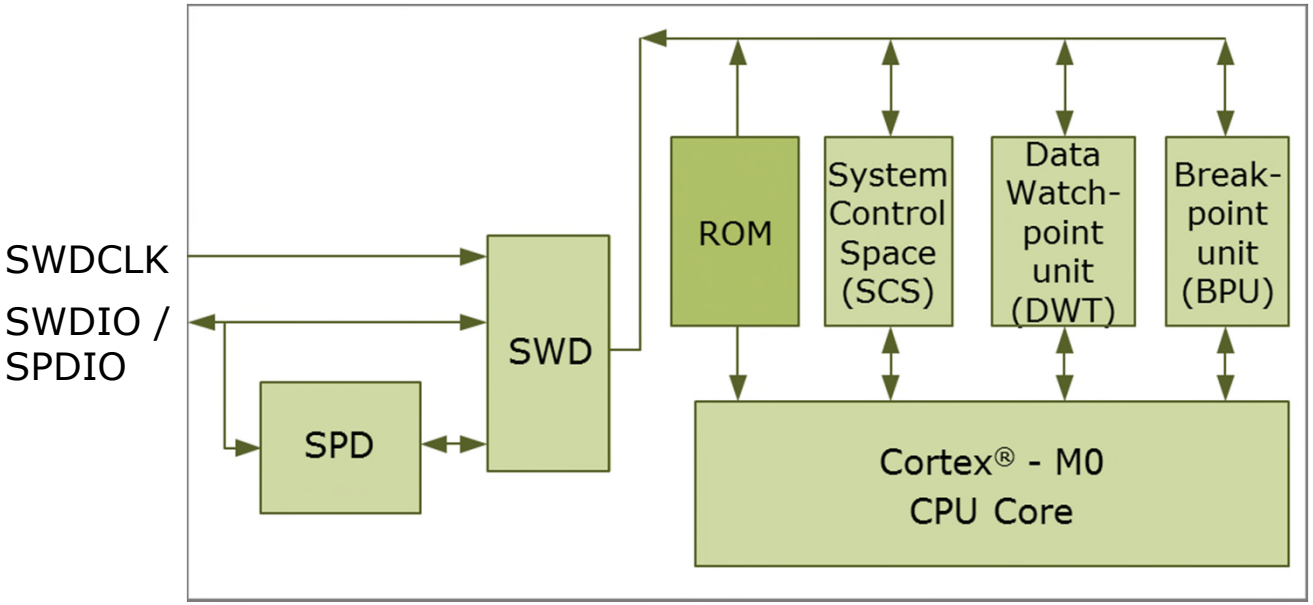
Debug system
ROM table

- ROM table is available to identify Debug System components
  - Infineon part number
  - Manufacturer's identity code (JEDEC JEP106)
  - Revision number
- Access ROM table through DAP interface



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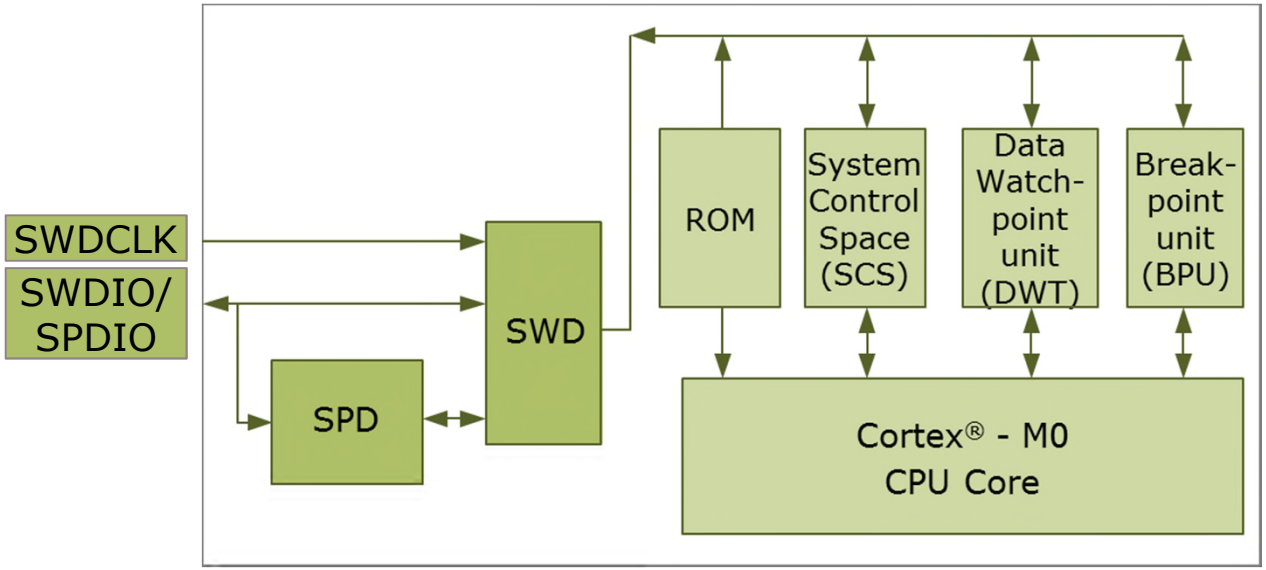
Debug system
Debug tool access

- Tool interface access requires BMI (Boot Mode Index) setting. Two modes to boot in debug mode after reset:
  - **UMD**: User Mode with Debug enabled
  - **UMHAR**: User Mode with Debug enabled Halt After Reset
- Hot-plug capability: prevents unintended transfers
- Availability of two tool access protocol
  - Serial Wire Debug (SWD)
  - Single Pin Debug (SPD)



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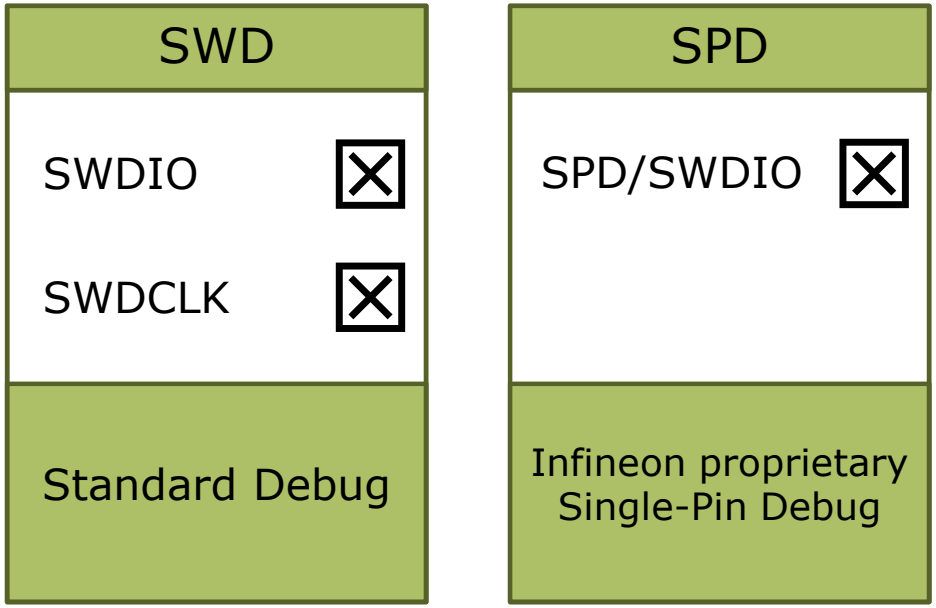

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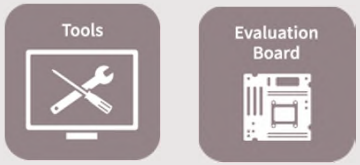
Support material

Collaterals and brochures 	› Product briefs › Selection guides › Application brochures › Presentations › Press releases, ads	› www.infineon.com/XMC
Technical material 	› Application notes › Technical articles › Simulation models › Datasheets, MCDS files › PCB design data	› www.infineon.com/XMC › Kits and Boards › DAVE™ › Software and Tool Ecosystem
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