Solar inverter design

The race to design high-efficiency, high-power-density inverters

Abstract

Due to the ever-increasing demand for a clean and renewable source of energy, installing solar systems has accelerated significantly in the last decade. Contemporary solar applications require highly efficient, power-dense, and lightweight grid-tied inverters.

Traditionally, IGBT has been the device of choice in both three-phase and single-phase (≤10 kW) solar inverter designs while Si superjunction (SJ) MOSFETs (600/650 V) also have been used in some single-phase designs. But both IGBTs and Si SJ MOSFETs have their drawbacks that limit the efficiency and power density of inverters.

Recently, engineers have focused on two different approaches to improve efficiency and power density of single-phase inverters to even higher levels. One is replacing IGBT and Si SJ MOSFETs with wide-bandgap devices like SiC MOSFETs. The other one is replacing traditional topologies (H4, H5, H6, etc.) with multilevel topologies using lower voltage silicon MOSFETs.

As we discuss in this paper, using these two approaches efficiency up to 99 percent is achievable, and very high power density inverters can be designed.

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1 Replacing IGBTs and Si SJ MOSFETs with SiC MOSFETs

IGBTs suffer from high switching losses that limit their utilization to only frequencies less than 20 kHz; while high \( Q_{rr} \), slow body diode, and relatively high \( R_{DS(on)} \) confine the usage of SJ MOSFETs in inverter applications. These constraints result in the limited efficiency and power density of conventional single-phase solar inverters to around 98 percent and below.

Different from the previously mentioned technologies, SiC MOSFETs offer very fast parallel diodes, very low \( Q_{rr} \), and switching losses much lower than IGBTs. Recently, Infineon has introduced its silicon carbide CoolSiC™ MOSFETs 650 V that can directly replace IGBTs and Si SJ MOSFETs with no need for change in the inverter topology. SiC MOSFETs enable switching at a higher frequency, which means a significantly smaller magnetic-, capacitor filter-, and enclosure size. As the power level goes up, the reduction in size and weight results in cost savings.

By replacing a Si SJ MOSFET with a SiC MOSFET, switching loss decreases significantly. Performances under the same measurement conditions are captured in Figure 1. In terms of drain-source charge (\( Q_{oss} \)), recovery charge (\( Q_{rr} \)) and gate charge (\( Q_g \)), SiC MOSFETs (i.e., CoolSiC™ MOSFET 650 V) have superior figures-of-merit compared the best alternative Si SJ MOSFET (i.e., 600 V CoolMOS™ CFD7) alternative.

![Figure 1](image-url)  
*Figure 1  Comparison of figures-of-merit between SiC and SJ MOSFETs*

Figure 2 shows the conduction loss comparison of three best-in-class devices, including the TRENCHSTOP™ 5 IGBT IKW30N65H5 (650 V), the 600 V CoolMOS™ CFD7 Si SJ MOSFET IPW60R031CFD7 (600 V) and the CoolSiC™ MOSFET 650 V SiC MOSFET IMW65R027M1H (650 V) at a junction temperature of 25°C. Figure 3 displays how conduction losses change over varying currents at 125°C.

As apparent from Figure 3:
- the conduction losses of IGBTs are significantly higher than of the other devices at 25 °C; however, it doesn’t rise significantly as temperature increases to 125 °C
- the conduction loss of the SJ MOSFET at 125°C is two times higher than at 25°C for the same device
- the SiC MOSFET shows only approximately 20 percent conduction loss increase over the 25°C-125°C temperature range which makes a clear difference between Si and SiC MOSFET technologies, especially at high current, high-temperature operating conditions.
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Figure 2 Conduction losses at 25°C

Figure 3 Conduction losses at 125°C
2 Switching to multilevel topologies

Traditionally, topologies based on IGBTs and SJ MOSFETs such as H4, H5, H6, etc. have been widely utilized in single-phase solar inverter applications. Recently, one novel approach has gained more attention that enables higher efficiency and power density: the multilevel topology (an example is shown in Figure 4) based on medium-voltage MOSFETs (60 V to 300 V). Infineon’s OptiMOS™ 5 product family of medium-voltage MOSFETs have excellent figures-of-merit (extremely low $R_{DS(on)} \times Q_g$, $R_{DS(on)} \times Q_{rr}$, and $R_{DS(on)} \times Q_{oss}$) and enable very high-efficiency (up to 99 percent) and power-density designs, when used in multilevel inverters.

![Figure 4](https://www.infineon.com/energy-storage-systems)

**Figure 4** Replacing a two-level conventional topology with a multilevel topology

Compared to the conventional design, the multilevel scheme allows for a significant reduction in the inductor- and capacitor filter sizes. This, along with the need for a smaller cooling system, leads to a much lighter design with a smaller enclosure. On the other hand, due to the lower voltage rating of MV MOSFETs, more MOSFETs are used in a multilevel design compared to conventional topologies. This also means that the generated heat due to the power loss in the multilevel inverter (which is less than in a conventional design) is distributed among more devices. As a result, the thermal management of the multilevel inverter is more efficient, which paves the way for heatsink-free and fanless designs.

In a typical single-phase string inverter (power ≥ 3 kW), semiconductors commonly cost less than 10 percent of the overall bill of material (BOM). However, cooling systems, magnetics, and filter capacitors cost around 30 to 40 percent of the total BOM. On the other hand, while prices of semiconductor devices are continuously dropping, the cost of other components such as magnetic and heatsinks remain unchanged. That means for single-phase solar inverters with a full power capability of more than 3 kW, where the cost of mechanical components is a significant portion of the design, using multilevel inverter contributes to production cost saving. As the power rating of power inverters increases, the cost share of mechanical parts (e.g., heatsink and filter size) increases in relation to the semiconductor devices’ portion. For this reason, multilevel inverters are even more beneficial as the power range increases.

One other significant advantage of multilevel inverters is that lower loss per MOSFET allows using SMD packages. Utilizing SMD packages helps with assembly cost saving by applying automated pick and place process. In addition, the reduced package inductances improve the switching performance at higher frequencies.

Scalability is another significant advantage of multilevel inverters. A multilevel inverter can be easily scaled to higher power design with almost the same design and PCB layout.
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But to mention, multilevel inverters face one big challenge too. Compared to conventional topologies, there is a need for a higher number of gate drivers and isolated power supplies to power them up. This challenge is tackled by using very cost-effective, low-power Eight-output Flyback power supplies (≤ 1 W).

### 2.1 A 4 kW heatsink-free, fanless, medium-voltage MOSFET-based multilevel inverter

In this section, we introduce a 4 kW, five-level single-phase flying-capacitor-based active neutral point clamped multilevel inverter demonstration board. This fanless, heatsink-free design offers more than 99 percent peak efficiency and full power efficiency as of 98.7 percent.

Figure 5 shows the schematic of the multilevel inverter demonstration board, while Table 1 lists the specification of this inverter. Given that this is a five-level inverter, 9.3 mΩ OptiMOS™ 5 150 V (BSC093N15NS5) MOSFETs were used despite the 400 V<sub>DC</sub> bus voltage. This device has much better figures-of-merit (orders of magnitude) compared to IGBTs and SJ MOSFETs.

![Multilevel inverter schematic](image)

Figure 5 Schematic of a single-phase, flying-capacitor-based active neutral point clamped five-level multilevel inverter

<table>
<thead>
<tr>
<th>Table 1</th>
<th>Multilevel inverter specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input DC voltage (V&lt;sub&gt;DC&lt;/sub&gt;), load</strong></td>
<td>400 V, passive RL load</td>
</tr>
<tr>
<td>Switch type</td>
<td>2×BSC093N15NS5 (150 V/9.3 mΩ), overall 48 MOSFETs, gate driver: 12×2EDF7275F</td>
</tr>
<tr>
<td>The effective output switching frequency</td>
<td>40 kHz</td>
</tr>
<tr>
<td>DC relay switch (DRS)</td>
<td>2×IPT60R022S7</td>
</tr>
<tr>
<td>Max. continuous power</td>
<td>4000 VA</td>
</tr>
</tbody>
</table>

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Figure 6 shows the multilevel inverter demonstration board with the 48 pieces of the BSC093N15NS5 power MOSFETs on it. Also, there are three gate-driver circuitry daughter boards with identical design connected to the mainboard. As can be seen, the output filter inductor and capacitors are noticeably small for a 4 kW power range single-phase inverter.

![The multilevel inverter demonstration board from Infineon](image)

Figures 7 and 8 show the output waveforms at full power (4 kW, 40 kHz). As seen, $V_{ab}$ (which is phase-to-phase output voltage) has five levels as expected. The load voltage (which is $V_{ab}$ after filtering) and the load current also can be captured in the graph.

![Output voltage $V_{out}$, load current $I_{out}$, phase-to-phase voltage $V_{ab}$ at 4 kW, 40 kHz](image)
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Figure 8 Filter inductor current $I_L$, load current $I_{out}$, flying capacitors voltages at 4 kW, 40 kHz

Figure 9 shows the heat map of the demonstration board after two hours of runtime (thermal steady-state) at full power. The heat map shows that despite the heatsink-free/fanless design, the components on the board show overall moderate temperatures. In fact, the maximum temperature (that is below 85 °C) on the board emitted by the MOSFETs in the middle.

Figure 9 Board heat map (4 kVA, 2 hours of runtime, no fan, no heatsink, open frame, at 25 °C of ambient temperature)

Figure 10 shows the efficiency of the demonstration board in relation to the output power. The maximum efficiency is achieved at around 2 kW (~ 99.1 percent). At full load (4 kW), the efficiency is still very high, at around 98.7 percent, which explains why this multilevel inverter can work continuously without the need for any heatsink or fan.
2.2 Eight-outputs flyback-based power supply for isolated gate-driver ICs

As was shown earlier, one challenge regarding designing this multilevel inverter is the need for twenty-four isolated power supplies to power up the isolated gate drivers. A cost-effective simple flyback-based power supply (<1 W) with eight outputs is used to power four dual-channel isolated gate drivers. This eight-outputs power supply is incorporated with four isolated EiceDRIVER™ 2EDF7275F gate drivers on one single daughterboard and the full system solution requires three of these daughter boards. Figure 11 shows the basic schematic of the eight outputs auxiliary power supply. A planar reduces design complexity, hence contributes to reduced costs and simplified manufacturability.

Figure 11 Flyback-based <1 W power supply with eight-outputs on a gate-driver board
3 Summary

Now the question for an inverter designer who is looking for higher efficiency and power density is which one of the above-described solutions to choose. Replacing IGBTs and SJ MOSFETs with SiC MOSFETs or replacing the conventional with the multilevel topology? Beyond question, replacing silicon-based devices with SiC MOSFETs requires less effort compared to altering the topology. Although this change to SiC increases efficiency and power density, still not as much as the multilevel solution. A heatsink is still needed, and for a higher power range (> 5 kW), forced cooling probably should also be considered.

Even though the multilevel topology is more complex than conventional topologies if a designer has previous experience with this type of topology or willing to learn and invest R&D effort into it, moving to the multilevel inverter is recommended. It enables 99 percent efficiency and very high power density.
References