Advanced gate drive options for silicon carbide (SiC) MOSFETs using EiceDRIVER™

About this document

Scope and purpose

This application note discusses the basic parameters of silicon carbide (SiC) MOSFETs and derives gate drive requirements. The document covers the following EiceDRIVER™ isolated and level-shift gate driver ICs:

- EiceDRIVER™ Compact isolated gate driver:
  - 1ED3122MC12H, 1ED3124MC12H, 1ED3124MU12F, 1ED3127MU12F, 1ED3142MU12F, 1ED3241MC12H, 1ED3251MC12H
- EiceDRIVER™ Enhanced isolated gate driver:
  - 1ED3321MC12N, 1ED3491MC12M, 1ED3890MC12M
- EiceDRIVER™ silicon-on-insulator (SOI) level-shift gate driver:
  - 2ED1323S12P

These gate driver IC families provide galvanic isolation based on a coreless transformer, or junction isolation based on silicon-on-insulator. Power transistors rated up to 2300 V with ultrafast switching capability can be handled optimally through these gate drivers. Therefore, this document concentrates mainly on suitable level-shift (1200 V) and galvanically isolated gate driver ICs (2300 V).

Please note that Infineon's advanced CoolSiC™ Trench MOSFET technology offers various benefits that reduce the complexity of gate driving. These benefits are mentioned in detail in this document. Also refer to other application notes that highlight the properties of CoolSiC™.

Note: This document does not refer to the SiC bipolar transistors or the SiC JFETs.

Intended audience

The intended audiences for this document are design engineers, technicians, and developers of electronic systems.

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1 Overview

For each gate driver, the functionalities required for driving a SiC MOSFET are listed in Table 1. The most important parameters are:

- Tight propagation delay matching
- Precise input filters
- Wide output side supply range
- Negative gate voltage capability
- Extended common mode transient immunity (CMTI) capability
- Active Miller clamp
- Fast desaturation (DESAT) protection

Table 1 Gate driver functionalities important for SiC MOSFETs

Function/property	X3 Compact family					F3 family	2L-SRC family		X3 Analog/ X3 Digital family		Level-shift SOI family
	1ED3122MC12H	1ED3124MC12H	1ED3124MU12F	1ED3127MU12F	1ED3142MU12F	1ED3321MC12N	1ED3241MC12H	1ED3251MC12H	1ED3491MC12M	1ED3890MC12M	2ED1323S12P
Propagation delay matching < 15 ns	✓	✓	✓	✓	✓	✓	✓	✓	–	–	–
Precise input filters < 150 ns	✓	✓	✓	✓	✓	✓	–	–	–	–	✓
Wide output supply range	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Negative gate voltage	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	–
Extended CMTI (> 200 kV/µs)	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	N.A.
Fast DESAT	–	–	–	–	–	✓	–	–	✓	✓	–
Fast OCP	–	–	–	–	–	–	–	–	–	–	✓
Slew rate control	–	–	–	–	–	–	✓	✓	–	–	–
$UVLO_{ON}$ ≥ 12 V	–	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
Active Miller clamp	✓	–	–	✓	–	✓	–	✓	✓	✓	✓
Separate output source and sink	–	✓	✓	–	✓	✓	–	–	✓	✓	–
Best use for	**Best price performance ratio, Miller clamp/negative gate voltage**					**Fast DESAT**	**Slew rate control**		**Configurable parameters and condition monitoring**		**Half-bridge**

1 Overview

Most popular power converter topologies used in industrial applications consist of power transistors connected in a half-bridge configuration. For such a configuration, the most simple and cost-effective choice is the EiceDRIVER™ X3 Compact (1ED31xx) or the SOI gate driver (2ED1323S12P) with 2-channel output. If no short circuit protection is required from the gate driver, EiceDRIVER™ X3 Compact (1ED31xx) in both DSO-8 150 mil and 300 mil are the most suitable for driving the SiC MOSFETs. However, when fast short circuit protection is required, EiceDRIVER™ Enhanced 1ED3321MC12N, 1ED3491MC12M, 1ED3890MC12M, and2ED1323S12P fit best. 1ED3491MC12M and 1ED3890MC12M belong to the X3 family and offer advanced functionalities that enable high level of configurability and parameter monitoring. This in turn enables flexible design and condition monitoring.

Single-transistor converter topologies, such as boost, buck, forward, or flyback, that use CoolSiC™ MOSFETs might benefit the most from parts that have separate source and sink output configurations.

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2.1 Synchronous rectification

When operating inductive loads such as motors in pulse-width modulation (PWM) mode, half-bridge configurations need a freewheeling path during the dead time and the off-state interval of the switch. The freewheeling path is automatically provided by the SiC MOSFET body diode. It is a good practice to support the body diode's forward operation by turning on the transistor part of the MOSFET, where the MOSFET's channel operates in the reverse direction. This kind of half-bridge control opens a path parallel to the body diode through the MOSFET channel. This is called synchronous rectification.

The advantage of this mode of operation is that the voltage drop of the channel is much lower than the forward voltage of the body diode. This reduces the voltage drop from the freewheeling current to a large extent, thereby reducing the conduction losses in the MOSFET. This operation mode is important for SiC MOSFETs because the forward voltage of the body diode is relatively high, as can be seen in Figure 1. To achieve high system efficiency, it is mandatory to avoid, as much as possible, a mode in which only the diode conducts.

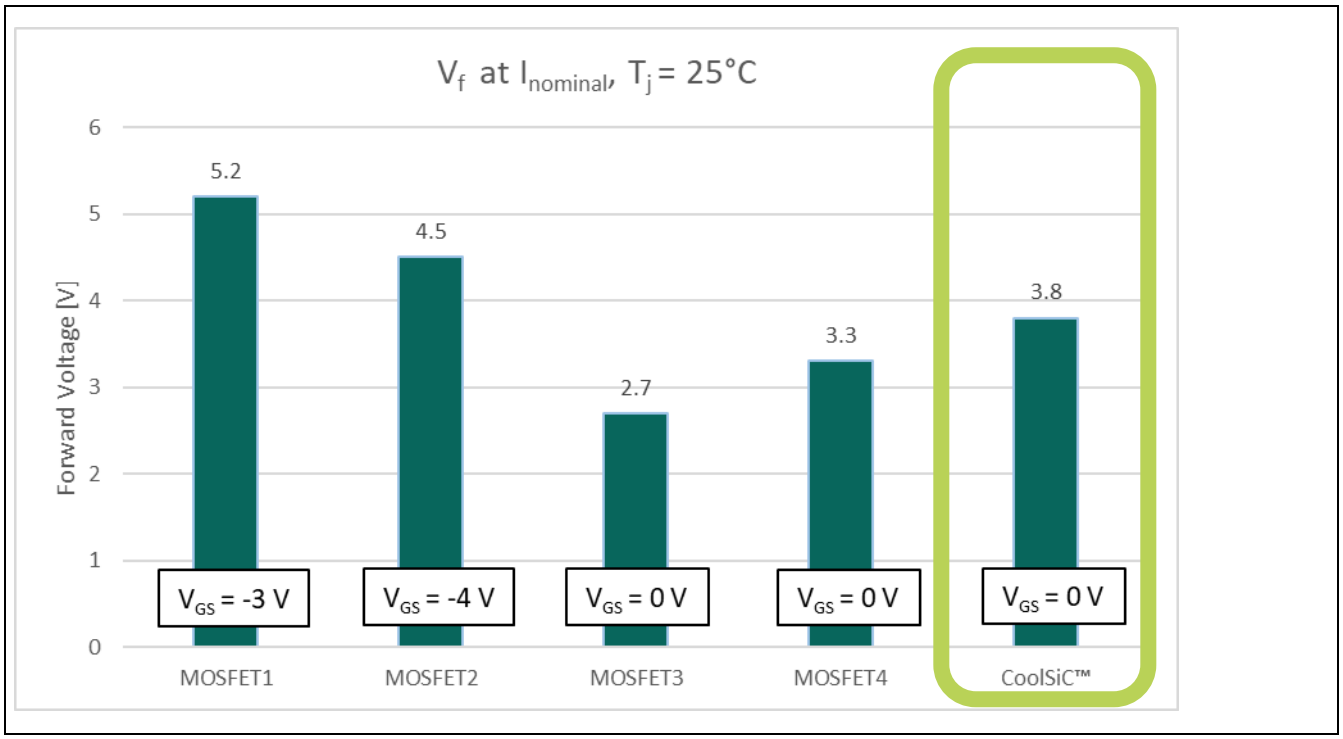

Figure 1 Forward voltage of the SiC MOSFET body diode at lowest gate voltage conditions

2.2 Enable short dead time for higher efficiency

In half-bridge topologies, the dead time inhibits shoot-through and cross-conduction. It is an important safety feature in any half-bridge application. However, long dead times can lead to low efficiency. During dead time, the current conducts only through the body diode or output power limitation because no energy is converted into load during the dead time. Achieving as short a dead time as possible without shoot-through is essential for high-performing power applications. The most important parameters of a gate driver to help achieve this goal are precise propagation delay matching and precise integrated filters. These are explained in the following sections.

2.2.1 Precise propagation delay matching

The gate driver parameters for calculating dead time are propagation delay and rise and fall time. As the rise and fall time are mostly insignificant (in single digit nanoseconds range), they are not generally considered. It is, however, different in the case of propagation delay of the control signal from the input to the output of the driver. The difference in propagation delay between any two components, under the same conditions, is called propagation delay matching. To reduce dead time, tight propagation delay matching of the gate driver is mandatory.

The datasheet specifications of EiceDRIVER™ isolated gate drivers include parameter variations over temperature and lifetime. This means that the datasheets consider the worst-case scenario. In real-world operating conditions, propagation delay matching is, typically, much smaller than the maximum value specified in the datasheet.

The EiceDRIVER™ gate drivers listed in Table 2 have extremely tight propagation delay matching. They enable high efficiency by reducing the required dead time.

Table 2 Maximum propagation delay matching

Gate driver	Maximum part-to-part propagation delay
EiceDRIVER™ X3 Compact (1ED31xx)	7 ns
EiceDRIVER™ F3 (1ED332x)	15 ns
EiceDRIVER™ 2L-SRC Compact (1ED32xx)	15 ns
EiceDRIVER™ X3 Analog/Digital (1ED34/38xx)	30 ns

It is important to know that individual combinations of a SiC MOSFET and gate driver must be evaluated carefully for properly dimensioning the dead time. Turn-on and turn-off propagation delays of the power transistor very often differ much more over the operating conditions (e.g., the gate voltage range, drain-source voltage V_{ds}, junction temperature T_{vj}, or gate resistance) than over the propagation delay of the gate driver. The parameters of the SiC MOSFET can, thus, dominate the dead time calculation.

2.2.2 Precise integrated filters

Filtering of input control signals is a state-of-the-art method to avoid false triggering caused by electrical noise. Two ways of filtering are often used in power electronics:

- RC filters at input terminals
- Combination of a short-time RC filter and a precise integrated filter in the gate driver itself

An external RC filter helps ensure that the voltages on the gate driver IC's input pins stay within the absolute maximum voltage ratings. These ratings are usually specified for a negative voltage of only -0.3 V. There is a high risk that any coupling might violate this rating if an RC filter is not used. The capacitive portion of the filter keeps the voltage within the operating range, while the resistive portion limits the coupled currents that stress the IC pins. Therefore, the best way to design an RC filter is to have a short filter time constant (in the range of a few nanoseconds) and the capacitor close to the IC's terminals. The IC itself should filter larger disturbances.

The two filtering methods are investigated here in a case study. The first method suffers from a relatively flat branch of the RC charging curve as shown in the Figure 2 (a). The component tolerances of the filter resistor and filter capacitor have a big influence on the filter time. The graph shows the influence of component

tolerances on the filter time tolerance. It can be seen that the minimum to maximum spread, t_{max} to t_{min} is not symmetrical with respect to the target value, t_{trig}.

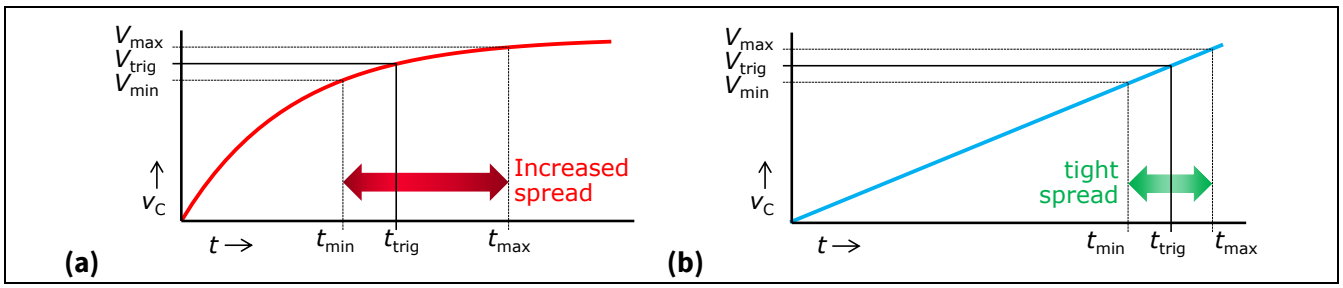

Figure 2 Filter topologies (a) RC filter (b) Integrated filter with a short-time RC filter

The Figure 2 (b) shows the time behavior of an RC filter with a short filter time combined with a dominant integrated filter. The spread of filter time against the target value is rather symmetric here and tighter than that with only a single RC filter. Therefore, the solution with an integrated filter is superior to the solution.

2.3 Negative gate voltage

Figure 3 gives an overview of the gate-source threshold voltage, $V_{GS(th)}$, of a few selected SiC MOSFETs in the market. It can be seen that Infineon's CoolSiC™ technology offers the highest gate-source threshold voltage levels. The advantage of the high gate-source threshold voltage level is that it can enable CoolSiC™ MOSFETs to operate with only unipolar gate voltages. Examples and conditions for operating in that mode are explained in Chapter 4.

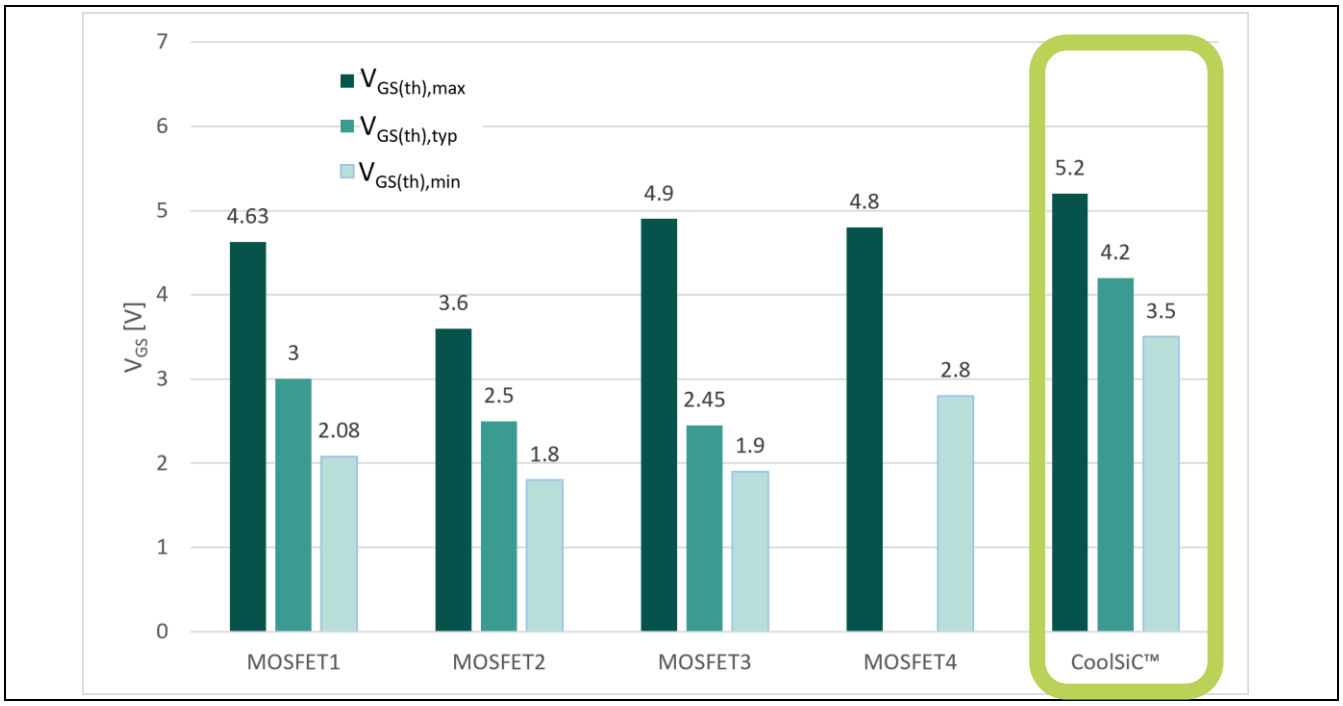

Figure 3 Gate-source threshold voltage range of SiC MOSFET devices

The minimum $V_{GS(th)}$ of SiC MOSFET devices from other manufacturers can be lower than 2 V at 25°C in some cases. There, even a minor ground bouncing can lead to a false and uncontrolled turn-on of the MOSFET at 0 V OFF state voltage. This situation gets more critical if the negative temperature drift of the gate-source voltage

threshold is taken into account. A negative turn-off gate voltage can improve this situation and keep the MOSFET in an OFF state even in noisy environments. The level of the negative gate voltage depends on the gate-source threshold voltage, the ratio of the gate-to-drain capacitance, and the gate-to-source capacitance of the MOSFET.

Thus, driver ICs for SiC MOSFETs should, preferably, have the capability of operating with negative gate voltage to provide a safe and stable OFF state condition for the SiC MOSFET.

As long as the absolute maximum ratings of the IC are not exceeded, any EiceDRIVER™ isolated and level-shift gate driver IC can be used to drive the SiC MOSFETs. Nevertheless, using driver ICs capable of working with negative gate voltages is recommended. Table 3 shows the maximum ratings of EiceDRIVER™ isolated and level-shift gate driver ICs for the maximum output supply voltage range V_{VCC2} - V_{VEE2}, V_{VCC2} - V_{GND2}, and V_{VCC} - V_{COM} respectively.

Sample circuits for using gate drivers with bipolar supply voltage are shown in Figure 4. Figure 4 (a) represents an implementation in case the EiceDRIVER™ isolated gate driver IC does not provide specific terminals for negative gate-source voltage, such as the X3 Compact (1ED31xx) devices. Figure 4 (b) depicts the gate drive circuit of a driver IC with dedicated terminals for negative gate voltage, such as F3 (1ED332x) devices.

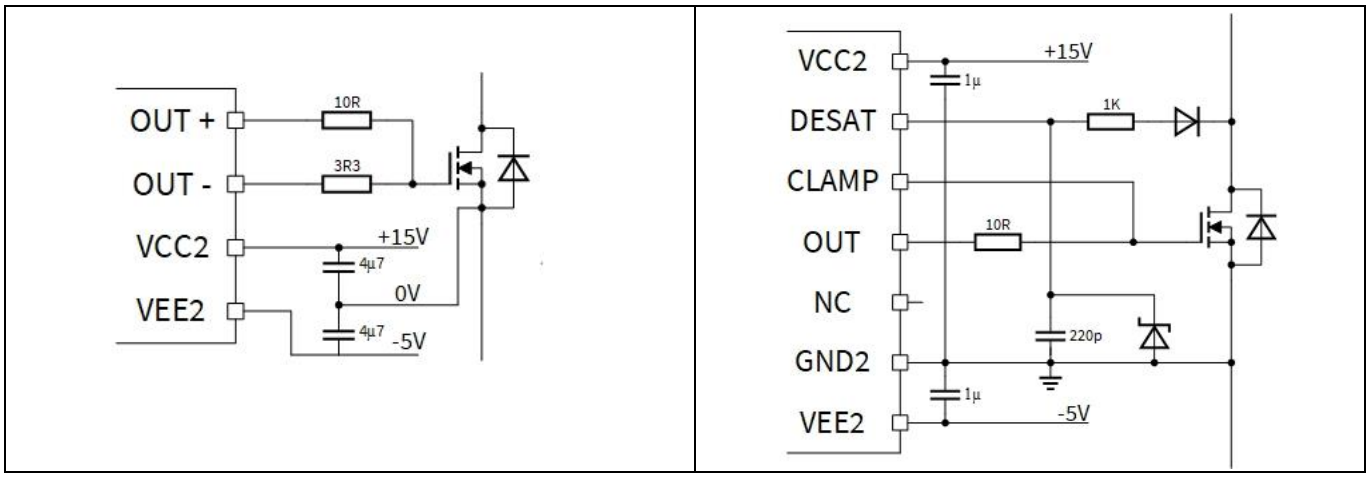

Figure 4 Sample schematics for using negative gate voltage (a) EiceDRIVER™ with a virtual reference point, (b) EiceDRIVER™ with negative gate voltage capability

The output side voltages of the gate driver can be generated easily with an isolated switched mode power supply (SMPS). The power supply for the high side can also be generated through bootstrapping when only a unipolar voltage is used for the gate drive. However, realizing a bipolar voltage for the gate drive normally requires an SMPS. The principles of such SMPS are discussed in [1] and [3]. However, those examples are designed for gate voltage ranges suitable for IGBTs and thus, cannot be used directly for SiC MOSFETs. It should be noted that considerable displacement currents can flow through the parasitic coupling capacitances of such SMPS transformers. Such currents can have a negative influence on the application's sensing functions. 2ED1323S12P cannot operate with a negative voltage. However, it can drive SiC MOSFETs even when only a unipolar voltage is used while reducing pinout complexity (the VEE2 pin is not required). When using unipolar voltage to drive SiC MOSFETs, using the active Miller clamp from the gate driver is highly recommended.

2.4 Wide range of gate voltages

The positive gate-source voltage defines the ON state $R_{DS(on)}$ of the SiC MOSFET. As Figure 5 shows, Infineon's CoolSiC™ MOSFETs achieve their nominal ON state $R_{DS(on)}$ at a gate voltage of 15 V. This is a big advantage in

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numerous applications, because no changes need to be made in the positive gate voltage supply design unlike in the case of IGBTs or even conventional silicon MOSFETs.

Other SiC MOSFETs that were reviewed required a relatively high gate voltage, compared to even IGBTs or conventional silicon MOSFETs. A lower gate voltage level is of course possible, but it results in an increase in the steady-state channel resistivity and, therefore, in higher conduction losses. Figure 5 shows the absolute maximum ratings of the gate-source voltage, V_{GS}, of the selected SiC MOSFETs. The orange bars represent negative gate-source voltage and the green bars represent positive gate-source voltage. The bars in lighter shade depict the recommended gate-source voltage levels as per each device's datasheet. A gate driver IC has to cover the entire range of positive and the negative gate voltages for optimized operation of the SiC MOSFET.

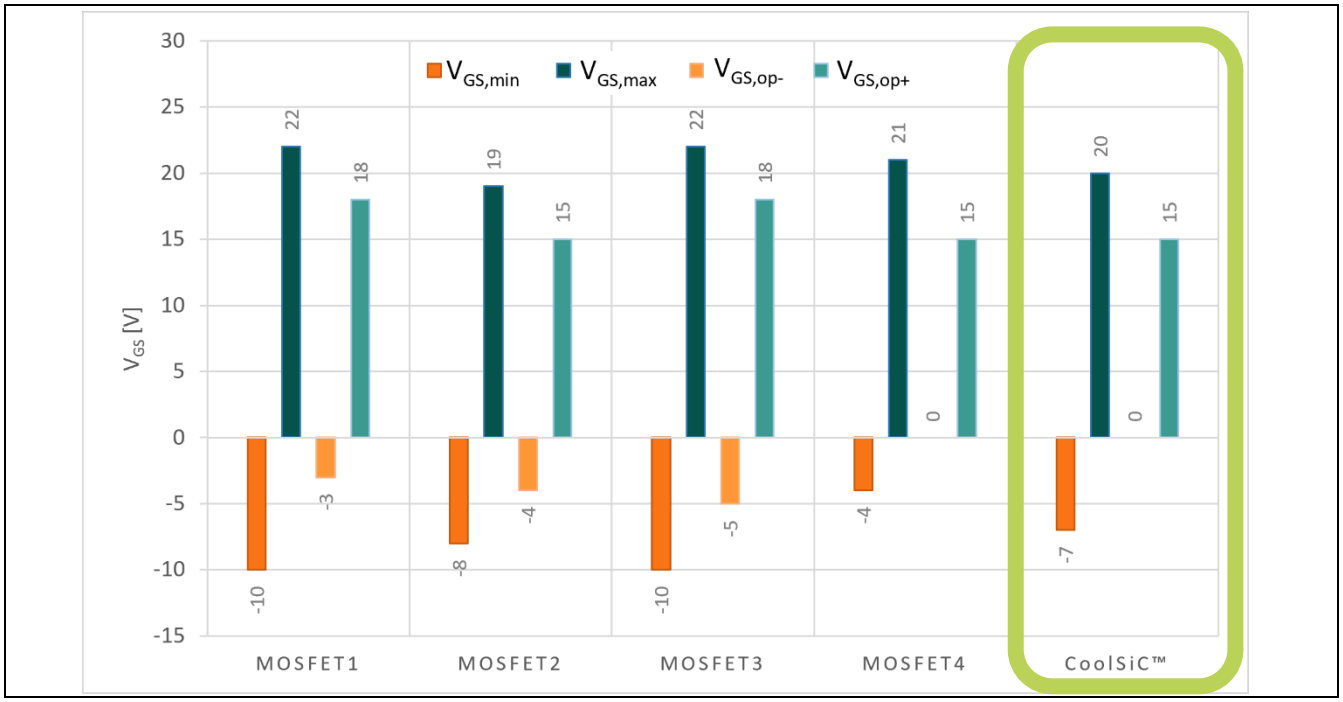

Figure 5 Gate-source voltage range of SiC MOSFETs (dark shade: absolute maximum ratings, light shade: recommended range as per the datasheet)

As seen in Figure 5, the highest recommended gate voltage for MOSFET 3 is 22 V. MOSFET 1 and MOSFET 2 also have a range beyond 19 V. However, CoolSiC™ can be driven with a total supply voltage range of below $V_{GS(on)} - V_{GS(off)} = 20$ V and without the necessity of a negative voltage during turn-off. This can be achieved, theoretically, by any EiceDRIVER™ with a maximum supply voltage rating of 20 V. Voltage spikes can easily exceed this maximum rating, even if only for very short durations. Therefore, selecting EiceDRIVER™ isolated or level-shift gate driver ICs with a rating of at least 25 V is recommended for output supply ranges ($V_{VCC2} - V_{VEE2}$, $V_{VCC2} - V_{GND2}$, or $V_{VCC} - V_{COM}$) for a reliable gate drive circuit design. Table 3 lists these parameters for the products under discussion.

Table 3 Output voltage parameters relevant for driving SiC MOSFETs

Gate driver	Maximum output supply range V_{VCC2} - V_{VEE2} / V_{VCC2} - V_{GND2} / V_{VCC} - V_{COM}	Minimum negative gate voltage
X3 Compact (1ED312x)	40 V	V_{VCC2} – 40 V
X3 Compact (1ED314x)	35 V	V_{VCC2} – 35 V
F3 (1ED332x)	40 V	-22 V
2L-SRC Compact (1ED32xx)	40 V	V_{VCC2} – 40 V
X3 Analog/Digital (1ED34/38xx)	40 V	-40 V
2ED1323S12P	25 V	0 V

2.5 Extended common mode transient immunity(CMTI) capability

SiC MOSFETs are capable of switching extremely fast. This fast switching of voltages causes a common mode noise injection from the output side to the input side of the galvanically isolated gate drivers, requiring a high CMTI robustness rating from the gate driver IC.

EiceDRIVER™ isolated gate driver ICs that use the coreless transformer technology for galvanic isolation between the input and output are very robust against voltage disturbances. As a result, these gate drivers have the best-in-class CMTI performance and rating in the market, reaching up to 300 kV/µs. The current standard IEC 60747-17 for magnetic and capacitive couplers specifies a measurement procedure. It requires CMTI tests with rising and falling edges of the applied voltage slope. This ensures a good comparability between CMTI specifications of various driver ICs.

Table 4 EiceDRIVER™ CMTI capability

CMTI capability	Device family			
	EiceDRIVER™ Compact		EiceDRIVER™ Enhanced	
200 V/ns	X3 Compact (1ED312x)	2L-SRC Compact (1ED32xx)	X3 Analog (1ED34x1)	X3 Digitl (1ED38x0)
300 V/ns	X3 Compact (1ED314x)		F3 (1ED332x)	

For level-shift products, CMTI tests are not required because of the different input to output junction isolation (these devices are not galvanically isolated).

2.6 Fast DESAT detection and overcurrent protection

SiC MOSFETs do not have a sharp saturation behavior under excessive current conditions. Short circuit current levels can, therefore, easily reach ten times the nominal current rating. Thus, the behavior of SiC MOSFETs during a short circuit condition is unlike that of an IGBT, which undergoes desaturation and the short circuit current is limited to four times the nominal current. The short circuit withstand time of CoolSiC™ is approximately 2 to 3 µs, which is relatively short. Fast detection and a fast shutdown are mandatory for the reliable operation of SiC MOSFETs and a long lifetime. Suitable techniques for overload handling in SiC MOSFETs are a fast DESAT function and overcurrent protection.

The well-known desaturation detection circuit for IGBTs can also be used for SiC MOSFETs if the DESAT circuit is designed to react fast enough. It is based on monitoring the drain-source voltage during the ON state of an IGBT. A leading-edge blanking is needed during turn-on of the IGBT to prevent false triggering of the DESAT by

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the spike in the collector current caused by the diode's reverse recovery. Further, several parasitic effects of power diodes and the IGBT itself, as well as the layout crosstalk during current commutation, require a so-called DESAT blanking time in the range of a few µs. Such a long blanking time is not acceptable for SiC MOSFET as described earlier. The gate driver for SiC MOSFETs should have the capability to react fast and the circuit should be designed to activate the protection in typically 1 µs – 3 µs time in case of a short circuit. A well optimized layout is mandatory to detect the short circuit condition safely and to avoid false DESAT triggers through ground bounce or signal cross talk. Refer to the technical description of the driver IC used for further information about adjusting the DESAT components: R_{DESAT}, C_{DESAT}, and D_{DESAT}.

A suitable way to avoid such effects is to apply all rules of a good PCB layout. One of these rules is to optimize for small PCB track loops. This will decouple the gate driver IC's power supplies in the MOSFET gate current paths and in the main current paths that include the DC link, as shown in Figure 6. This prevents parasitic stray inductances that could lead to inductive coupling of switched currents.

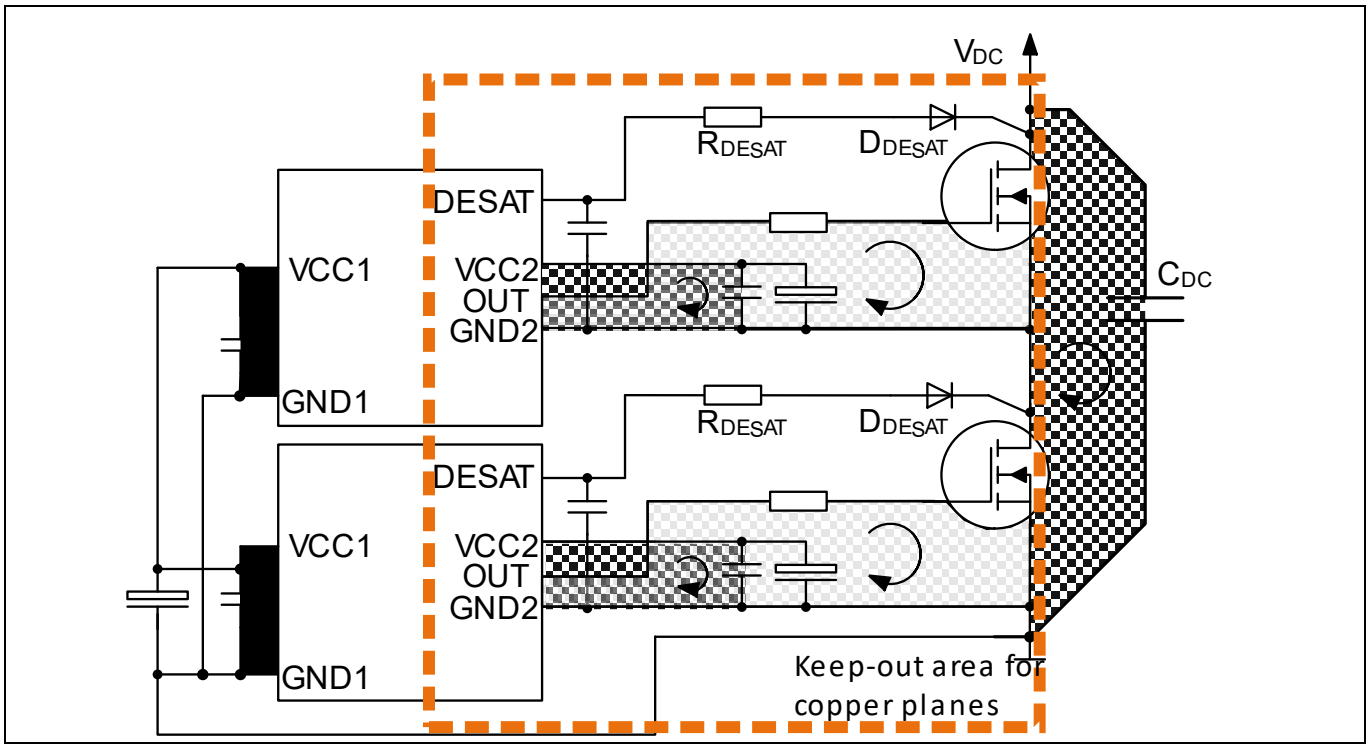

Figure 6 Example of a suitable layout for a fast DESAT-detection function

Specific care should be taken to avoid parasitic capacitive coupling. The fast-switching speed of a SiC MOSFET cannot be compared with the switching speed of IGBT. It is, therefore, recommended that the area of the gate drives circuit be kept free of planes that are connected to GND1, GND2, or V_{DC}. This prevents unnecessary capacitive coupling with high dV/dt. Note, however, that this approach can create a conflict with the cooling demands of the gate driver IC that might require specific copper areas.

The placement of the DESAT diode, D_{DESAT}, and the resistor, R_{DESAT}, and the routing of the DESAT sense track should avoid both inductive and capacitive coupling to generate a DESAT signal with minimum interferences and delays.

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The following gate driver products in the EiceDRIVER™ Enhanced family provide the DESAT function:

- F3 (1ED332x)
- X3 Analog (1ED34xx)
- X3 Digital (1ED38xx)

The EiceDRIVER™ SOI gate driver, 2ED1323S12P, uses another protection feature for short circuit events: overcurrent protection (ITRIP input pin). It can sense overcurrent events in the DC bus. When the IC detects an overcurrent event, the outputs are shut down and a fault-enable pin (RFE) is pulled to VSS.

The level of current at which the overcurrent protection is initiated is determined by the resistor network (i.e., R_0, R_1, and R_2) connected to ITRIP as (shown in Figure 7) and the ITRIP threshold, $V_{th,OCP}$. The circuit designer will need to determine the maximum allowable level of current in the DC bus and select R_0, R_1, and R_2 such that the voltage at node Vx reaches the overcurrent threshold, $V_{th,OCP}$, at that current level.

$$V_{th,OCP} = R_0 * I_{DC-} * \frac{R_1}{R_1 + R_2}$$

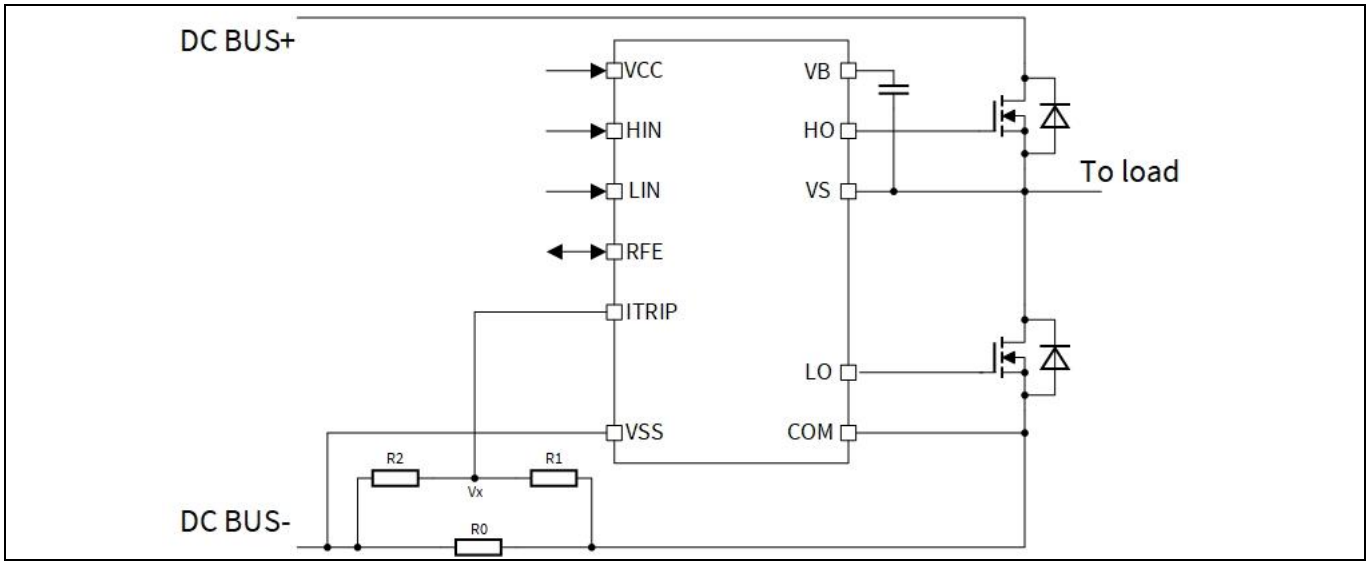

Figure 7 Programming overcurrent protection

In motor control applications, a typical value for resistor R_0 would be 50 mΩ. This protection has a fast (650 ns) response, as can be seen in the oscilloscope snapshot in Figure 8.

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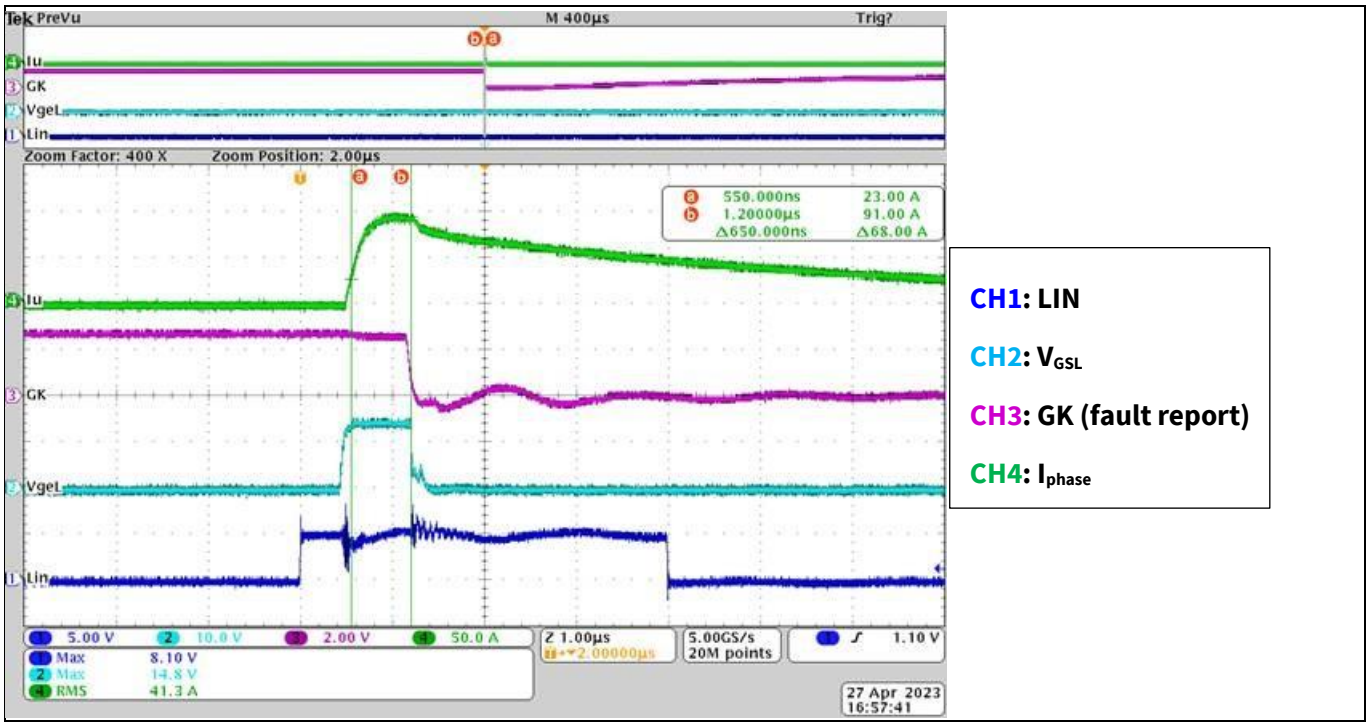

Figure 8 ITRIP lab measurement response

In applications that require more than one device, such as 3-phase circuits, this protection can be implemented in two different ways: leg-shunt protection or single-shunt protection.

The leg-shunt protection configuration, shown in Figure 9, implies overcurrent detection for every leg. This implementation requires a network of resistors for every leg, and every single device can, independently from the others gate drivers, shut down its own output when a failure occurs.

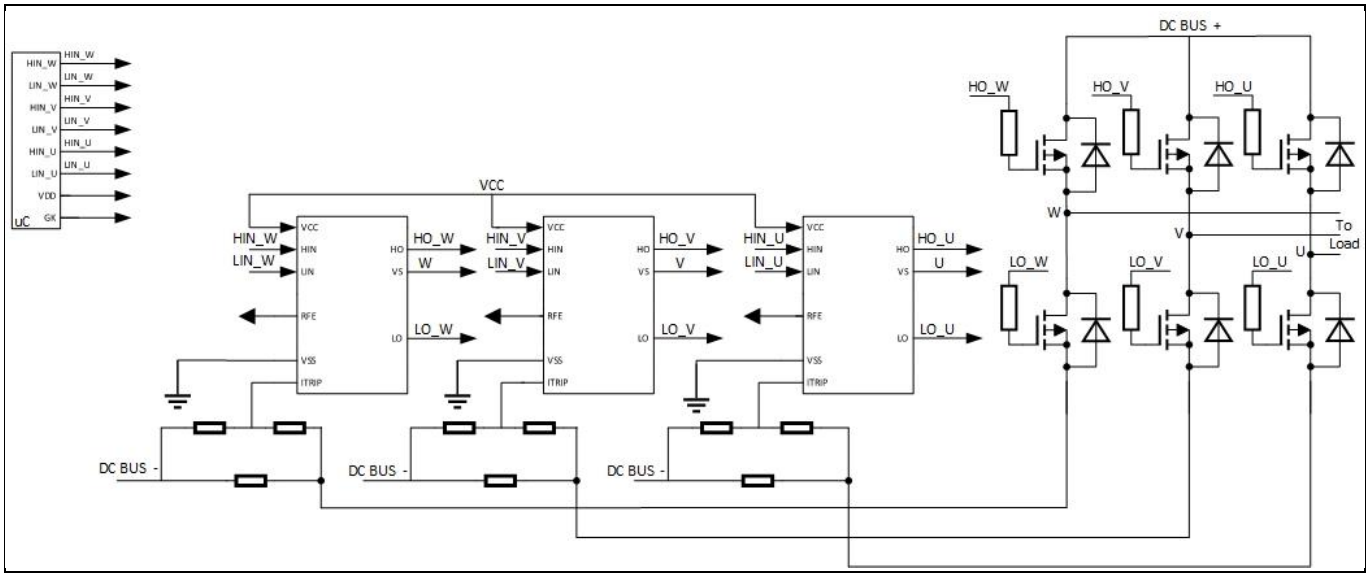

Figure 9 Leg-shunt protection configuration

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On the other hand, the single-shunt protection configuration reduces the number of external resistors relying on the RFE pin and the daisy chain configuration.

The gate drivers can be daisy chained, as shown in Figure 10. The three fault-enable RFE pins are connected together. ITRIP sensing is only used on the first IC and the other two ITRIP pins are disabled by tying them to VSS. The programmable fault clear timing components, R_{RFE} and C_{RFE}, are populated only once for the RFE pin. When a fault occurs, either from ITRIP or UVLO, or an external command, all the three HVICs are disabled by pulling the daisy-chained RFE pin low to VSS.

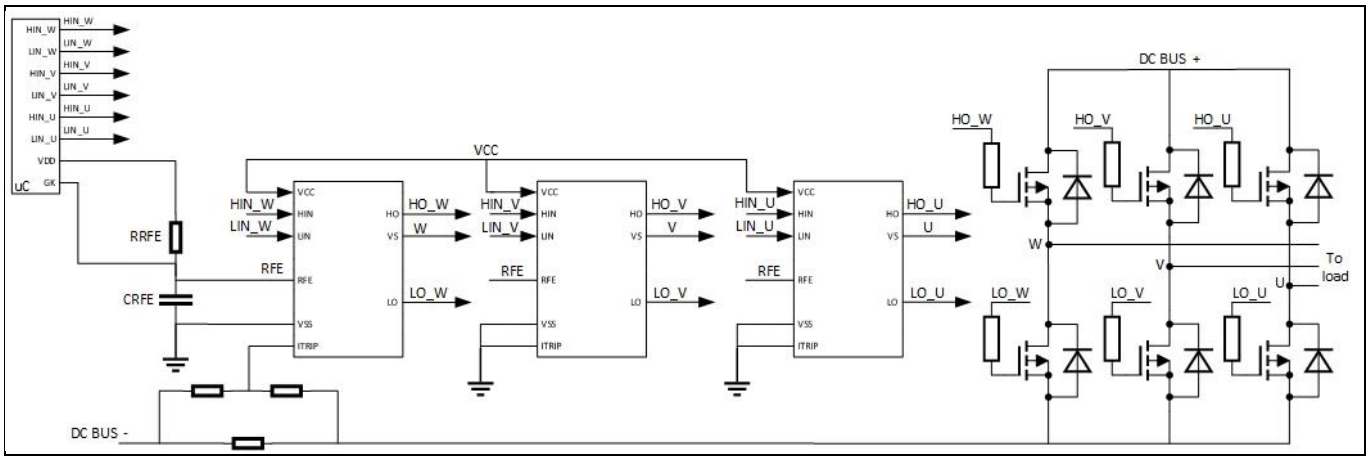

Figure 10 Single-shunt and daisy chain configuration

The overcurrent protection feature is implemented in the EiceDRIVER™ level-shift SOI device, 2ED1323S12P.

2.7 Active Miller clamping

Active Miller clamping is a well-known technique to avoid parasitic dV/dt induced turn-on. This function uses a CLAMP terminal directly connected to the power transistor's gate terminal, as shown in Figure 11. It pulls down the gate during OFF state. The OFF state condition is monitored by sensing the gate voltage with the same terminal. The clamp function is activated as soon as the gate voltage drops below a specified threshold, which is typically $V_{CLAMP} = V_{VEE2} + 2\ V$ or $V_{COM} + 2\ V$.

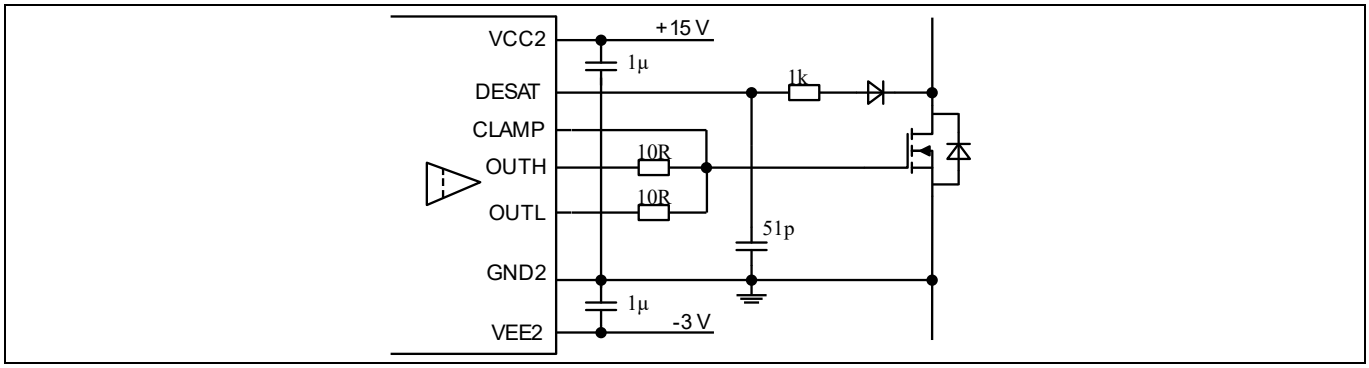

Figure 11 Schematic example for implementation of the active Miller clamp function

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The monitoring comparator threshold, V_{CLAMP}, is referenced to the lowest available voltage inside the IC. The lowest voltage occurs at terminal VEE2 of the EiceDRIVER™ isolated gate driver family or at the terminal COM of the family and 2ED1323S12P.

EiceDRIVER™ Compact isolated gate driver ICs with active Miller clamp are:

- X3 Compact: 1ED3122MC12H, 1ED3127MU12F
- 2L-SRC Compact: 1ED3251MC12H

Products from the EiceDRIVER™ Enhanced isolated gate driver IC families that offer active Miller clamp in combination with a DESAT function are:

- F3 (1ED332x)
- X3 Analog (1ED34x1)
- X3 Digital (1ED38x0)

Gate drivers 1ED3491 from the X3 Analog and 1ED3890 from the X3 Digital family offer a Miller clamp driver instead of an internal Miller clamp. The miller clamp driver drives an external MOSFET that can be placed very close to the gate and source terminals of the SiC MOSFET on the PCB. As a result, the active Miller clamp function improves significantly in the application, especially, when the gate driver is placed at some distance from the SiC MOSFET on the PCB.

Lastly, the 2ED1323S12P level-shift gate driver provides both an active Miller clamp function and overcurrent (ITRIP) protection.

These gate driver ICs with integrated active Miller clamp function are a good choice in applications where switching involves high dV/dt and in applications where only unipolar voltage is used for the gate drive.

3 Power dissipation

3.1 Isolated gate driver power dissipation

Calculating the power dissipated of a gate driver IC is important to prevent very high operating conditions. This section describes how to calculate the power dissipated by gate driver ICs in general.

Regarding EiceDRIVER™ products, the main contributors for power dissipation are:

- The input side operating supply current
- The input side input bias currents
- The output side quiescent current
- The output side gate charge losses

These individual values can be calculated through the following equations:

1. Measure the operating current, $I_{q,in}$, to get the maximum switching frequency of the application. The power transistors should not be connected.

$$P_{\mathrm{d,VCC1}} = I_{\mathrm{q,in}} \cdot V_{\mathrm{VCC1,max}} \quad (1)$$

The input bias currents of the logic input terminals contribute with:

$$P_{\mathrm{d,bias}} = n \cdot I_{\mathrm{IN}} \cdot V_{\mathrm{VCC1,max}} \quad (2)$$

Here n is the number of input terminals of the gate driver IC. This portion of the dissipated power is usually very small compared to the portion contributed by the supply voltage.

2. The output side section continuously dissipates power with respect to the quiescent current, $I_{q,out}$. This is given by:

$$P_{\mathrm{d,VCC2}} = I_{\mathrm{q,out}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \quad (3)$$

The output side quiescent current value should also be measured at the maximum switching frequency without connecting the power transistors.

3. Calculate the losses of the output section through the total gate charge of the power transistor, Q_{Gtot}, the supply voltage $V_{VCC2} – V_{VEE2}$, the switching frequency f_S, and the external gate resistor. Different cases for turn-on and turn-off have to be considered, because many designs use different resistors for turn-on and turn-off. This leads to a specific distribution of losses that depends on:
   - The external gate resistors $R_{Gon,ext}$ and $R_{Goff,ext}$
   - The internal resistances of the output section of the gate driver, $R_{Gon,IC}$ and $R_{Goff,IC}$
   - The internal gate resistance of the SiC MOSFET, $R_{G,int}$

$$P_{\mathrm{d,on}} = \frac{1}{2} Q_{\mathrm{G,tot}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \cdot f_{\mathrm{S}} \cdot \frac{R_{\mathrm{Gon,IC}}}{R_{\mathrm{Gon,ext}} + R_{\mathrm{Gon,IC}} + R_{G,int}} \quad \text{, for turn-on} \quad (4)$$

3 Power dissipation

$$P_{\mathrm{d,off}} = \frac{1}{2} Q_{\mathrm{G,tot}} \cdot (V_{\mathrm{VCC2}} - V_{\mathrm{VEE2}}) \cdot f_{\mathrm{S}} \cdot \frac{R_{\mathrm{Goff,IC}}}{R_{\mathrm{Goff,ext}} + R_{\mathrm{Goff,IC}} + R_{G,int}} \quad \text{, for turn-off} \tag{5}$$

The sum of $P_{\mathrm{d,on}}$ and $P_{\mathrm{d,off}}$ is the output stage loss due to the gate drive.

4. The final power dissipation during operation at highest switching frequency is then the sum of both the contributions:

$$P_d = P_{d,VCC1} + P_{d,bias} + P_{d,VCC2} + P_{d,on} + P_{d,off} + P_{d,add} \tag{6}$$

5. Some gate drivers may have additional portions of dissipated power or a different partitioning of losses, such as the DESAT function or the active Miller clamping. This portion is represented by the term $P_{\mathrm{d,add}}$ in equation (6). It is important to analyze the individual effect of each of these functions with respect to power dissipation.

The datasheet shows specific layouts for which the given thermal resistance junction to ambient ($R_{\mathrm{th(j\text{-}a)}}$) is valid. Note that different layouts may lead to different thermal resistances. Therefore, it is always a good engineering practice to additionally examine the package temperature through experiments.

3.2 Level-shift gate driver power dissipation

In level-shift products, the power dissipated by the driver IC is a combination of several sources such as:

- Static losses
- Output stage losses
- CMOS losses
- Level-shift losses
- Bootstrap diode losses
- Leakage losses

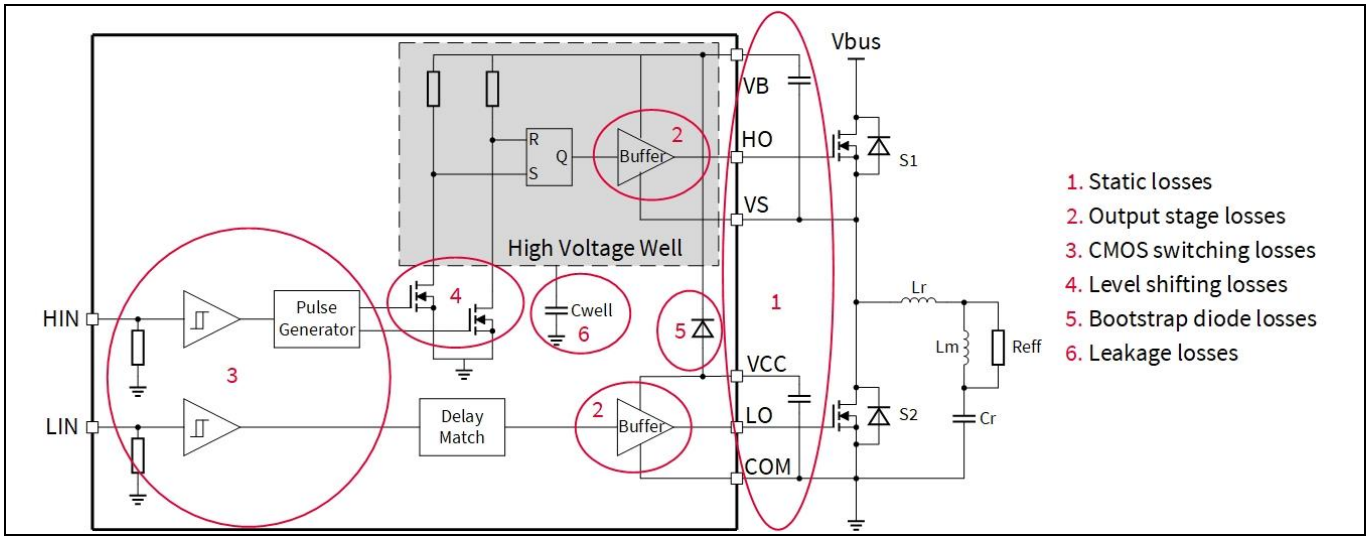

Figure 12 Different power losses within the level-shift gate driver

The output stage is the major contributor to the power dissipated by the gate driver IC. The external gate resistors also contribute to the power dissipated by the gate driver IC. The bigger the external gate resistor, the smaller the power dissipated by the gate driver.

3 Power dissipation

Within the gate driver IC, the different losses include:
1. Static losses are calculated for a given supply voltage and quiescent/bootstrap charging currents:

$$Static\ losses\ in\ the\ low\ side = V_{\mathrm{CC}} \times I_{\mathrm{QCC}} \quad (7)$$

$$Static\ losses\ in\ the\ high\ side = V_{\mathrm{BS}} \times I_{\mathrm{QBS}} \quad (8)$$

$$Static\ losses\ at\ input\ stage = \frac{1}{2} \times \frac{V_{\mathrm{CC}} \times V_{\mathrm{CC}}}{R_{\mathrm{pullup}}} \quad (9)$$

2. Output stage losses are calculated through the total gate charge of the SiC MOSFET. It drives $Q_{G,tot}$, the supply voltage V_{VCC}, the switching frequency f_s, the external gate resistor $R_{Gon,ext}$ and $R_{Goff,ext}$, and the internal resistor of the SiC MOSFET $R_{G,int}$. Different cases of turn-on and turn-off must be considered, because many designs use different resistors for turn-on and turn-off. This leads to a specific distribution of losses from the output section:

$$Turn\ on\ losses: P_{\mathrm{d,on}} = \frac{1}{2} \times Q_{\mathrm{G,tot}} \times V_{\mathrm{CC}} \times f_{\mathrm{s}} \times \frac{R_{\mathrm{Gon,IC}}}{R_{\mathrm{Gon,ext}} + R_{\mathrm{Gon,IC}} + R_{\mathrm{G,int}}} \quad (10)$$

$$Turn\ off\ losses: P_{\mathrm{d,off}} = \frac{1}{2} \times Q_{\mathrm{G,tot}} \times V_{CC} \times f_{\mathrm{s}} \times \frac{R_{\mathrm{Gon,IC}}}{R_{\mathrm{Gon,ext}} + R_{\mathrm{Gon,IC}} + R_{\mathrm{G,int}}} \quad (11)$$

3. CMOS losses are calculated for a given switching frequency and supply voltage:

$$CMOS\ losses = Q_{\mathrm{COMS}} \times V_{\mathrm{CC}} \times f_{\mathrm{s}} \quad (12)$$

$$Junction\ capacitance\ switching\ losses = \frac{1}{2} \times C_{\mathrm{J}} \times {V_{\mathrm{BUS}}}^2 \times f_{\mathrm{s}} \quad (13)$$

4. Level-shift losses are calculated for a given switching frequency and supply voltages:

$$Loss\ per\ level\ shifter\ (ON) = (V_{\mathrm{BUS}} + V_{\mathrm{CC}}) \times I_{\mathrm{LSON}} \times t_{\mathrm{on}} \times f_{\mathrm{s}} \quad (14)$$

$$Loss\ per\ level\ shifter\ (OFF) = (V_{\mathrm{BUS}} + V_{\mathrm{CC}}) \times I_{\mathrm{LSOFF}} \times t_{\mathrm{off}} \times f_{\mathrm{s}} \quad (15)$$

5. Bootstrap diode losses are calculated for given switching frequency and supply voltages:

$$Dynamic\ losses\ in\ boot\ diode = EB \times f_{\mathrm{s}} \times 2 \times \frac{I_{\mathrm{QBS}} + (Q_{\mathrm{G,tot}} \times f_{\mathrm{s}})}{10^{-3} \times \frac{V_{\mathrm{BUS}}}{400}} \quad (16)$$

$$Static\ losses\ in\ boot\ diode = \frac{\left(V_{\mathrm{TH}} + 2 \times \left[I_{\mathrm{QBS}} + \left(Q_{\mathrm{G,tot}} \times f_{\mathrm{s}}\right)\right] \times R_{\mathrm{D}}\right) \times 2 \times \left[I_{\mathrm{QBS}} + (Q_{\mathrm{G,tot}} \times f_{\mathrm{s}})\right]}{2} \quad (17)$$

6. Leakage losses are calculated for a given switching frequency and supply voltages:

$$Leakage\ loss = I_{\mathrm{LEAK}} \times V_{\mathrm{BUS}} \quad (10)$$

Similar to the case of the isolated gate driver, any other contribution related to specific functions such as DESAT or active Miller clamp should be analyzed individually.

4 Considerations for single transistor topologies and applications with low dV/dt stress during an OFF state

This chapter explains special conditions for SiC MOSFET gate drives in single-transistor topologies. Popular topologies using a single SiC MOSFET are boost, buck, or flyback converters. The low-side referenced switch, e.g., of a boost topology, does not necessarily require an isolated gate driver. However, the non-isolated drivers can often suffer from heavy ground bouncing. This can lead to a latch-up of the driver IC or to additional switching losses due to stray inductances that hinder a proper switching process. Isolated gate drivers, on the other hand, do not suffer from ground bouncing due to the large offset voltage range that provides extra gate drive performance, particularly in single transistor topologies. New level-shift products are more reliable with respect to ground bouncing (transient negative VS). It is, thus, better to do a case-by-case evaluation of the application conditions is.

A parasitic turn-on of a MOSFET that can be a challenge for half-bridge configurations is not a problem in single transistor topologies. Therefore, only a unipolar gate voltage is often sufficient to control the SiC MOSFET. CoolSiC™ MOSFETs have special benefits because the gate-source threshold voltage, $V_{GS,th}$, is high (as discussed in Section 2.3). Therefore, these devices are very robust against turn-on triggered by noise. This simplifies the gate drive circuits to a large extent because a unipolar non-isolated power supply is sufficient e.g., for boost or flyback converters.

A unipolar gate driver power supply can be used in drive applications where the switching speed is limited. The dV/dt is often limited to 5 V/ns in such applications due to motor lifetime considerations. Infineon's CoolSiC™ transistors offer a relatively high gate-source threshold voltage, as shown in Figure 3. Therefore, the parasitic turn-on triggered by dV/dt is very unlikely even in half-bridge configurations. Additionally, applications using only a positive gate voltage can be supported by active Miller clamping, explained in Section 2.7.

5 Summary

SiC MOSFETs offer several advantages over traditional silicon-based systems, including higher efficiency and power density. Gate drivers are key components in any power electronic system and to take full advantage of the SiC MOSFETs, choosing the right gate driver is crucial for any design. EiceDRIVER™ gate drivers from Infineon offer all the features required for driving SiC MOSFETs; such as high gate currents, active Miller clamp, fast DESAT protection, excellent part-to-part matching of propagation delay, and best-in-class CMTI performance. EiceDRIVER™ gate drivers when used with CoolSiC™ MOSFETs from Infineon enable the system to provide the best possible performance.

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Revision history

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V1.1	2018-06-24	Update product range for 1EDC-family and 1EDS-SRC family
V1.2	2024-04-22	Updated with new parts

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