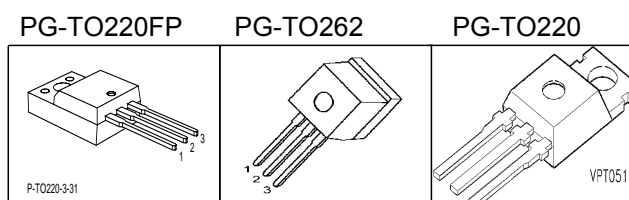


Cool MOS™ Power Transistor

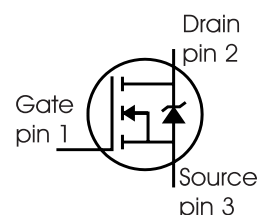
Feature

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme dv/dt rated
- Ultra low effective capacitances
- Improved transconductance
- PG-TO-220-3-31;-3-111: Fully isolated package (2500 VAC; 1 minute)
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC⁰⁾ for target applications

$V_{DS} @ T_{jmax}$	650	V
$R_{DS(on)}$	0.28	Ω
I_D	15	A



Type	Package	Ordering Code	Marking
SPP15N60C3	PG-TO220	Q67040-S4600	15N60C3
SPI15N60C3	PG-TO262	Q67040-S4601	15N60C3
SPA15N60C3	PG-TO220FP	SP000216325	15N60C3



Maximum Ratings

Parameter	Symbol	Value		Unit
		SPP_I	SPA	
Continuous drain current $T_C = 25\text{ °C}$ $T_C = 100\text{ °C}$	I_D	15 9.4	15 ¹⁾ 9.4 ¹⁾	A
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\text{ puls}}$	45	45	A
Avalanche energy, single pulse $I_D=7.5\text{A}, V_{DD}=50\text{V}$	E_{AS}	460	460	mJ
Avalanche energy, repetitive t_{AR} limited by T_{jmax} ²⁾ $I_D=15\text{A}, V_{DD}=50\text{V}$	E_{AR}	0.8	0.8	
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	15	15	A
Gate source voltage static	V_{GS}	± 20	± 20	V
Gate source voltage AC ($f > 1\text{Hz}$)	V_{GS}	± 30	± 30	
Power dissipation, $T_C = 25\text{ °C}$	P_{tot}	156	34	W
Operating and storage temperature	T_j, T_{stg}	-55...+150		°C
Reverse diode dv/dt ⁶⁾	dv/dt	15		V/ns

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope $V_{DS} = 480\text{ V}$, $I_D = 15\text{ A}$, $T_j = 125\text{ °C}$	dv/dt	50	V/ns

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	0.8	K/W
Thermal resistance, junction - case, FullPAK	$R_{thJC\text{ FP}}$	-	-	3.7	
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
Thermal resistance, junction - ambient, FullPAK	$R_{thJA\text{ FP}}$	-	-	80	
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s ³)	T_{sold}	-	-	260	°C

Electrical Characteristics, at $T_j=25\text{ °C}$ unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}$, $I_D=0.25\text{mA}$	600	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	$V_{GS}=0\text{V}$, $I_D=15\text{A}$	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	$I_D=675\mu\text{A}$, $V_{GS}=V_{DS}$	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=600\text{V}$, $V_{GS}=0\text{V}$, $T_j=25\text{ °C}$ $T_j=150\text{ °C}$	-	0.1	1	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=30\text{V}$, $V_{DS}=0\text{V}$	-	-	100	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}$, $I_D=9.4\text{A}$ $T_j=25\text{ °C}$ $T_j=150\text{ °C}$	-	0.25	0.28	Ω
Gate input resistance	R_G	$f=1\text{MHz}$, open drain	-	1.23	-	

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Transconductance	g_{fs}	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$, $I_D = 9.4A$	-	11.9	-	S
Input capacitance	C_{iss}	$V_{GS} = 0V$, $V_{DS} = 25V$,	-	1660	-	pF
Output capacitance	C_{oss}	$f = 1MHz$	-	540	-	
Reverse transfer capacitance	C_{rss}		-	40	-	
Effective output capacitance, ⁴⁾ energy related	$C_{o(er)}$	$V_{GS} = 0V$, $V_{DS} = 0V$ to 480V	-	80	-	
Effective output capacitance, ⁵⁾ time related	$C_{o(tr)}$		-	127	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 480V$, $V_{GS} = 0/10V$,	-	10	-	ns
Rise time	t_r	$I_D = 15A$,	-	5	-	
Turn-off delay time	$t_{d(off)}$	$R_G = 4.3\Omega$	-	50	80	
Fall time	t_f		-	5	10	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	$V_{DD} = 480V$, $I_D = 15A$	-	7	-	nC
Gate to drain charge	Q_{gd}		-	29	-	
Gate charge total	Q_g	$V_{DD} = 480V$, $I_D = 15A$, $V_{GS} = 0$ to 10V	-	63	-	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 480V$, $I_D = 15A$	-	5	-	V

⁰J-STD20 and JESD22

¹Limited only by maximum temperature

²Repetitive avalanche causes additional power losses that can be calculated as $P_{AV} = E_{AR} \cdot f$.

³Soldering temperature for TO-263: 220°C, reflow

⁴ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁵ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

⁶ $I_{SD} \leq I_D$, $di/dt \leq 400A/\mu s$, $V_{DClink} = 400V$, $V_{peak} < V_{BR, DSS}$, $T_j < T_{j,max}$.

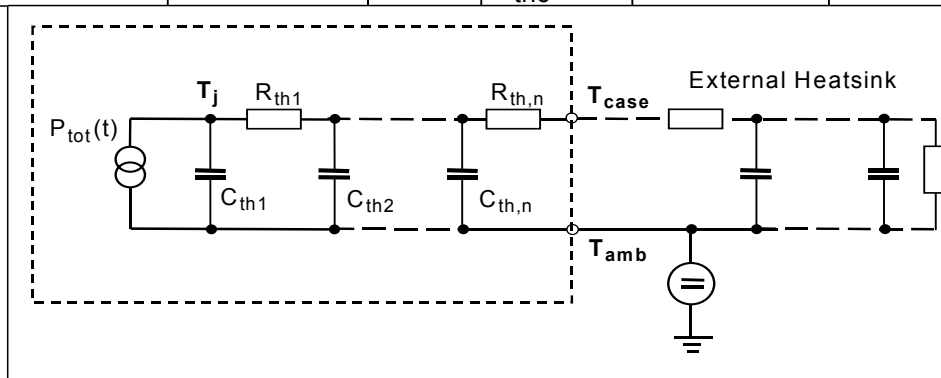
Identical low-side and high-side switch.

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Inverse diode continuous forward current	I_S	$T_C=25^\circ\text{C}$	-	-	15	A
Inverse diode direct current, pulsed	I_{SM}		-	-	45	
Inverse diode forward voltage	V_{SD}	$V_{GS}=0\text{V}, I_F=I_S$	-	1	1.2	V
Reverse recovery time	t_{rr}	$V_R=480\text{V}, I_F=I_S,$	-	460	-	ns
Reverse recovery charge	Q_{rr}	$di_F/dt=100\text{A}/\mu\text{s}$	-	27	-	μC
Peak reverse recovery current	I_{rrm}		-	55	-	A
Peak rate of fall of reverse recovery current	di_{rr}/dt	$T_j=25^\circ\text{C}$	-	1300	-	$\text{A}/\mu\text{s}$

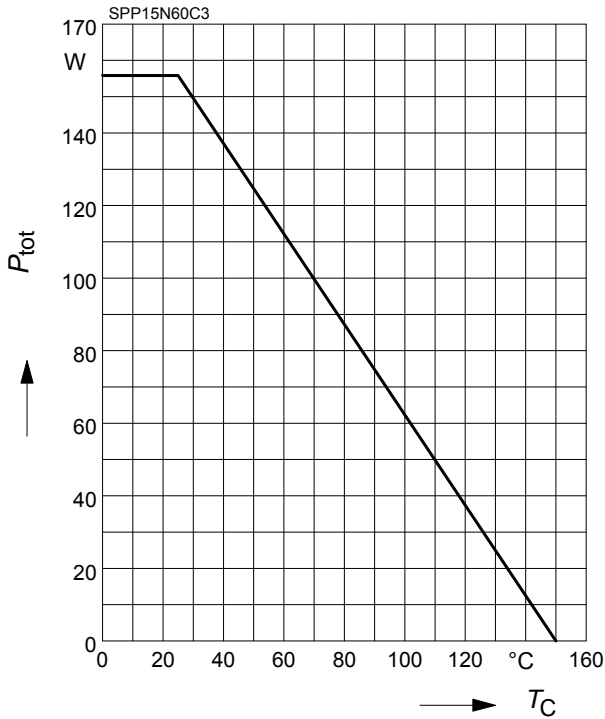
Typical Transient Thermal Characteristics

Symbol	Value		Unit	Symbol	Value		Unit
	SPP_I	SPA			SPP_I	SPA	
R_{th1}	0.012	0.012	K/W	C_{th1}	0.0002495	0.0002495	Ws/K
R_{th2}	0.023	0.023		C_{th2}	0.0009406	0.0009406	
R_{th3}	0.043	0.043		C_{th3}	0.001298	0.001298	
R_{th4}	0.156	0.176		C_{th4}	0.00362	0.00362	
R_{th5}	0.178	0.371		C_{th5}	0.009046	0.008025	
R_{th6}	0.072	2.522		C_{th6}	0.412	0.412	



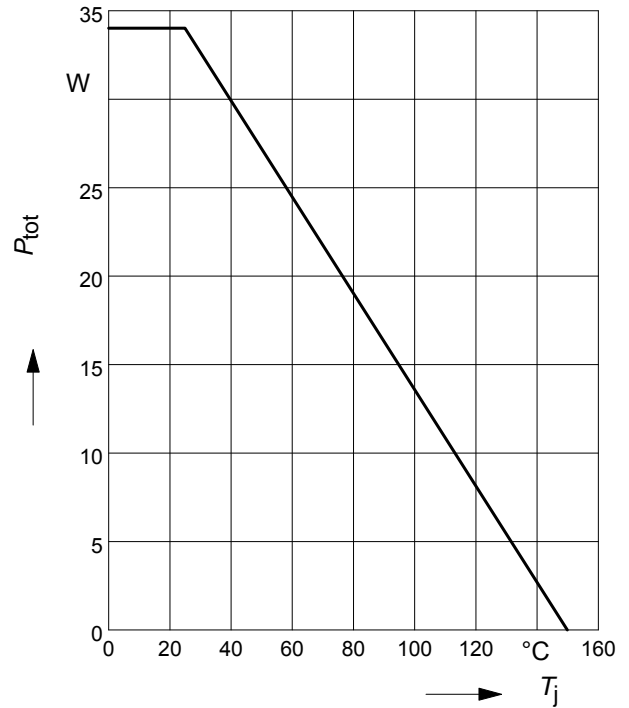
1 Power dissipation

$P_{tot} = f(T_C)$



2 Power dissipation FullPAK

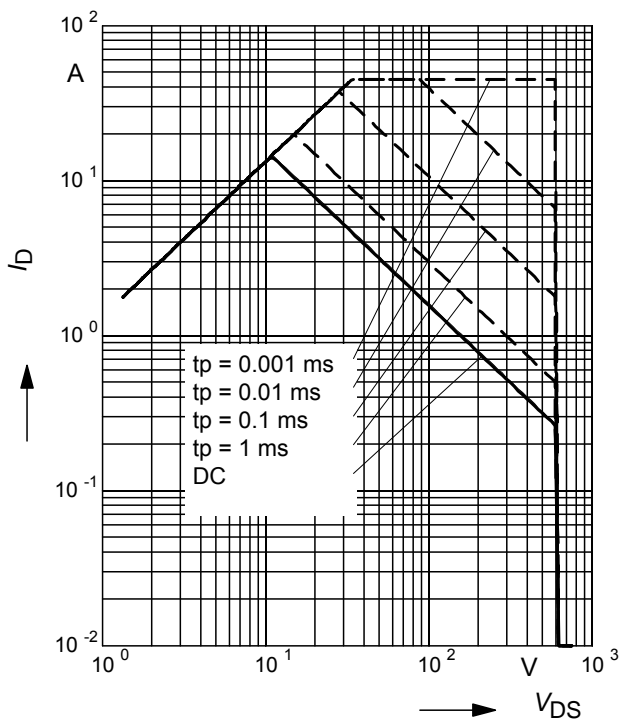
$P_{tot} = f(T_j)$



3 Safe operating area

$I_D = f(V_{DS})$

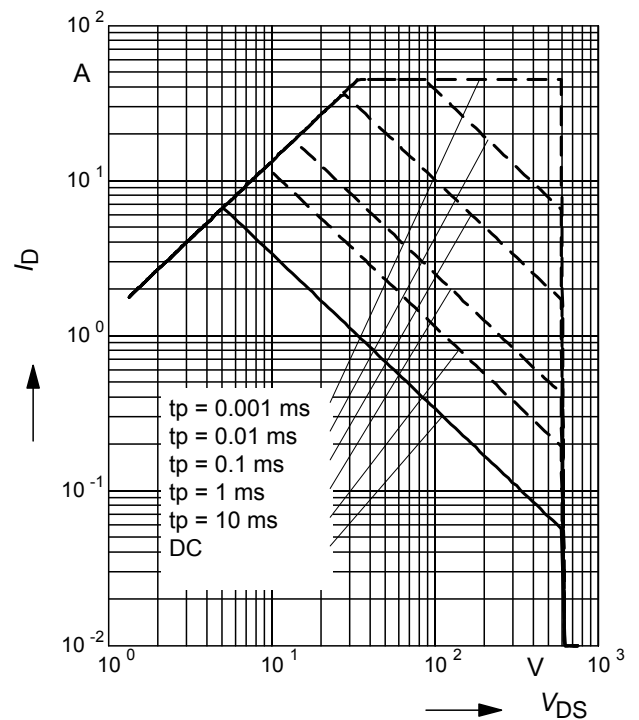
parameter : $D = 0$, $T_C = 25^\circ\text{C}$



4 Safe operating area FullPAK

$I_D = f(V_{DS})$

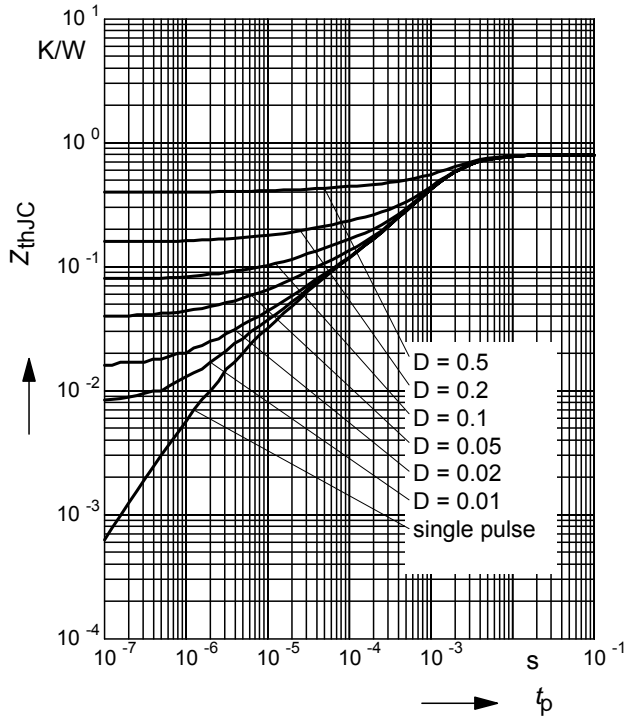
parameter: $D = 0$, $T_C = 25^\circ\text{C}$



5 Transient thermal impedance

$$Z_{thJC} = f(t_p)$$

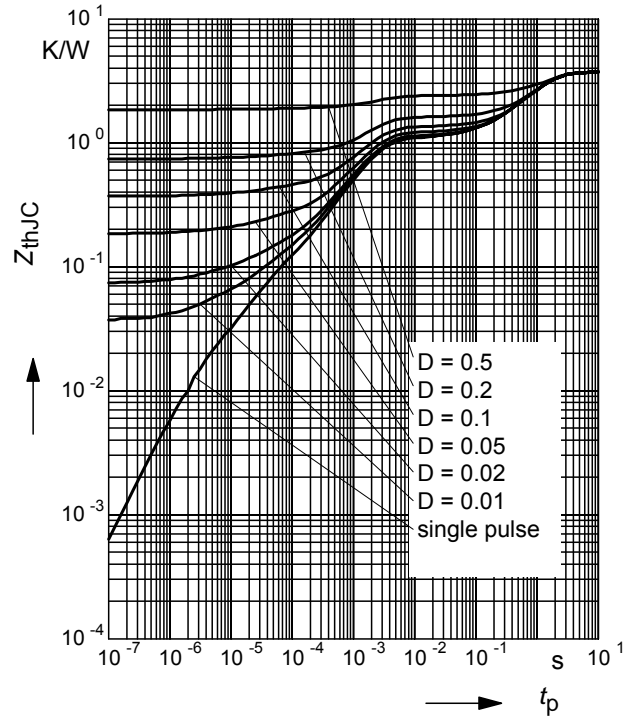
parameter: $D = t_p/T$



6 Transient thermal impedance FullPAK

$$Z_{thJC} = f(t_p)$$

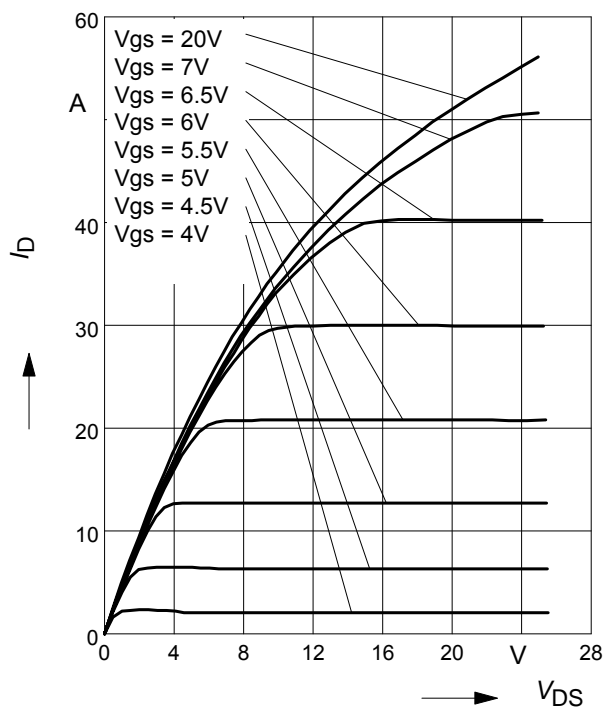
parameter: $D = t_p/t$



7 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$$

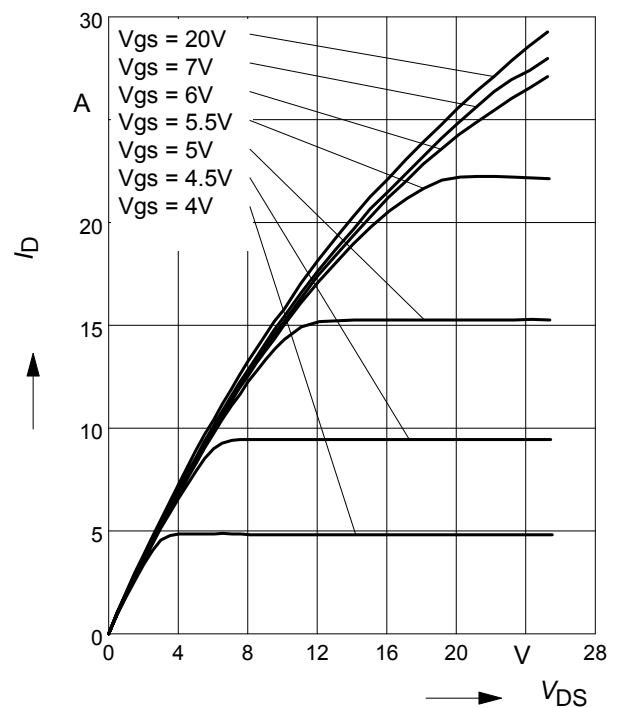
parameter: $t_p = 10 \mu\text{s}, V_{GS}$



8 Typ. output characteristic

$$I_D = f(V_{DS}); T_j = 150^\circ\text{C}$$

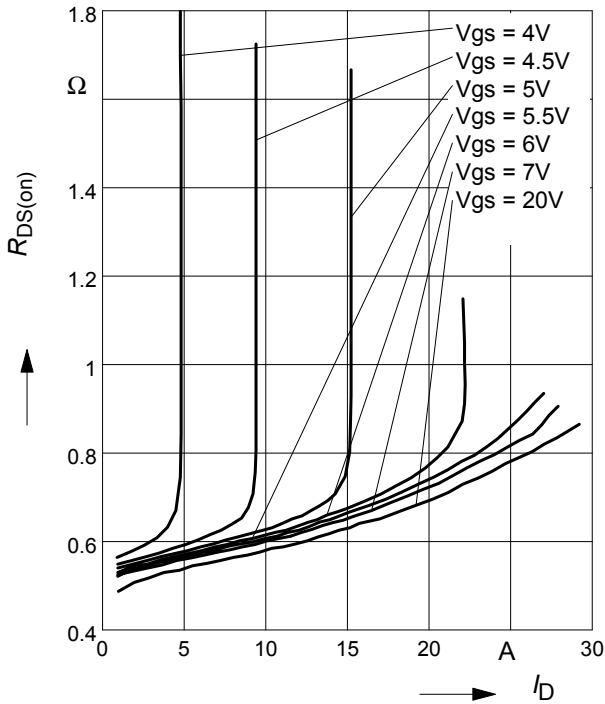
parameter: $t_p = 10 \mu\text{s}, V_{GS}$



9 Typ. drain-source on resistance

$$R_{DS(on)} = f(I_D)$$

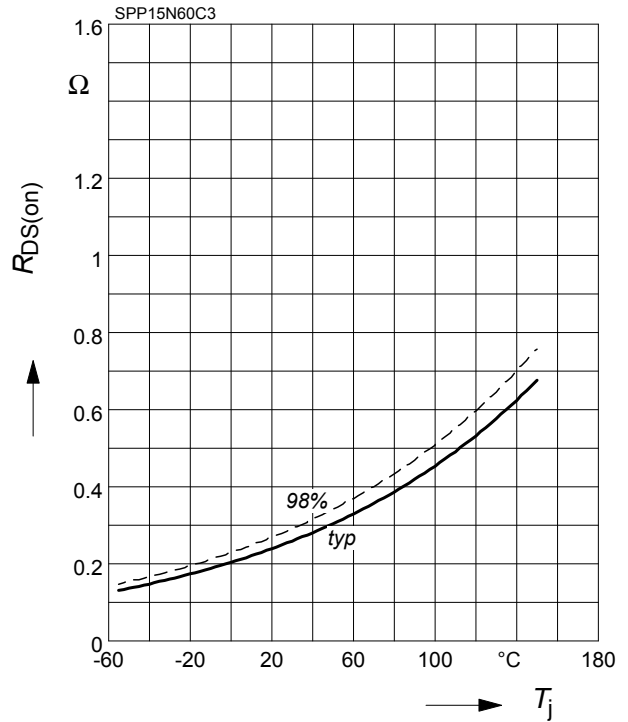
parameter: $T_j = 150^\circ\text{C}$, V_{GS}



10 Drain-source on-state resistance

$$R_{DS(on)} = f(T_j)$$

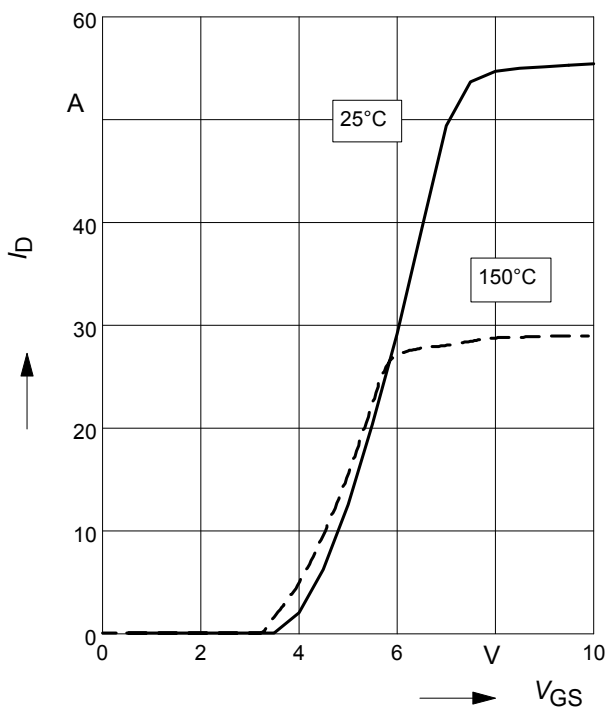
parameter: $I_D = 9.4\text{ A}$, $V_{GS} = 10\text{ V}$



11 Typ. transfer characteristics

$$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$$

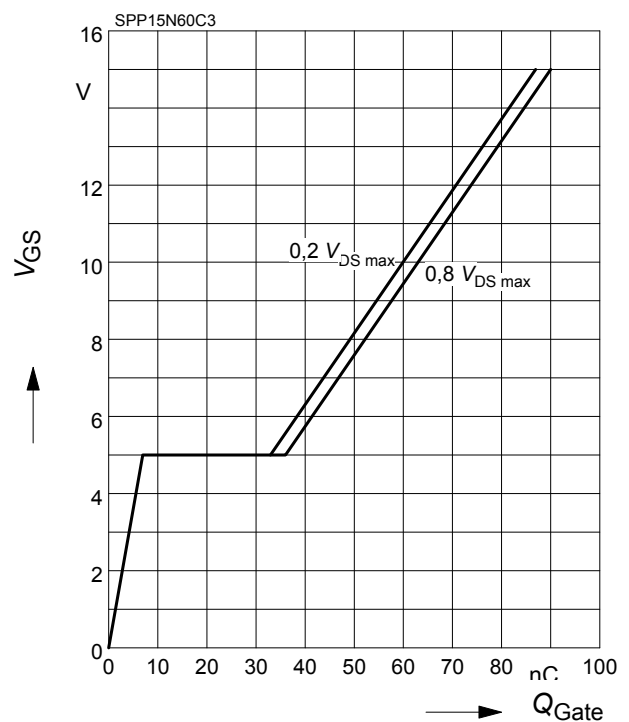
parameter: $t_p = 10\ \mu\text{s}$



12 Typ. gate charge

$$V_{GS} = f(Q_{Gate})$$

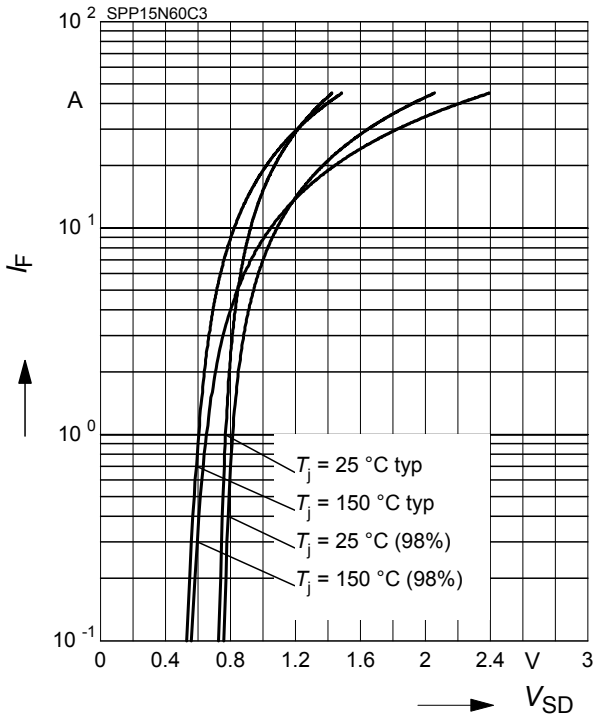
parameter: $I_D = 15\text{ A pulsed}$



13 Forward characteristics of body diode

$$I_F = f(V_{SD})$$

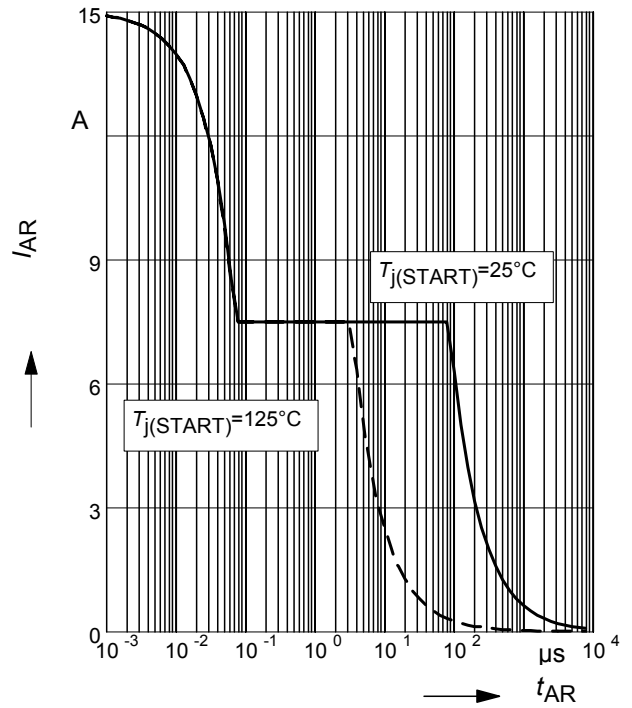
parameter: T_j , $t_p = 10 \mu s$



14 Avalanche SOA

$$I_{AR} = f(t_{AR})$$

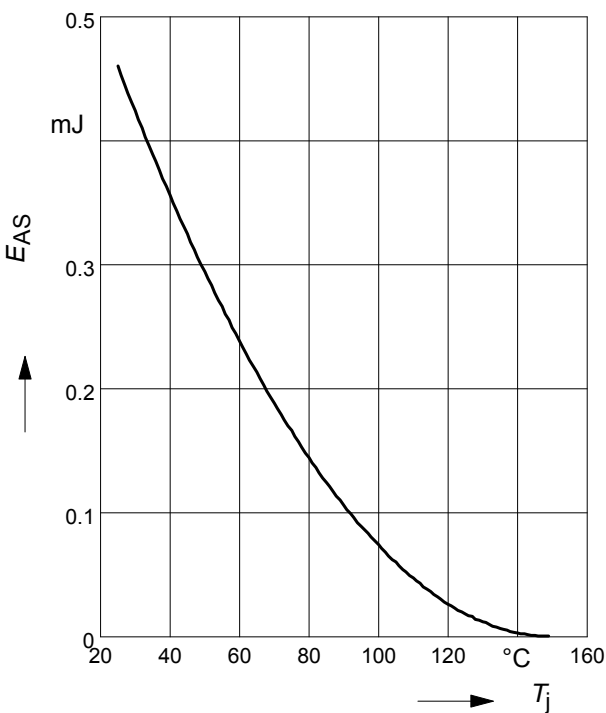
par.: $T_j \leq 150 \text{ °C}$



15 Avalanche energy

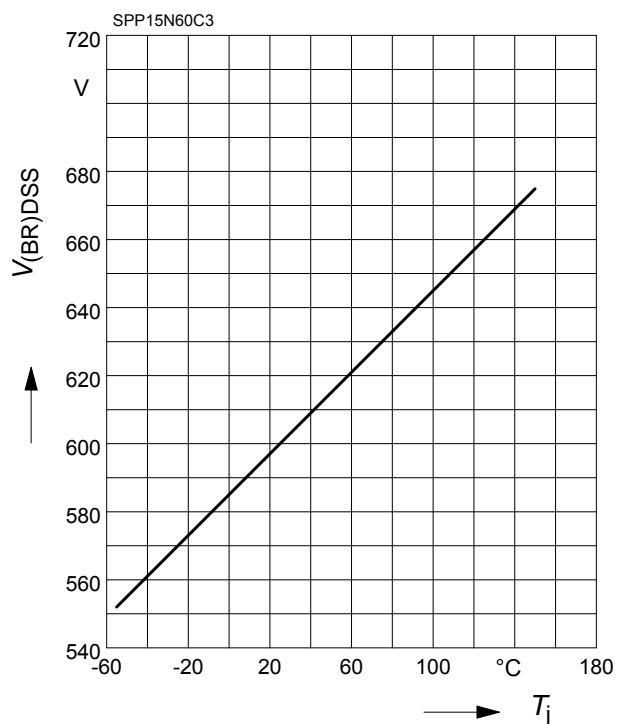
$$E_{AS} = f(T_j)$$

par.: $I_D = 7.5 \text{ A}$, $V_{DD} = 50 \text{ V}$



16 Drain-source breakdown voltage

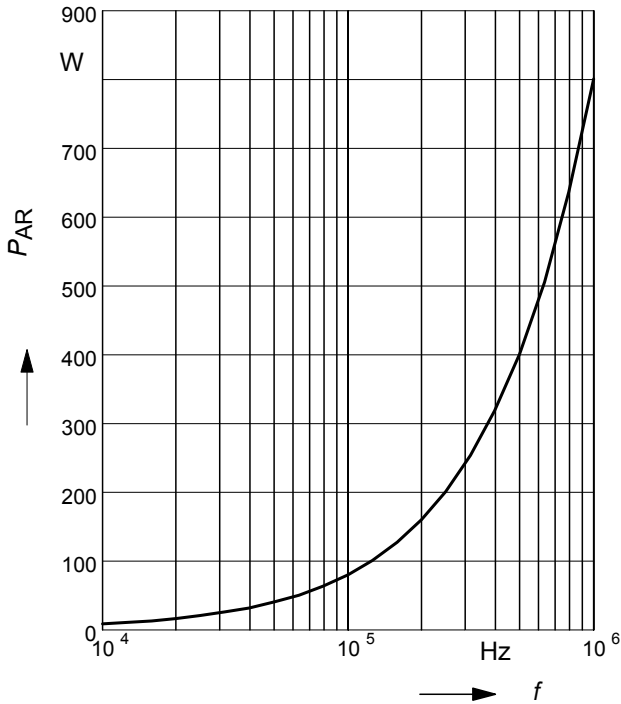
$$V_{(BR)DSS} = f(T_j)$$



17 Avalanche power losses

$$P_{AR} = f(f)$$

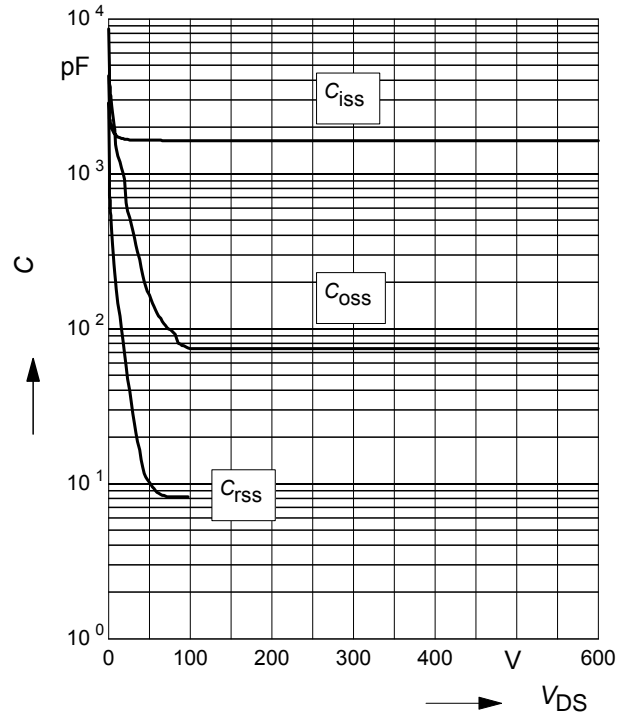
parameter: $E_{AR}=0.8\text{mJ}$



18 Typ. capacitances

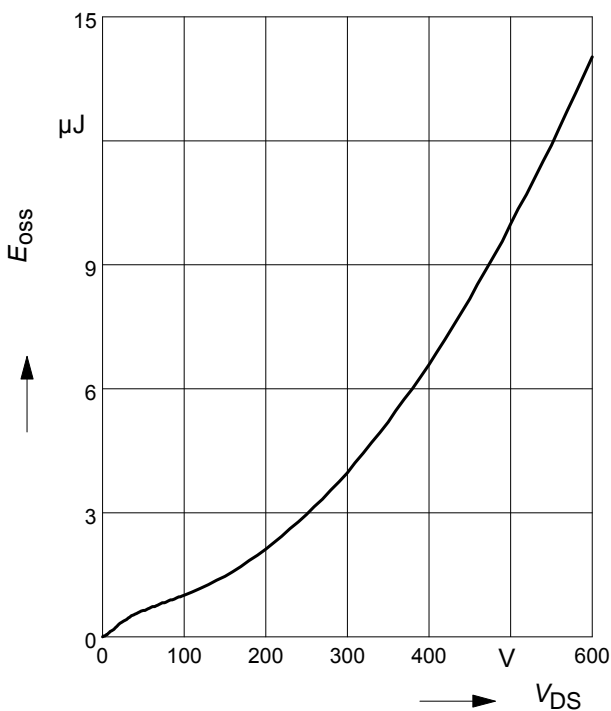
$$C = f(V_{DS})$$

parameter: $V_{GS}=0\text{V}$, $f=1\text{ MHz}$

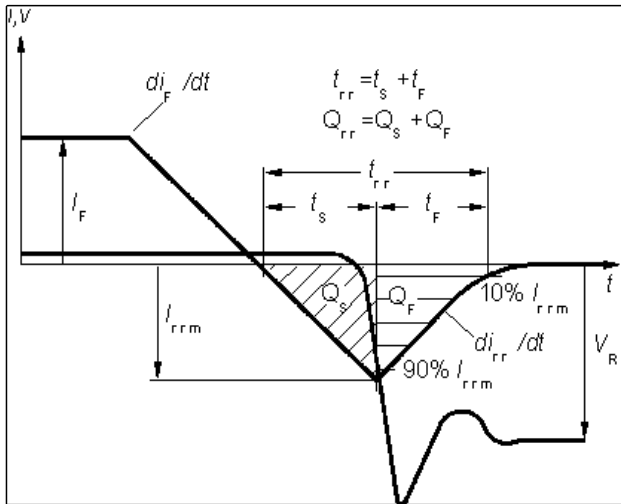


19 Typ. C_{oss} stored energy

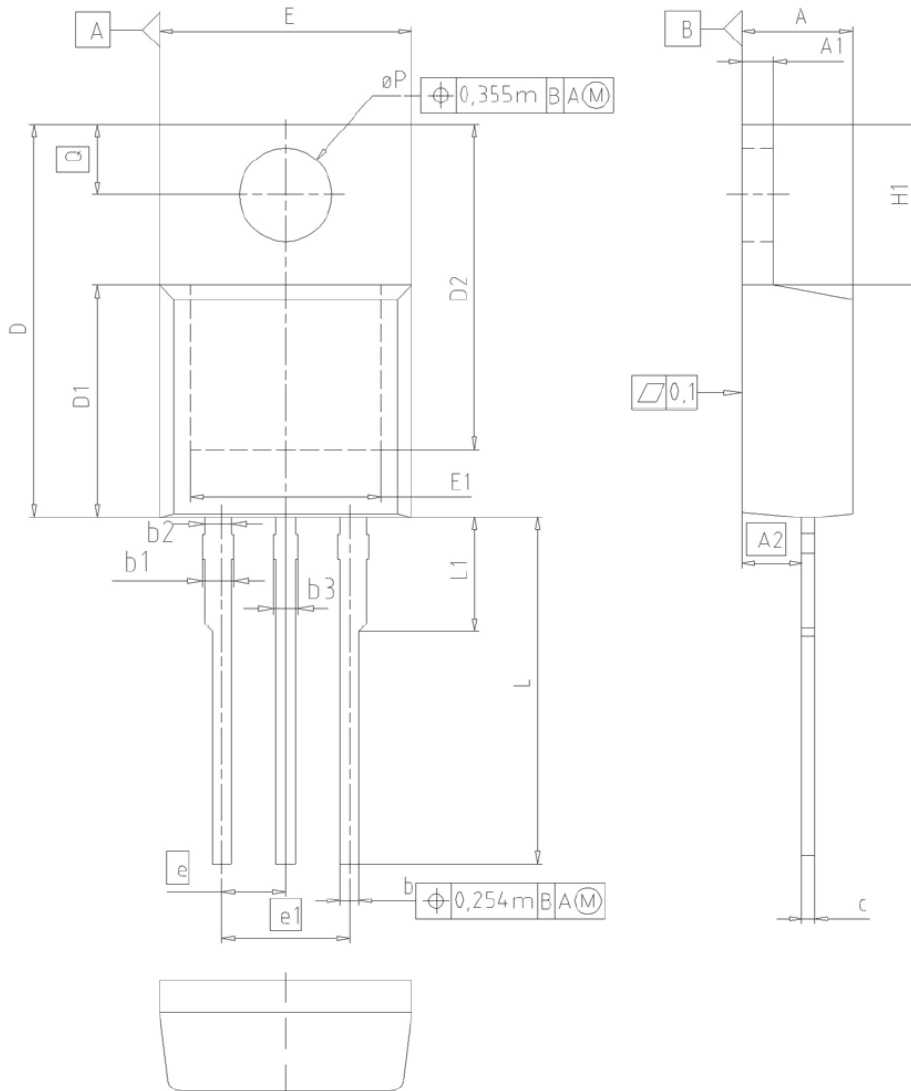
$$E_{Oss} = f(V_{DS})$$



Definition of diodes switching characteristics



PG-TO220-3-1, PG-TO220-3-21 : Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.30	4.57	0.169	0.180
A1	1.17	1.40	0.046	0.055
A2	2.15	2.72	0.085	0.107
b	0.65	0.86	0.026	0.034
b1	0.95	1.40	0.037	0.055
b2	0.95	1.15	0.037	0.045
b3	0.65	1.15	0.026	0.045
c	0.33	0.60	0.013	0.024
D	14.81	15.95	0.583	0.628
D1	8.51	9.45	0.335	0.372
D2	12.19	13.10	0.480	0.516
E	9.70	10.36	0.382	0.408
E1	6.50	8.60	0.256	0.339
e	2.54		0.100	
e1	5.08		0.200	
N	3		3	
H1	5.90	6.90	0.232	0.272
L	13.00	14.00	0.512	0.551
L1	-	4.80	-	0.189
ϕP	3.60	3.89	0.142	0.153
Q	2.60	3.00	0.102	0.118

DOCUMENT NO.
Z8B00003318

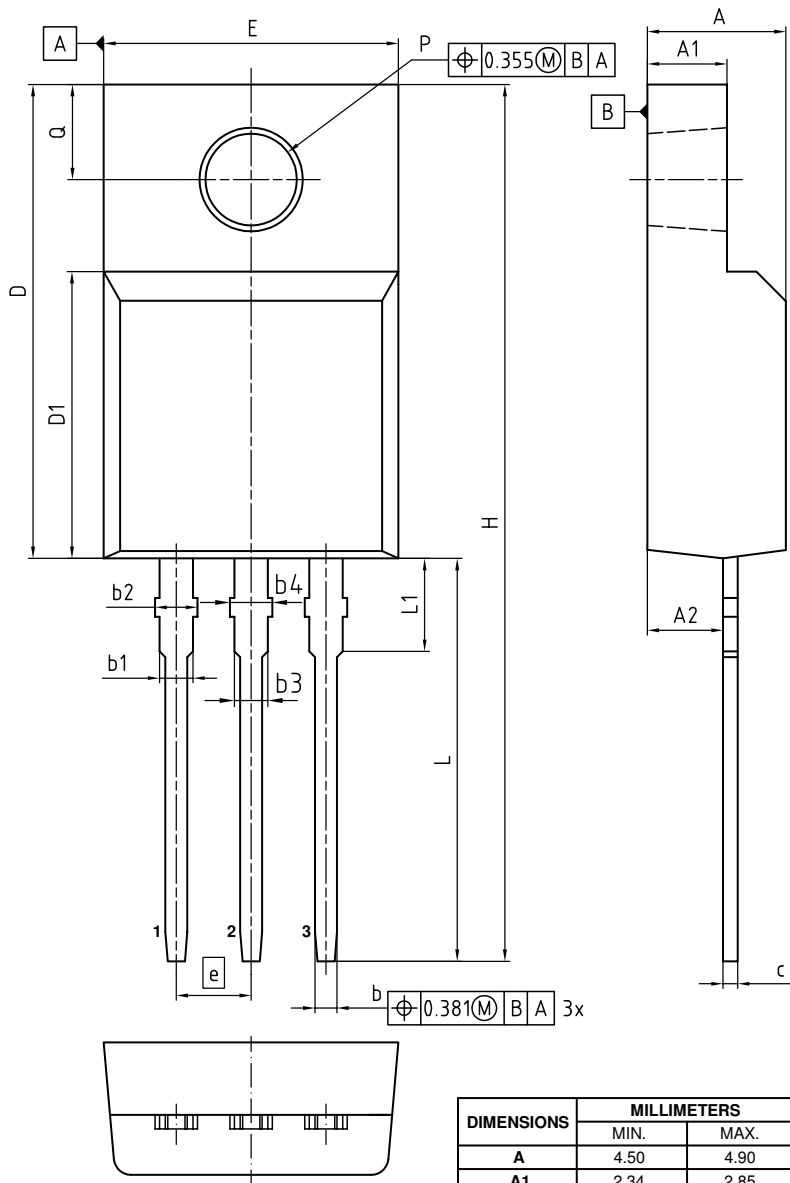
SCALE

EUROPEAN PROJECTION

ISSUE DATE
23-08-2007

REVISION
05

Outline PG-TO220 FullPAK

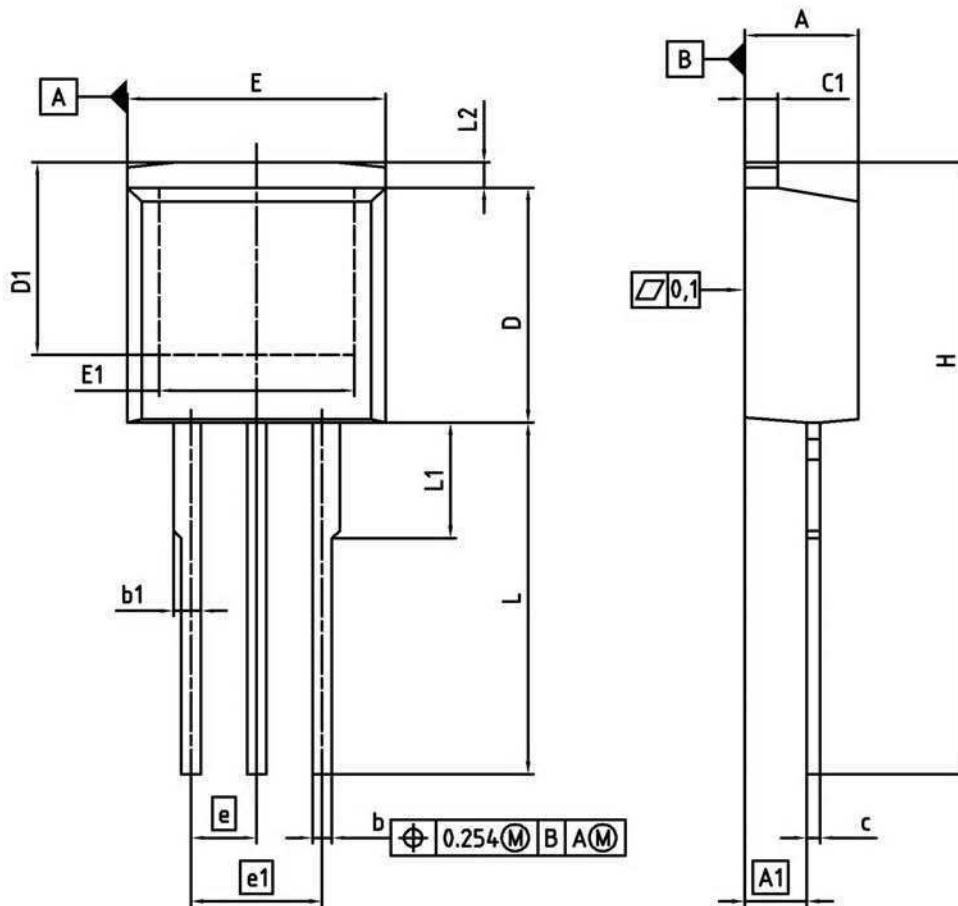


NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD TO-281
AND DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS
OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.50	4.90
A1	2.34	2.85
A2	2.42	2.86
b	0.65	0.90
b1	0.95	1.38
b2	0.95	1.51
b3	0.65	1.38
b4	0.65	1.51
c	0.40	0.63
D	15.67	16.15
D1	8.97	9.83
E	10.00	10.65
e	2.54	
H	28.70	29.75
L	12.78	13.75
L1	2.83	3.45
øP	3.00	3.30
Q	3.15	3.50

DOCUMENT NO. Z8B00003319
REVISION 07
SCALE 5:1 0 1 2 3 4 5mm
EUROPEAN PROJECTION
ISSUE DATE 27.01.2017

PG-TO262-3-1/PG-TO262-3-21 (I²-PAK)



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.635	1.400	0.025	0.055
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE
JEDEC TO262

EUROPEAN PROJECTION

ISSUE DATE
05-05-2006

FILE
TO262_1

600V CoolMOS™ C3 Power Transistor

SPx15N60C3

Revision History

SPx15N60C3

Revision: 2018-02-27, Rev. 2.3

Previous Revision

Revision	Date	Subjects (major changes since last revision)
3.3	2018-02-27	Outline PG-TO-220 FullPAK update

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