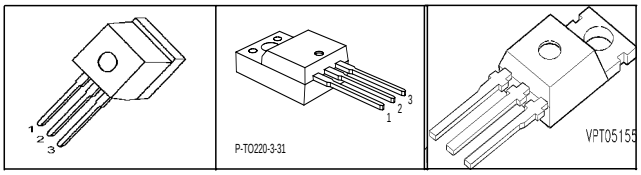
Cool MOS™ Power Transistor

V_{DS}	650	V
$R_{DS(on)}$	0.19	Ω
I_D	20.7	A

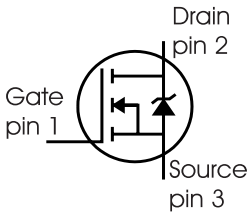
Feature

- New revolutionary high voltage technology
- Worldwide best $R_{DS(on)}$ in TO 220
- Ultra low gate charge
- Periodic avalanche rated
- Extreme d*v*/d*t* rated
- High peak current capability
- Improved transconductance
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[0)] for target applications

PG-TO262 PG-TO220FP PG-TO220



Type	Package	Ordering Code	Marking
SPP20N65C3	PG-TO220	Q67040-S4556	20N65C3
SPA20N65C3	PG-TO220FP	SP000216362	20N65C3
SPI20N65C3	PG-TO262	Q67040-S4560	20N65C3



Maximum Ratings

Parameter	Symbol	Value		Unit
		SPP_I	SPA	
Continuous drain current	I_D			A
T_C = 25 °C		20.7	20.7[1)]	
T_C = 100 °C		13.1	13.1[1)]	
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\ puls}$	62.1	62.1	A
Avalanche energy, single pulse	E_{AS}	690	690	mJ
I_D=3.5A, V_{DD}=50V				
Avalanche energy, repetitive t_{AR} limited by T_{jmax}[2)]	E_{AR}	1	1	
I_D=7A, V_{DD}=50V				
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	7	7	A
Gate source voltage	V_{GS}	±20	±20	V
Gate source voltage AC (f >1Hz)	V_{GS}	±30	±30	
Power dissipation, T_C = 25°C	P_{tot}	208	34.5	W
Operating and storage temperature	T_j , T_{stg}	-55...+150		°C

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope V_{DS} = 480 V, I_D = 20.7 A, T_j = 125 °C	d*v*/d*t*	50	V/ns

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	0.6	K/W
Thermal resistance, junction - case, FullPAK	R_{thJC_FP}	-	-	3.6	
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
Thermal resistance, junction - ambient, FullPAK	R_{thJA_FP}	-	-	80	
SMD version, device on PCB: @ min. footprint @ 6 cm^2 cooling area [3)]	R_{thJA}	 - -	 - 35	 62 -	
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s	T_{sold}	-	-	260	°C

Electrical Characteristics, at T_j=25°C unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=0.25mA	650	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	V_{GS}=0V, I_D=7A	-	730	-	
Gate threshold voltage	$V_{GS(th)}$	I_D=1000µA, V_{GS}=V_{DS}	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C T_j=150°C	 - -	 0.1 -	 1 100	µA
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=13.1A T_j=25°C T_j=150°C	 - -	 0.16 0.43	 0.19 -	Ω
Gate input resistance	R_G	*f*=1MHz, open drain	-	0.54	-	

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Transconductance	g_{fs}	$V_{DS}\geq 2*I_D*R_{DS(on)max}$, I_D=13.1A	-	17.5	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	2400	-	pF
Output capacitance	C_{oss}		-	780	-	
Reverse transfer capacitance	C_{rss}		-	50	-	
Effective output capacitance,[4] energy related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0V to 480V	-	83	-	
Effective output capacitance,[5] time related	$C_{o(tr)}$		-	160	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=380V, V_{GS}=0/13V, I_D=20.7A, R_G=3.6Ω, T_j=125	-	10	-	ns
Rise time	t_r	V_{DD}=380V, V_{GS}=0/13V, I_D=20.7A, R_G=3.6Ω	-	5	-	
Turn-off delay time	$t_{d(off)}$		-	67	100	
Fall time	t_f		-	4.5	12	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	V_{DD}=480V, I_D=20.7A	-	11	-	nC
Gate to drain charge	Q_{gd}		-	33	-	
Gate charge total	Q_g	V_{DD}=480V, I_D=20.7A, V_{GS}=0 to 10V	-	87	114	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=480V, I_D=20.7A	-	5.5	-	V

[0]J-STD20 and JESD22

[1]Limited only by maximum temperature

[2]Repetitve avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

[3]Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

[4]$C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[5]$C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.