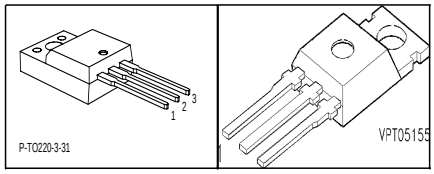
Cool MOS™ Power Transistor

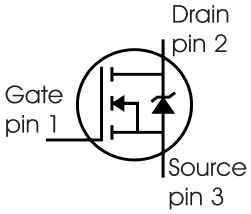
V_{DS} @ T_{jmax}	650	V
$R_{DS(on)}$	1.4	Ω
I_D	3.2	A

Feature

- New revolutionary high voltage technology
- Ultra low gate charge
- Periodic avalanche rated
- Extreme d*v*/d*t* rated
- High peak current capability
- Improved transconductance
- PG-TO-220-3-31;-3-111: Fully isolated package (2500 VAC; 1 minute)
- Pb-free lead plating; RoHS compliant
- Qualified according to JEDEC[0)] for target applications

PG-TO220FP PG-TO220





Type	Package	Ordering Code	Marking
SPP03N60C3	PG-TO220	Q67040-S4401	03N60C3
SPA03N60C3	PG-TO220FP	SP000216296	03N60C3

Maximum Ratings

Parameter	Symbol	Value		Unit
		SPP	SPA	
Continuous drain current	I_D			A
T_C = 25 °C		3.2	3.2[1)]	
T_C = 100 °C		2	2[1)]	
Pulsed drain current, t_p limited by T_{jmax}	$I_{D\ puls}$	9.6	9.6	A
Avalanche energy, single pulse	E_{AS}	100	100	mJ
I_D=2.4A, V_{DD}=50V				
Avalanche energy, repetitive t_{AR} limited by T_{jmax}[2)]	E_{AR}	0.2	0.2	
I_D=3.2A, V_{DD}=50V				
Avalanche current, repetitive t_{AR} limited by T_{jmax}	I_{AR}	3.2	3.2	A
Gate source voltage static	V_{GS}	±20	±20	V
Gate source voltage AC (f >1Hz)	V_{GS}	±30	±30	
Power dissipation, T_C = 25°C	P_{tot}	38	29.7	W
Operating and storage temperature	T_j , T_{stg}	-55...+150		°C
Reverse diode dv/dt [7)]	dv/dt	15		V/ns

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Source voltage slope V_{DS} = 480 V, I_D = 3.2 A, T_j = 125 °C	dv/dt	50	V/ns

Thermal Characteristics

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
Thermal resistance, junction - case	R_{thJC}	-	-	3.3	K/W
Thermal resistance, junction - case, FullPAK	R_{thJC_FP}	-	-	4.1	
Thermal resistance, junction - ambient, leaded	R_{thJA}	-	-	62	
Thermal resistance, junction - ambient, FullPAK	R_{thJA_FP}	-	-	80	
SMD version, device on PCB: @ min. footprint @ 6 cm^2 cooling area [3]	R_{thJA}	 - -	 - 35	 62 -	
Soldering temperature, wavesoldering 1.6 mm (0.063 in.) from case for 10s [4]	T_{sold}	-	-	260	°C

Electrical Characteristics, at T_j=25°C unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=0.25mA	600	-	-	V
Drain-Source avalanche breakdown voltage	$V_{(BR)DS}$	V_{GS}=0V, I_D=3.2A	-	700	-	
Gate threshold voltage	$V_{GS(th)}$	I_D=135µA, V_{GS}=V_{DS}	2.1	3	3.9	
Zero gate voltage drain current	I_{DSS}	V_{DS}=600V, V_{GS}=0V, T_j=25°C T_j=150°C	 - -	 0.5 -	 1 70	µA
Gate-source leakage current	I_{GSS}	V_{GS}=30V, V_{DS}=0V	-	-	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=2A T_j=25°C T_j=150°C	 - -	 1.26 3.8	 1.4 -	Ω
Gate input resistance	R_G	f=1MHz, open drain	-	10	-	

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Transconductance	g_{fs}	$V_{DS}\geq 2*I_D*R_{DS(on)max}$, I_D=2A	-	3.4	-	S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V, f=1MHz	-	400	-	pF
Output capacitance	C_{oss}		-	150	-	
Reverse transfer capacitance	C_{rss}		-	5	-	
Effective output capacitance,[5] energy related	$C_{o(er)}$	V_{GS}=0V, V_{DS}=0V to 480V	-	12	-	
Effective output capacitance,[6] time related	$C_{o(tr)}$		-	26	-	
Turn-on delay time	$t_{d(on)}$	V_{DD}=350V, V_{GS}=0/10V, I_D=3.2A, R_G=20Ω	-	7	-	ns
Rise time	t_r		-	3	-	
Turn-off delay time	$t_{d(off)}$		-	64	100	
Fall time	t_f		-	12	20	

Gate Charge Characteristics

Gate to source charge	Q_{gs}	V_{DD}=420V, I_D=3.2A	-	2	-	nC
Gate to drain charge	Q_{gd}		-	6	-	
Gate charge total	Q_g	V_{DD}=420V, I_D=3.2A, V_{GS}=0 to 10V	-	13	17	
Gate plateau voltage	$V_{(plateau)}$	V_{DD}=420V, I_D=3.2A	-	5.5	-	V

[0]J-STD20 and JESD22

[1]Limited only by maximum temperature

[2]Repetitve avalanche causes additional power losses that can be calculated as $P_{AV}=E_{AR}*f$.

[3]Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical without blown air.

[4]Soldering temperature for TO-263: 220°C, reflow

[5]$C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[6]$C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

[7]I_{SD}<=I_D, di/dt<=400A/us, V_{DClink}=400V, V_{peak}<$V_{BR, DSS}$, T_j<$T_{j,max}$.
Identical low-side and high-side switch.