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SPG032D970R3R

2M x 16 bit Asynchronous pSRAM

Features

- Organization: 2M × 16 bit
- Power Supply Voltage: 2.7 ~ 3.6V
- Three state outputs
- Byte read/write control by UB# / LB#
- Auto-TCSR for power saving
- 8 page mode
- Deep Power Down (DPD) support

General Description

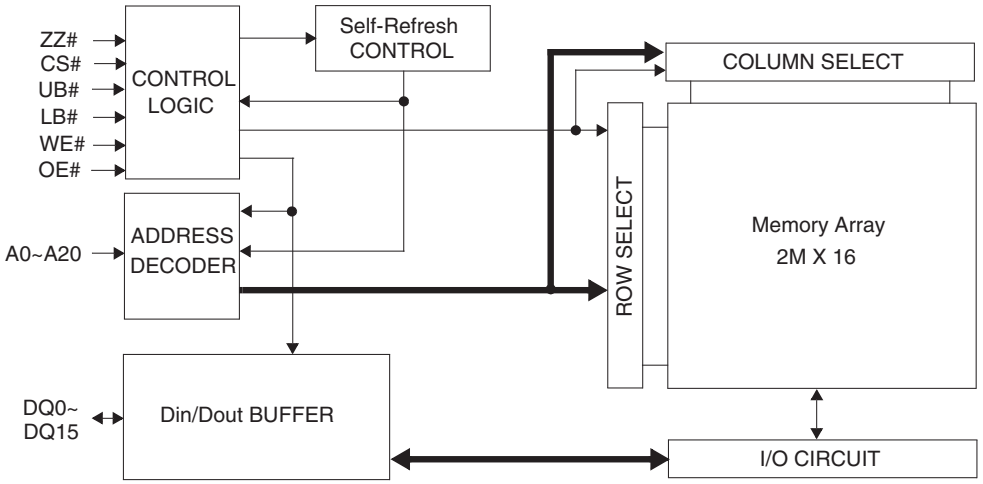
The SPG032D970R3R is 33,554,432 bits of Pseudo SRAM which uses DRAM type memory cells, with on-chip self-refresh control. The interface is compatible to a low power asynchronous SRAM.

The SPG032D970R3R is organized as 2,097,152 Words × 16 bit.

Device Features

Operating Temp	Power Supply	Speed (t_{RC})	Power Dissipation		
			Standby (ISB, Max.)	Operating ICC (Max.)	
				ICC1 (f = 1 MHz)	ICC2 (f = f_{max})
–40°C to 85°C	2.7V to 3.6V	70 ns	120 µA	5 mA	25 mA

Functional Block Diagram



Pad Description

Name	Function	Name	Function
CS#	Chip select input	LB#	Lower byte ($DQ_{0\sim7}$)
OE#	Output enable input	UB#	Upper byte ($DQ_{8\sim15}$)
WE#	Write enable input	VCC	Power supply
ZZ#	Low power control	VCCQ	I/O power supply
$DQ_{0\text{-}15}$	Data in-out	VSS(Q)	Ground
$A_{0\text{-}20}$	Address inputs	—	—

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	–0.2 to V_{CCQ}+0.3V	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}, V_{CCQ}	–0.2 (Note 2) to V_{CCQ} +0.3V	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{STG}	–65 to 150	^oC
Operating Temperature	T_A	–40 to 85	^oC

Notes:

1. *Stresses greater than those listed above "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*
2. *Undershoot at power-off: -1.0V in case of pulse width ≤ 20 ns.*

1. Functional Description

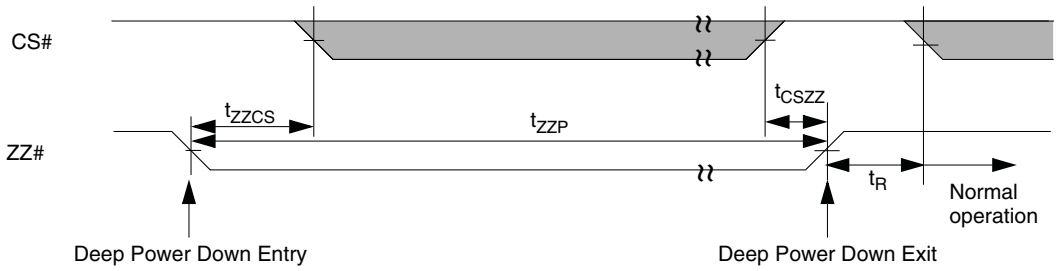
Table 1. Bus Operations

CS#	ZZ#	OE#	WE#	LB#	UB#	$DQ_{0\sim7}$	$DQ_{8\sim15}$	Mode	Power
H	H	X	X	X	X	High-Z	High-Z	Deselected	Standby
X	L	X	X	X	X	High-Z	High-Z	Deselected	Low Power Mode
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	Data Out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	Data Out	Upper Byte Read	Active
L	H	L	H	L	L	Data Out	Data Out	Word Read	Active
L	H	X	L	L	H	Data In	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	Data In	Upper Byte Write	Active
L	H	X	L	L	L	Data In	Data In	Word Write	Active

Note:
1. X means don't care. (Must be low or high state).

2. Low Power Modes

Figure 1. Deep Power Down



Notes (Deep Power Down):
1. During Deep Power Down mode, all refresh related activity is disabled.

Table 2. Low Power Modes

Parameter	Description	Min	Max	Units
t_{ZZCS}	ZZ# low to CS# low	0	–	ns
t_{CSZZ}	CS# high to ZZ# high	0	–	ns
t_R	Operation Recovery Time	200	–	µs
t_{ZZP}	ZZ# pulse width	20	–	ns

Table 3. Low Power Mode Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Deep Power Down Current	I_{ZZ}	ZZ# ≤ 0.2V, Other inputs = 0 ~ V_{CCQ} (Max. condition: V_{CC} = 3.6V @ 85°C)	–	–	10	µA

3. Electrical Characteristics

Table 4. Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.3	3.6	V
	V_{CCQ}	2.7	3.3	3.6	V
Ground	V_{SS}, V_{SSQ}	0	0	0	V
Input high voltage	V_{IH}	0.7 x V_{CCQ}	–	V_{CCQ} + 0.2 (2)	V
Input low voltage	V_{IL}	–0.2 (3)	–	0.2 x V_{CCQ}	V

Notes:
1. *T_A= –40°C to 85°C, otherwise specified*
2. *Overshoot: V_{CC} +1.0 V in case of pulse width ≤ 20 ns*
3. *Undershoot: –1.0 V in case of pulse width ≤ 20 ns*
4. *Overshoot and undershoot are sampled, not 100% tested.*

Table 5. Capacitance (f =1 MHz, T_A=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	–	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	–	8	pF

Note:
1. *Capacitance is sampled, not 100% tested.*

Table 6. DC and Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN} = V_{SS} to V_{CCQ}, V_{CC} = V_{CCmax}	–1	–	1	µA
Output leakage current	I_{LO}	CS# = V_{IH}, ZZ# = V_{IH}, OE# = V_{IH} or WE# = V_{IL}, V_{IO} = V_{SS} to V_{CCQ}, V_{CC} = V_{CCmax}	–1	–	1	µA
Average operating current	I_{CC1}	Cycle time = 1 µs, I_{IO} = 0 mA,100% duty, CS# ≤ 0.2V, ZZ# ≥ V_{CCQ}–0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CCQ}–0.2V	–	–	5	mA
	I_{CC2}	Cycle time = Min, I_{IO} = 0 mA, 100% duty, CS# = V_{IL}, ZZ# = V_{IH}, V_{IN} = V_{IL} or V_{IH}	–	–	25	mA
Page access operating current	I_{CCP}	t_{PC} = Min, CS# = V_{IL}, ZZ# = V_{IH}, I_{IO} = 0 mA, Page add. cycling.	–	–	15	mA
Output low voltage	V_{OL}	I_{OL} = 0.5 mA, V_{CC} = V_{CCmin}	–	–	0.2 x V_{CCQ}	V
Output high voltage	V_{OH}	I_{OH} = –0.5 mA, V_{CC} = V_{CCmin}	0.8 x V_{CCQ}	–	–	V
Standby Current (CMOS)	I_{SB}	CS#, ZZ# ≥ V_{CCQ}-0.2V, Other inputs = 0~V_{CCQ} (Max. condition: V_{CC} = 3.6V at 85 °C)	–	–	120	µA

Note:
1. *Maximum I_{CC} specifications are tested with V_{CC} = V_{CCmax}*

3.1 AC Operating Conditions

Test Conditions (Test Load and Test Input/Output Reference)

- Input Pulse Level: 0.2V to V_{CCQ}-0.2V
- Input Rise and Fall Time: 5 ns
- Input and Output Reference Voltage: $V_{CCQ}/2$
- Output Load: CL(1) = 30 pF (See Figure 2)

Note:
1. Including scope and Jig capacitance.

Figure 2. Output Load

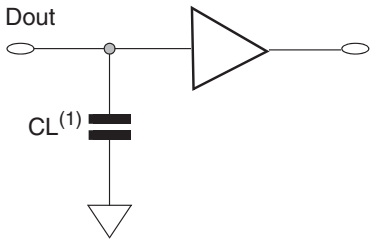


Table 7. AC Characteristics

Parameter List		Symbol	Speed		Unit
			Min	Max	
Read	Read Cycle Time	t_{RC}	70	10,000	ns
	Address access time	t_{AA}	—	70	ns
	Chip enable to data output	t_{CO}	—	70	ns
	Output enable to valid output	t_{OE}	—	25	ns
	UB#, LB# enable to data output	t_{BA}	—	25	ns
	Chip enable to low-Z output	t_{LZ}	10	—	ns
	UB#, LB# enable to low-Z output	t_{BLZ}	0	—	ns
	Output enable to low-Z output	t_{OLZ}	0	—	ns
	Chip disable to high-Z output	t_{HZ}	0	20	ns
	UB#, LB# disable to high-Z output	t_{BHZ}	0	20	ns
	Output disable to high-Z output	t_{OHZ}	0	20	ns
	Output hold from Address change	t_{OH}	5	—	ns
Write	Write Cycle Time	t_{WC}	70	10,000	ns
	Chip enable to end of write	t_{CW}	60	—	ns
	Address setup time	t_{AS}	0	—	ns
	Address valid to end of write	t_{AW}	60	—	ns
	UB#, LB# valid to end of write	t_{BW}	60	—	ns
	Write pulse width	t_{WP}	50	—	ns
	Write recovery time	t_{WR}	0	—	ns
	Write to output high-Z	t_{WHZ}	0	20	ns
	Data to write time overlap	t_{DW}	20	—	ns
	Data hold from write time	t_{DH}	0	—	ns
	End write to output low-Z	t_{OW}	5	—	ns
Page	Maximum cycle time	t_{MRC}	—	10,000	ns
	Page mode cycle time	t_{PC}	25	—	ns
	Page mode address access time	t_{PAA}	—	25	ns

4. Timing Diagrams

Figure 3. Read Cycle (1) (Address controlled, CS#=OE#=V_{IL}, ZZ#=WE#=V_{IH}, UB# or/and LB#=V_{IL})

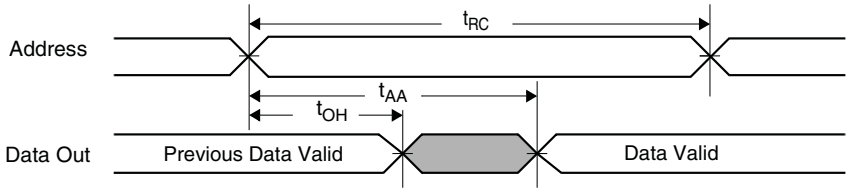
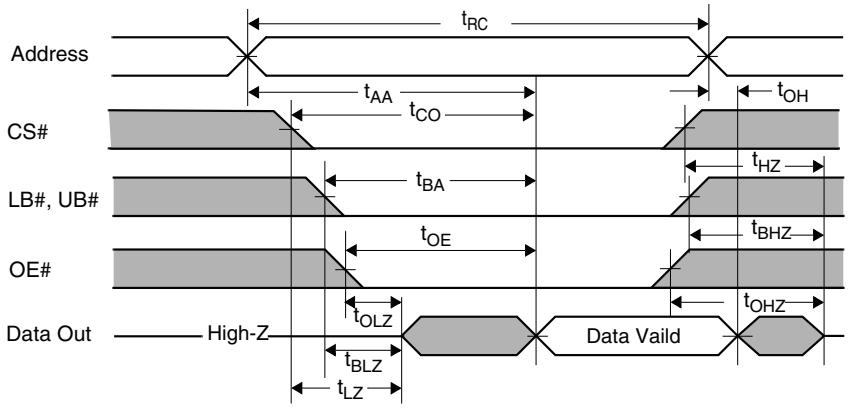


Figure 4. Read Cycle (2) (ZZ#=WE#=V_{IH})



Note: (Read Cycle 1, 2)

1. *t_{HZ}, t_{BHZ}, and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
2. *Do not Access device with cycle timing shorter than t_{RC} for continuous periods > 10 µs.*

Figure 5. Write Cycle (1) (WE# controlled, ZZ#=V_{IH})

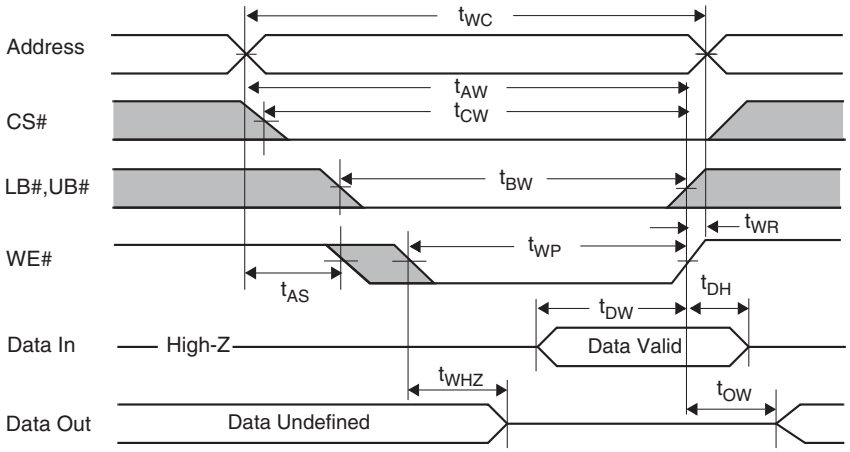


Figure 6. Write Cycle (2) (CS# controlled, ZZ#=V_{IH})

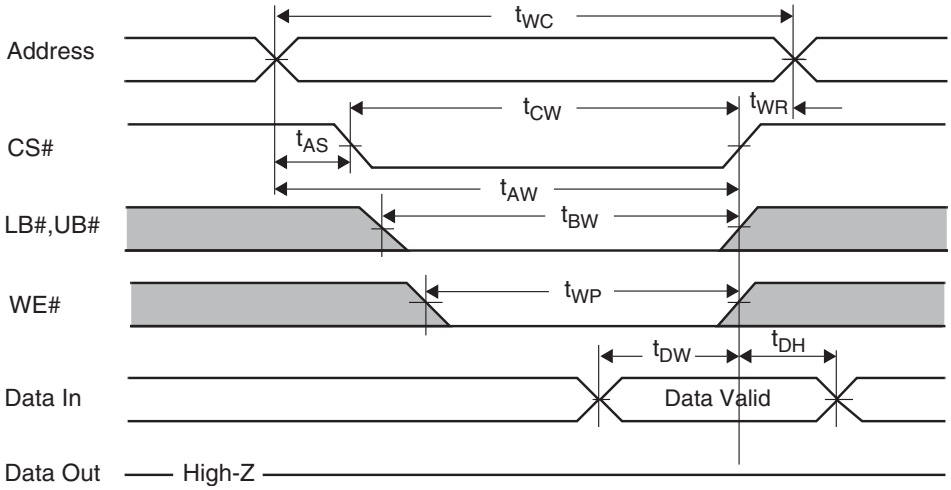
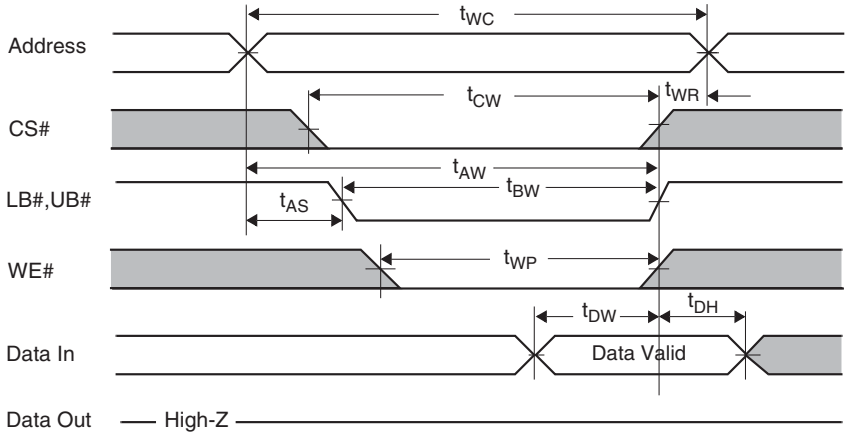


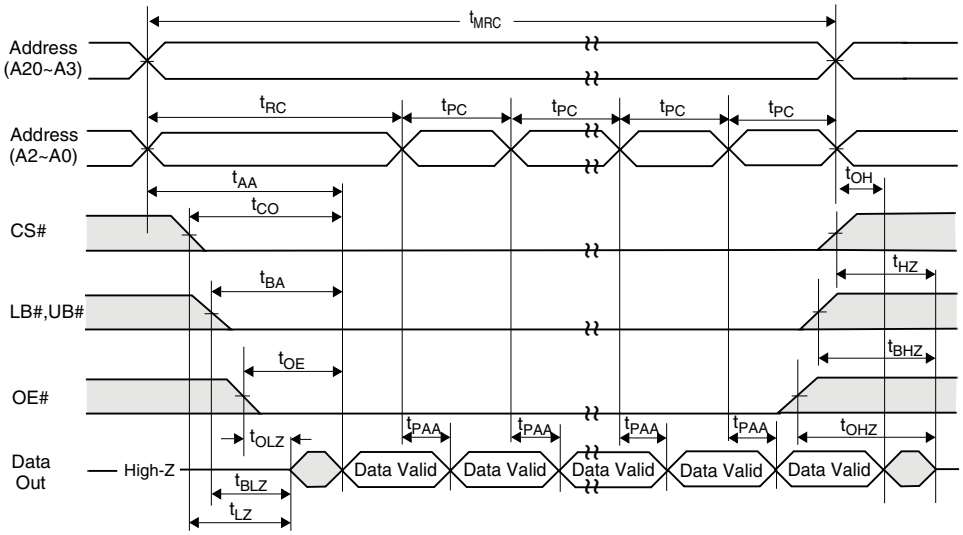
Figure 7. Write Cycle (3) (UB#/LB# controlled, ZZ#=V_{IH})



Notes (Write Cycle):

1. *A write occurs during the overlap (t_{WP}) of low CS#, low WE# and low UB# or LB#. A write begins at the last transition among low CS# and low WE# with asserting UB# or LB# low for single byte operation or simultaneously asserting UB# and LB# low for word operation. A write ends at the earliest transition among high CS# and high WE#. The t_{WP} is measured from the beginning of write to the end of write.*
2. *t_{CW} is measured from CS# going low to end of write.*
3. *t_{AS} is measured from the address valid to the beginning of write.*
4. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CS# or WE# going high.*
5. *Do not access device with cycle timing shorter than t_{WC} for continuous periods > 10 us.*

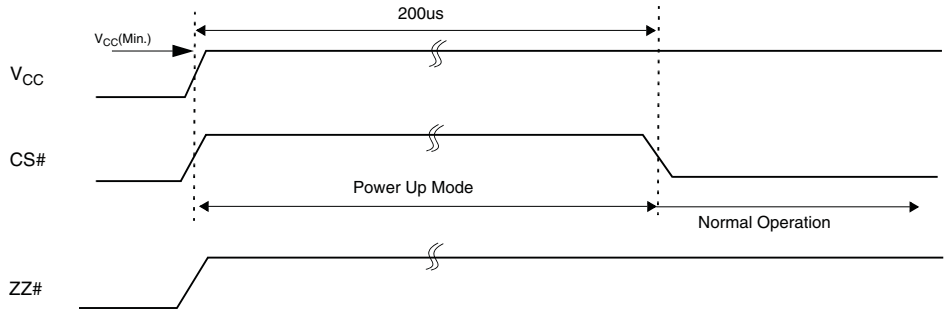
Figure 8. Page Read Cycle (ZZ#=WE#=V_{IH}, 8 Words access)



Notes (Page Read Cycle)

1. *t_{HZ}, t_{BHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
2. *Do not Access device with cycle timing shorter than t_{RC} for continuous periods > 10 µs.*

Figure 9. Timing Waveform of Power Up



Note:

1. *After V_{CC} reaches V_{CC}(Min.), wait 200 µs with CS# high.Then you get into the normal operation.*

Document History

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Section	Description
Revision 01 (August 31, 2009)	
	Initial release

Document Title: SPG032D970R3R, 2M x 16 bit Asynchronous pSRAM Document Number: 002-19563				
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—	—	—	08/31/2009	Initial release.
**	5725329	NFB	05/05/2017	Updated to Cypress template.

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