Small-Signal Transistor

PG-SOT23-3

Features

- N-channel
- Enhancement mode
- Logic level
- dv/dt rated
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC JESD47, JESD22 and J-STD-020.

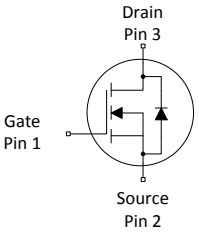


Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$, V_{GS}=10 V	5	Ω
$R_{DS(on),max}$, V_{GS}=4.5 V	7.5	Ω
I_D	0.2	A
ESD Sensitivity, JESD22-A114 (HBM)	Class 0 (<250V)	

Part number	Package	Marking	Related links
SN7002I	PG-SOT23-3	NI	-

Table of contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	0.20	A	V_{GS}=10 V, T_A=25 °C
				0.16		V_{GS}=4.5 V, T_A=70 °C
Pulsed drain current	$I_{D,pulse}$	-	-	0.8	A	T_A=25 °C
Reverse diode dv/dt	dv/dt	-	-	6	kV /µs	I_D=0.2 A, V_{DS}=48 V, di/dt=200 A/µs, $T_{j,max}$=150 °C
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	0.36	W	T_A=25 °C, R_{thJA}=350 °C/W
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - ambient, minimum footprint	R_{thJA}	-	-	350	K/W	-

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=250 µA
Gate threshold voltage	$V_{GS(th)}$	0.8	1.4	1.8	V	V_{DS}=V_{GS}, I_D=26 µA
Zero gate voltage drain current	I_{DSS}	-	-	0.1	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C
				5		V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	10	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	2.3	5	Ω	V_{GS}=10 V, I_D=0.5 A
			3.5	7.5		V_{GS}=4.5 V, I_D=0.17 A
Transconductance	g_{fs}	0.09	0.17	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=0.16 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	32	-	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance	C_{oss}		6.6			
Reverse transfer capacitance	C_{rss}		2.6			
Turn-on delay time	$t_{d(on)}$	-	2.4	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=0.5 A, $R_{G,ext}$=6 Ω
Rise time	t_r		3.2			
Turn-off delay time	$t_{d(off)}$		5.3			
Fall time	t_f		3.6			

Table 6 Gate charge characteristics

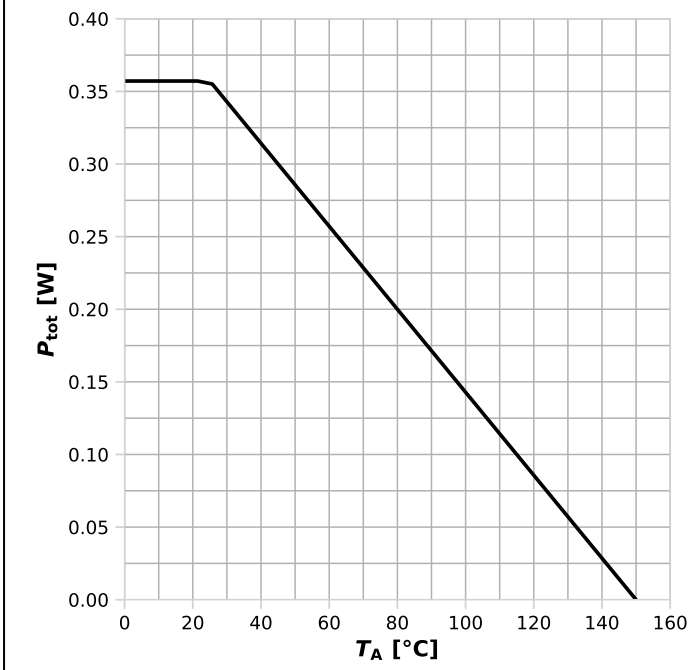
Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	0.14	-	nC	V_{DD}=30 V, I_D=0.5 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}		0.29		nC	
Gate charge total	Q_g		0.9		nC	
Gate plateau voltage	$V_{plateau}$		4.5		V	

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	0.2	A	T_A=25 °C
Diode pulse current	$I_{S,pulse}$			0.8		
Diode forward voltage	V_{SD}	-	0.83	1.2	V	V_{GS}=0 V, I_F=0.2 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	14.2	21.3	ns	V_R=30 V, I_F=0.2 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}		5.9	8.8	nC	

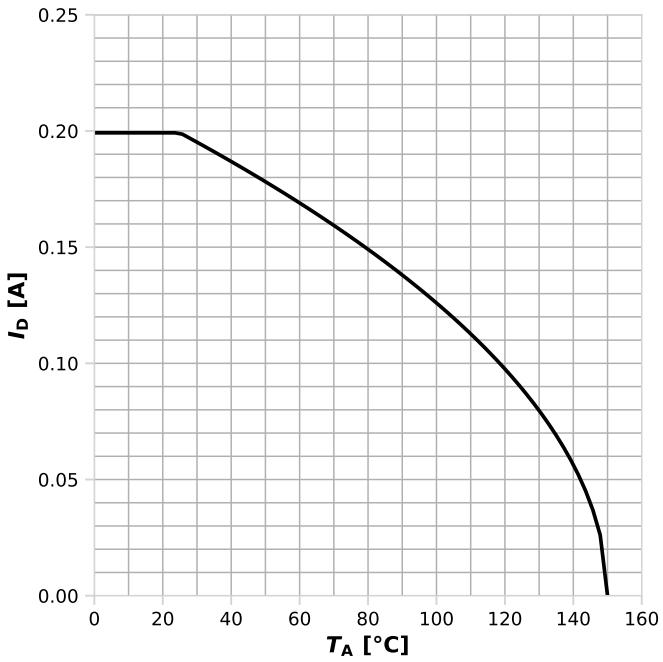
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



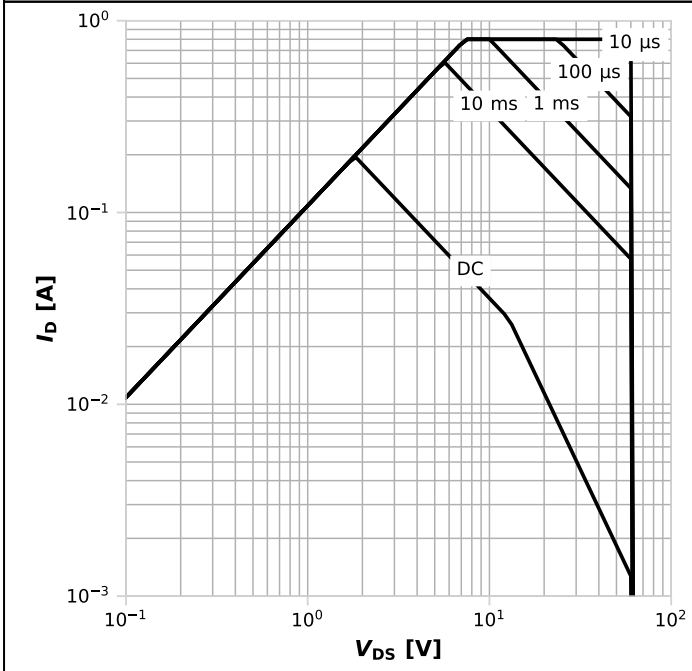
P_{tot}=f(T_A)

Diagram 2: Drain current



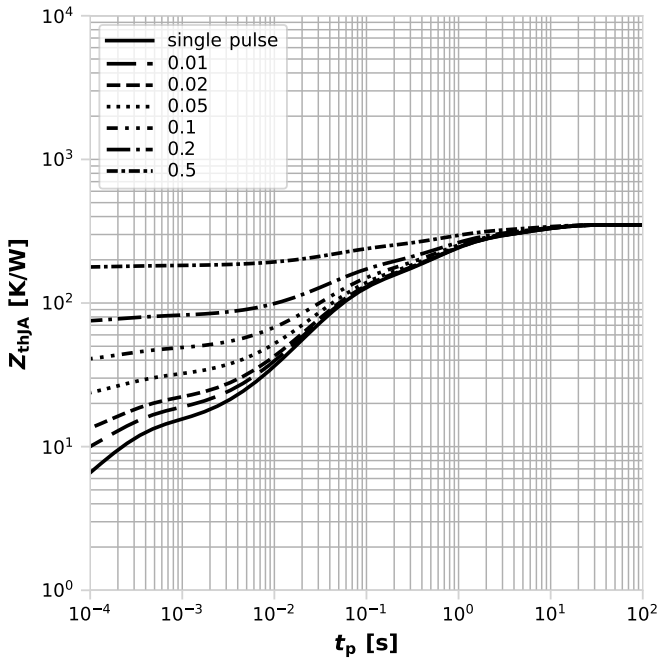
I_D=f(T_A); V_{GS}≥10 V

Diagram 3: Safe operating area



I_D=f(V_{DS}); T_A=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



Z_{thJA}=f(t_p); parameter: D=t_p/T

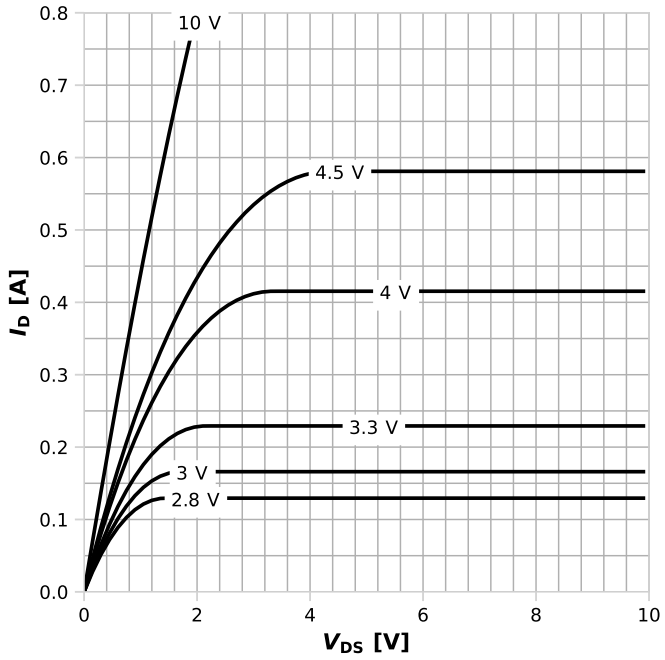
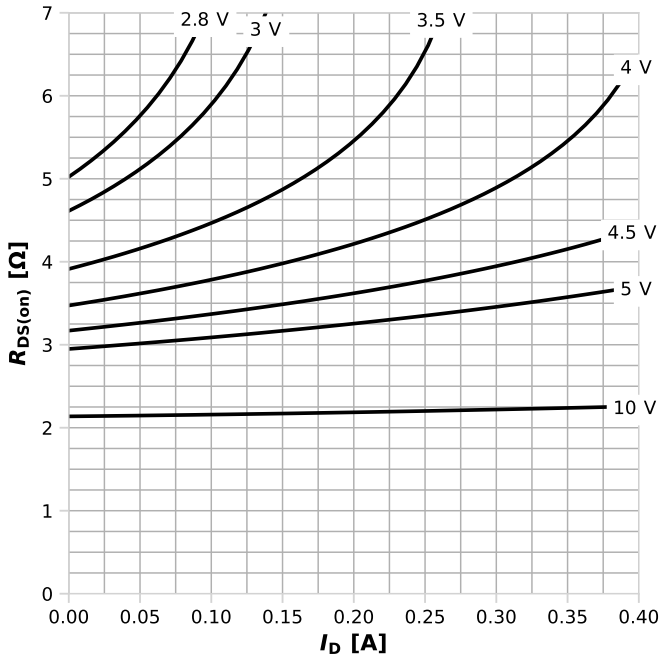
Diagram 5: Typ. output characteristics	Diagram 6: Typ. drain-source on resistance
	
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

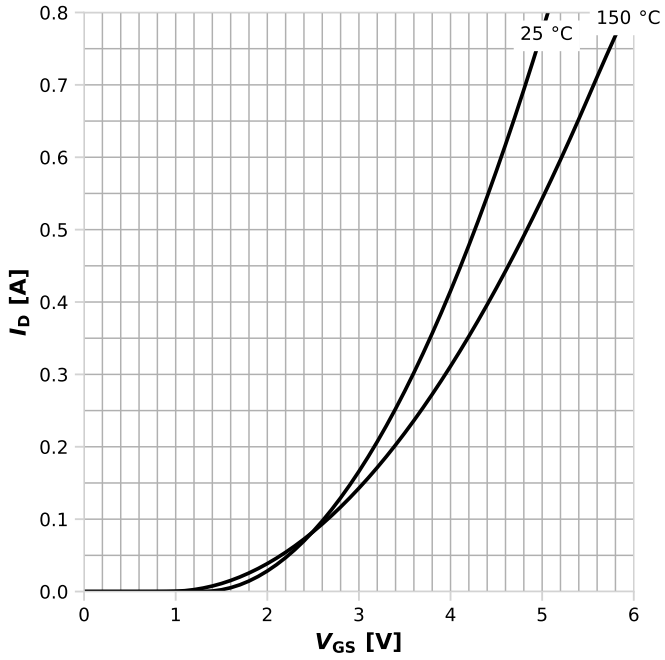
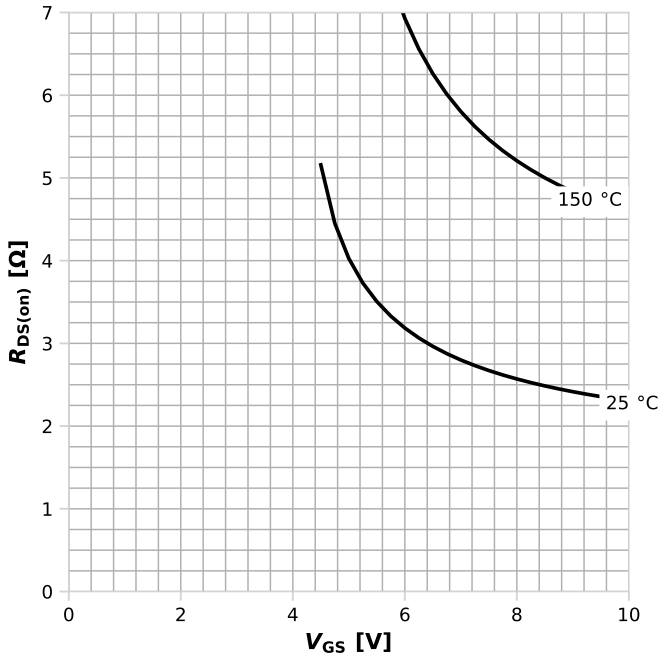
Diagram 7: Typ. transfer characteristics	Diagram 8: Typ. drain-source on resistance
	
I_D=f(V_{GS}), |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j	$R_{DS(on)}$=f(V_{GS}), I_D=0.5 A; parameter: T_j

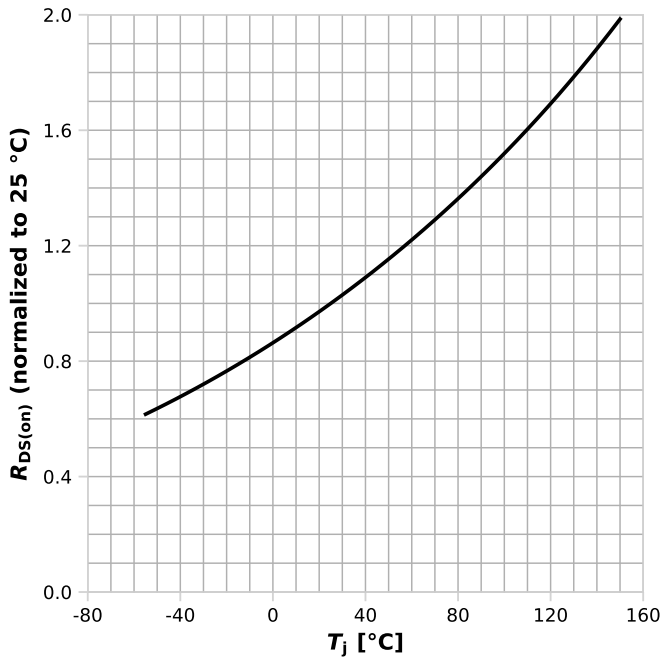
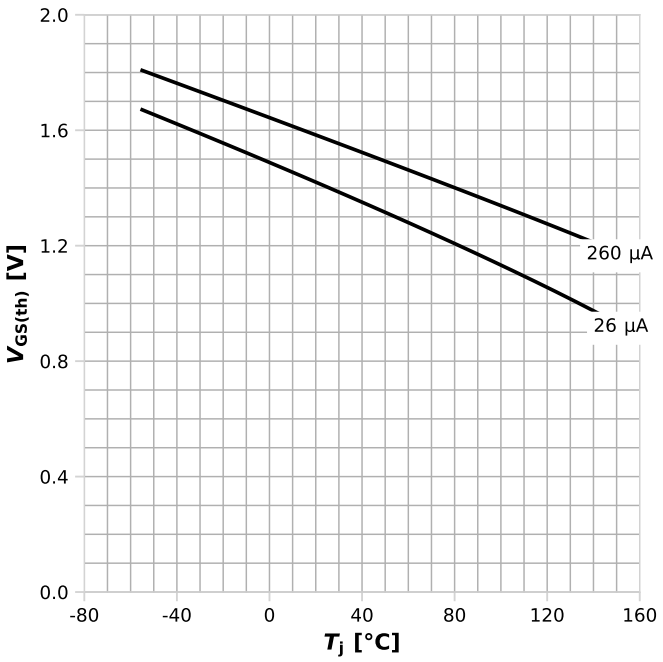
Diagram 9: Normalized drain-source on resistance	Diagram 10: Typ. gate threshold voltage
	
$R_{DS(on)}$=f(T_j), I_D=0.5 A, V_{GS}=10 V	$V_{GS(th}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

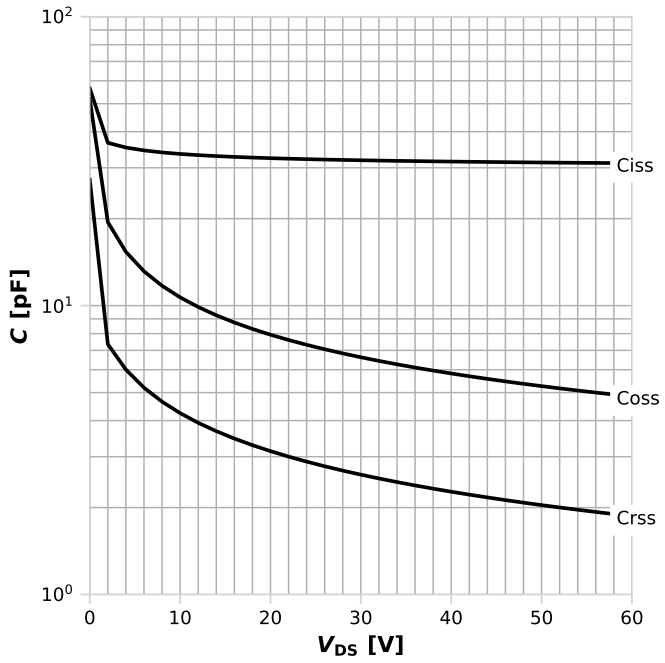
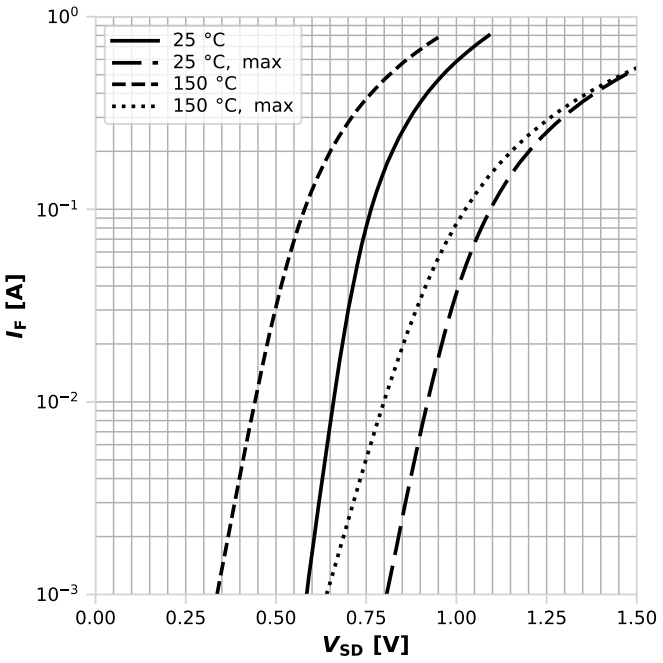
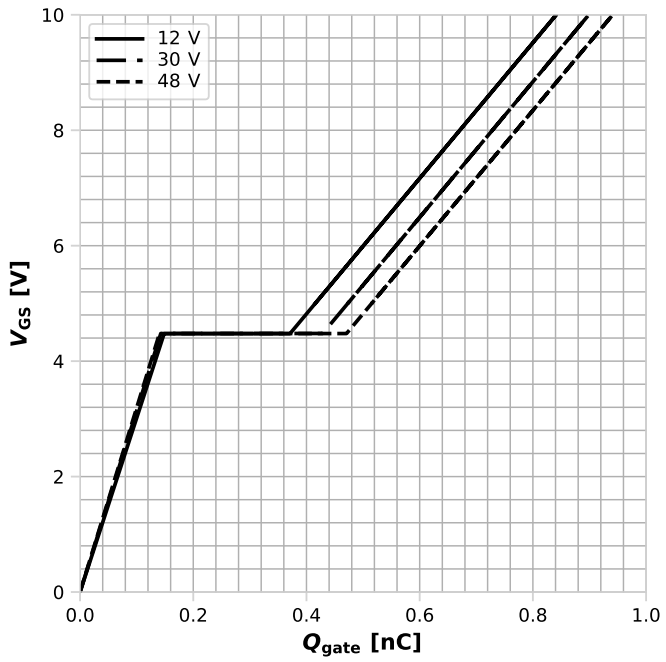
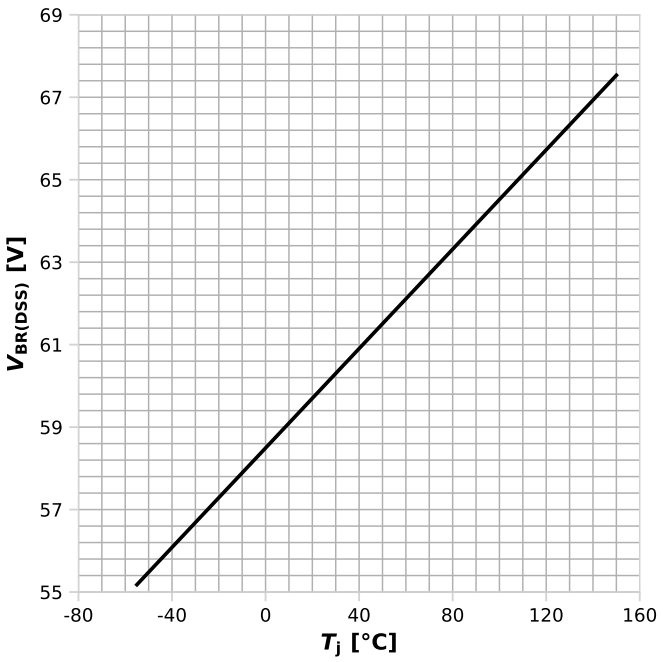
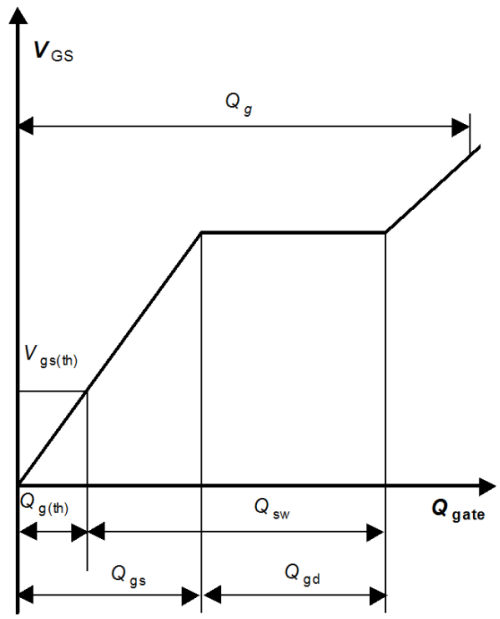
Diagram 11: Typ. capacitances	Diagram 12: Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	I_F=f(V_{SD}); parameter: T_j

Diagram 13: Typ. gate charge	Diagram 14: Drain-source breakdown voltage
	
V_{GS}=f(Q_{gate}), I_D=0.5 A pulsed, T_j=25 °C; parameter: V_{DD}	$V_{BR(DSS)}$=f(T_j); I_D=250 µA

Gate charge waveforms

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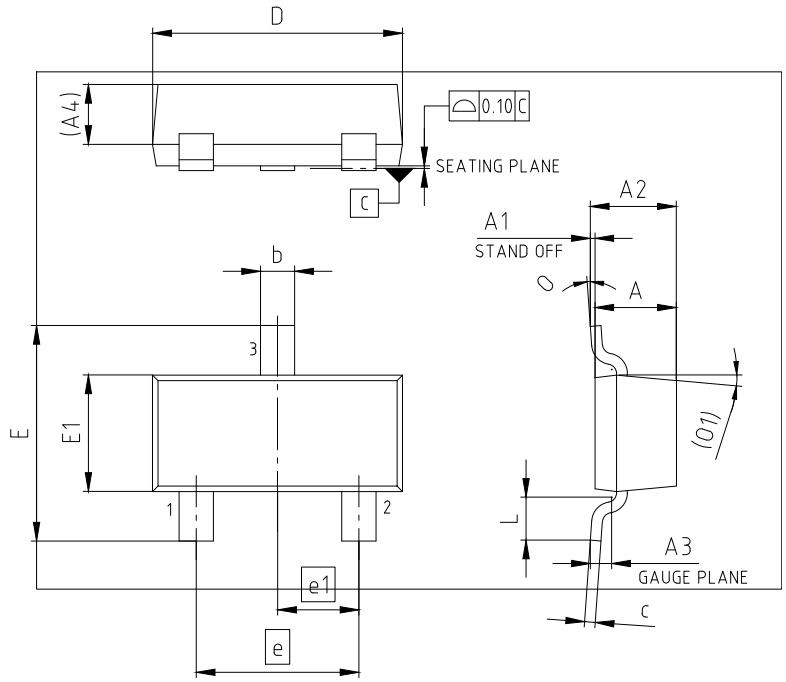
5 Package outlines



PACKAGE - GROUP NUMBER:	PG-SOT23-3-U03				
DIMENSIONS	MILLIMETERS		DIMENSIONS	MILLIMETERS	
	MIN.	MAX.		MIN.	MAX.
A	0.88	1.02	e	1.90	
A1	0.01	0.10	e1	0.95	
A2	0.89	1.12	L	0.40	0.60
A3	0.15	0.35	N	3	
A4	0.70		O	3°	8°
b	0.32	0.47	O1	6°	8°
c	0.08	0.18			
D	2.80	3.04			
E	2.40	2.64			
E1	1.32	1.40			

NOTE: ALL DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Figure 1 Outline PG-SOT23-3mm

Revision history

SN7002I

Revision 2025-09-30, Rev. 2.4

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2021-01-26	Release of final version
2.1	2021-03-16	Update technology naming
2.2	2023-02-07	Update Coss and Crss
2.3	2025-03-13	Update package outline drawing
2.4	2025-09-30	Update marking

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