Card Coil Design Guide

Contactless memories compliant to ISO/IEC 14443-3 Type A

Application Note

Devices

- SLE 66R01P
- SLE 66R01PN
- SLE 66RxxP
- SLE 66RxxS
- SLE 66R01L
- SLE 66R01LN
- SLE 66R35, SLE 66R35I, SLE 66R35R
- SLE 66R35E7, SLE 66R35E7H

About this document

Scope and purpose

This document serves as a guideline for the design of card coils for Infineon's contactless memory products compliant to ISO/IEC 14443-3 Type A. The recommendations given are for orientation only. The specific behaviour of the coil design shall be verified by measurement as described within this document.

Intended audience

The information within this document is intended for antenna designers and card manufacturers, who want to understand the theory behind card coil design and card coil characterization.

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1 General information

This document gives details on ISO/IEC 14443-3 Type A [1] devices and shall assist designers of tag antenna inlays. The recommendations given are for guidance only. The specific behaviour of the antenna design shall be verified by measurement according to ISO/IEC 10373-6 Test methods for proximity cards [2].

Following ISO/IEC 14443-3 Type A [1] compliant contactless memory chips are available:

Table 1 Chip variants

Device name	Type
my-d™ move	SLE 66R01P
my-d™ move NFC	SLE 66R01PN
my-d™ NFC	SLE 66RxxP
my-d™ proximity 2	SLE 66RxxS
my-d™ move lean NFC	SLE 66R01L
my-d™ move lean NFC	SLE 66R01LN
1 kByte Memory Chip with NRG™	SLE 66R35, SLE 66R35I, SLE 66R35R
1 kByte Memory Chip with NRG™	SLE 66R35E7, SLE 66R35E7H

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1.1 Inlay requirements

The resonance frequency of a complete card should be in the range of 15 MHz operating at the lower limit of the field strength. If two or more cards are magnetically coupled (by being close or even on top of each other) the resonance frequency of all of them will be reduced.

The target is to minimize the impact on the operating range if at least two cards are stacked. For this reason the lower limit of the resonance frequency of a single card should not be below 15 MHz.

On the other hand the operating distance of a card will be reduced if the resonance frequency deviates too much from the operating frequency. To ensure a full operability of a card at the minimum value for the magnetic field H_{min} =1.5 A/m (as defined by ISO/IEC 14443-2) the upper limit of the resonance frequency of a single card should not exceed 17 MHz.

Applications requiring only one card in the magnetic field (e.g. tokens or watches), the resonance frequency of a complete card can be close to the carrier frequency to enhance the coupling distance.

Figure 1 below shows a typical construction of a contactless memory card based on the ID1 form factor. The design of other form factors deviates and is not scope of this document.

Figure 1 Contactless memory card

2 Electrical characteristics

The electrical characteristics are part of the data sheet, but they can also be measured at the L_A and L_B pads of the chip. Based on the circuit model the different parameters are listed having impact on the tuning.

2.1 Circuit model

An equivalent circuit of the chip and antenna coil is shown in Figure 2.

An antenna coil L_{coil} is connected to the antenna pads L_A and L_B. When the chip is powered it represents an AC load resistance $_{RIC}$ and an input capacitance C_{chip} to the antenna coil. From the electrical point of view the mounting of the chip adds the capacitance C_{mount} to the resonance circuit, but the main portion of the capacitance is still given by the ICs input capacitance.

The coil will include some stray capacitance C_{stray} and a series AC resistance R_{coil}. An external tuning capacitor C_{ext} can also be added to the coil if required.

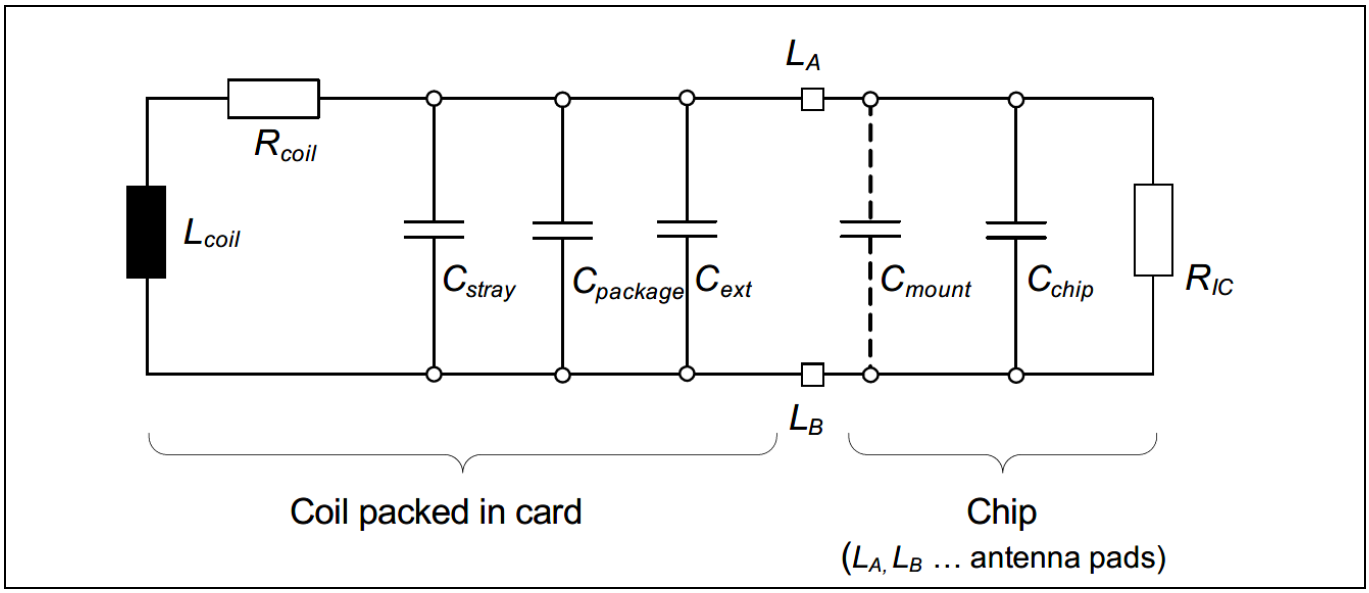

Figure 2 Equivalent circuit of chip and antenna coil

2.2 Calculations and formulas

Based on the equivalent circuit (see Figure 2) following correlations may be used to estimate the tuning of a card.

2.2.1 Card capacitance

The entire capacitance of the inlay/card comprises following components:

- stray capacitance C_{stray}
- package capacitance $C_{package}$ due to dielectric properties of the package material
- an optional external capacitance C_{ext} to achieve the desired tuning
- chip capacitance C_{chip}
- parasitic mounting capacitor C_{mount}

Due to the dielectric property of the card package material $C_{package}$ has to be added to the resonant circuit. This value is influenced by the card manufacturing process and must be considered in the verification of a coil design.

It is recommended to keep this dependence in mind, when changing from one to another package material and verify the new card material with the given limits.

The resulting capacitance is the sum of those capacitors:

Resulting capacitance (1)

$$C_{res} = C_{stray} + C_{package} + C_{ext} + C_{chip} + C_{mount}$$

2.2.2 Coil inductance

From the electrical point of view the coil is not only an ideal inductivity (L_{coil}) but has also a resistive (R_{coil}) and a capacitive component (C_{stray}). The value of these components is of essential importance for the cards electrical and functional properties.

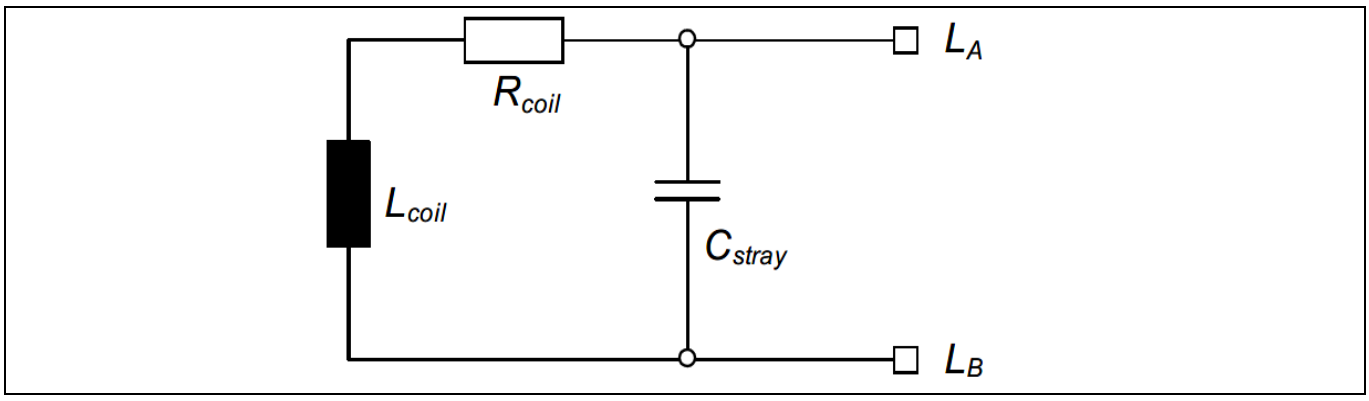

Figure 3 Equivalent circuit of the coil

The inductivity of the coil L_{coil} may be estimated with following equation:

Estimation of coil inductance (2)

$$L_{coil} = 2 \times l \times \left(\ln \frac{l}{D} - 1,04 \right) \times N^{P} \; [nH]$$

– l ...length of one turn of the coil [mm]
– N ... number of turns
– D ... diameter of wire or width of conductor [mm]
– P ... exponent of N depends on the coil manufacturing technology

P gives the exponent for the calculation of the inductivity and depends on the different coil manufacturing technologies. The table below gives the estimated values for turn exponent P.

Table 2 Coil manufacturing parameter

P	Coil manufacturing technology
1.8	wired coil
1.7	etched coil
1.5 - 1.7	printed coil

Note: The equation is only considered for a first estimation. The real value of the inductivity has to be verified by measurement.

Q factor estimation coil (3)

$$Q_{coil} = \frac{2 \times \pi \times f_{operating} \times L_{coil}}{R_{coil}}$$

From the formula above it is obvious that the resistive part of the coil R_{coil} must be as small as possible to achieve a high coil quality factor $Q_{coil.}$ With a higher coil quality factor Q_{coil} the operating distance will increase.

2.2.3 Resonance frequency

The entire capacitance together with the inductance of the coil influence the resonance frequency of the card and thus its performance:

Resonance frequency (4)

$$f_{res} = \frac{1}{2\pi\sqrt{L_{coil} \times C_{res}}}$$

2.2.4 Q factor

R_{IC} mainly determines the quality factor of the chip. The Q factor of the chip can be calculated using following equation:

Q factor estimation chip (5)

$$Q_{chip} = 2 \times \pi \times f_{operating} \times C_{chip} \times R_{IC}$$

The total Q factor can be estimated when using following equation:

Total Q factor estimation (6)

$$Q_{total} = \frac{1}{\frac{1}{Q_{coil}} + \frac{1}{Q_{chip}}}$$

For good energy transmission a high Q factor is desirable.

3 Electrical specifications

The electrical specifications are of the different contactless memory chips supporting the ISO/IEC 14443 Type A standard [1] are listed below.

3.1 my-d™ move (NFC) and my-d™ move lean (NFC)

Values for the chip input capacitance C_{chip} and AC load resistance R_{IC} are given below. All values are measured at 13.56 MHz and 25°C.

Table 3 Electrical Parameters my-d™ move (NFC) and my-d™ move lean (NFC)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Chip input capacitance L_A-L_B	C_{chip}	16.15	17	17.85	pF	$V_{AB\ peak}$ = 3.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 °C
Chip load resistance L_A-L_B	R_{IC}	3	4.5	6	kΩ	$V_{AB\ peak}$ = 3.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 °C

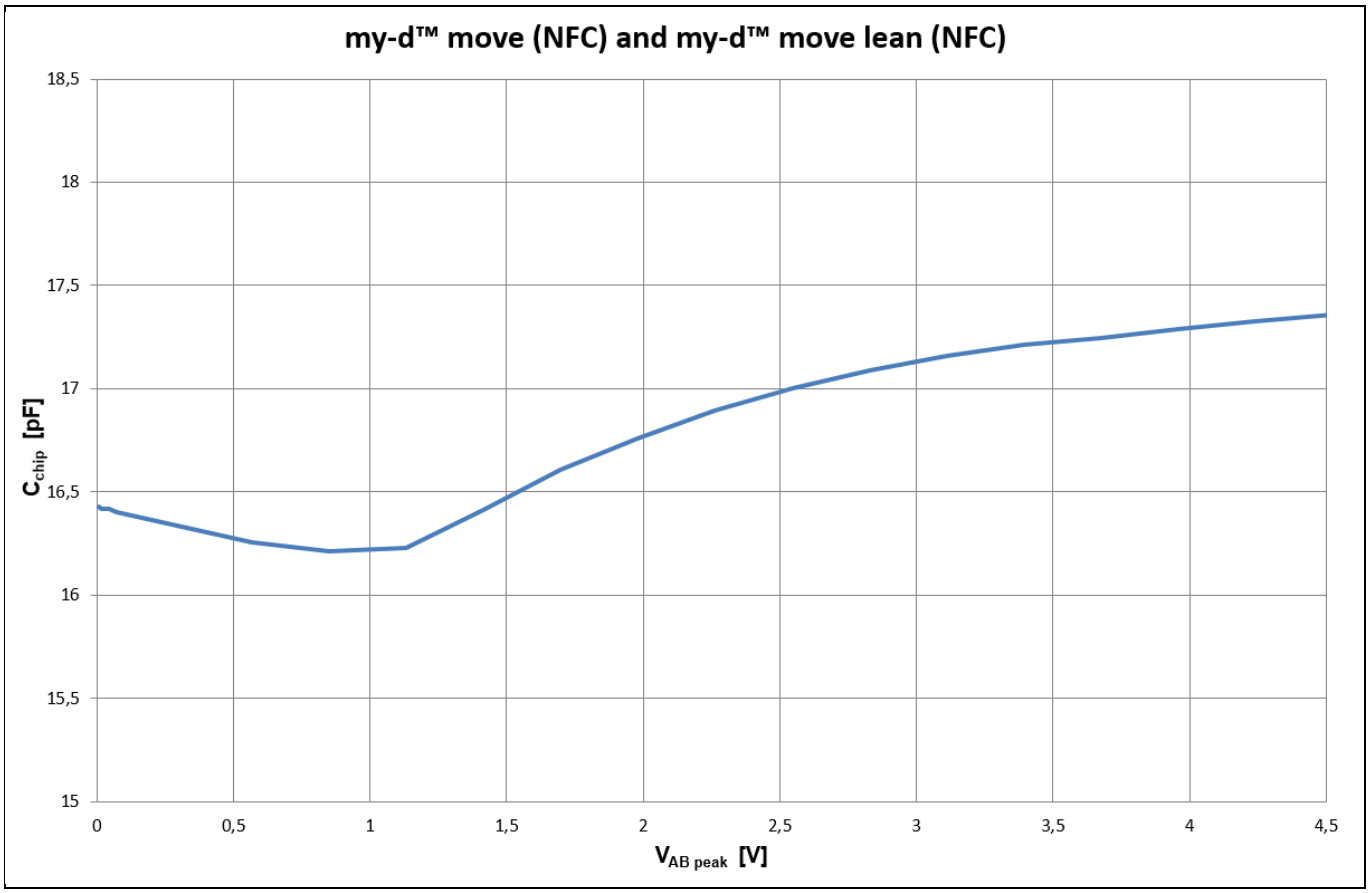

Figure 4 Chip Input Capacitance of my-d™ move (NFC) and my-d™ move lean (NFC)

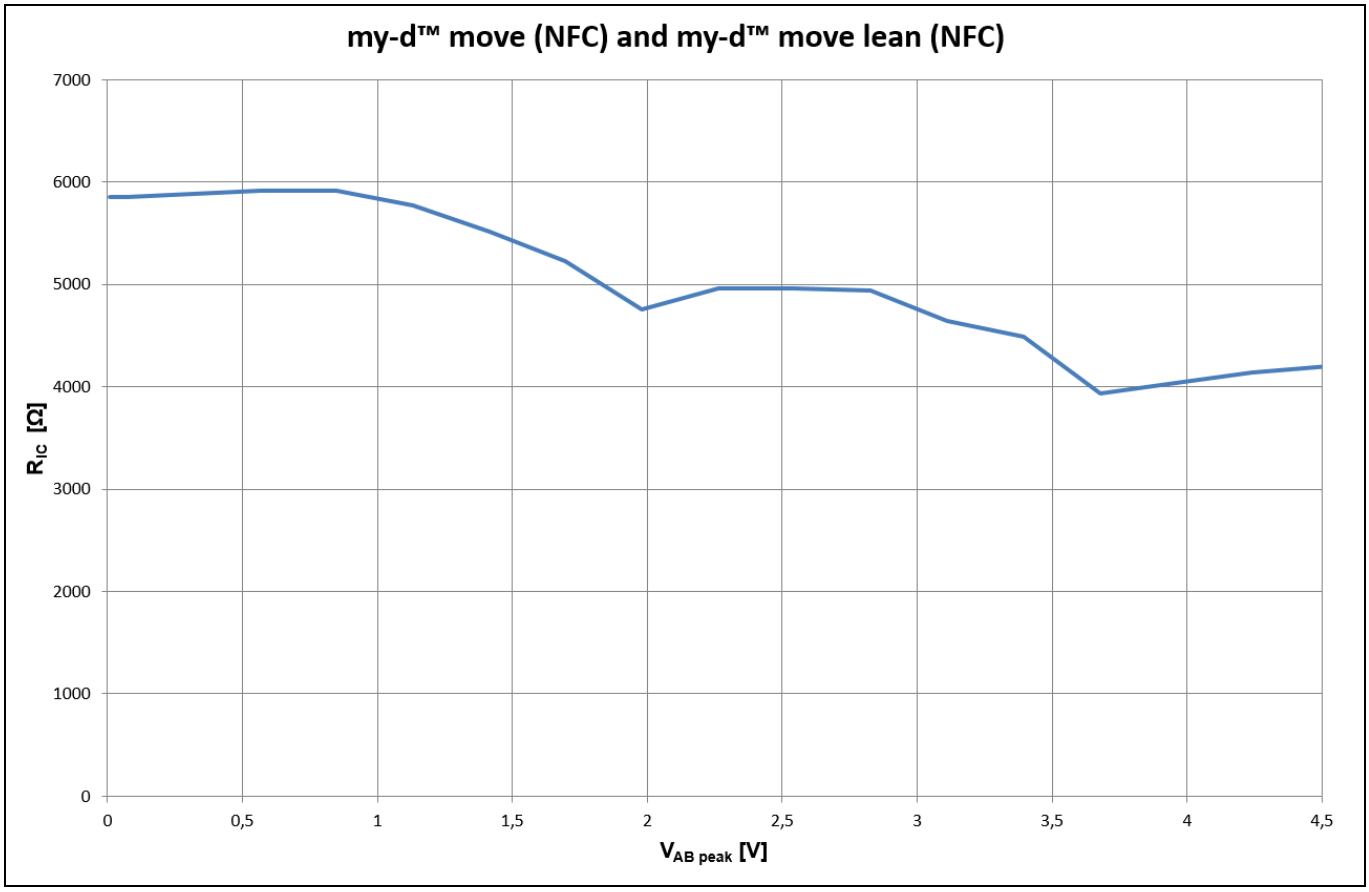

Figure 5 Chip Input Resistance of my-d™ move (NFC) and my-d™ move lean (NFC)

Table 4 Absolute Maximum Ratings my-d™ move (NFC) and my-d™ move lean (NFC)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input peak voltage between L_A-L_B	$V_{AB\ peak}$			6	V	
Input current through L_A-L_B	I_{IN}			30	mA	
Storage temperature	$T_{storage}$	-40		+125	°C	
ESD Protection voltage (L_A, L_B pins)	V_{ESD}	2			kV	JEDEC STD EIA / JESD22 A114-B

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability, including EEPROM data retention and write/erase endurance.

3.2 my-d™ NFC and my-d™ proximity 2

Values for the chip input capacitance C_{chip} and AC load resistance R_{IC} are given below. All values are measured at 13.56 MHz and 25°C.

Table 5 Electrical Parameters my-d™ NFC and my-d™ proximity 2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Chip input capacitance L_A-L_B	C_{chip}	16.6	17.5	18.4	pF	$V_{AB\ peak}$ = 3.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 °C
Chip load resistance L_A-L_B	R_{IC}	12.8	16	19.2	kΩ	$V_{AB\ peak}$ = 3.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 °C

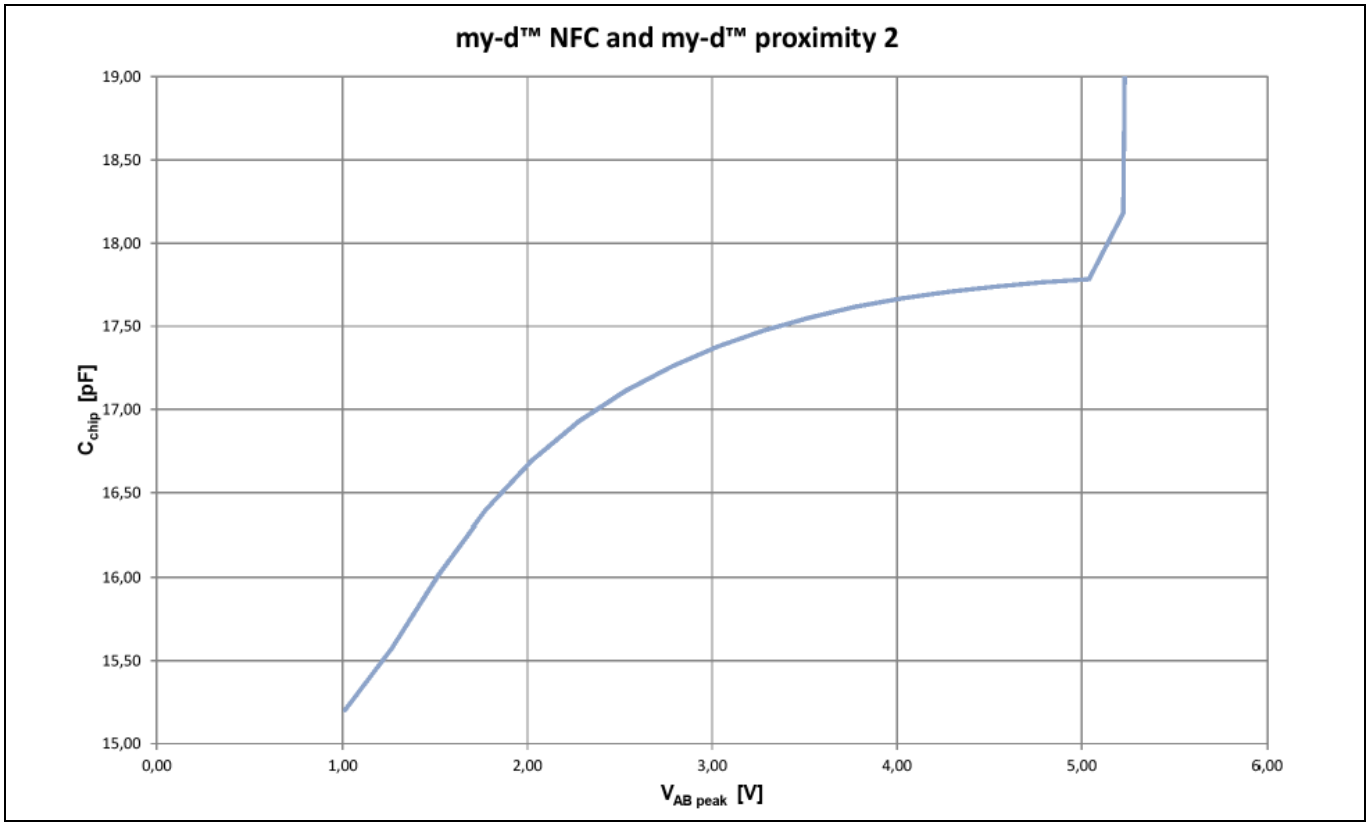

Figure 6 Chip Input Capacitance of my-d™ NFC and my-d™ proximity 2

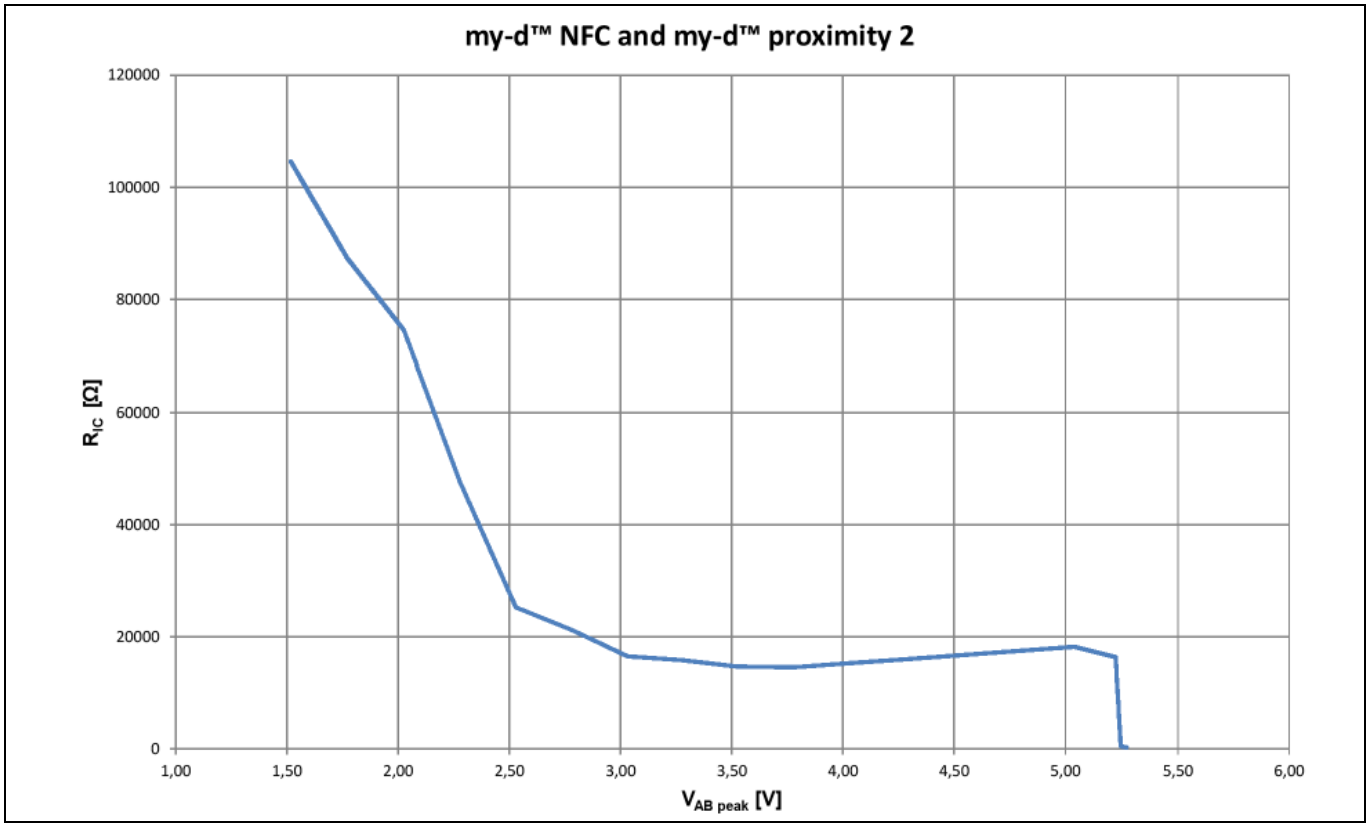

Figure 7 Chip Input Resistance of my-d™ NFC and my-d™ proximity 2

Table 6 Absolute Maximum Ratings my-d™ NFC and my-d™ proximity 2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input peak voltage between L_A-L_B	V_{AB} peak	3		6	V	
Input current through L_A-L_B	I_{IN}			30	mA	
Storage temperature	$T_{storage}$	-40		+125	°C	
ESD Protection voltage (L_A, L_B pins)	V_{ESD}	2			kV	JEDEC STD EIA / JESD22 A114-B

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3.3 SLE 66R35, SLE 66R35I, SLE 66R35R

Values for the chip input capacitance C_{chip} and AC load resistance R_{IC} are given below. All values are measured at 13.56 MHz and 25°C.

Table 7 Electrical Parameters SLE 66R35, SLE 66R35I, SLE 66R35R

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Chip input capacitance L_A-L_B	C_{chip}	16.5	18.3	20.1	pF	$V_{AB\ peak}$ = 2.3 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 °C
Chip load resistance L_A-L_B	R_{IC}	13.6	17	20.4	kΩ	$V_{AB\ peak}$ = 2.3 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 °C

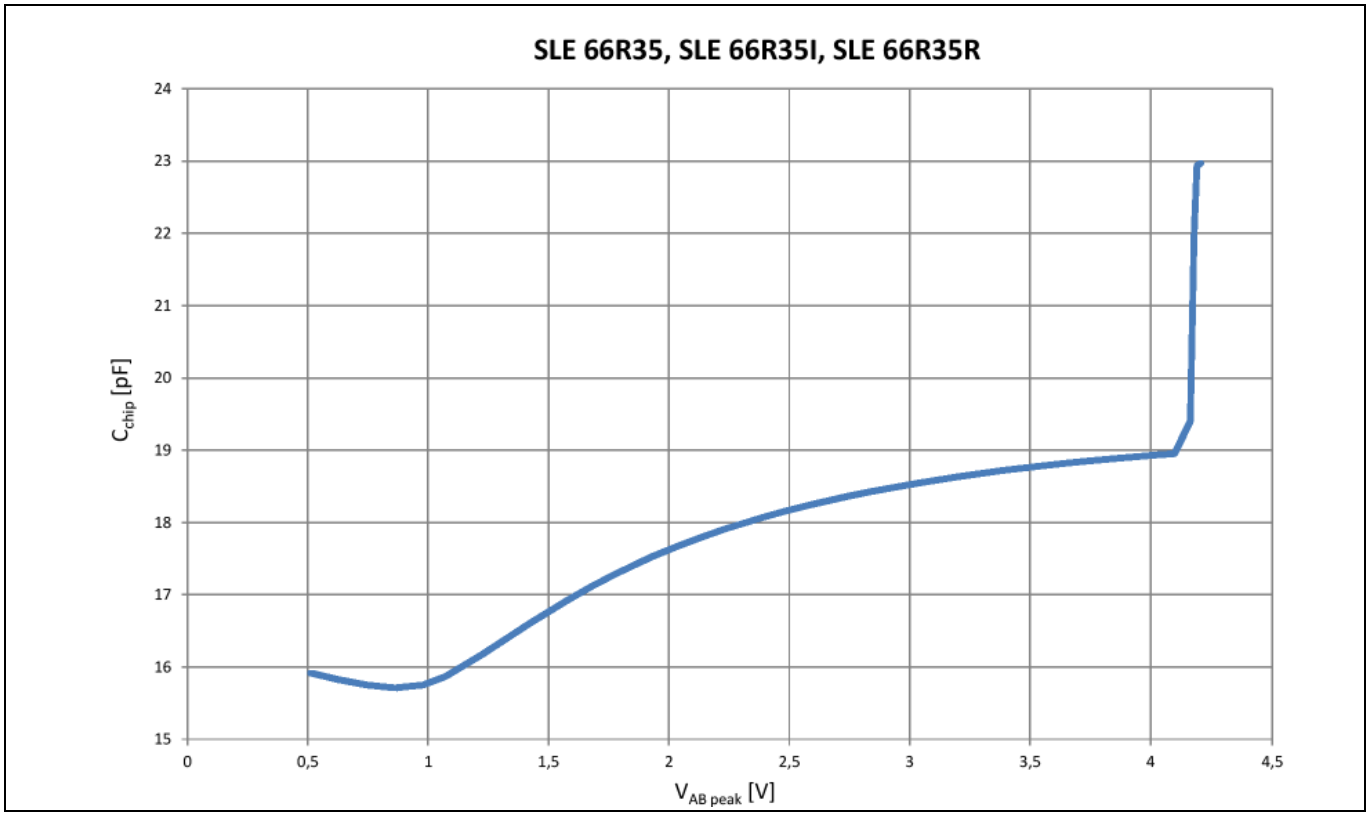

Figure 8 Chip Input Capacitance of SLE 66R35, SLE 66R35I, SLE 66R35R

Figure 9 Chip Input Resistance of SLE 66R35, SLE 66R35I, SLE 66R35R

Table 8 Absolute Maximum Ratings SLE 66R35, SLE 66R35I, SLE 66R35R

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input peak voltage between L_A-L_B	$V_{AB\ peak}$	-7		+7	V	
Input current through L_A-L_B	I_{IN}			50	mA	
Storage temperature	$T_{storage}$	-40		+125	°C	
ESD Protection voltage (L_A, L_B pins)	V_{ESD}	2			kV	JEDEC STD EIA / JESD22 A114-B

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3.4 SLE 66R35E7, SLE 66R35E7H

Values for the chip input capacitance C_{chip} and AC load resistance R_{IC} are given below. All values are measured at 13.56 MHz and 25°C.

Table 9 Electrical Parameters SLE 66R35E7, SLE 66R35E7H

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Chip input capacitance L_A-L_B	C_{chip}	17.3	18.3	19.3	pF	$V_{AB\ peak}$ = 2.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 °C Tolerance: +/-5%
Chip load resistance L_A-L_B	R_{IC}		4.5		kΩ	$V_{AB\ peak}$ = 2.0 V, f_{CAR} = 13.56 MHz, $T_{ambient}$ = 25 °C

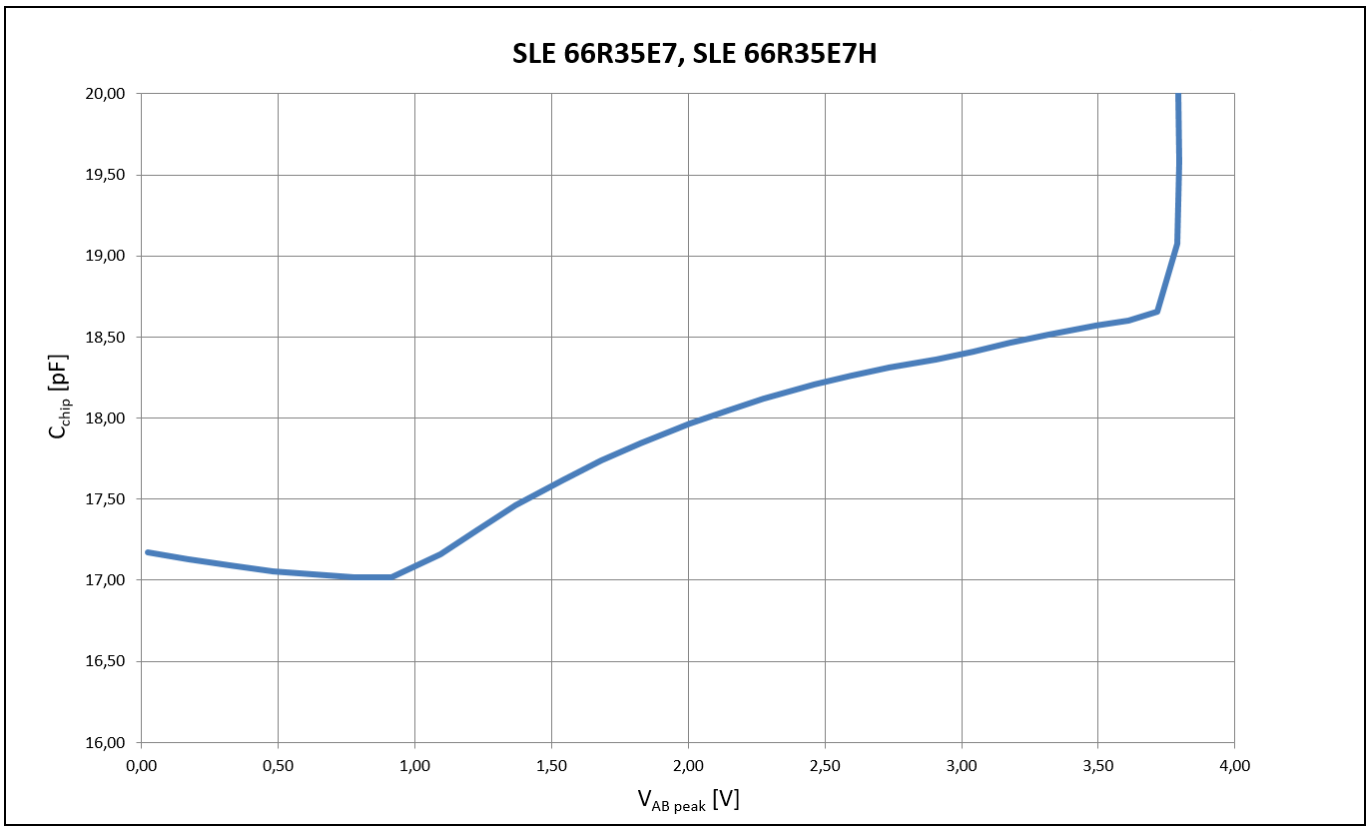

Figure 10 Chip Input Capacitance of SLE 66R35E7, SLE 66R35E7H

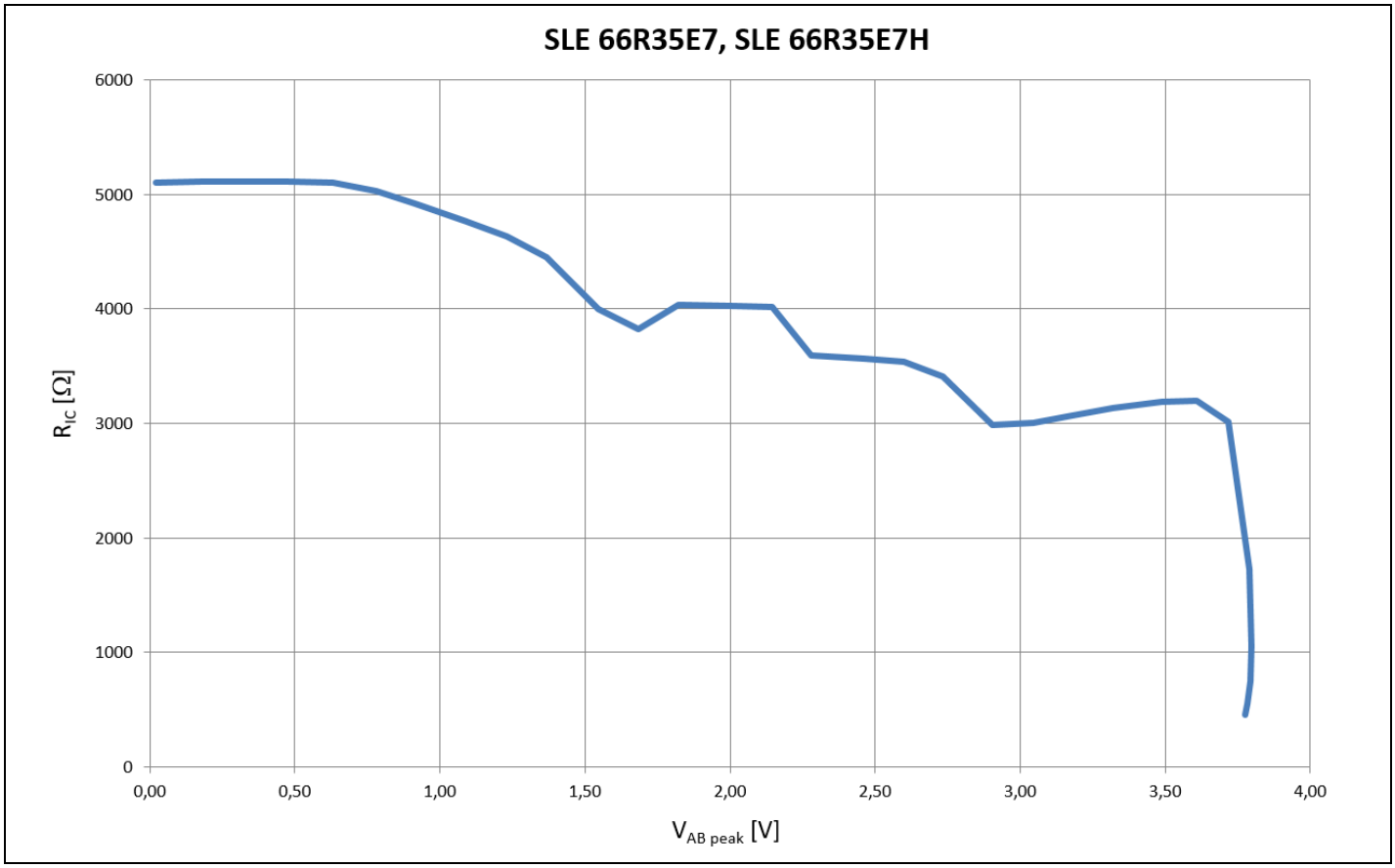

Figure 11 Chip Input Resistance of SLE 66R35E7, SLE 66R35E7H

Table 10 Absolute Maximum Ratings SLE 66R35E7, SLE 66R35E7H

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input peak voltage between L_A-L_B	V_{AB} peak			6	V	
Input current through L_A-L_B	I_{IN}			50	mA	
Storage temperature	$T_{storage}$	-40		+125	°C	
ESD Protection voltage (L_A, L_B pins)	V_{ESD}	2			kV	JEDEC STD EIA / JESD22 A114-B

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3.5 Physical parameters

Physical specifications are listed in the “Chip Delivery Specification for Wafer”.

References

[1] ISO/IEC 14443 Identification cards – Contactless integrated circuit(s) cards Proximity cards, Parts 1, 2 and 3

[2] ISO/IEC 10373-6 Identification cards – Test methods – Proximity cards

Revision history

Reference	Description
Revision 1.3, 2021-04-14	
all	Removing “confidential” marking
Revision 1.2, 2019-07-23	
all	Editorial changes
	Added SLE 66R35E7H and SLE 66R01LN
Revision 1.1, 2017-05-12	
all	Major review
Revision 1.0, 2017-03-28	
all	Initial version

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