

IGBT

TRENCHSTOP™ IGBT3 Chip
SIGC128T170R3E

Data Sheet

Industrial Power Control



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TRENCHSTOP™ IGBT3 Chip

Features:

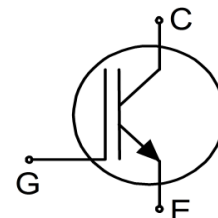
- 1700V trench & field stop technology
- Low turn-off losses
- Short tail current
- Positive temperature coefficient
- Easy paralleling

Recommended for:

- Power modules

Applications:

- Drives



Chip Type	V_{CE}	I_{cn}^1	Die Size	Package
SIGC128T170R3E	1700V	100A	11.33mm x 11.33mm	Sawn on foil

Mechanical Parameters

Die size	11.33 x 11.33	mm ²
Emitter pad size	See chip drawing	
Gate pad size	1.303 x 0.838	
Area total	128.369	
Thickness	190	μm
Wafer size	200	mm
Maximum possible chips per wafer	198	
Passivation frontside	Photoimide	
Pad metal	3200nm AlSiCu	
Backside metal	Ni Ag – system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process	
Die bond	Electrically conductive epoxy glue and soft solder	
Wire bond	Al, ≤500μm	
Reject ink dot size	Ø 0.65mm; max. 1.2mm	
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C, <6 months
	for open MBB bags	Acc. to IEC62258-3: atmosphere >99% Nitrogen or inert gas, humidity <25%RH, temperature 17°C – 25°C, <6 months

¹ Nominal collector current at $T_C=100^\circ\text{C}$ for chip packaged in power modules, see application example cited on page 5.

Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj}=25^{\circ}\text{C}$	V_{CE}	1700	V
DC collector current, limited by $T_{vj\max}^2$	I_C	-	A
Pulsed collector current, t_p limited by $T_{vj\max}^3$	$I_{C,puls}$	300	A
Gate-emitter voltage	V_{GE}	± 20	V
Junction temperature range	T_{vj}	-40 ... +175	$^{\circ}\text{C}$
Operating junction temperature	T_{vj}	-40 ... +150	$^{\circ}\text{C}$
Short circuit data ^{3/4} $V_{GE}=15\text{V}$, $V_{CC}=1000\text{V}$, $T_{vj}=150^{\circ}\text{C}$	t_{sc}	10	μs
Reverse bias safe operating area ³ (RBSOA)	$I_{C,max}=200\text{A}$, $V_{CE,max}=1700\text{V}$, $T_{vj}\leq 150^{\circ}\text{C}$		

Static Characteristics (tested on wafer), $T_{vj}=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$, $I_C=3.5\text{mA}$	1700	-	-	V
Collector-emitter saturation voltage	V_{CEsat}	$V_{GE}=15\text{V}$, $I_C=100\text{A}$	1.6	2	2.4	
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C=4\text{mA}$, $V_{GE}=V_{CE}$	5.2	5.8	6.4	
Zero gate voltage collector current	I_{CES}	$V_{CE}=1700\text{V}$, $V_{GE}=0\text{V}$	-	-	5.6	μA
Gate-emitter leakage current	I_{GES}	$V_{CE}=0\text{V}$, $V_{GE}=20\text{V}$	-	-	600	nA
Integrated gate resistor	r_G		7.5			Ω

Electrical Characteristics ³

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter saturation voltage	V_{CEsat}	$V_{GE}=15\text{V}$, $I_C=100\text{A}$, $T_{vj}=125^{\circ}\text{C}$	-	2.4	-	V
Input capacitance	C_{ies}	$V_{CE}=25\text{V}$, $V_{GE}=0\text{V}$, $f=1\text{MHz}$, $T_{vj}=25^{\circ}\text{C}$	-	8815	-	pF
Reverse transfer capacitance	C_{res}		-	292	-	

² Depending on thermal properties of assembly.

³ Not subject to production test - verified by design/characterization.

⁴ Allowed number of short circuits: <1000; time between short circuits: >1s.



SIGC128T170R3E

Further Electrical Characteristics

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

Application example	FS100R17KE3	Rev. 2.0
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SIGC128T170R3E

Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

Description

AQL 0.65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Revision History

Revision	Subjects (major changes since last revision)	Date
2.1	Change wafer size to 200mm	14.04.2010
2.2	Additional basic types L7787M, L7787T, L7787E; new gate pad design	01.07.2014
2.3	Minor changes, chip drawing	06.02.2015
2.4	Update disclaimer	19.08.2015

Relevant Application Notes

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