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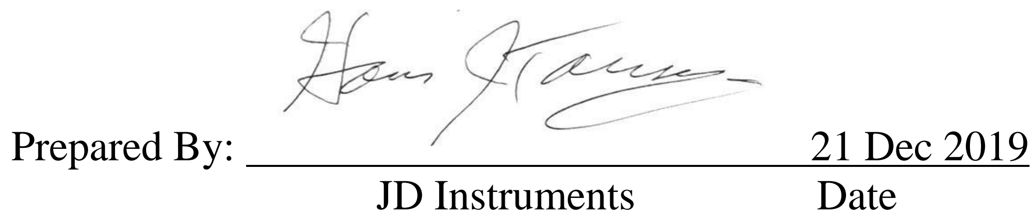
SEE/SEL Final Report for Cypress Semiconductor CYRS1061, 16-Mbit SRAMs

Fab Lot: L9903000, Wafer #2

Date: 21 Dec 2019 Revision: Original

Purchase Order:
Cypress Semiconductor Corporation 4700011208



Prepared By: ________________ 21 Dec 2019
JD Instruments Date

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1.0 Test Overview

Single Event Effects (SEE) and Single Event Latchup (SEL) testing was performed on Cypress Semiconductor CYRS1061G 16-Mbit SRAMs, fab (diffusion) lot L9903000, wafer #2 on 13-14 Dec, 2019 at the Texas A&M University Cyclotron facility.

These devices have the architecture shown in Figure 1. During normal operation these devices use internal Hamming EDAC (Error Detection and Correction) which can correct single bit errors at any address or detect double bit errors. They have a special test mode which can be used to disable EDAC so raw bit errors can recorded.

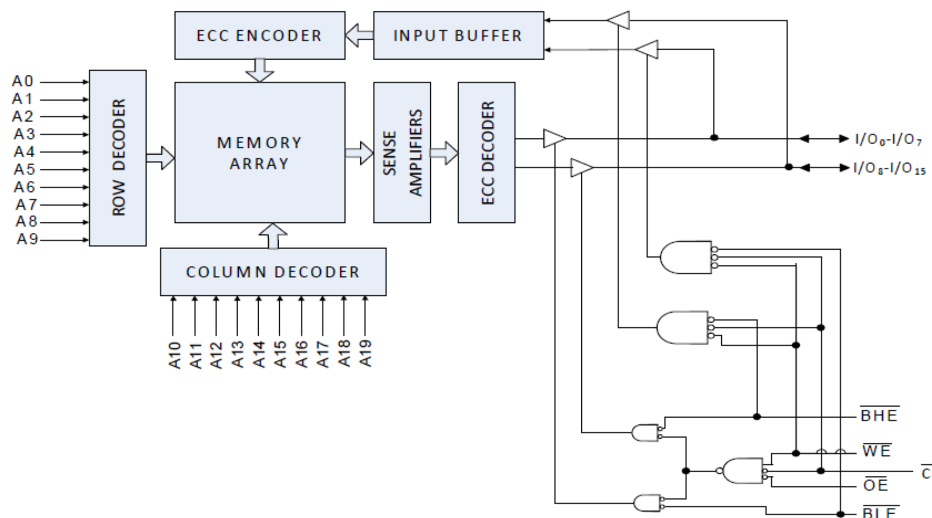

Figure 1. Functional Diagram for CYRS1061 16Mb SRAMs

Parts were provided in 54 pin ceramic SOIC packages.

Testing was performed using a JD Instruments Algorithmic Test Vector (ATV) system shown in Figure 2. The main chassis of the tester was located in the SEE irradiation room and connected to the test head mounted on the actuating arm of the chamber. A USB cable connected the tester to a controlling computer located in the experimenter area.

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Figure 2. ATV Test System used for SEE Testing

All testing was done with one device at a time inserted into a test card mounted on the ATV test head.

Testing was performed by Jake Tausch of JD Instruments and Helmut Puchner of Cypress Semiconductor.

Parts were irradiated in air at a distance of 30mm from the aramica window of the source. Testing was performed using four ion species in the 15 MeV SEE beam. Xenon (^{129}Xe) was used for LETs between 52 and 80 (MeV*cm^2)/mg, Krypton (^{84}Kr) for LETs of 28 and 38 (MeV*cm^2)/mg, Argon (^{40}Ar) for an LET of 8.4 (MeV*cm^2)/mg and Nitrogen (^{14}N) for LETs of 1.3 and 2.1 (MeV*cm^2)/mg.

Figures 3 and 4 show ranges vs. LET for various ions available with this set-up. Note that all ions used had a range of at least 100u in silicon

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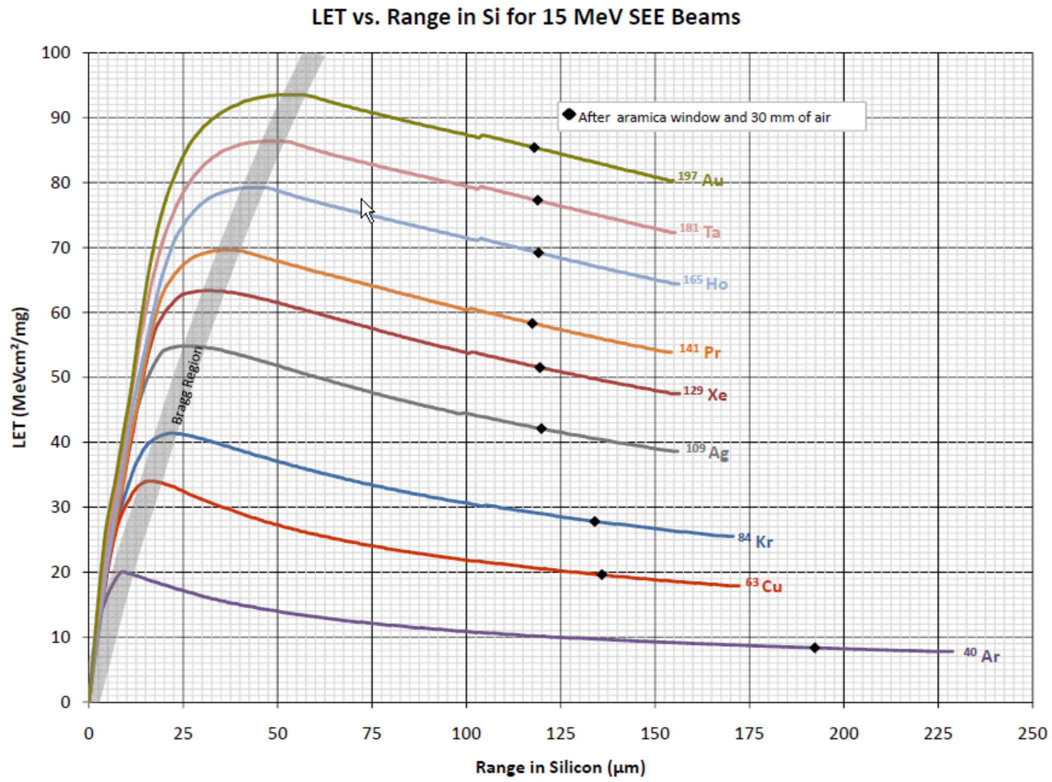

Figure 3. Ion Range vs. LET, Various Ions, 15 MeV beam, Texas A&M Cyclotron

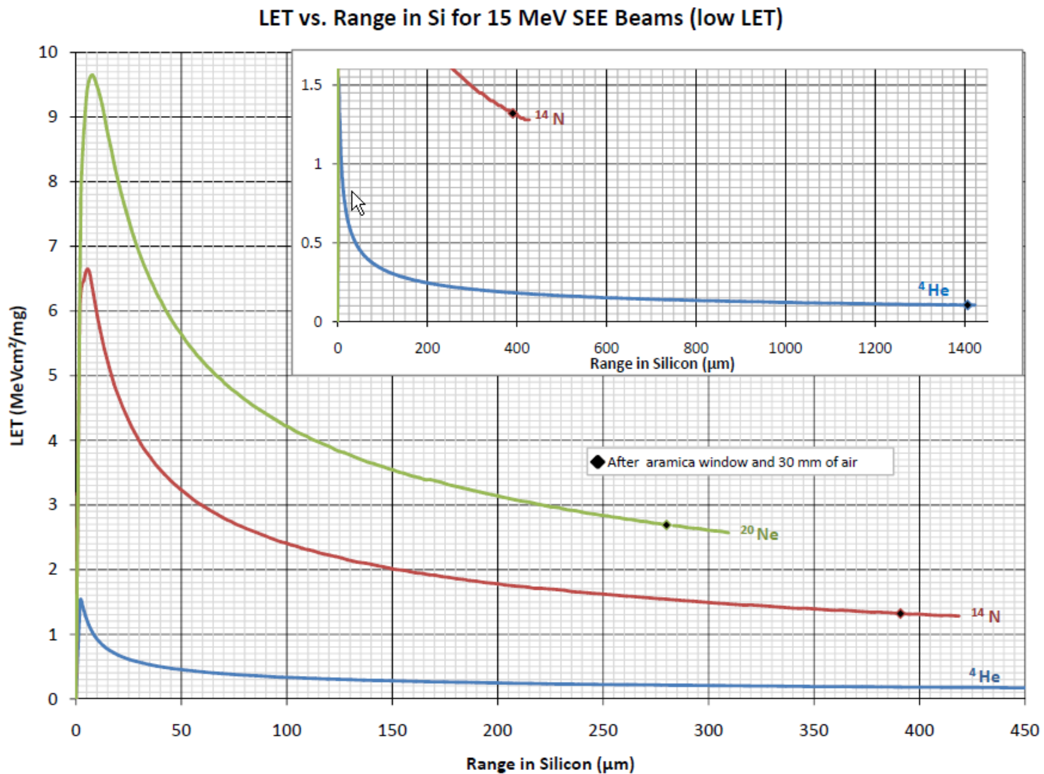

Figure 4. Ion Range vs. LET, low LET Ions, 15 MeV beam, Texas A&M Cyclotron

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Testing was done in compliance with ASTM F1192, "Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices" and also in compliance with EIA/JESD57, "Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation".

Latch-up testing was performed to determine the upper limits of temperature and Linear Energy Transfer (LET) where these parts could be safely operated.

Static memory upsets were measured vs. LET to generate a capture cross-section curve for raw memory bits (EDAC OFF) and to verify that these errors were corrected when read when the devices were operated in their normal mode (EDAC ON).

Dynamic upset tests were performed vs. LET to determine functional upset rates of internal logic paths, sense amps, etc.

2.0 Dosimetry

Dosimetry was provided by TAMU personnel in electronic form. Records of this testing will be maintained along with test data as described in JD Instruments test procedures.

3.0 Test Results

Four production screened units were used for this testing. All units were from Cypress Fab Lot L9903000, wafer #2. Devices were serialized by the manufacturer with serial numbers 86, 87, 88 and 89.

3.1 Latch-Up

These parts were tested for single event latch-up (SEL) over a range of LETs from 60 to 80 (MeV*cm^2)/mg with device temperatures between 95^0C and 125^0C. Vdd was held constant at 5.5V for all latchup tests.

For SEE/SEL testing the metal lid of each part was removed to expose the bare die to radiation and parts were inserted into a socket. Figure 5 shows that the socket was modified so a heater strip could be inserted underneath the DUT. During heating an infrared thermometer (see Figure 6) was used to measure the actual die temperature. The infrared thermometer had a calibrated accuracy of +/- 1^0C.

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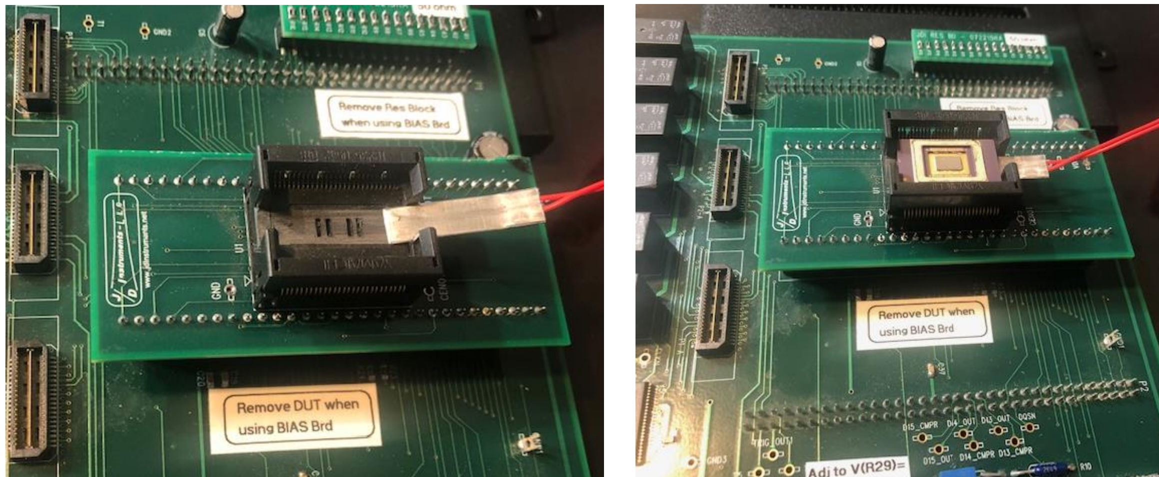

Figure 5. SEE Test Board, DUT and Heater

Figure 6. Infrared Thermometer

LETs greater than 60 (MeV*cm^2)/mg were achieved by degrading the Xe ion to a normal incident LET of 60 (MeV*cm^2)/mg and irradiating the DUT at an angle.

A series of LET and temperature conditions were tested to see if a combination could be determined at which no parts would latch. Figure 7 shows the SEL portion of the run log which details the results of these tests. Runs that do not have an entry under "Fluence to Latch" did not latch up to the target fluence of 1.00E+07 ions/cm^2. Figure 8 plots these results.

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			Temp (deg-C)		
RUN	SN	LET	No Latch	Latch	Fluence at Latch
44	89	80		105	2.00E+06
45	"	60		125	1.00E+06
46	"	60		120	1.60E+06
47	"	60	115		
48	"	80		115	9.50E+06
54	88	60	115		
55	"	80		115	6.80E+06
61	87	60		115	9.00E+06
64	"	60	105		
65	"	80		105	4.00E+06
71	86	80		103	6.00E+05
73	"	60		103	5.00E+06
75	"	60	95		
76	"	60		98	8.00E+06

Figure 7. SEL RUN Log for CYRS1061 Memories

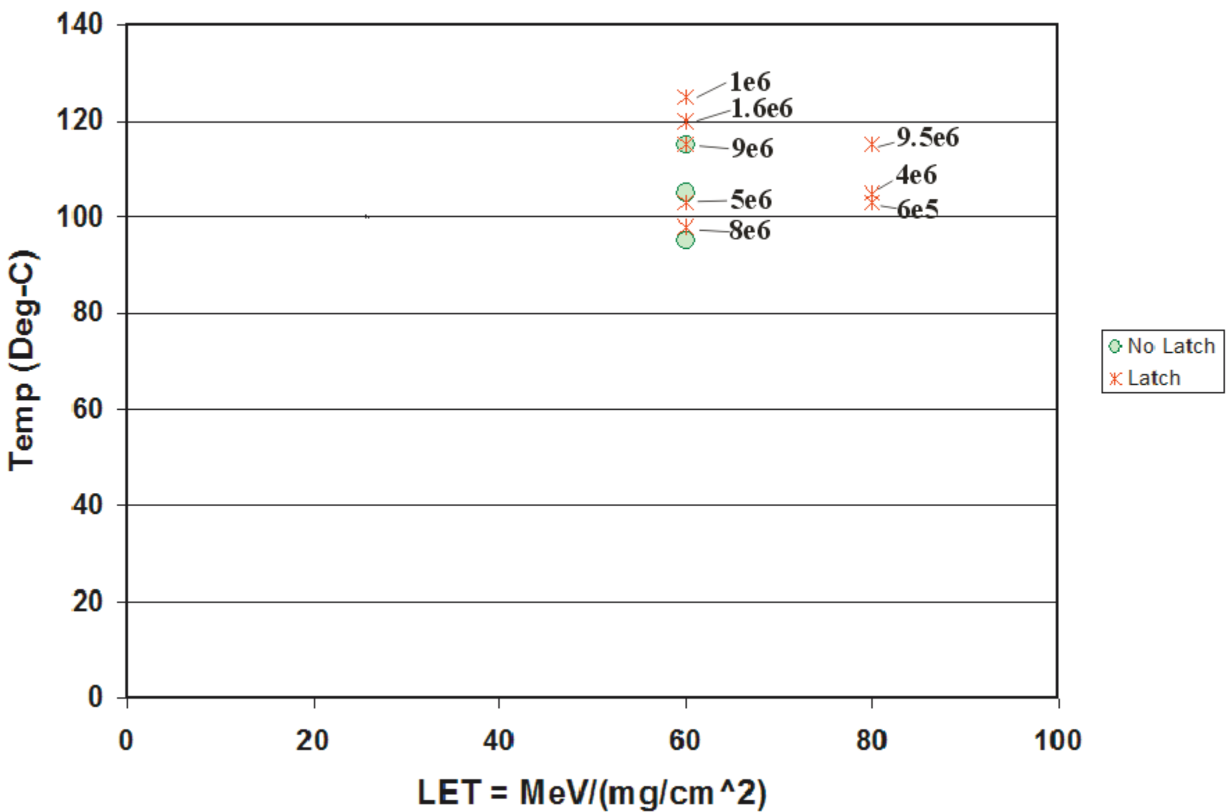

Figure 8. SEL RUN Log for CYRS1061 QDR Memories

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The target fluence to demonstrate no SEL is 1e7 ions/cm^2. The data show that 3 exposures with an LET of 60 MeV/(mg/cm^2) did not latch. Several other exposures at 60 MeV/(mg/cm^2) almost made the 1e7 threshold (e.g. 8e6, 9e6 ions/cm^2).

3.2 Current Increase During SEL Exposures

During SEL testing it was noted that Idd would increase and decrease over the course of exposure. Figure 9 shows the variation in Idd over the course of exposure during a typical SEL run (RUN 46, LET = 60 MeV/(mg/cm^2), Temperature 120^0C).

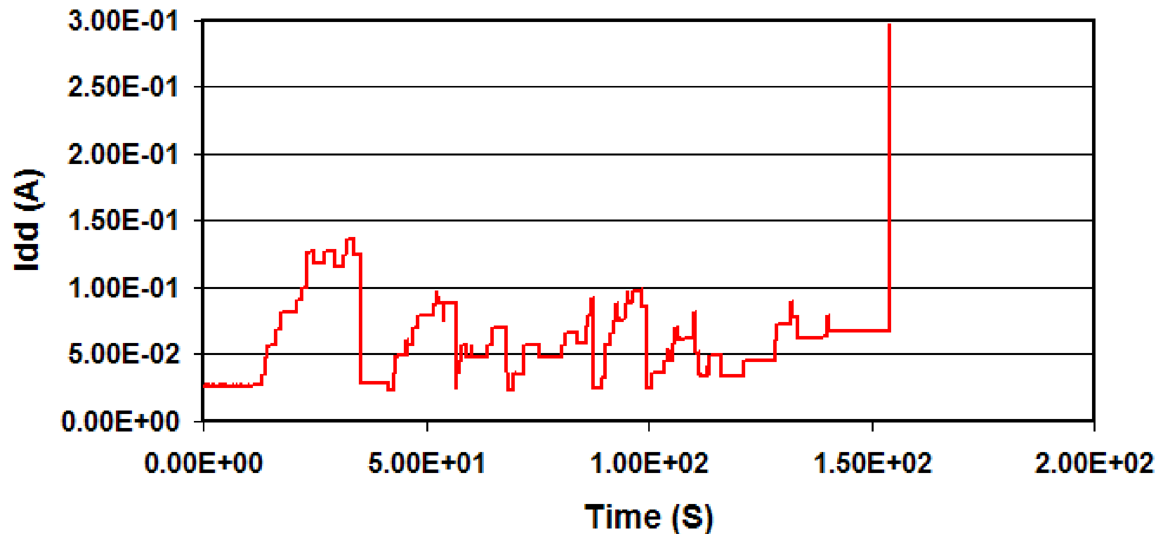

Figure 9. Idd vs Fluence during SEL Exposure, Run 46

In this figure note that Idd would repeatedly follow a pattern where it would step up to some level and then reset back to ~30mA. After an exposure to ~1.6e6 ions.cm^2 the current suddenly jumped to the current limit of 300mA indicating a latch.

The fact that Idd increased and then decreased over the course of radiation indicates that some conditions were being triggered and later reset in the SRAM circuit and not an indication of latchup. The exact location and mechanism for the current decrease and increase could not be determined on site. It is speculated that the current fluctuation is attributed logic state changes in peripheral logic circuits that are not used for normal operation of the memory. Read and Write operations were carried out with a device in a particular high current state to confirm that the memory was still operating normally.

The variation of Idd vs. fluence in figure 9 was typical of that seen in most of the SEL exposures. Figure 10 shows a slightly different behavior in run #45 (LET = 60 MeV/(mg/cm^2), Temperature 125^0C).

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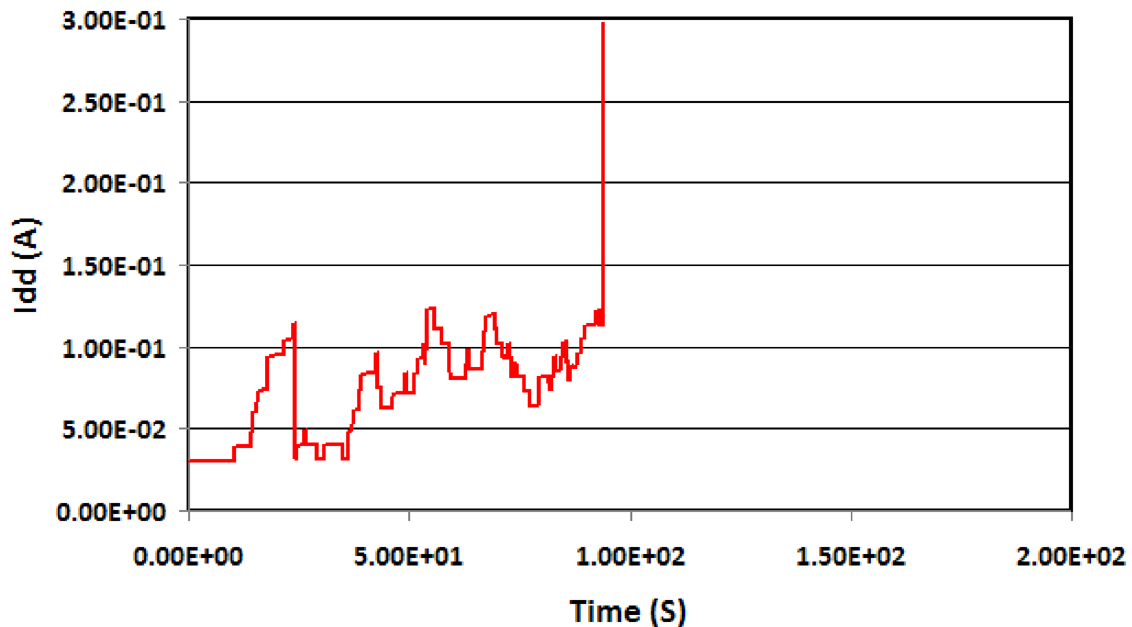

Figure 10. Idd vs Fluence during SEL Exposure, Run 45

In run 45 Idd appeared to continuously rise and then stabilize around 100mA. There was some speculation that this higher average current might have caused self heating that made the DUT more susceptible to latchup resulting in latchup at the relatively low fluence of 1e6 ions/cm^2.

For completeness the Idd profile for run #54 is shown in figure 11. In this run the DUT did not latch. Nevertheless Idd displayed the same behavior of stepping up and then being reset over the course of the entire exposure.

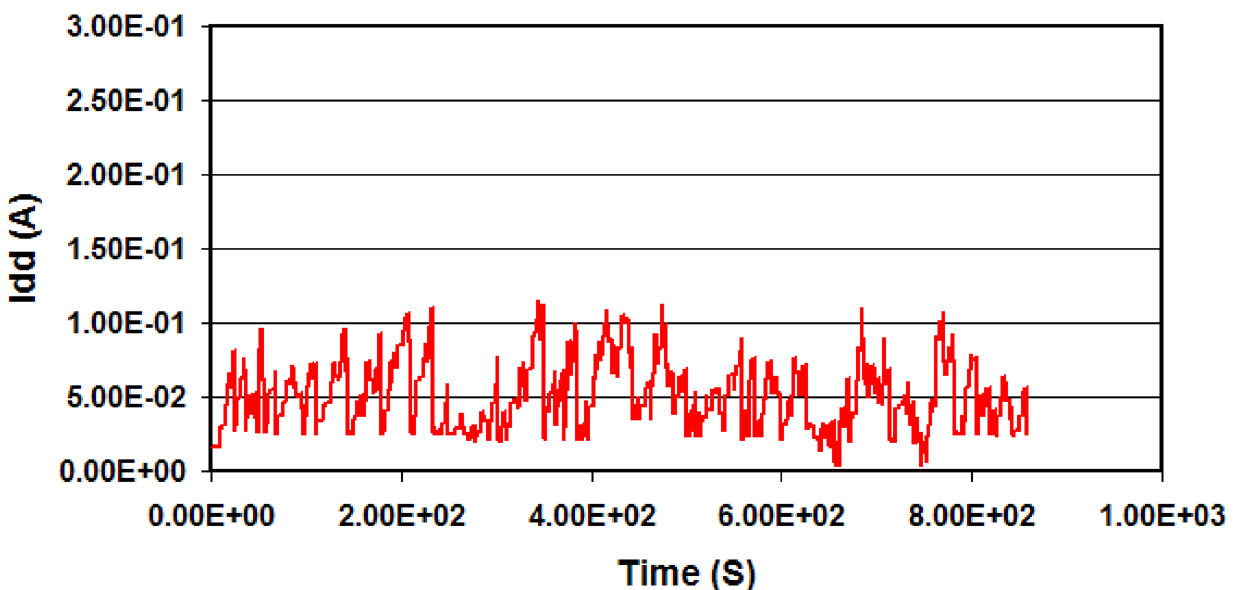

Figure 11. Idd vs Fluence during SEL Exposure, Run 54 (No Latch)

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3.3 Memory Upset Testing

Memory upset testing on these parts tests was performed with Vdd = 5V.

As stated earlier, these SRAMs include Hamming Error Detection and Correction (EDAC) circuitry which can correct a single bit upset and detect a double bit upset at any address. The devices have a special test mode in which EDAC can be turned off so individual bit upsets can be detected. For each exposure a DUT would be loaded with a checkerboard pattern, irradiated to some level and then read back with EDAC ON and then OFF.

Four DUTs were exposed to ions having LETs between 1.3 and 80 MeV/(mg/cm^2). Fluence was adjusted at every LET so the count of bit upsets would be several hundred or less. Theoretical analysis[1] showed this would keep the probability of upsets with EDAC ON very low. The run log in figure 12 shows this was the case and EDAC ON errors only occurred in 2 of the 33 static upset exposures. Thus, uncorrectable errors occurred in 6.1% of the exposures which is in line with predictions when random bit errors are in the range of 200.

Curiously, both runs where EDAC ON errors occurred were in SN86. Further bitmapping analysis is required to determine whether these two failure events were originating from the same single event. Possible spallation events in metal overlayers can sometimes cause random multibit events that ECC cannot correct. Another possibility for SN86 showing a worse behavior than the other units could be related to the repair strategy of the device and whether a redundant column repair caused a decrease in the interleaving distance. Further analysis is required by the device manufacturer to confirm above speculations.

[1] Tausch, Hans J, “Simplified Birthday Statistics and Hamming EDAC”, IEEE Transactions On Nuclear Science, Vol 56 No 2, April 2009, Pp474-478

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					ERRORS							
					Sn86		SN87		SN88		SN89	
Run	Ion	LET	Flux	Fluence	Off	On	Off	On	Off	On	Off	On
6	Kr	38	16.7	489	225	0						
8	Kr	28.3	177	449	225	2						
10	Kr	28.3	139	473			219	0				
12	Kr	38	112	525			406	0				
14	Kr	38	141	554					424	0		
16	Kr	28.3	169	400					152	0		
18	Kr	28.3	192	533							350	0
20	Kr	38	126	447							216	0
22	Ar	8.4	172	1063							167	0
24	Ar	8.4	285	947					146	0		
26	Ar	8.4	339	847			141	0				
28	Ar	8.4	281	1065	189	2						
29	Ar	8.4	288	965	163	0						
31	N	1.3	216	5011	78	0						
32	N	2.1	855	5278	164	0						
33	N	2.1	860	4717			141	0				
34	N	1.3	1595	5078			78	0				
35	N	1.3	1672	4180					61	0		
36	N	2.1	840	4690					128	0		
37	N	2.1	931	5231							97	0
38	N	1.3	1415	4150							55	0
39	Xe	52.3	78	466							324	0
41	Xe	60	272	621							601	0
43	Xe	80	263	539							625	0
49	Xe	52.3	182	593					403	0		
51	Xe	60	206	505					329	0		
53	Xe	80	189	441					388	0		
56	Xe	52.3	187	544			391	0				
58	Xe	60	146	468			338	0				
60	Xe	80	136	475			401	0				
66	Xe	52.3	225	446	310	0						
68	Xe	60	231	621	424	0						
70	Xe	80	253	573	595	0						

Figure 12. Upset Run Logs

Calculated cross-sections for upsets with EDAC OFF are shown in figure 13 along with a fitted Weibull curve. Even though this curve shows bit upset cross-sections when devices are operating in a non-standard mode, it is important because any analysis of device behavior should include how long data would be stored before being read. For example, if memory was periodically read and re-written (scrubbed) then the devices internal EDAC circuitry would correct single bit errors while being read so data that was re-written to memory would be error free. Error generation rates in some orbit could be used to determine an appropriate scrub rate so the count of random errors never exceeded, perhaps, 100 between scrub operations.

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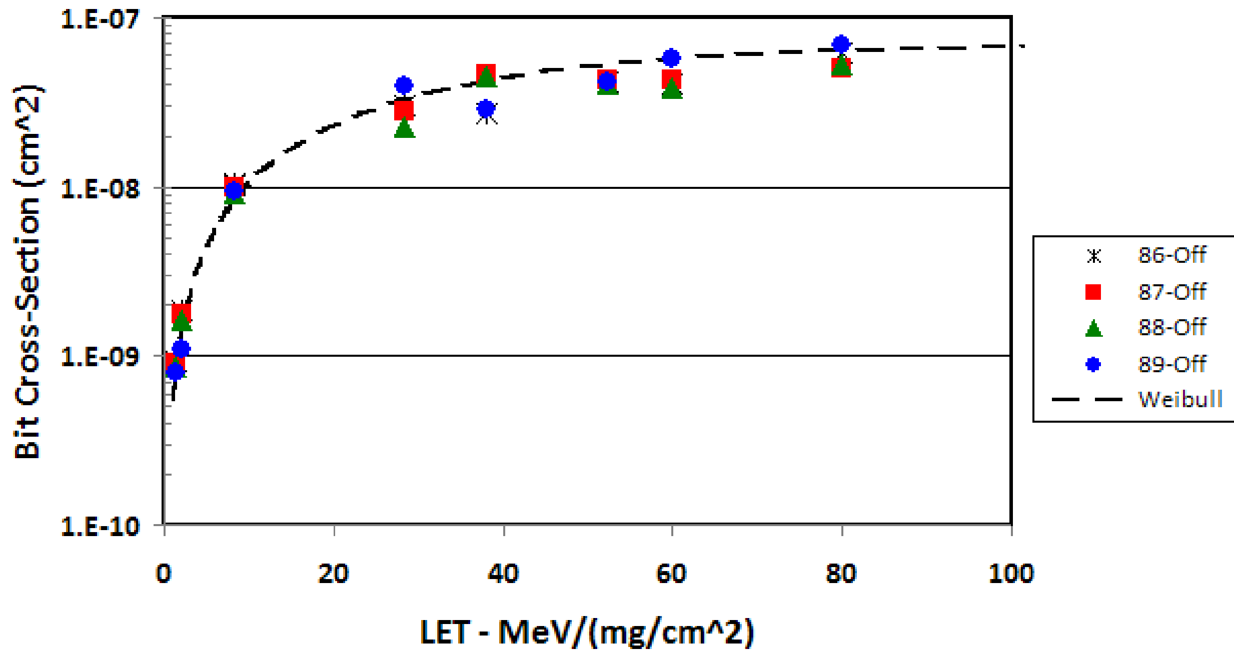

Figure 13. Static Memory Upset Cross-Section Curve (EDAC Off)

Weibull parameters for the curve in Figure 13 are as follows:

OnSet LET = 0.13 MeV/(mg/(cm^2))
Width = 40
Exponent = 1.3
Saturated X-Section = 7.0 u^2 = 7.0e-8 cm^2

Using these parameters figure 14 shows bit error generation rates for these devices in a selection of orbits and solar conditions

	EDAC Off Bit-Errs/Device/Day
Space Station, Solar Minimum	0.614
Space Station, Worst Day (Flare)	2.65E+02
Geosynchronous, Solar Minimum	5.022
Geosynchronous, Worst Day (Flare)	3.29E+04

Figure 14. Upset Rates for Various Orbits and Conditions

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3.4 Memory Upset Patterns

Detailed failure information was collected as part of this test. When the ATV system detects an error it automatically records the address of that error along with the expected data pattern and the location of failing bits. Figure 15 shows an excerpt of the data log from Run 31 where SN86 was exposed to Nitrogen ions having an LET of 1.3 MeV/(mg/(cm^2)).

Test#	Time	Date	#Logged Entries	#failing Vctr/Addr	#failing Bits	Idd (amps)	DATA EXP	ERR	#BIT	ADDR
31	50:34.2	12/13/2019	78	78	78	3.04E-02	HLHLHLHLHLHLHLHL	-------F--------	1	0x1366d
							HLHLHLHLHLHLHLHL	-------------F--	1	0x159cf
							LHLHLHLHLHLHLHLH	--------------F-	1	0x1740c
							LHLHLHLHLHLHLHLH	-----F----------	1	0x17956
							LHLHLHLHLHLHLHLH	-F--------------	1	0x1d90a
							LHLHLHLHLHLHLHLH	--F-------------	1	0x247be
							HLHLHLHLHLHLHLHL	------F---------	1	0x2628b
							HLHLHLHLHLHLHLHL	-----F----------	1	0x2661f
							LHLHLHLHLHLHLHLH	------------F---	1	0x2926e
							LHLHLHLHLHLHLHLH	------------F---	1	0x29e4e
							HLHLHLHLHLHLHLHL	--------------F-	1	0x2cf25
							LHLHLHLHLHLHLHLH	-----F----------	1	0x2e764
							LHLHLHLHLHLHLHLH	--------------F-	1	0x34518
							LHLHLHLHLHLHLHLH	--------------F-	1	0x34918
							HLHLHLHLHLHLHLHL	--F-------------	1	0x3660d
							HLHLHLHLHLHLHLHL	-F--------------	1	0x3c23d
							HLHLHLHLHLHLHLHL	----F-----------	1	0x465eb

Figure 15. Partial Error Log from Run 31, SN86, Nitrogen Ion, LET = 1.3 MeV/(mg/(cm^2))

In this log the first failure was located at address 0x1366D where there was a single bit failure at the bit D8 location of the "DATA" pin group. The second error occurred at address 0x159CF where there was another single bit error at the D2 location.

Note that all failing addresses had single bit errors. Also note that there were 2 single bit failures in the same bit location at addresses 0x2926E and 0x29E4E. Because of the similarity in addresses these 2 bits might both have been upset by one ion strike (multi-cell upset). A similar pair of upsets occurred at addresses 0x34518 and 0x34918.

These memories are organized such that memory cells associated with any data bit are physically close. An ion strike that causes a multi-cell upset will show up as a series of errors occurring at the same bit location across a series of closely related addresses. This phenomena is further illustrated in Figure 16 which shows partial error logs for runs where LETs were 28.3 and 60 MeV/(mg/(cm^2)) . As LET increases the cluster of bits upset by a single ion strike will get larger and there will be an increase in the number of closely related addresses with the same failing bit pattern.

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DATA EXP	ERR	#BIT	ADDR
LHLHLHLHLHLHLHLH	------F---------	1	0x9f3e
LHLHLHLHLHLHLHLH	------F---------	1	0xb1be
LHLHLHLHLHLHLHLH	------F---------	1	0xb33e
LHLHLHLHLHLHLHLH	------F---------	1	0xb59e
LHLHLHLHLHLHLHLH	------F---------	1	0xb71e
LHLHLHLHLHLHLHLH	------F---------	1	0xb99e
LHLHLHLHLHLHLHLH	------F---------	1	0xb9be
LHLHLHLHLHLHLHLH	------F---------	1	0xbb1e
HLHLHLHLHLHLHLHL	--------F-------	1	0x116c5
HLHLHLHLHLHLHLHL	--------F-------	1	0x1a10b
HLHLHLHLHLHLHLHL	--------F-------	1	0x1a12b
HLHLHLHLHLHLHLHL	--------F-------	1	0x1a50b
HLHLHLHLHLHLHLHL	--------F-------	1	0x1a90b
HLHLHLHLHLHLHLHL	-----F----------	1	0x1b739
HLHLHLHLHLHLHLHL	-----F----------	1	0x1bdb9
HLHLHLHLHLHLHLHL	-----F----------	1	0x1bf39
HLHLHLHLHLHLHLHL	-----F----------	1	0x1d319
HLHLHLHLHLHLHLHL	-----F----------	1	0x1d339
LHLHLHLHLHLHLHLH	--------------F-	1	0x1d566
HLHLHLHLHLHLHLHL	-----F----------	1	0x1d599
HLHLHLHLHLHLHLHL	-----F----------	1	0x1d719
HLHLHLHLHLHLHLHL	-----F----------	1	0x1d999
HLHLHLHLHLHLHLHL	-----F----------	1	0x1db19
LHLHLHLHLHLHLHLH	--------------F-	1	0x1f146
LHLHLHLHLHLHLHLH	--------------F-	1	0x1f1c6
HLHLHLHLHLHLHLHL	--F-------------	1	0x222af
HLHLHLHLHLHLHLHL	--F-------------	1	0x226af
HLHLHLHLHLHLHLHL	--F-------------	1	0x2286f
HLHLHLHLHLHLHLHL	--F-------------	1	0x22aaf
HLHLHLHLHLHLHLHL	--F-------------	1	0x22eaf
HLHLHLHLHLHLHLHL	--------------F-	1	0x240ad
HLHLHLHLHLHLHLHL	--F-------------	1	0x2428f
HLHLHLHLHLHLHLHL	--F-------------	1	0x2444f
HLHLHLHLHLHLHLHL	--------------F-	1	0x244ad

LET = 28.3

DATA EXP	ERR	#BIT	ADDR
LHLHLHLHLHLHLHLH	-------F--------	1	0xa190
LHLHLHLHLHLHLHLH	-------F--------	1	0xa590
LHLHLHLHLHLHLHLH	-------F--------	1	0xa990
LHLHLHLHLHLHLHLH	-------F--------	1	0xad10
LHLHLHLHLHLHLHLH	-------F--------	1	0xad90
LHLHLHLHLHLHLHLH	F---------------	1	0xb3d0
LHLHLHLHLHLHLHLH	F---------------	1	0xb7d0
LHLHLHLHLHLHLHLH	F---------------	1	0xbbd0
HLHLHLHLHLHLHLHL	-------------F--	1	0xd227
HLHLHLHLHLHLHLHL	-------------F--	1	0xd2a7
HLHLHLHLHLHLHLHL	-------------F--	1	0xd627
HLHLHLHLHLHLHLHL	-------------F--	1	0xd867
HLHLHLHLHLHLHLHL	-------------F--	1	0xda27
HLHLHLHLHLHLHLHL	-------------F--	1	0xdaa7
HLHLHLHLHLHLHLHL	-------------F--	1	0xdc47
HLHLHLHLHLHLHLHL	-------------F--	1	0xdc67
HLHLHLHLHLHLHLHL	-------------F--	1	0xde07
HLHLHLHLHLHLHLHL	-------------F--	1	0xde27
HLHLHLHLHLHLHLHL	-------------F--	1	0xde87
HLHLHLHLHLHLHLHL	-------------F--	1	0xf207
HLHLHLHLHLHLHLHL	-------------F--	1	0xf287
HLHLHLHLHLHLHLHL	-------------F--	1	0xf687
HLHLHLHLHLHLHLHL	-------------F--	1	0xf847
HLHLHLHLHLHLHLHL	-------------F--	1	0xfa87
LHLHLHLHLHLHLHLH	--F-------------	1	0x1f076
LHLHLHLHLHLHLHLH	--F-------------	1	0x1f456
LHLHLHLHLHLHLHLH	--F-------------	1	0x1f616
LHLHLHLHLHLHLHLH	--F-------------	1	0x1f6b6
LHLHLHLHLHLHLHLH	--F-------------	1	0x1f856
LHLHLHLHLHLHLHLH	--F-------------	1	0x1f876
LHLHLHLHLHLHLHLH	--F-------------	1	0x1fa36
LHLHLHLHLHLHLHLH	--F-------------	1	0x1fa96
LHLHLHLHLHLHLHLH	--F-------------	1	0x1fab6
LHLHLHLHLHLHLHLH	--F-------------	1	0x1fc56

LET = 60

Figure 16. Partial Error Logs from Runs 8 and 68, SN86, Krypton (LET = 28.3) and Xenon (LET=60)

3.5 Logic Upsets

The primary upset mechanism for these devices is memory upsets. In fact, with normal testing, so many memory upsets occur at low fluences that other upset mechanisms will probably never be observed. With this in mind a special test algorithm was developed in which a pattern (Data = CB) was written to a burst of 256 addresses and then immediately read back with EDAC ON. The alternate pattern (CB*) was then written over the same address range and immediately read back. If no errors were detected then the next 256 addresses would written/read, etc until the entire memory space had been tested. The test program would repeatedly scan the entire memory space using this write/read/step method until an error was detected.

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Testing of each address subset took 35uS.and there was a 5.2uS “dead time” before testing began on the next address subset. When any errors were detected the high speed ATV test would immediately stop and errors would be recorded. The test would then be restarted and the event would be counted as a single device level upset. The number of upset events would be counted over a long exposure to determine device level upset cross-sections.

Since there was very little time between writing and reading any set of 256 memory patterns then there would be a correspondingly low probability of random memory upsets. Consequently, any upsets that occurred would probably come from strikes in other circuitry.

The pattern of memory upsets detected during this testing was always very similar and had the signature shown in figure 17. This figure shows a large number of upsets occurring at the same bit location over a large portion of the address subset being tested. Errors occurred in every second address indicating bit “0”, in this case, was stuck at a high level. Since the stored pattern was CB then the expected output on passing addresses would be high so a bit stuck high would not fail. In other dynamic tests the failing bit was stuck low.

Test#	Time	Date	#Logged Entries	#failing Vctr/Addr	#failing Bits	Idd (amps)	DATA EXP	ERR	#BIT	ADDR
333	16:00.9	12/14/2019	182	182	182	5.47E-02	HLHLHLHLHLHLHLHL	---------------F	1	0x8024a
							HLHLHLHLHLHLHLHL	---------------F	1	0x8024c
							HLHLHLHLHLHLHLHL	---------------F	1	0x8024e
							HLHLHLHLHLHLHLHL	---------------F	1	0x80250
							HLHLHLHLHLHLHLHL	---------------F	1	0x80252
							HLHLHLHLHLHLHLHL	---------------F	1	0x80254
							HLHLHLHLHLHLHLHL	---------------F	1	0x80256
							HLHLHLHLHLHLHLHL	---------------F	1	0x80258
							HLHLHLHLHLHLHLHL	---------------F	1	0x8025a
							HLHLHLHLHLHLHLHL	---------------F	1	0x8025c
							HLHLHLHLHLHLHLHL	---------------F	1	0x8025e
							HLHLHLHLHLHLHLHL	---------------F	1	0x80260
							HLHLHLHLHLHLHLHL	---------------F	1	0x80262
							HLHLHLHLHLHLHLHL	---------------F	1	0x80264
							HLHLHLHLHLHLHLHL	---------------F	1	0x80266
							HLHLHLHLHLHLHLHL	---------------F	1	0x80268
							HLHLHLHLHLHLHLHL	---------------F	1	0x8026a
							HLHLHLHLHLHLHLHL	---------------F	1	0x8026c

Figure 17. Partial Data Log for Run #52, Dynamic Test, SN88, LET = 60 MeV/(mg/(cm^2))

No dynamic tests were performed with EDAC OFF.

Figure 18 shows the number of device level failing events over the course of testing. Note that all dynamic tests were performed to a fluence of 5e4 ions/cm^2 which was ~20X higher than fluences used for bit upset testing.

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					# DEVICE ERRORS			
Run	Ion	LET	Flux	Fluence	Sn86	SN87	SN88	SN89
7	Kr	38	927	5.00E+04	1			
9	Kr	28.3	227	5.00E+04	0			
11	Kr	28.3	176	5.00E+04		0		
13	Kr	38	150	5.00E+04		4		
15	Kr	38	165	5.00E+04			3	
17	Kr	28.3	208	5.00E+04			0	
19	Kr	28.3	304	5.00E+04				0
21	Kr	38	240	5.00E+04				0
23	Ar	8.4	187	5.00E+04				0
25	Ar	8.4	439	5.00E+04			0	
27	Ar	8.4	423	5.00E+04		0		
30	Ar	8.4	374	5.00E+04	0			
40	Xe	52.3	267	5.23E+04				0
42	Xe	60	353	5.00E+04				0
50	Xe	52.3	242	5.00E+04			0	
52	Xe	60	203	5.00E+04			2	
57	Xe	52.3	195	5.00E+04		0		
59	Xe	60	179	5.00E+04		1		
67	Xe	52.3	318	5.00E+04	0			
69	Xe	60	288	5.00E+04	0			

Figure 18. Partial Data Log for Dynamic Tests Showing the Number of Device Level Failing Events per Run

Figure 19 is a plot of the device level upset cross-sections for dynamic errors along with a Weibull curve that encloses all detected failures.

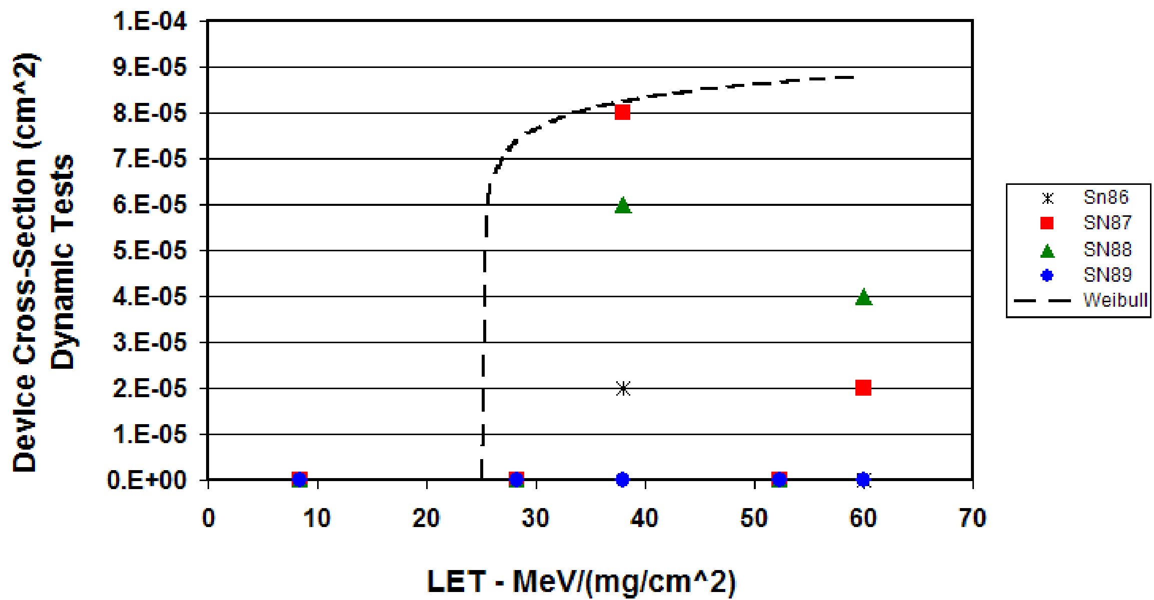

Figure 19. Device Level Upsets Cross-Sections, Dynamic Testing

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Weibull parameters for the curve in Figure 19 are as follows:

OnSet LET = 25 MeV/(mg/(cm^2))
Width = 0.7
Exponent = 0.2
Saturated X-Section = 9.9e3 u^2 = 9.9e-5 cm^2

Using these parameters figure 20 shows the device level upset rates for these devices in a selection of conditions

	Dynamic Operation SEUs/Device/Day
Space Station, Solar Minimum	4.52E-06
Space Station, Worst Day (Flare)	2.06E-03
Geosynchronous, Solar Minimum	5.33E-05
Geosynchronous, Worst Day (Flare)	5.11E-02

Figure 20. Dynamic Operating Upset Rates for Various Orbits and Conditions

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4.0 Conclusions

Single event effects testing has been conducted on the 16M Async SRAM CYRS1061G30-10GGMB platform device:

1) No latch-up events were observed for devices at 95^0C and irradiated with ions having an LET of 60MeV(mg/cm^2) to a fluence of1E7 ions/cm^2.
2) Memory cell upset testing was performed on 4 devices in normal operating mode (EDAC ON) and a special test mode (EDAC OFF). Upset cross-sections were very repeatable across all devices for the ECC OFF test mode. In normal operating mode (EDAC ON) random memory upsets were corrected in almost all cases.
3) Device level upset cross-sections were measured when devices were operated in a dynamic mode. Dynamic operating error rates were calculated for several orbits and solar conditions.
4) No SEFI events were observed up to 80 MeV(mg/cm^2)

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