Single Event Effect Test Report on Infineon Rad-Hard MOSFETs
*****BUY65CS family*****

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§1 SCOPE

This test report describes Single Event Effect (SEE) tests and results for radiation hardened MOSFETs from Infineon for device types BUY65CS, in accordance to ESCC Basic Specification 25100.

In total two (2) different chip sizes of the same wafer technology numbered #1 and #2 have been tested with 124Xe and 208Pb ions of LET and penetration as given in table 1. Concurrently, TID hardness tests were performed for the same device designs, see separated report.

Tests have been performed at the facilities SPIRAL of Grand Accélérateur National d'Ions Lourds (GANIL), Caen, France (Tests SEE2) and CYCLONE at Louvain-la-Neuve, Belgium (Test SEE3).

Run	Location	Ion	Acc.Energy [MeV]	Chip size	Degrader	Air [mm]	LET [MeVcm^2/mg]	Range [µm]
SEE2	GANIL	$^{208}Pb^{56+}$	1624	#1	Al 100µm	90	90.8	122.6
SEE3	Louvain	$^{124}Xe^{35+}$	995	#1,2	---	---	62.5	73.1

Table 1: Overview of SEE Tests for BUY65CS chip size #1,2 and beam characteristics (LET and ion penetration depths) for Xe and Pb ions for sources CYCLONE (Louvain) and SPIRAL (GANIL).

§2 DEVICE INFORMATION

Chip size	Part Type	BVdss [V]	Vgs(th) [V]	Rds(on) [mOhm]	Idmax [A]
#1	BUY65CS08J	650	2.0 – 4.0	450	8 (RT)
#2	BUY65CS28A	650	2.0 – 4.0	150	28 (RT)

§2.1 APPLICABLE DOCUMENTS

- BUY65CS ESCC Draft Detail Specification for HiRel RadHard Power-MOS 650V family, Version June 2019.
- ESCC Basic Specification 25100

§2.2 DEVICES MARKINGS AND SAMPLE PREPARATION

In order to contact devices with the TO test sockets on bias boards, chips have been soldered and bonded to respective 3-pin PCB-TO-adapter boards to connect Gate/Drain/Source contacts of the MOSFETs.

Devices' numbers are written on the PCB with a permanent marker. The number correlates in the sample list to the lot and wafer number.

§2.3 PARAMETER MEASUREMENTS

Test samples have passed on-wafer tests, notably BVDSS, Vgs(th), RDSON, IDSS, IGSS with their parameters within predetermined upper/lower limits.

Parameter measurements have been performed on adapter-mounted devices to check that devices have not been degraded. Specifically, IDSS(650V), IGSS(+/-20V), RDSON(18/5A, Ugs=10V), VSD(28/8 A), Vgs(th)(1 mA), BVDSS(0.25 mA) are determined.

§3 TEST SET-UP

§3.1 TEST BOARD

The test board was designed to accommodate up to 10 test samples, each consisting of an individual bias circuit (fig. 1). This test board (fig. 2) was fixed to the mechanical positioning stage provided at the Louvain/GANIL beam line. All voltages UDS and UGS were provided via a flat band cable from a switch board. The oscilloscope output was left unconnected.

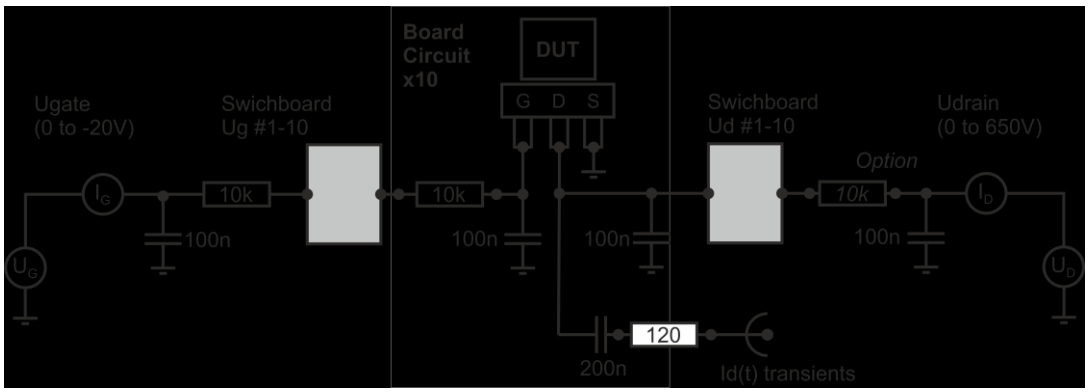

Fig. 1: Test circuit for SEB/SEGR test.

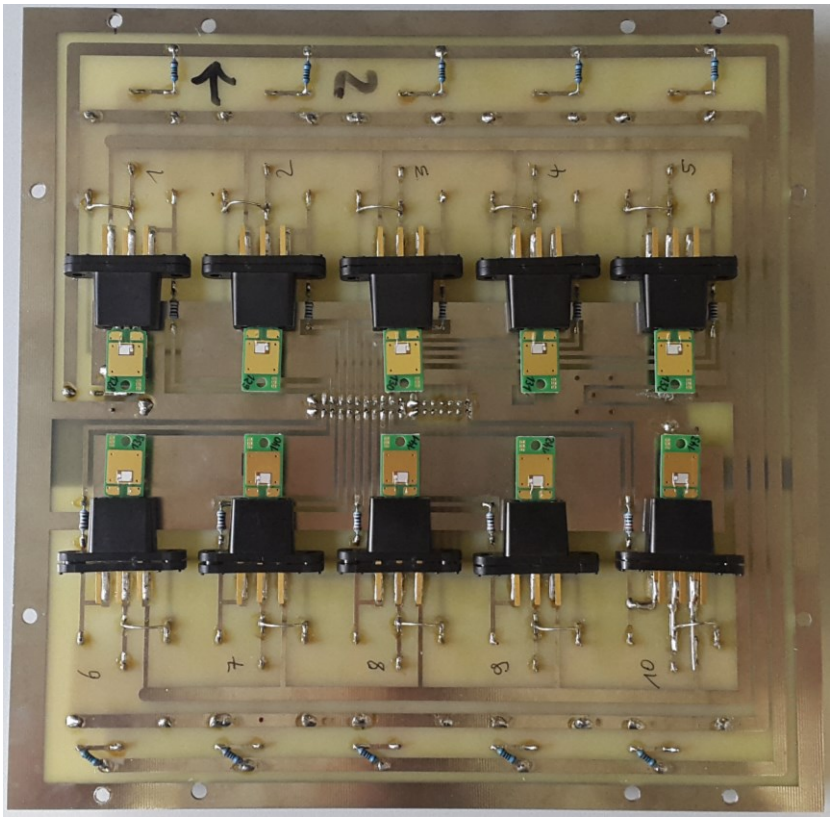

Fig. 2: Test-Board with 10 positions with TO test sockets. Separate bias of UDS and UGS for each device. Flat-band connector on back side.

§3.2 MEASUREMENT EQUIPMENT

As a voltage source for UDS and for ID current measurements a Keithley 237 High Voltage Measurement Unit has been employed. Gate voltage UGS and measurement of IG are provided by a Keithley 236 Source Measure Unit.

Voltages were set manually as were all recordings of run number, time, sample number, all current readings, specifically PIGS currents, are logged. The irradiation report provided by GANIL operators, in addition, give fluence values for each test run.

§4 HEAVY ION IRRADIATION FACILITIES

§4.1 BEAM PARAMETERS

SPIRAL at GANIL Caen is a cyclotron capable of providing heavy ions of very high energy, in the order 28MeV/u, i.e. 6 GeV per ion for 208Xe (56+ charge state) employed in irradiation run SEE2.

CYCLONE at UCL Louvain-la-Neuve is a cyclotron capable of providing a “cocktail” of heavy ions with about the same M/Q ratio. From a HIF cocktail 124Xe (35+ charge state) are selected with an energy of 995 MeV yielding the characteristics in Table 2. CYCLONE source was employed in irradiation run SEE3.

Parameters were chosen to provide the highest possible LET for a given minimum of penetration depth about 70 µm, determined by the thickness of the – active – epitaxial layer of the MOSFETs (less than 35µm including top metallization and imide), see table 1.

§4.2 TESTING POSITION AND TEST BOARD MOUNTING

At GANIL irradiation is performed in air. The test board is screwed onto a motorized positioning frame (fig. 3). The beam exit of the vacuum tube has a 10 µm stainless steel window. Beam size is 200 mm (horizontal) and 50 mm (vertical). With the bias board as in fig. 2, all devices are irradiated simultaneously and further device positioning is usually not necessary. To achieve the desired LET/penetration, aluminium foil degraders and adjusted air distances are used.

In both facilities, ion incidence was chosen to be 0°, i.e., vertical incidence.

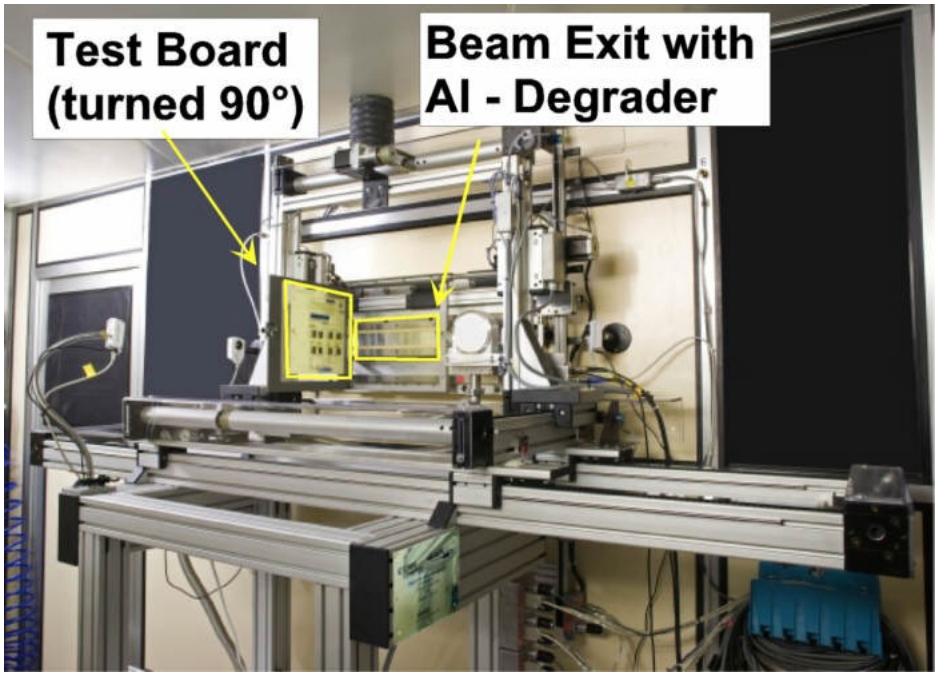

Fig. 3: Test Board positioning at GANIL beam line exit window

At CYCLONE test boards are mounted within a vacuum chamber with feedthroughs for electrical bias and signals. The ion beam is positioned on the device under test.

§4.3 DOSIMETRY

Control of beam homogeneity and dosimetry as well as beam operation is the responsibility of ion beam providers. An irradiation log provided by GANIL gives actual flux values for each test run, including fluence-to-fail, if applicable.

§5 TEST SEQUENCE

§5.1 BEAM PARAMETERS AND TEST CRITERIA FOR ALL TESTS

- LET see Table 1
- Flux 3E+3 ions/cm^2/s
- Fluence 3E+5 ions/cm^2
- Normal incidence of ion beam
- Destructive mode. FAIL current criteria: IDS>2 µA or IGS>100 nA.
- Required number of test samples per test case: 1(for FAIL)/3(for PASS)
- Post Irradiation Gate Stress (PIGS) test at any UDS (at respective UDS, UGS down to -25V, in steps of -5V). FAIL criterion: either IDS or IGS>100nA

§5.2 TEST BIAS SEQUENCE FOR SEB-SOA

Test sequence for Single Event Breakdown (SEB-SOA):

UGS: 0 V
UDS: Start at 650V (or UDS,max). If *FAIL* occurs UDS is stepped-down by 10V until *PASS*.

§5.3 TEST BIAS SEQUENCE FOR SEGR-SOA

Test sequence for Single Event Gate Rupture (SEGR-SOA):

UGS: negative, starting at -15 V, steps of -5 V. For UGS at the edge of the SOA curve, smaller steps (-2,-3V) have been tested as well.

UDS: Start at maximum UDS at which PASS value was obtained for previous UGS-test sequence (or UGS=0V). If FAIL occurs UDS is stepped-down by 10V until PASS.

The combination of SEB-SOA and SEGR-SOA yields the Single Event Effect (SEE)-SOA.

§6 TEST RESULTS

Devices of type BUY65CS in two chip sizes numbered #1,2 has been tested and maximum SEE-SOA for UDS/(negative)UGS combinations established.

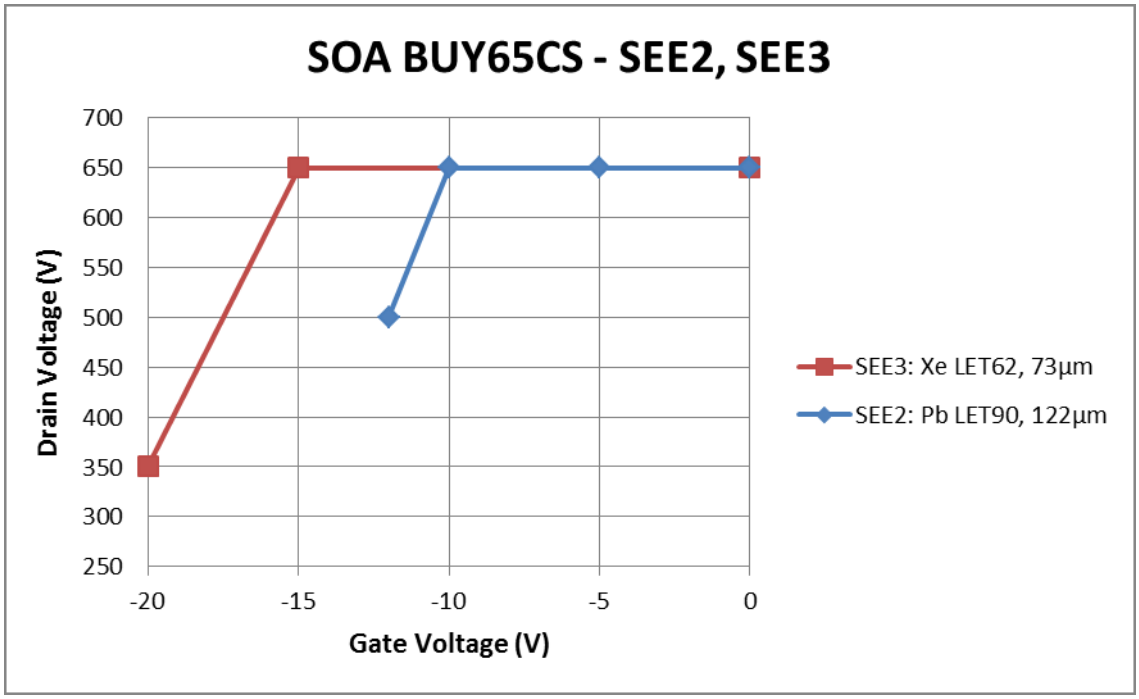

Fig. 5: Maximum SEE-SOA of BUY65CS as determined at test SEE2 (GANIL) and SEE3 (CYCLONE) with Pb and Xe ions respectively.

§7 CONCLUSION

A series of SEE tests for two chips sizes of BUY65CS family MOSFETs have been performed.

Ion source CYCLONE (Louvain) with elevated LET and Xe ion penetration of 73 µm confirms a SOA in which the drain voltage satisfies the rated UDS (650V) up to UGS = -15V.

Ion source GANIL with high LET and Pb ion penetration range shows that the tested wafer technology is radiation hard even in extreme application conditions.

§8 DETAILS OF TEST RUNS

Details of individual test runs SEE2 and SEE3 are tabulated in this section.

test	*Board Pos*	*chip*	*Flux (i/cm2/sec)*	*Fluence (/cm²)*	*Vds test(V)*	*Vgs test (V)*	*PIGS*	*COMMENTS*
no. 6	1	37	3000	3.00E+05	600	0		shutter closed - no irradiation
					650	0	ok	
					650	-5	ok	
					650	-10	ok	
					600	-15	ID, IG fail	
	2	38			650	0	ok	
					650	-5	ok	
					650	-10	ok	
					300	-15	ok	
					400	-15	ID, IG fail	
	3	39			650	0	ok	
					650	-5	ok	
					650	-10	ok	
					300	-15	ok	
					350	-15	ID, IG fail	
	4	40			300	-15	ID, IG fail	
	5	41			300	-12	ok	
					350	-12	ok	
					400	-12	ok	
					450	-12	ok	
					500	-12	ok	
					550	-12	IG fail	
	6	42			450	-12	ok	
					500	-12	ok	
					520	-12		no beam - broken down accelerator
					520	-12		beam fail - not enough fluence
					520	-12	ok	small IG at PIGS -27V, but pass
					500	-12	ok	
					520	-12	ID, IG fail	Gate could have been damaged before with PIGS-27
	7	43			500	-12	ok	
					520	-12	ok	
	8	44			520	-12	ok	
	9	45			520	-12	ok	

Tab. 2: Test SEE2: Pb– Wafer VE802327 #03– size #1.

test	*Board Pos*	*chip*	*Flux (i/cm2/sec)*	*Fluence (/cm²)*	*Vds test(V)*	*Vgs test (V)*	*PIGS*	*COMMENTS*
No.10	7	194	3000	3.00E+05	650	0	ok	size #1
					650	-15	ok	
					350	-20	ok	
	8	195			650	0	ok	
					650	-15	ok	
					350	-20	ok	
	9	196			650	0	ok	
					650	-15	ok	
					350	-20	ok	
No.11	2	173			650	0	ok	size #2
					650	-15	ok	
					350	-20	ok	
	3	174			650	0	ok	
					650	-15	ok	
					350	-20	ok	
	4	175			650	0	ok	
					650	-15	ok	
					350	-20	ok	

Tab. 3: Test SEE3: Xe – Wafer VE801160 #1– size #1 and VE840444 #6 – size #2