Irradiation Test Report

Single Event Effect Test on Infineon Rad-Hard-MOSFETs

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1 SCOPE

This test report describes Single Event Effect (SEE) tests and results for radiation hardened MOSFETs from Infineon with designated device types BUY25CS12J and BUY25CS54A, in accordance to ESCC Basic Specification 25100.

Tests have been performed at the facility SPIRAL of Grand Accélérateur National d'Ions Lourds (GANIL), Caen, France, week 14 (test GANIL2) and week 23 (test GANIL3) in 2011.

For each test session Test Plans have been established and reviewed by ESA:

- Test Plan GANIL2, April 04, 2011
- Test Plan GANIL3, June 20, 2011



Fig. 1: Device packages: SMD2 on 3-pin TO-adapter for BUY25CS54A (left) and TO257 (right) for BUY25CS12J

2 DEVICE INFORMATION

Part Type	Vds [V]	Vgs(th) [V]	Rds(on) [Ohm]	Idmax [A]
BUY25CS12J-01	250	2.0 - 4.0	0.13	12.5 (RT)
BUY25CS54A-01	250	2.0 - 4.0	0.03	54 (RT)

2. 1Applicable Documents

- BUY25CS12J01_V3 Target Data Sheet for HiRel RadHard Power-MOS (12.5A SMD05 package), Revision V3c, July 2011
- BUY25CS54A01_V1 Target Data Sheet for HiRel RadHard Power-MOS (54A, SMD2 package), Revision V1c, July 2011

2.2 Devices Markings and Sample Preparation

Devices are mounted either in SMD2 packages (BUY25CS54A) or TO257/SMD05 packages (BUY25CS12J) with the packages left unlidded. In order to contact devices with the TO test sockets on bias boards SMD-packages have been soldered to respective 3-pin-adapter boards (fig. 1) to connect Gate/Drain/Source contacts of the MOSFETs.

Devices numbers are engraved on the backside of the TO257 package or scribed on the metallization of adapter boards in the case of SMD. The engraving represents information on wafer lot and wafer number as well as device number.

Prior to SEE tests imide layers on the chip's surface have been chemically removed.

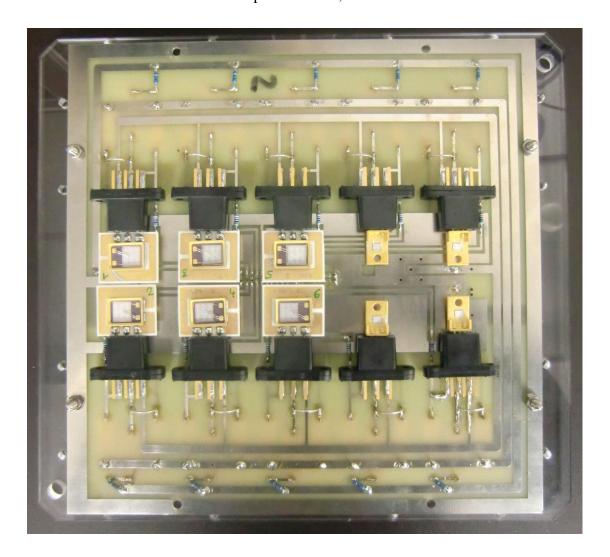


Fig. 2: Test-Board with 10 positions with TO test sockets. Separate bias of UDS and UGS for each device. Flat-band connector on back side. The arrangement of devices is such that the GANIL ion beam irradiations all of the devices simultaneously (beam area: 200mm (horizontal) x 50mm (vertical).

2.3 Parameter Measurements

Test samples have passed on-wafer tests, notably BVDSS, Vgs(th), RDSON, IDSS, IGSS with their parameters within predetermined upper/lower limits. Parameter measurements have been performed on package- and adaptermounted devices to check that devices have not been degraded.

3. TEST SET-UP

3.1 Test Board

The test board was designed to accommodate up to 10 test samples, each consisting of an individual bias circuit (fig. 2). This test board was fixed to the mechanical positioning stage provided at the GANIL beam line. All voltages UDS and UGS were provided via a flat band cable from a switch board. The oscilloscope output was left unconnected. The bias circuit is given in fig. 3.

3.2 Measurement Equipment

As a voltage source for UDS and for ID current measurements a *Keithley 237 High Voltage Measurement Unit* has been employed.

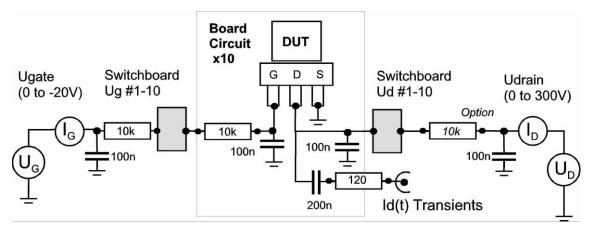


Fig. 1: Test circuit for SEB/SEGR test (GANIL 2011).

Gate voltage UGS was provided by an *Agilent E3649A Dual Output DC Power Supply* with gate current measured by *a HP34401A Multimeter*.

Voltages were set manually as were all recordings of run number, time, sample number, PIGS current. The irradiation log provided by GANIL operators, in addition, give fluence values for each test run (GANIL Report on Infineon Irradiations April 20, 2011, and July 5, 2011).

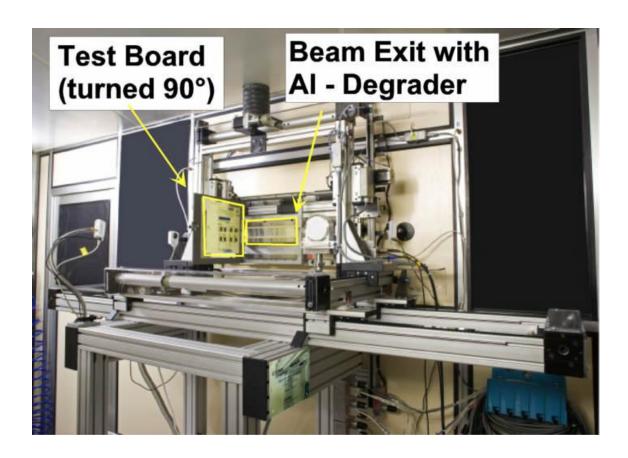


Fig. 4: Test Board positioning at GANIL beam line exit window

4 HEAVY ION IRRADIATION FACILITY

4. 1 Beam Parameters

SPIRAL at GANIL is a cyclotron capable of providing heavy ions of very high energy, in the order 50MeV/u, i.e. 6 GeV per ion for 129Xe (46+ charge state) employed in irradiation runs GANIL2 and GANIL3.

Table 5-1: GANIL beam characteristics for 129Xe (TRIM based).

Run	Setting	Degrader	Air [mm]	LET [MeVcm²/mg]	Range [µm]
GANIL2		Al 500µm	98	55.14	90.03
GANIL3	А	Al 500µm	93	55.1	90.28
GANIL3	В	Al 300µm	150	38.02	278.9

The change of beam parameters, i.e. insertion of Al-degraders and adjustment of appropriate air space takes a few minutes.

Parameters of GANIL2 and GANIL3(A) were chosen to provide the highest possible LET for a given minimum of penetration depth, determined by the thickness of the – active – epitaxial layer of the MOSFETs (less than $50\mu m$ including top metallization).

Parameter GANIL3B was chosen to not only penetrate the epitaxial layer but also to fully penetrate the device substrate.

4.2 Testing Position and Test Board Mounting

Irradiation is performed in air with a minimum gap spacing of 53 mm. The test board is screwed onto a motorized positioning frame (fig. 4). The beam exit of the vacuum tube has a 10 μ m stainless steel window. Beam size is 200 mm (horizontal) and 50 mm (vertical). With the bias board as in fig. 2, all devices are irradiated simultaneously and further device positioning is usually not necessary.

4.3 Dosimetry

Control of beam homogeneity and dosimetry lies within the responsibility of GANIL operators. An irradiation log provided by GANIL gives fluence values for each test run (GANIL Report on Infineon Irradiations April 20, 2011, and July 5, 2011), including fluence-to-fail, if applicable.

5 TESTING SEQUENCE

5.1 Beam Parameters and Test Criteria for all Tests:

- LET see Table 5-1
- Flux 1E4 ions/cm²/s (plan). GANIL2: 7E3-1.1E4; GANIL3: 1.3E3-4.2E3
- Fluence 3E+5 ions/cm²
- Normal incidence of ion beam
- Destructive mode. FAIL current criteria: IDS>2 µA or IGS>100 nA.
- Required number of test samples per test case: 1(for FAIL)/3(for PASS)

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 Post Irradiation Gate Stress (PIGS) test at any UDS (at respective UDS, UGS down to -20V, in steps of -5V). FAIL criterion: either IDS or IGS>100nA

5.2 Test Bias Sequence to determine Single Event Breakdown (SEB)-SOA

UGS: 0 V

UDS: Start at 260V (or UDS,max). If FAIL occurs UDS is stepped-down by 10V until PASS.

5.3 Test Bias Sequence to determine Single Event Gate Rupture (SEGR)-SOA

UGS: -5 V to -20 V, starting at -5 V, steps of -5 V.

UDS: Start at maximum UDS at which PASS value was obtained for previous UGS-test sequence (or UGS=0°V). If *FAIL* occurs UDS is stepped-down by 10V until PASS.

6. TEST Results

6.1 Test Devices

In the two campaigns GANIL2 and GANIL3 devices groups originating from four wafer lots underwent ion irradiation tests (see Tab: 6-1). Devices are mounted in SMD and TO257 packages, as indicated in the "descriptor" of Tab.6-1.

Tab. 6-1: Device groups in SEE tests GANIL2 and GANIL3 of 4 different wafer lots.

Lot	Wafer	GANIL2	GANIL3	Descriptor
VE106719.01	7			SMD05
VE112380	2			SMD2
VE109331	25			TO257
VE109331	25			TO257
VE117988	5			SMD2

6.2 Details of Test Runs

Details of individual test runs are given in Tab. 6-2 (GANIL2) and Tab. 6-3 (GANIL3).

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Tab. 6-2: Devices tested in campaign GANIL2.

April 5, 2011		GANIL2							
Lot	Wafer	Chip	Pos	Ion	Fluence (/cm²)	Vgs test (V)	Vds test (V)	Nb events	PIGS test
VE109331	25	1	1		3.0E+05	0 V	260 V	0	ok
VE109331	25	1			3.0E+05	-5 V	260 V	0	ok
VE109331	25	1			3.0E+05	-10 V	260 V	0	ok
VE109331	25	1			3.0E+05	-15 V	260 V	0	ok
VE109331	25	1			2.7E+05	-20 V	260 V	0	ok
VE109331	25	1			3.0E+05	-20 V	260 V	0	ok
VE109331	25	1			3.5E+04	-25 V	260 V	1	
VE109331	25	2	2		8.7E+04	-20 V	260 V	1	
VE109331	25	3	3		3.0E+05	-15 V	260 V	0	ok
VE109331	25	3			3.0E+05	-20 V	200 V	0	ok
VE109331	25	3			3.0E+05	-20 V	220 V	0	ok
VE109331	25	3			3.0E+05	-20 V	240 V	0	ok
VE109331	25	3			3.0E+05	-20 V	260 V	0	ok
VE109331	25	3			5.5E+04	-25 V	160 V	1	
VE109331	25	4	4		3.00E+05	-15 V	260 V	0	ok
VE109331	25	4			3.00E+05	-20 V	220 V	0	ok
VE109331	25	4			3.00E+05	-20 V	240 V	0	ok
VE109331	25	4			3.00E+05	-20 V	260 V	0	ok
VE109331	25	4			3.00E+05	-25 V	100 V	0	ok
VE109331	25	4			7.99E+04	-25 V	120 V	1	
VE109331	25	5	5		3.00E+05	-20 V	220 V	0	ok
VE109331	25	5			3.00E+05	-20 V	240 V	0	ok
VE109331	25	5			3.00E+05	-20 V	260 V	0	ok
VE109331	25	5			3.00E+05	-25 V	100 V	0	ok
VE109331	25	5			3.00E+05	-25 V	120 V	0	ok
VE109331	25	5			7.90E+03	-25 V	140 V	1	
VE112380	2	46	1		3.00E+05		260 V	0	ok
VE112380	2	56	6		3.00E+05	0 V	260 V	0	ok
VE112380	2	47	2		3.00E+05	0 V	260 V	0	ok
VE112380	2	55	7		3.00E+05	-5 V	260 V	0	ok
VE112380	2	48	3		3.00E+05	-5 V	260 V	0	ok
VE112380	2	54	8		3.00E+05	-5 V	260 V	0	ok
VE112380	2	49	4		3.00E+05	-10 V	260 V	0	ok
VE112380	2	53	9		3.00E+05	-10 V	260 V	0	ok
VE112380	2	50	5		3.00E+05	-10 V	260 V	0	ok
VE112380	2	52	10		3.00E+05	-15 V	260 V	0	ok
VE112380	2	57	1		3.00E+05	-15 V	260 V	0	ok
VE112380	2	58	2		3.00E+05	-15 V	260 V	0	ok
VE112380	2	63	7		8.05E+04		200 V	1	<u> </u>
VE112380	2	59	3		3.00E+05		140 V	0	ok
VE112380	2	59	3		3.00E+05		160 V	0	ok
VE112380	2	59	3		3.00E+05		180 V	0	ok
VE112380	2	59	3		1.92E+05		200 V	1	
VE112380	2	64	8		3.00E+05		160 V	0	ok
VE112380	2	64	8		3.00E+05		180 V	0	ok
VE112380	2	64	8		3.00E+05		200 V	0	ok
VE112380	2	64	8		3.00E+05		220 V	0	ok
VE112380	2	64	8		2.47E+05		240 V	1	- OK
VE112380	2	60	4		3.00E+05		80 V	0	ok
VE112380	2	60	4		4.43E+04		100 V	1	- OK
VE112380 VE112380	2	65	9		3.00E+05		60 V	0	ok
VE112380 VE112380	2	65	9		3.00E+05		80 V	0	ok
VE112380 VE112380	2	65	9		3.00E+05		100 V	0	ok
VE112380 VE112380	2	65	9		4.88E+04		100 V	1	UK
VE112380 VE112380		61	5		3.00E+05		60 V	0	٥k
VE112380 VE112380	2	61	5		3.00E+05 3.00E+05		80 V	0	ok ok
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April 5, 201	1		GANIL2	2					
Lot	Wafer	Chip	Pos	Ion	Fluence (/cm²)	Vgs test (V)	Vds test(V)	Nb events	PIGS test
VE106719.01	7	47	2		3.00E+05	0 V	260 V	0	ok
VE106719.01	7	46	1		3.00E+05	0 V	260 V	0	ok
VE106719.01	7	48	6		3.00E+05	0 V	260 V	0	ok
VE106719.01	7	49	1		3.00E+05	-5 V	260 V	0	ok
VE106719.01	7	54	6		3.00E+05	-5 V	260 V	0	ok
VE106719.01	7	50	2		3.00E+05	-5 V	260 V	0	ok
VE106719.01	7	55	7		3.00E+05	-10 V	260 V	0	ok
VE106719.01	7	51	3		3.00E+05	-10 V	260 V	0	ok
VE106719.01	7	56	8		3.00E+05	-10 V	260 V	0	ok
VE106719.01	7	52	4		3.00E+05	-15 V	260 V	0	ok
VE106719.01	7	57	9		3.00E+05	-15 V	260 V	0	ok
VE106719.01	7	53	5		3.00E+05	-15 V	260 V	0	ok
VE106719.01	7	58	10		3.00E+05	-15 V	180 V	0	ok
VE106719.01	7	58	10		3.00E+05	-15 V	200 V	0	ok
VE106719.01	7	58	10		3.00E+05	-15 V	220 V	0	ok
VE106719.01	7	58	10		3.00E+05	-15 V	240 V	0	ok
VE106719.01	7	58	10		3.00E+05	-15 V	260 V	0	ok
VE106719.01	7	59	1		3.00E+05	-25 V	100 V	0	ok
VE106719.01	7	59	1		3.00E+05	-25 V	120 V	0	ok
VE106719.01	7	59	1		3.00E+05	-25 V	140 V	0	ok
VE106719.01	7	59	1		4.70E+04	-25 V	160 V	1	
VE106719.01	7	59	1		3.00E+05	-20 V	220 V	0	ok
VE106719.01	7	60	6		3.00E+05	-20 V	240 V	0	ok
VE106719.01	7	60	6		4.90E+04	-20 V	260 V	1	
VE106719.01	7	61	2		3.00E+05	-20 V	220 V	0	ok
VE106719.01	7	61	2		3.00E+05	-20 V	240 V	0	ok
VE106719.01	7	62	7		3.00E+05	-25 V	100 V	0	ok
VE106719.01	7	62	7		3.00E+05	-25 V	120 V	0	ok
VE106719.01	7	62	7		4.70E+04	-25 V	140 V	1	
VE106719.01	7	64	3		3.00E+05	-25 V	100 V	0	ok
VE106719.01	7	64	3		2.35E+05	-25 V	120 V	1	

Tab. 6-2 continued: Devices tested in campaign GANIL2.

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Tab. 6-3: Devices tested in campaign GANIL3. Ion parameters A, B with reference to Tab. 5-1

June 22, 20	11	(GANIL:	3					
Lot	Wafer	Chip	Pos	lon	Fluence (/cm²)	Vgs test (V)	Vds test (V)	Nb events	PIGS test
VE109331	25	7	1	Α	300000	0	200	ok	ok
VE109331	25				300000	0	260	ok	ok
VE109331	25				300000	-15	260	ok	ok
VE109331	25				300000	-20	240	ok	ok
VE109331	25				300000	-20	260		fail
VE109331	25	8	6		<300000	-25	100	fail	
VE117988	5	1	1		300000	0	260		ok
VE117988	5				300000	-15	260		fail
VE117988	5	2	6		300000	-10	260		ok
VE117988	5				300000	-15	220		ok
VE117988	5				300000	-15	240		ok
VE117988	5				300000	-15	260		ok
VE117988	5				137900	-20	200	fail	
VE117988	5	3	2		300000	-20	140		ok
VE117988	5				300000	-20	160		ok
VE117988	5				300000	-20	170		ok
VE117988	5				93600	-20	180	fail	
VE117988	5	4	7		300000	-25	80		ok
VE117988	5				273000	-25	100	fail	
VE117988	5	5	3		300000	-10	260		ok
VE117988	5				300000	-15	240		ok
VE117988	5				300000	-15	260		ok
VE117988	5				300000	-20	160		ok
VE117988	5				300000	-20	180		ok
VE117988	5				201000	-20	200	fail	
VE117988	5	6	8		300000	-20	160		ok
VE117988	5				300000	-20	180		ok
VE117988	5				300000	-25	80		ok
VE117988	5				49000	-25	100	fail	
VE109331	25	1	1	Α	300000	0	260		ok
VE109331	25				300000	-15	260		ok
VE109331	25				300000	-20	220		ok
VE109331	25				300000	-20	240		ok
VE109331	25				300000	-20	260		ok
VE109331	25				300000	-25	80		ok
VE109331	25				300000	-25	100		ok
VE109331	25				69600	-25	120	fail	
VE109331	25	2	6		300000	-25	80		ok
VE109331	25				117600	-25	100		
VE109331	25				300000	-25	100		ok
VE109331	25				300000	-25	120		ok
VE109331	25				30900	-25	140	fail	
VE109331	25	3	2	В	300000	0	260		ok
VE109331	25				300000	-10	260		ok
VE109331	25				300000	-15	260		ok
VE109331	25				300000	-20	260		ok
VE109331	25				300000	-25	260		ok
VE109331	25				300000	-30	260		ok
VE109331	25	4	7		300000	-25	260		ok
VE109331	25				89900	-30	260	fail	
VE109331	25	5	3		300000	-25	260		ok
VE109331	25		_		300000	-30	220		ok
VE109331	25				300000	-30	240		ok
VE109331	25				300000	-30	260		ok
VE109331	25	6	8		300000	-30	220		ok
VE109331	25		_		300000	-30	240		ok
VE109331	25				300000	-30	260		ok

6.3 Safe Operation Area Diagram

From pass/fail results as shown in Tab. 6-2 and Tab. 6-3 Safe-Operation-Area (SOA) plots pertaining to (negative) UGS and UDS can be derived in which individual curves connects "PASS"- UDS values as a function of UGS (Fig. 6-1). Maximum UDS of 260 V in all tests was limited by device breakdown (device rated to 250 V). As a typical result, Fig. 6-1 shows that SEB and SEGR fails do not occur at negative gate voltages UGS = 0 V to -15 V for ion beam parameters given in Tab. 5-1.

Additionally, for beam parameters B in Tab. 5-1 (i.e. LET = 38 MeVcm²/mg and 279 μ m of projected range), a "PASS" – UGS of -25 V is obtained at full UDS of 260 V, which shows a significant decrease of SEE sensitivity at lower LET despite the much longer penetration length.

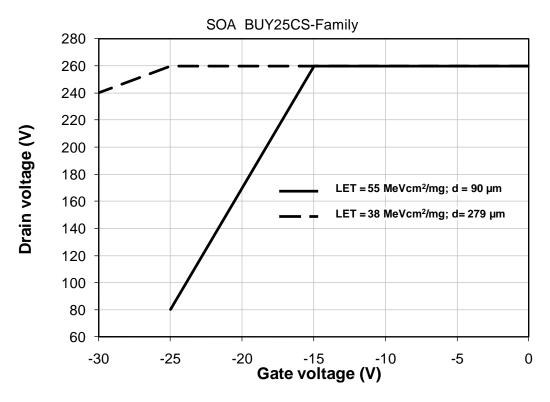


Fig. 6-1: SOA in terms of (negative) Gate voltage (UGS) and Drain voltage (UDS) for the "Standard" technology of BUY25CS Family. Results show no "FAIL" at full UDS of 260 V for UGS = 0 V to -15 V. At LET = $38 \text{ MeVcm}^2/\text{mg}$, no FAIL was recorded to UGS = -25 V.

8. CONCLUSION

As a typical result, Fig. 6-1 shows that SEB and SEGR fails do not occur at negative gate voltages UGS = 0 V to -15 V for ion beam parameters given in Tab. 5-1.

Additionally, for beam parameters B in Tab. 5-1 (i.e. LET = 38 MeVcm²/mg and 279 μ m of projected range), a "PASS" – UGS of -25 V is obtained at full UDS of 260 V, which shows a significant decrease of SEE sensitivity at lower LET despite the much longer penetration length.