

Irradiation Test Report – 1228SR10

Single Event Effect Test on Infineon Rad-Hard-MOSFETs

****BUY15CS****

Dr Gerald Soelkner	IPC TD T PP LV	
Dietmar Schwertberger	PMM RFS D HIR	
Dr. Bernd Eisener	PMM RFS D HIR	

Table of Contents

1	SCOPE	2
2	DEVICE INFORMATION	2
2.1	Applicable Documents	2
2.2	Devices Markings and Sample Preparation	2
2.3	Parameter Measurements	3
3	TEST SET-UP	3
3.1	Test Board	3
3.2	Measurement Equipment ...	4
4	HEAVY ION IRRADIATION FACILITY	5
4.1	Beam Parameters	5
4.2	Test Chamber	5
4.3	Dosimetry	5
5	TEST SEQUENCE	5
5.1	Beam Parameters and Test Criteria for all Tests	5
5.2	Test Bias Sequence for SEB-SOA	5
5.3	Test Bias Sequence for SEGR-SOA	5
6	TEST RESULTS	6
7	CONCLUSION	6
8	DETAILS OF TEST RUNS	7

1 SCOPE

This test report describes Single Event Effect (SEE) tests and results for radiation hardened MOSFETs from Infineon for device type BUY15CS23J01, in accordance to ESCC Basic Specification 25100.

As SEE hardness is technology based, this report is valid for all device types of the same technology, namely BUY15CS23J01, BUY15CS57A01, BUY15CS23K01 and BUY15CS45B01.

Device BUY15CS23J01 has been tested with $^{136}\text{Xe}(48+)$ ions as given in table 1. Concurrently, TID hardness tests were performed for the same device designs issued from the same wafer lots, see separated report.

Tests have been performed at the facilities SPIRAL of Grand Accélérateur National d'Ions Lourds (Tests campaign G10), Caen, France.

Beam	Campaign	Devices	Degrader [μm]	Air [mm]	LET [MeVcm ² /mg]	Range [μm]
A	GANIL10	11	500	138	55.14	94.94

Table 1: Overview of SEE Tests for BUY15CS23J01 and beam characteristics (LET and ion penetration depths) for Xe ions for source SPIRAL (GANIL).

A Test Plan "SEGR-SEB Characterisation of Power MOSFETs BUY15CS23J01" for these tests has been established and reviewed by ESA.

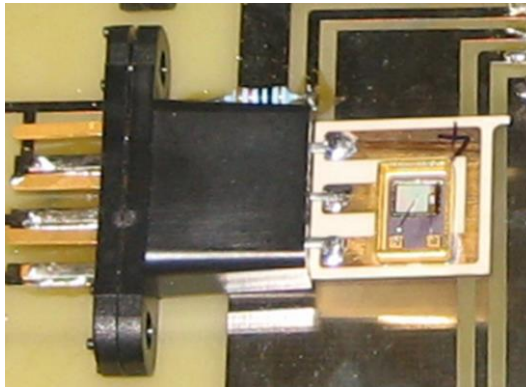


Fig. 1: Device packages: SMD05, unidded, on 3-pin TO-adaptor for BUY15CS23.

2 DEVICE INFORMATION

Part Type	Vds [V]	Vgs(th) [V]	Rds(on) [Ohm]	Idmax [A]
BUY15CS23	150	2.0 - 4.0	0.06	23 (RT)

2. 1 Applicable Documents

- ESCC 5205/031

2.2 Devices Markings and Sample Preparation

Devices are mounted in SMD05 packages with the packages left unlidded. In order to contact devices with the TO test sockets on bias boards SMD-packages have been soldered to respective 3-pin-adaptor boards (fig. 1) to connect Gate/Drain/Source contacts of the MOSFETs.

Devices numbers are engraved on the scribed on the metallization of adapter boards in the case of SMD. The engraving represents information on wafer lot and wafer number as well as device number.

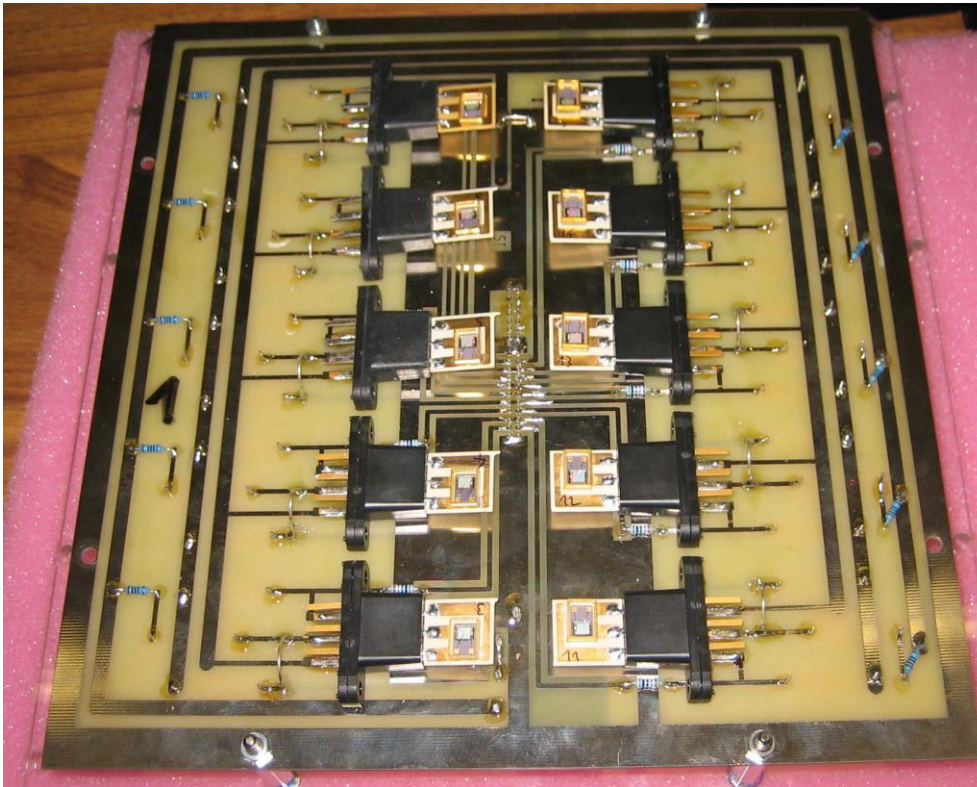


Fig. 2: Test-Board with 10 positions with TO test sockets. Separate bias of UDS and UGS for each device. Flat-band connector on back side.

2.3 Parameter Measurements

Test samples have passed on-wafer tests, notably BVDSS, $V_{gs(th)}$, $R_{DS(on)}$, I_{DSS} , I_{GSS} with their parameters within predetermined upper/lower limits.

Parameter measurements have been performed on package- and adapter-mounted devices to check that devices have not been degraded. Specifically, $I_{DSS}(150V)$, $I_{GSS}(+/-20V)$, $R_{DS(on)}(15A, U_{gs}=10V)$, $V_{SD}(23 A)$, $V_{gs(th)}(1 mA)$, $BVDSS(0.25 mA)$ are determined.

3. TEST SET-UP

3.1 Test Board

The test board was designed to accommodate up to 10 test samples, each consisting of an individual bias circuit (fig. 2). This test board was fixed to the mechanical positioning stage provided at the GANIL beam line. All voltages UDS and UGS were provided via a flat band cable from a switch board. The oscilloscope output was left unconnected. The bias circuit is given in fig. 3.

3.2 Measurement Equipment

As a voltage source for UDS and for ID current measurements a *Keithley 237 High Voltage Measurement Unit* has been employed. Gate voltage UGS and measurement of IG are provided by an *Keithley 236 Source Measure Unit*.

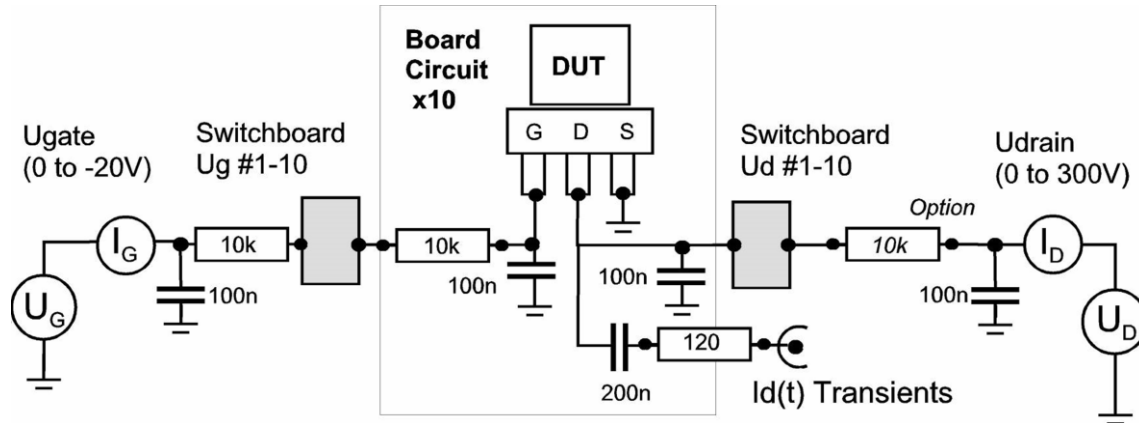


Fig. 3: Test circuit for SEB/SEGR test.

Voltages were set manually as were all recordings of run number, time, sample number, all current readings, specifically PIGS currents, are logged. The irradiation report provided by GANIL operators, in addition, give fluence values for each test run.

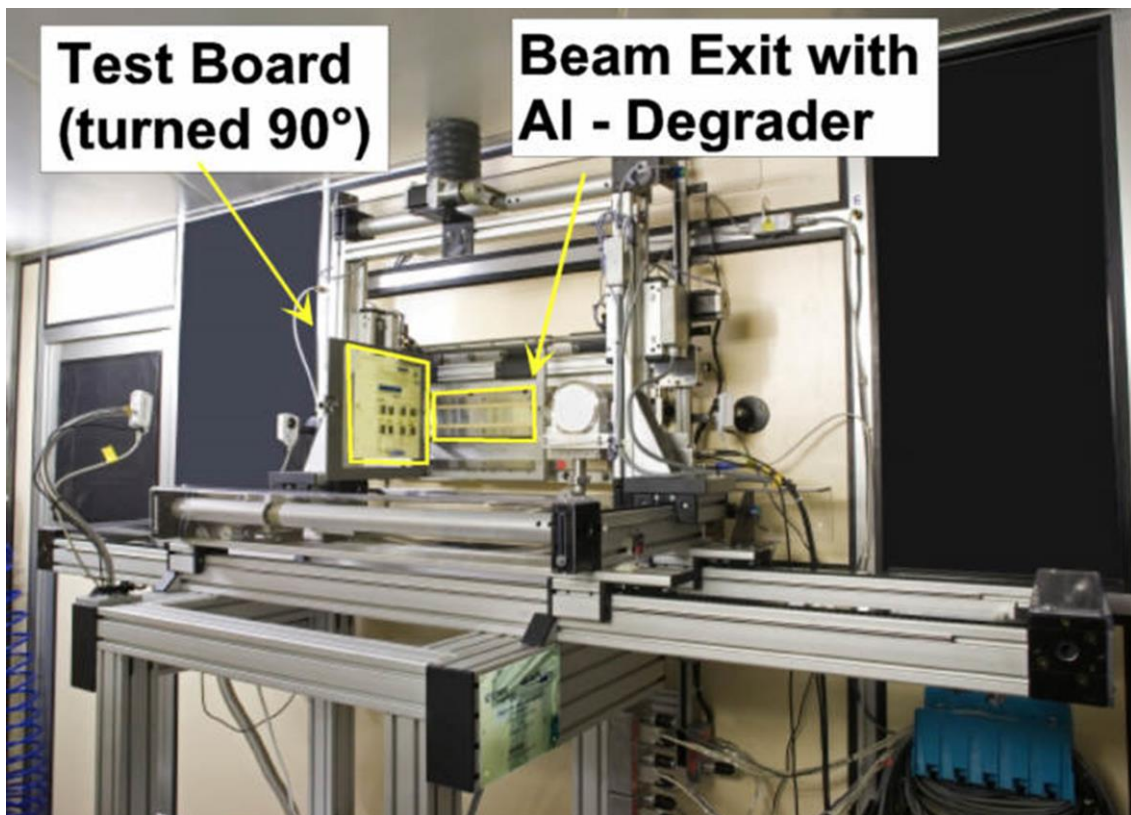


Fig. 4: Test Board positioning at GANIL beam line exit window

4 HEAVY ION IRRADIATION FACILITIES

4.1 Beam Parameters

SPIRAL at GANIL Caen is a cyclotron capable of providing heavy ions of very high energy, in the order 50MeV/u, i.e. 6 GeV per ion for ^{136}Xe (48+ charge state) employed in irradiation run G10.

Parameters were chosen to provide the highest possible LET for a given minimum of penetration depth about 90 μm (Parameter setting "A").

4.2 Testing Position and Test Board Mounting

At GANIL irradiation is performed in air. The test board is attached to a motorized positioning frame (fig. 4). The beam exit of the vacuum tube has a 10 μm stainless steel window. Beam size is 200 mm (horizontal) and 50 mm (vertical). With the bias board as in fig. 2, all devices are irradiated simultaneously and further device positioning is usually not necessary. To achieve the desired LET/penetration, aluminium foil degraders and adjusted air distances are used.

Ion incidence was chosen to be 0° , i.e., vertical incidence.

4.3 Dosimetry

Control of beam homogeneity and dosimetry as well as beam operation is the responsibility of ion beam providers. An irradiation log provided by GANIL gives actual flux values for each test run, including fluence-to-fail, if applicable.

5 TESTING SEQUENCE

5.1 Beam Parameters and Test Criteria for all Tests:

- LET see Table 5-1
- Flux $3\text{E}3 \text{ ions/cm}^2/\text{s}$
- Fluence $3\text{E}+5 \text{ ions/cm}^2$
- Normal incidence of ion beam
- Destructive mode. FAIL current criteria: $\text{IDS} > 2 \mu\text{A}$ or $\text{IGS} > 100 \text{ nA}$.
- Required number of test samples per test case: 1(for FAIL)/3(for PASS)
- Post Irradiation Gate Stress (PIGS) test at any UDS (at respective UDS, UGS down to -25V, in steps of -5V). FAIL criterion: either IDS or $\text{IGS} > 100\text{nA}$

5.2 Test Bias Sequence to determine Single Event Breakdown (SEB)-SOA

UGS: 0 V

UDS: Start at 160V (or UDS,max). If *FAIL* occurs UDS is stepped-down by 10V until PASS.

5.3 Test Bias Sequence to determine Single Event Gate Rupture (SEGR)-SOA

UGS: -5 V to -25 V, starting at -5 V, steps of -5 V.

UDS: Start at maximum UDS at which PASS value was obtained for previous UGS-test sequence (or $\text{UGS} = 0^\circ\text{V}$). If *FAIL* occurs UDS is stepped-down by 10V until PASS.

6. TEST RESULTS

The device has been tested and the SOA diagram is shown in Fig. 5.

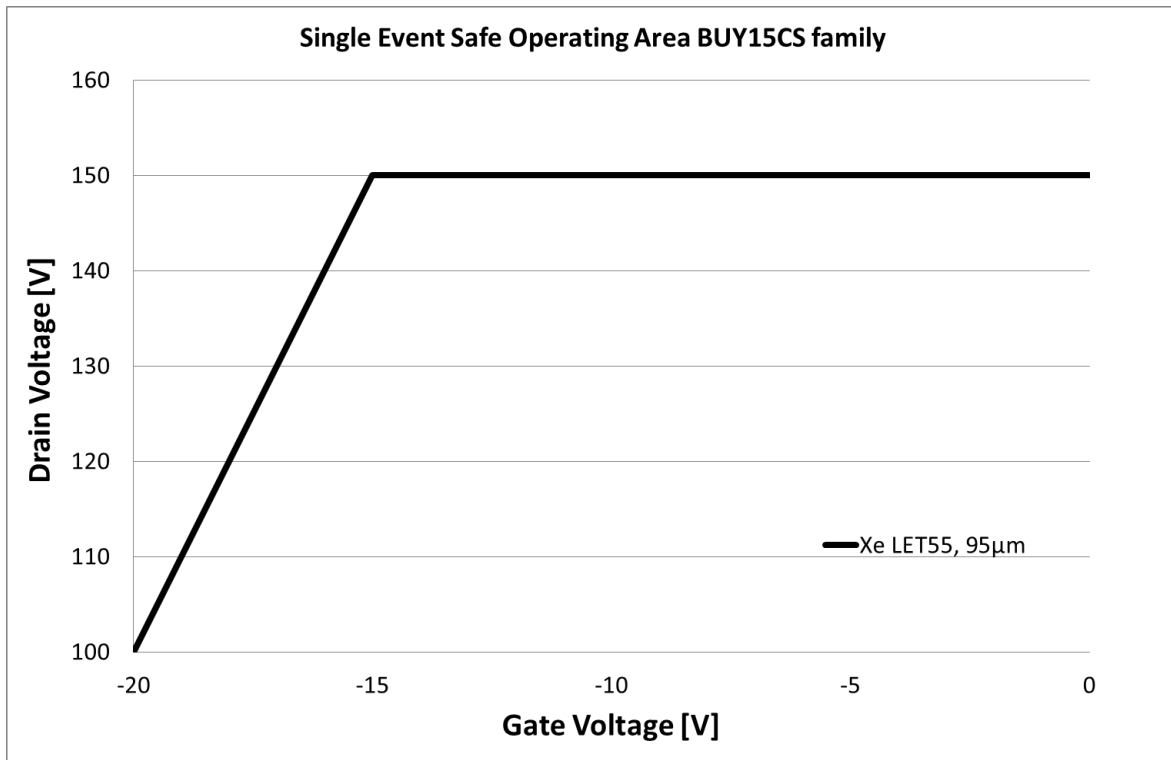


Fig. 5: SOA of device BUY15CS23J as determined at test G10 (GANIL).

7. CONCLUSION

SEE tests of BUY15CS23J MOSFETs have been performed. The device is immune to SEE failure (tested up to LET 59.8) up to rated UDS voltage and for negative gate voltages down to -15 .

Single Event Effect Test on Infineon Rad-Hard MOSFETs Types BUY15CS23J
January 21, 2016

8 DETAILS OF TEST RUNS

Details of individual test runs G10:

hh:mm	Run	lot	test no.	Board Pos	chip	test no.	Flux (i/cm2/sec)	Fluence (/cm ²)	Vds test(V)	Vgs test (V)	File	Nb events	Nb events
Beam Setting 'A'													
18:09	769	VE333260/18	no.11	6	1	1	4500	3,0E+05	160	0	t11d1n01		ok
	770	C15J(Ref)				2			160	-5	t11d1n02		ok
	771	150V				3			160	-10	t11d1n03		ok
	772	Bd.1(4)				4			160	-15	t11d1n04		ok
	773	Reference				5			120	-20	t11d1n05		ok
	774					6			140	-20	t11d1n06		fail
18:24	775			7	2	1			160	0	t11d2n01		ok
	776					2			160	-10	t11d2n02		ok
	777					3			160	-15	t11d2n03		ok
	778					4			120	-20	t11d2n04		fail
				8	3	1							ok
18:34	779			9	4	1			160	0	t11d4n01		ok
	780					2			160	-10	t11d4n02		ok
18:41	781					3			160	-15	t11d4n03		ok
	782					4			100	-20	t11d4n04		ok
	783					5			110	-20	t11d4n05		fail
18:46	784			10	5	1			160	0	t11d5n01		ok
	785					2			160	-15	t11d5n02		ok
	786					3			100	-20	t11d5n03		ok
	787					4			40	-25	t11d5n04		ok
18:55	788					5			60	-25	t11d5n05		fail