512Mb SEMPER™ Flash and 64Mb HYPERRAM™ 2.0

Octal interface, multi-chip package, 1.8 V/3.0 V

Features

- SEMPER™ Flash and HYPERRAM™ 2.0 with Octal interface in multi-chip package (MCP)
  - 1.8 V, 512Mb SEMPER™ Flash and 64Mb HYPERRAM™ 2.0 (S78HS512TC0)
  - 3.0 V, 512Mb SEMPER™ Flash and 64Mb HYPERRAM™ 2.0 (S78HL512TC0)
  - FBGA 24-ball, 8 × 8 × 1.2 mm packages
- Octal interface
  - 1.8V I/O (S78HS-TC0)
  - 3.0V I/O (S78HL-TC0)
  - Chip select (CS#)
  - 8-bit data bus (DQ[7:0])
  - Data strobe (DS/RWDS)
    - Bidirectional DS/mask
    - Output at the start of all transactions to indicate refresh latency
    - Output during read transactions as read DS
    - Input during write transactions as write data mask (HYPERRAM™ only)
- Optional signals
  - INT# output to generate external interrupt
    - Busy to ready transition
- High-performance
  - DDR
    - Two data transfers per clock
  - Up to 200 MHz clock rate (400-MBps) at 1.8 V V_{CC}
  - Up to 166 MHz clock rate (333-MBps) at 3.0 V V_{CC}

Table of contents

1 General description

This supplementary datasheet provides MCP device related information for Octal MCP family, incorporating both SEMPER™ Flash and HYPERRAM™ 2.0 with Octal interface memories. The document describes how the features, operation, and ordering options of the related memories have been enhanced or changed from the standard memory devices incorporated in the MCP. The information contained in this document modifies any information on the same topics established by the documents listed in **Table 1** and should be used in conjunction with those documents. This document may also contain information that was not previously covered by the listed documents. The information is intended for hardware system designers and software developers of applications, operating systems, or tools.

Table 1 Affected documents/related documents

Title	Infineon publication number
S28HS256T, S28HS512T, S28HS01GT, S28HL256T, S28HL512T, S28HL01GT 256Mb/512Mb/1Gb SEMPER™ Flash Octal interface, 1.8 V/3.0 V	002-18216
S27KL0643, S27KS0643 64Mb HYPERRAM™ self-refresh DRAM (PSRAM) Octal xSPI, 1.8 V/3.0 V	002-24693

1.1 Octal MCP family with SEMPER™ Flash and HYPERRAM™

For systems needing both Flash and self-refresh DRAM, the Octal product family includes MCP devices that combine SEMPER™ Flash and HYPERRAM™ in a single package. A Octal MCP reduces board space and printed circuit board (PCB) signal routing congestion while also maintaining or improving signal integrity over separately packaged memory configurations.

The Octal MCP family offers 1.8 V/3.0 V interface SEMPER™ Flash densities of 512Mb (64MB) in combination with HYPERRAM™ 2.0 64Mb (8MB).

The SEMPER™ Flash default configuration is Legacy Single SPI Protocol with configuration bit OPI-IT = 0.

This supplemental datasheet addresses only the MCP related differences from the Octal specification and the individual SEMPER™ Flash and HYPERRAM™ datasheets. For other information related to the individual memories in the MCP, refer to the SEMPER™ Flash, and HYPERRAM™ 2.0 datasheets with Octal interface.

2 Octal MCP signal description

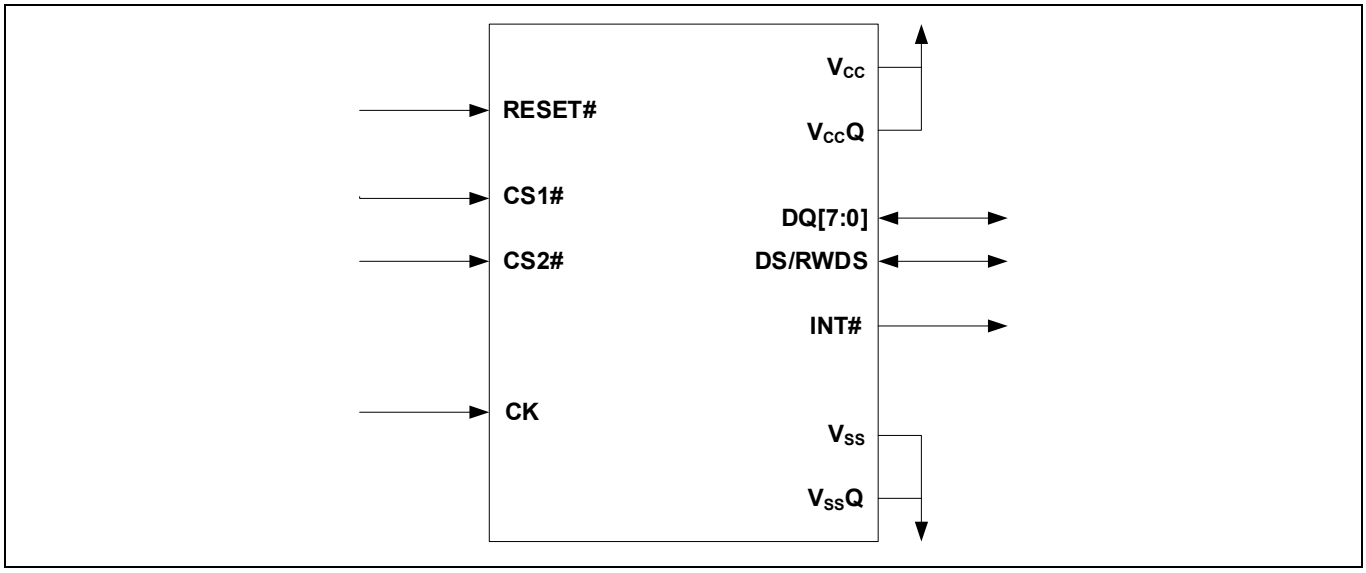


Figure 1 Octal MCP signal diagram

Table 2 Signal description

Symbol	Type	Description
CS1#	Input	**Chip select 1.** Chip Select for the SEMPER™ Flash memory. Octal transactions are initiated with a HIGH-to-LOW transition. Octal transactions are terminated with a LOW- to-HIGH transition.
CS2#	Input	**Chip select 2.** Chip Select for the HYPERRAM™ memory. Octal transactions are initiated with a HIGH-to-LOW transition. Octal transactions are terminated with a LOW-to-HIGH transition.
CK	Input	**Single-ended clock.** Command-address/data information is input or output with respect to the edges of the CK.
DS / RWDS	Input / Output	**Read data strobe (DS).** DS is used for SEMPER™ Flash data read operations only and indicates output data valid for the Octal interface. During a read transaction, while CS# is LOW, DS toggles to synchronize the data output until CS# goes HIGH. Output data during read transactions is edge-aligned with DS. **Read-write data strobe (RWDS):** Output data during HYPERRAM™ read transactions is edge-aligned with RWDS. RWDS is an input during write transactions to function as a HYPERRAM™ data mask.
DQ[7:0]	Input / Output	**Data input/output.** Command-address/data information is transferred on these DQs during read and write transactions.
INT#	Output (open drain)	**INT output (optional).** When LOW, the SEMPER™ Flash device is indicating that an internal event has occurred. This signal is intended to be used as a system-level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output.
RESET#	Input	**Hardware RESET (optional).** When LOW, the SEMPER™ Flash and HYPERFLASH™ memory's will self-initialize and return to the idle state. DS/RWDS and DQ[7:0] is placed into the HIGH-Z state when RESET# is LOW. RESET# includes a weak pull-up; if RESET# is left unconnected, it will be pulled up to the HIGH state.
V_{CC}	Power supply	Core power
$V_{CC}Q$	Power supply	Input/output power
V_{SS}	Power supply	Core ground
$V_{SS}Q$	Power supply	Input/output ground

3 Octal MCP block diagram

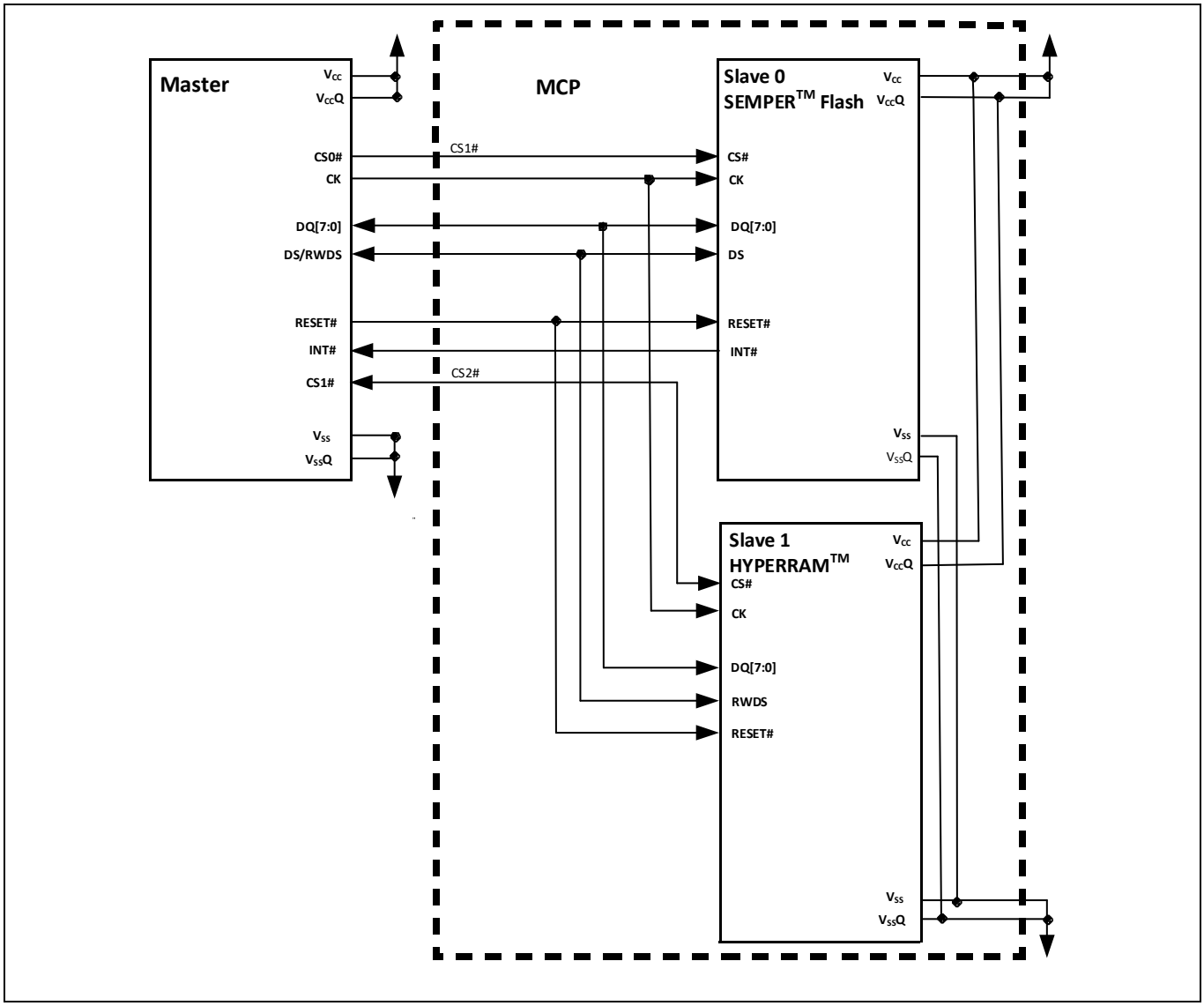


Figure 2 Octal connections including optional signals

4 Physical interface

4.1 Octal MCP — FBGA 24-ball, 5 × 5 footprint

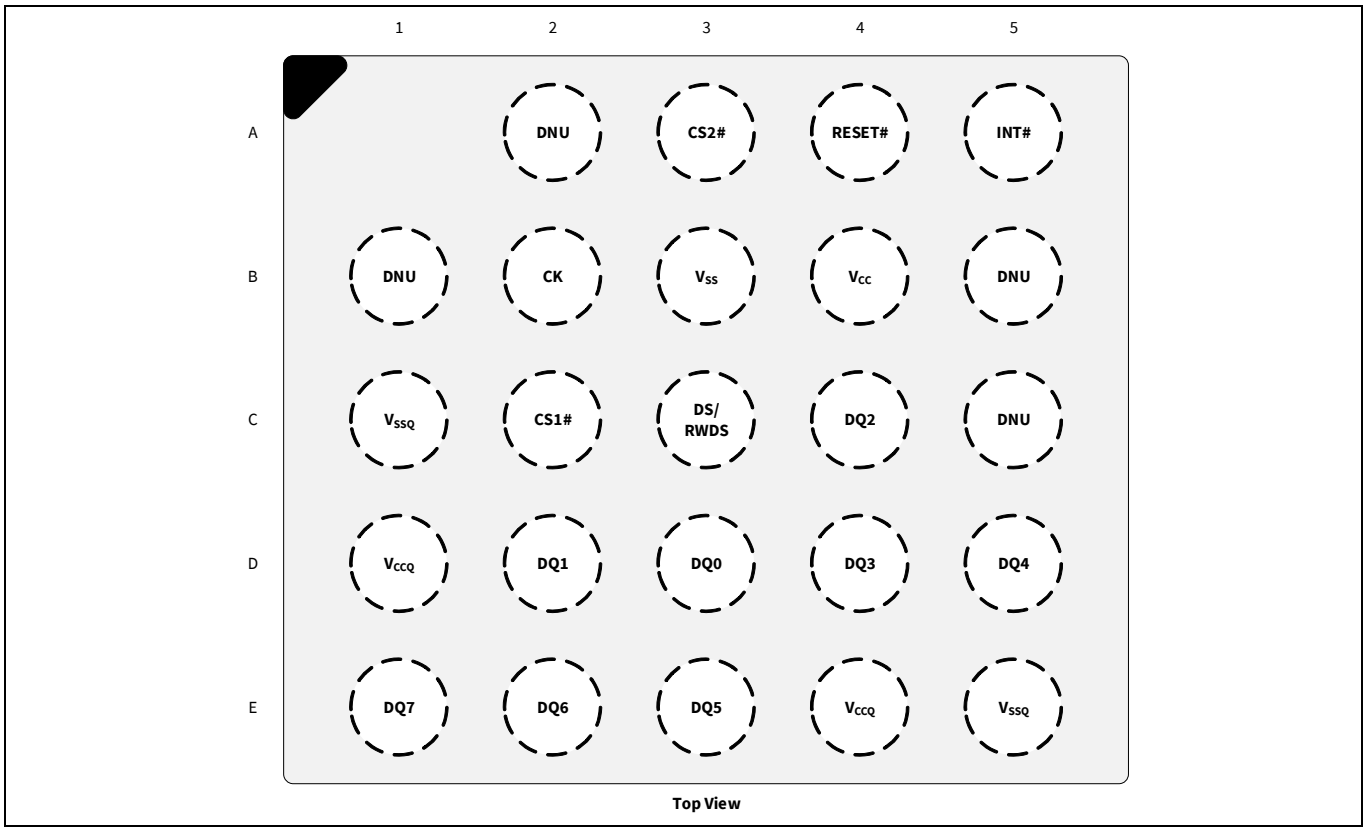


Figure 3 24-ball FBGA, 8 × 8 mm, 5 × 5 ball footprint (Top view)

Notes
1. C2 and A3 are chip select (CS#) signals 1 and 2 used for SEMPER™ Flash and HYPERRAM™ devices respectively.
2. V_{SS} and $V_{SS}Q$ are internally connected.

5 Electrical specifications

The following section describes the device dependent aspects of electrical specifications.

5.1 Absolute maximum ratings

Ambient temperature with power applied: –65°C to +115°C.

5.2 DC characteristics

Only one memory may have its Chip Select active (LOW) at any point in time. For each condition below, refer to the SEMPER™ Flash and HYPERRAM™ datasheets for the most accurate information:

- Active core read or write current will be that of the selected device plus the standby current of the non-selected device. However, the added standby current is generally not significant because it is less than 300 µA.
- Active I/O read current will be that of the selected device.
- Active clock stop current will be that of the selected device plus the standby current of the non-selected device. However, the added standby current is generally not significant because it is less than 300 µA.
- Program or erase current will be that of the SEMPER™ Flash device. Note however, that program and erase operations are long-time-frame events that extend beyond the duration of a SEMPER™ Flash Chip Select period. Thus, if the HYPERRAM™ is selected for read or write during an on going SEMPER™ Flash program or erase operation, the active current will be the sum of the SEMPER™ Flash program or erase operation and the HYPERRAM™ read or write current.
- Standby current, when neither memory is selected and no embedded flash operation is in progress, is the sum of the memory standby currents.
- Deep power down (DPD) current is the sum of the memory DPD currents.
- POR current is the sum of the memory standby currents.
- Input leakage current is the sum of the memory input leakage currents.

For reference purpose, **Table 3** aids in the estimation of the current consumption in these operating conditions. However, see the SEMPER™ Flash and HYPERRAM™ datasheets for the most accurate information.

Table 3 3.0 V DC characteristics (CMOS compatible)

Parameter	Description	Test conditions	Min	Typ[6]	Max	Unit
I_{LI}	Input leakage current (RESET# HIGH)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	±3.1	µA
	Input leakage current (RESET# LOW)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	+18.0	
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ max	–	–	±3.1	
I_{CC1HF}	V_{CC} active read current - SEMPER™ Flash reading (core current only, I/O switching current is not included)	CS# = V_{IL}, @ 166 MHz, V_{CC} = 3.60 V	–	126	150	mA
		CS# = V_{IL}, @ 200 MHz, V_{CC} = 2.00 V	–	156	173	
I_{CC1HR}	V_{CC} active read current - HYPERRAM™ reading	CS# = V_{IL}, @ 166 MHz, V_{CC} = 3.60 V	–	15	28	mA
		CS# = V_{IL}, @ 200 MHz, V_{CC} = 2.00 V	–	15	25	
I_{CC2HR}	V_{CC} active write current - HYPERRAM™ writing	CS# = V_{IL}, @ 166 MHz, V_{CC} = 3.60 V	–	15	28	
		CS# = V_{IL}, @ 200 MHz, V_{CC} = 2.00 V	–	15	25	
$I_{CC1HFHR}$	V_{CC} Active program / erase current - SEMPER™ Flash embedded operation plus HYPERRAM™ reading[4]	CS# = V_{IL}, @ 166 MHz, V_{CC} = 3.60 V	–	65	92	
		CS# = V_{IL}, @ 200 MHz, V_{CC} = 2.00 V	–	65	91	
$I_{CC2HFHR}$	V_{CC} active program / erase current - SEMPER™ Flash embedded operation plus HYPERRAM™ reading[4]	CS# = V_{IL}, @ 100 MHz, V_{CC} = 3.60 V	–	75	135	
		CS# = V_{IL}, @ 166 MHz, V_{CC} = 2.00 V	–	75	160	
I_{CC3P}	V_{CC} active program current[3, 4] SEMPER™ Flash (512T)	$V_{CC} = V_{CC}$ max	–	50	55	
I_{CC3E}	V_{CC} active erase current[3, 4] SEMPER™ Flash (512T)	$V_{CC} = V_{CC}$ max	–	50	55	
I_{CC4I}	V_{CC} standby current (512T) SEMPER™ Flash + HYPERRAM™	CS#, RESET# = V_{CC}, V_{CC} = 2.00 V, 85°C	–	91	333	µA
		CS#, RESET# = V_{CC}, V_{CC} = 2.00 V, 105°C	–	91	518	
		CS#, RESET# = V_{CC}, V_{CC} = 3.60 V, 85°C	–	104	376	
		CS#, RESET# = V_{CC}, V_{CC} = 3.60 V, 105°C	–	104	548	

Notes
3. I_{CC} active while embedded algorithm (EA) is in progress.
4. Not 100% tested.
5. Active Clock Stop mode enables the lower power mode when the CK signals remain stable for t_{ACC} + 30 ns.
6. Typical I_{CC} values are measured at t_{AI} = 25°C and $V_{CC} = V_{CC}Q$ = 1.8 V/3.0 V (not applicable to I_{DPD} for 85°C and 105°C).
7. Current specification includes both the SEMPER™ Flash and HYPERRAM™ die current consumption per the mode of operation of each die.

Table 3 3.0 V DC characteristics (CMOS compatible) (Continued)

Parameter	Description	Test conditions	Min	Typ[6]	Max	Unit
I_{CC6}	Active clock Stop mode[5] HYPERRAM™	$V_{IH} = V_{CC}$, $V_{IL} = V_{SS}$, V_{CC} = 2.00 V/3.6 V, 85°C	–	5	8	mA
		$V_{IH} = V_{CC}$, $V_{IL} = V_{SS}$, V_{CC} = 2.00 V/3.6 V, 105°C	–	8	12	
I_{CC7}	V_{CC} current during power-up (POR) SEMPER™ Flash + HYPERRAM™	CS# = X, $V_{CC} = V_{CC}$ max	–	–	115	
I_{DPD1}	DPD current SEMPER™ Flash + HYPERRAM™ (512T)	CS#, RESET#, V_{CC} = 2.0 V, 85°C	–	–	28	µA
		CS#, RESET#, V_{CC} = 2.0 V, 105°C	–	–	30	
		CS#, RESET#, V_{CC} = 3.6 V, 85°C	–	–	30	
		CS#, RESET#, V_{CC} = 3.6 V, 105°C	–	–	33	
I_{HS}	Hybrid sleep current HYPERRAM™ SEMPER™ Flash in DPD (512T)	CS# = V_{CC}, V_{CC} = 2.0 V; 85°C	–	27	218	
		CS# = V_{CC}, V_{CC} = 2.0 V; 105°C	–	37	318	
		CS# = V_{CC}, V_{CC} = 3.6 V; 85°C	–	27	318	
		CS# = V_{CC}, V_{CC} = 3.6 V; 105°C	–	38	328	

Notes
3. I_{CC} active while embedded algorithm (EA) is in progress.
4. Not 100% tested.
5. Active Clock Stop mode enables the lower power mode when the CK signals remain stable for t_{ACC} + 30 ns.
6. Typical I_{CC} values are measured at t_{AI} = 25°C and $V_{CC} = V_{CC}Q$ = 1.8 V/3.0 V (not applicable to I_{DPD} for 85°C and 105°C).
7. Current specification includes both the SEMPER™ Flash and HYPERRAM™ die current consumption per the mode of operation of each die.

5.3 Capacitance characteristics

Table 4 1.8 V/3.0 V capacitive characteristics

Description	Parameter	Min	Max	Unit
Input capacitance (CK, CK#)[8-10]	CI	6.0	10.5	pF
Output capacitance (DS/RWDS)[8-10]	CO	9.5	10.5	
I/O pin capacitance (DQx)[8-10]	CIO	9.5	10.5	
I/O pin capacitance delta (DQx)[8-10]	CIOD	–	0.25	
INT#, RSTO# pin capacitance, RST#[8-10]	COP	9.5	10.5	

Notes

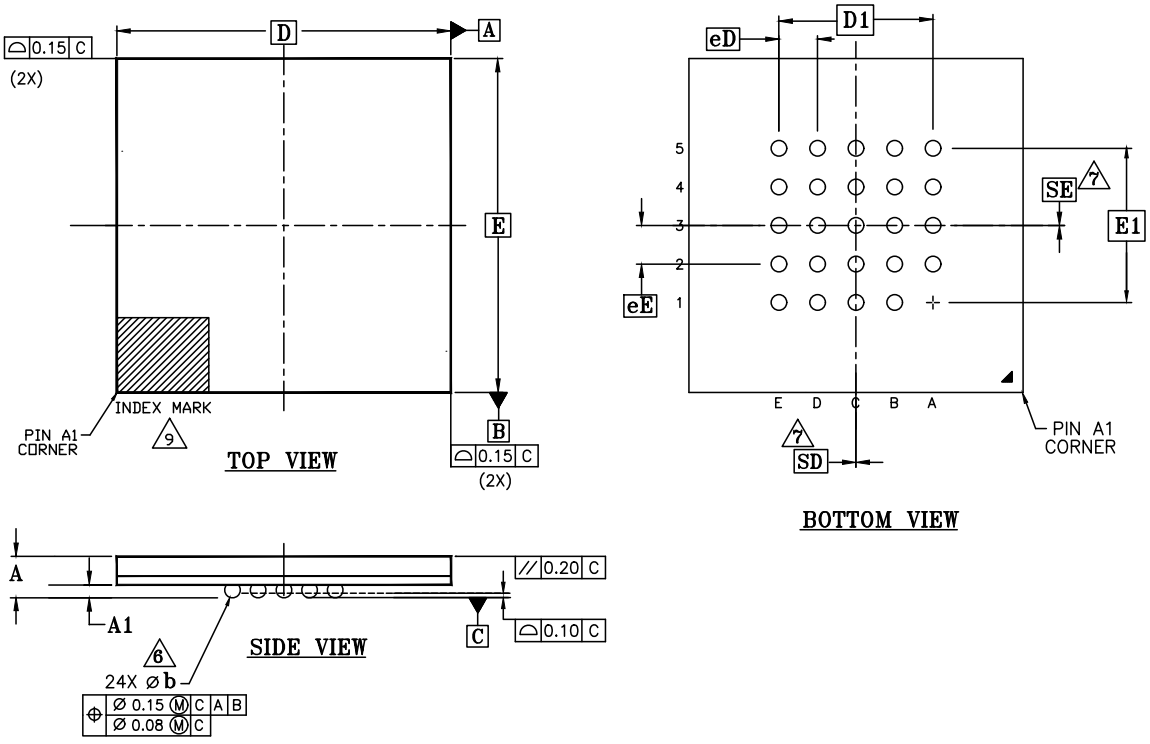
8. These values are guaranteed by design and are tested on a sample basis only.
9. Pin capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. V_{CC}, $V_{CC}Q$ are applied and all other pins (except the pin under test) floating. DQs should be in the HIGH-Z state.
10. The capacitance values for the CK, CK#, RWDS and DQx pins must have similar capacitance values to allow for signal propagation time matching in the system. The capacitance value for CS# is not as critical because there are no critical timings between CS# going active (LOW) and data being presented on the DQs bus.

5.4 Thermal resistance

Table 5 Thermal resistance

Parameter	Description	Test condition	24-ball BGA	Unit
Theta JA	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51. With Still Air (0 m/s)	53.6	°C/W
Theta JB	Thermal resistance (Junction to board)		28.3	
Theta JC	Thermal resistance (Junction to case)		16.2	

6 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.20	-	-
D		8.00 BSC	
E		8.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
⌀ b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

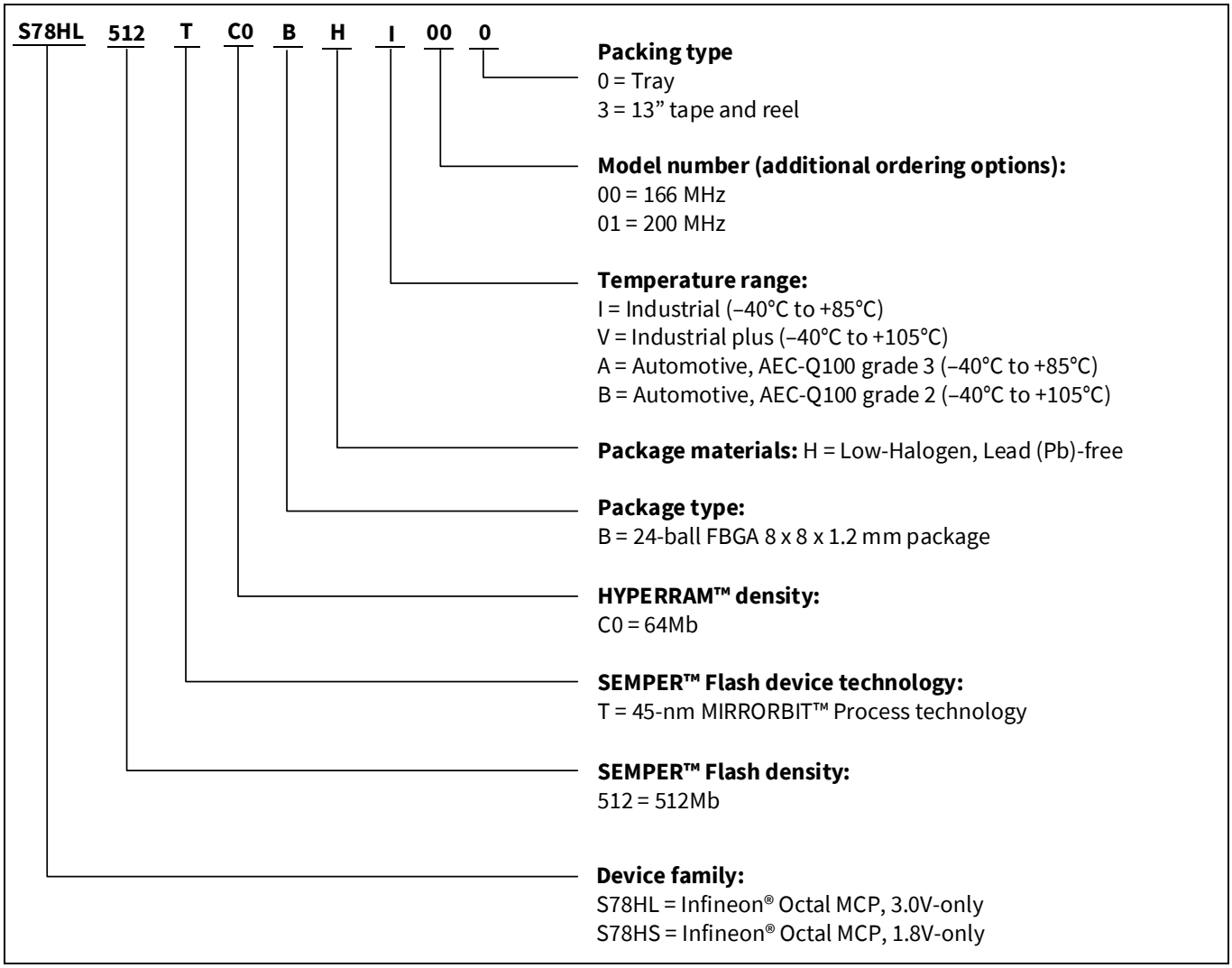
002-24801 *A

Figure 4 24-ball BGA (8 × 8 × 1.2 mm) package outline, 002-24801

7 Ordering information

7.1 Ordering code definitions

The ordering part number is formed by a valid combination of the following:



7.2 Valid combinations — Standard

Table 6 lists configurations planned to be available in volume. The table will be updated as new combinations are released. Contact your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Table 6 Valid combinations — Standard (Contact Sales)

Device number	HYPERRAM™ density	Package and material	Temperature range	Model number	Packing type	Ordering part number (x = Packing type)	Package marking
S78HL512T	C0	BH	I	00	0, 3	S78HL512TC0BHI00x	8HL512TC0I00
			V			S78HL512TC0BHV00x	8HL512TC0V00
S78HS512T	C0	BH	I	01	0, 3	S78HS512TC0BHI01x	8HS512TC0I01
			V			S78HS512TC0BHV01x	8HS512TC0V01

7.3 Valid combinations — Automotive grade / AEC-Q100

Table 8 lists configurations that are Automotive grade / AEC-Q100 qualified and are planned to be available in volume. The table will be updated as new combinations are released. Consult your local sales representative to confirm availability of specific combinations and to check on newly released combinations.

Production part approval process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements.

AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 7 Valid Combinations — Automotive grade / AEC-Q100 (In Production)

Device number	HYPERRAM™ density	Package and material	Temperature range	Model number	Packing type	Ordering part number (x = Packing type)	Package marking
S78HL512T	C0	BH	B	00	0, 3	S78HL512TC0BHB00x	8HL512TC0B00
S78HS512T	C0	BH	B	01	0, 3	S78HS512TC0BHB01x	8HS512TC0B01

Table 8 Valid Combinations — Automotive grade / AEC-Q100 (Contact Sales)

Device number	HYPERRAM™ density	Package and material	Temperature range	Model number	Packing type	Ordering part number (x = Packing type)	Package marking
S78HL512T	C0	BH	A	00	0, 3	S78HL512TC0BHA00x	8HL512TC0A00
S78HS512T	C0	BH	A	01	0, 3	S78HS512TC0BHA01x	8HS512TC0A01

Revision history

Document revision	Date	Description of changes
**	2021-02-05	Initial release.
*A	2021-11-18	Updated **Octal MCP signal description**: Updated **Figure 1**. Updated**Table 2**: Updated Description for CK#. Updated **Octal MCP block diagram**: Updated **Figure 2**. Updated **Electrical specifications**: Updated **DC characteristics**: Updated **Table 3**: Updated Description for I_{LI}. Updated Max. value for I_{CC2HR} and I_{HS}. Added **Thermal resistance**.
*B	2022-09-21	Changed status from “Preliminary Supplement” to “Supplement”. Updated Document Title to read as “S78HS512TC0, S78HL512TC0, 512Mb SEMPER™ Flash and 64Mb HYPERRAM™ 2.0 Octal interface, multi-chip package, 1.8 V/3.0 V”. Remove 1Gb SEMPER™ Flash related information in all instances across the document. Updated **General description**: Updated **Table 1**. Updated **Electrical specifications**: Updated **DC characteristics**: Updated **Table 3**. Updated **Ordering information**: Updated **Valid combinations — Standard**: Updated **Table 6**. Updated **Valid combinations — Automotive grade / AEC-Q100**: Added **Table 7**. Updated **Table 8**. Updated to new template.

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